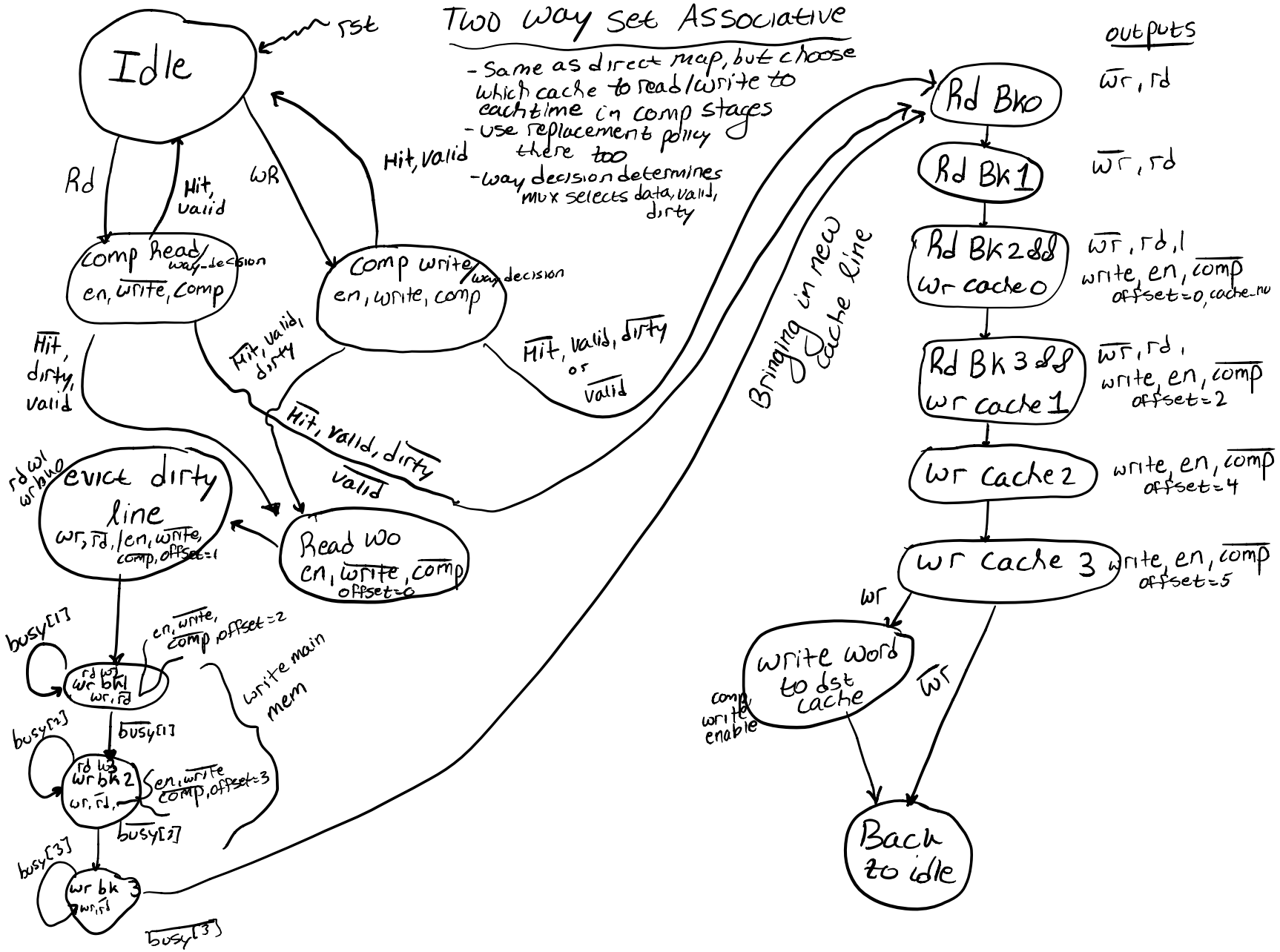
Two way set Associative
- Same as direct map, but choose which cache to read/write to each time in comp stages
- use replacement policy there too
- way decision determines mux selects data, valid, dirty
Idle
rst
Rd
Hit, valid
WR
comp read / way_decision
en, write, comp
comp write / way decision
en, write, comp
Hit, valid, dirty
Hit, valid, dirty
Hit, valid, dirty or valid
Hit, valid, dirty
valid
Bringing in new cache line
rd wl wr bk 0
evict dirty line
wr, rd, en, write, comp, offset=1
Read w0
en, write, comp
offset=0
busy[1]
en, write, comp offset=2
rd wl wr bk 1
wr, rd
write main mem
busy[2]
busy[1]
rd wl wr bk 2
wr, rd, en, write comp, offset=3
busy[2]
busy[3]
wr bk 3
wr, rd
busy[3]
outputs
Rd Bk0
wr, rd
Rd Bk 1
wr, rd
Rd Bk 2 & wr cache 0
wr, rd, write, en, comp offset=0, cache_no
Rd Bk 3 & wr cache 1
wr, rd, write, en, comp offset=2
wr cache 2
write, en, comp offset=4
wr cache 3
write, en, comp offset=5
wr
write word to dst cache
comp write enable
wr
Back to idle