ANALOG DEVICES

# Ultralow Distortion Differential ADC Driver

Data Sheet

# ADA4937-1/ADA4937-2

## FEATURES

- **Extremely low harmonic distortion (HD)**
  - **−112 dBc HD2 at 10 MHz**
  - **−84 dBc HD2 at 70 MHz**
  - **−77 dBc HD2 at 100 MHz**
  - **−102 dBc HD3 at 10 MHz**
  - **−91 dBc HD3 at 70 MHz**
  - **−84 dBc HD3 at 100 MHz**
- **Low input voltage noise: 2.2 nV/√Hz**
- **High speed**
  - **−3 dB bandwidth of 1.9 GHz, G = 1**
  - **Slew rate: 6000 V/µs, 25% to 75%**
  - **Fast overdrive recovery of 1 ns**
- **0.5 mV typical offset voltage**
- **Externally adjustable gain**
- **Differential-to-differential or single-ended-to-differential operation**
- **Adjustable output common-mode voltage**
- **Single-supply operation: 3.3 V to 5 V**

## APPLICATIONS

- **ADC drivers**
- **Single-ended-to-differential converters**
- **IF and baseband gain blocks**
- **Differential buffers**
- **Line drivers**

## GENERAL DESCRIPTION

The ADA4937-1/ADA4937-2 are low noise, ultralow distortion, high speed differential amplifiers. They are an ideal choice for driving high performance ADCs with resolutions up to 16 bits from dc to 100 MHz. The adjustable level of the output common mode allows the ADA4937-1/ADA4937-2 to match the input of the ADC. The internal common-mode feedback loop also provides exceptional output balance as well as suppression of even-order harmonic distortion products.

With the ADA4937-1/ADA4937-2, differential gain configurations are easily realized with a simple external feedback network of four resistors that determine the closed-loop gain of the amplifier.

The ADA4937-1/ADA4937-2 are fabricated using Analog Devices, Inc., proprietary silicon-germanium (SiGe), complementary bipolar process, enabling them to achieve very low levels of distortion with an input voltage noise of only 2.2 nV/√Hz. The low dc offset and excellent dynamic performance of the ADA4937-1/ADA4937-2 make them well-suited for a wide variety of data acquisition and signal processing applications.

## FUNCTIONAL BLOCK DIAGRAMS

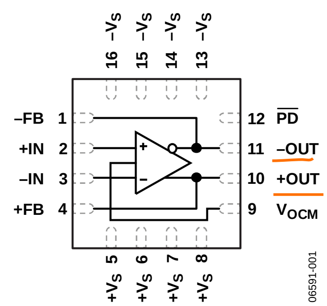


*Figure 1. ADA4937-1*

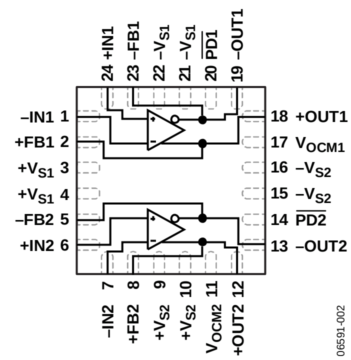


*Figure 2. ADA4937-2*

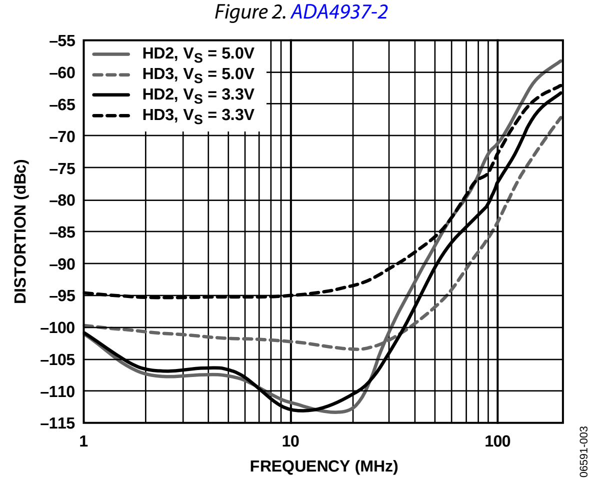


*Figure 3. Harmonic Distortion vs. Frequency*

The ADA4937-1/ADA4937-2 are available in a Pb-free, 3 mm × 3 mm, 16-lead LFCSP (ADA4937-1, single) or a Pb-free, 4 mm × 4 mm, 24-lead LFCSP (ADA4937-2, dual). The pinout has been optimized to facilitate PCB layout and minimize distortion. The ADA4937-1/ADA4937-2 are specified to operate over the automotive (−40°C to +105°C) temperature range and between 3.3 V and 5 V supplies.


**Rev. F** **Document Feedback**




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# SPECIFICATIONS

## 5 V OPERATION

$T_A$ = 25°C, $+V_S$ = 5 V, $-V_S$ = 0 V, $V_{OCM}$ = $+V_S/2$, $R_T$ = 61.9 Ω, $R_G$ = $R_F$ = 200 Ω, Gain (G) = +1, $R_{L,\,dm}$ = 1 kΩ, unless otherwise noted. All specifications refer to single-ended input and differential outputs, unless otherwise noted.

### ±$D_{IN}$ to ±OUT Performance

**Table 1.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | | |
| −3 dB Small Signal Bandwidth | $V_{OUT,\,dm}$ = 0.1 V p-p | | 1900 | | MHz |
| Bandwidth for 0.1 dB Flatness | $V_{OUT,\,dm}$ = 0.1 V p-p | | 200 | | MHz |
| Large Signal Bandwidth | $V_{OUT,\,dm}$ = 2 V p-p | | 1700 | | MHz |
| Slew Rate | $V_{OUT,\,dm}$ = 2 V p-p; 25% to 75% | | 6000 | | V/µs |
| Settling Time | $V_{OUT,\,dm}$ = 2 V p-p | | 7 | | ns |
| Overdrive Recovery Time | $V_{IN}$ = 0 V to 1.5 V step; G = 3.16 | | <1 | | ns |
| NOISE/HARMONIC PERFORMANCE | See Figure 51 for distortion test circuit | | | | |
| Second Harmonic | $V_{OUT,\,dm}$ = 2 V p-p; 10 MHz | | −112 | | dBc |
| | $V_{OUT,\,dm}$ = 2 V p-p; 70 MHz | | −84 | | dBc |
| | $V_{OUT,\,dm}$ = 2 V p-p; 100 MHz | | −77 | | dBc |
| Third Harmonic | $V_{OUT,\,dm}$ = 2 V p-p; 10 MHz | | −102 | | dBc |
| | $V_{OUT,\,dm}$ = 2 V p-p; 70 MHz | | −91 | | dBc |
| | $V_{OUT,\,dm}$ = 2 V p-p; 100 MHz | | −84 | | dBc |
| IMD | $f_1$ = 70 MHz; $f_2$ = 70.1 MHz; $V_{OUT,\,dm}$ = 2 V p-p | | −91 | | dBc |
| Voltage Noise (RTI) | f = 100 kHz | | 2.2 | | nV/√Hz |
| Input Current Noise | f = 100 kHz | | 4 | | pA/√Hz |
| Noise Figure | G = 4; $R_T$ = 136 Ω; $R_F$ = 200 Ω; $R_G$ = 37 Ω; f = 100 MHz | | 15 | | dB |
| Crosstalk (ADA4937-2) | f = 100 MHz | | −72 | | dB |
| INPUT CHARACTERISTICS | | | | | |
| Offset Voltage | $V_{OS,\,dm}$ = $V_{OUT,\,dm}/2$; $V_{DIN+}$ = $V_{DIN-}$ = 2.5 V | −2.5 | ±0.5 | +2.5 | mV |
| | $T_{MIN}$ to $T_{MAX}$ variation | | ±1 | | µV/°C |
| Input Bias Current | | −50 | −30 | −10 | µA |
| | $T_{MIN}$ to $T_{MAX}$ variation | | 0.01 | | µA/°C |
| Input Offset Current | | −2 | +0.5 | +2 | µA |
| Input Resistance | Differential | | 6 | | MΩ |
| | Common mode | | 3 | | MΩ |
| Input Capacitance | | | 1 | | pF |
| Input Common-Mode Voltage | | | 0.3 to 3.0 | | V |
| CMRR | $\Delta V_{OUT,\,dm}/\Delta V_{IN,\,cm}$; $\Delta V_{IN,\,cm}$ = ±1 V | −69 | −80 | | dB |
| OUTPUT CHARACTERISTICS | | | | | |
| Output Voltage Swing | Maximum $\Delta V_{OUT}$; single-ended output; $R_F$ = $R_G$ = 10 kΩ | 0.9 | | 4.1 | V |
| Linear Output Current | Per amplifier; $R_{L,\,dm}$ = 20 Ω; f = 10 MHz | | ±70 | | mA |
| Output Balance Error | $\Delta V_{OUT,\,cm}/\Delta V_{OUT,\,dm}$; $\Delta V_{OUT,\,dm}$ = 1 V; f = 10 MHz; see Figure 50 for test circuit | | −61 | | dB |

### *$V_{OCM}$ to ±OUT Performance*

**Table 2.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{OCM}$ DYNAMIC PERFORMANCE | | | | | |
| −3 dB Bandwidth | | | 440 | | MHz |
| Slew Rate | $V_{IN}$ = 1.5 V to 3.5 V; 25% to 75% | | 1150 | | V/μs |
| Input Voltage Noise (RTI) | f = 100 kHz | | 7.5 | | nV/√Hz |
| $V_{OCM}$ INPUT CHARACTERISTICS | | | | | |
| Input Voltage Range | | 1.2 | | 3.8 | V |
| Input Resistance | | 8 | 10 | 12 | kΩ |
| Input Offset Voltage | $V_{OS, cm} = V_{OUT, cm}$; $V_{DIN+} = V_{DIN-} = +V_S/2$ | | 2 | 7.1 | mV |
| Input Bias Current | | | 0.5 | | μA |
| $V_{OCM}$ CMRR | $\Delta V_{OUT, dm}/\Delta V_{OCM}$; $\Delta V_{OCM} = \pm 1$ V | −70 | −75 | | dB |
| Gain | $\Delta V_{OUT, cm}/\Delta V_{OCM}$; $\Delta V_{OCM} = \pm 1$ V | 0.97 | 0.98 | 1.00 | V/V |
| POWER SUPPLY | | | | | |
| Operating Range | | 3.0 | | 5.25 | V |
| Quiescent Current per Amplifier | Enabled | 38.0 | 39.5 | 42.0 | mA |
| | $T_{MIN}$ to $T_{MAX}$ variation | | 17 | | μA/°C |
| | Powered down | 0.02 | 0.3 | 0.5 | mA |
| Power Supply Rejection Ratio | $\Delta V_{OUT, dm}/\Delta V_S$; $\Delta V_S = 1$ V | −70 | −90 | | dB |
| POWER-DOWN ($\overline{PD}$) | | | | | |
| $\overline{PD}$ Input Voltage | Powered down | | ≤1 | | V |
| | Enabled | | ≥2 | | V |
| Turn-Off Time | | | 1 | | μs |
| Turn-On Time | | | 200 | | ns |
| $\overline{PD}$ Bias Current per Amplifier | | | | | |
| Enabled | $\overline{PD}$ = 5 V | 10 | 30 | 50 | μA |
| Powered Down | $\overline{PD}$ = 0 V | −300 | −200 | −150 | μA |
| OPERATING TEMPERATURE RANGE | | −40 | | +105 | °C |

## 3.3 V OPERATION

$T_A$ = 25°C, $+V_S$ = 3.3 V, $-V_S$ = 0 V, $V_{OCM}$ = $+V_S/2$, $R_T$ = 61.9 Ω, $R_G$ = $R_F$ = 200 Ω, G = 1, $R_{L,\,dm}$ = 1 kΩ, unless otherwise noted. All specifications refer to single-ended input and differential outputs, unless otherwise noted.

### ±$D_{IN}$ to ±OUT Performance

Table 3.

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DYNAMIC PERFORMANCE | | | | | |
| −3 dB Small Signal Bandwidth | $V_{OUT,\,dm}$ = 0.1 V p-p | | 1800 | | MHz |
| Bandwidth for 0.1 dB Flatness | $V_{OUT,\,dm}$ = 0.1 V p-p | | 200 | | MHz |
| Large Signal Bandwidth | $V_{OUT,\,dm}$ = 2 V p-p | | 1300 | | MHz |
| Slew Rate | $V_{OUT,\,dm}$ = 2 V p-p; 25% to 75% | | 4000 | | V/μs |
| Settling Time | $V_{OUT,\,dm}$ = 2 V p-p | | 7 | | ns |
| Overdrive Recovery Time | $V_{IN}$ = 0 V to 1.0 V step; G = 3.16 | | <1 | | ns |
| NOISE/HARMONIC PERFORMANCE | See Figure 51 for distortion test circuit | | | | |
| Second Harmonic | $V_{OUT,\,dm}$ = 2 V p-p; 10 MHz | | −113 | | dBc |
| | $V_{OUT,\,dm}$ = 2 V p-p; 70 MHz | | −85 | | dBc |
| | $V_{OUT,\,dm}$ = 2 V p-p; 100 MHz | | −77 | | dBc |
| Third Harmonic | $V_{OUT,\,dm}$ = 2 V p-p; 10 MHz | | −95 | | dBc |
| | $V_{OUT,\,dm}$ = 2 V p-p; 70 MHz | | −77 | | dBc |
| | $V_{OUT,\,dm}$ = 2 V p-p; 100 MHz | | −71 | | dBc |
| IMD | $f_1$ = 70 MHz; $f_2$ = 70.1 MHz; $V_{OUT,\,dm}$ = 2 V p-p | | −87 | | dBc |
| Voltage Noise (RTI) | f = 100 kHz | | 2.2 | | nV/√Hz |
| Input Current Noise | f = 100 kHz | | 4 | | pA/√Hz |
| Noise Figure | G = 4; $R_T$ = 136 Ω; $R_F$ = 200 Ω; $R_G$ = 37 Ω; f = 100 MHz | | 15 | | dB |
| Crosstalk (ADA4937-2) | f = 100 MHz | | −72 | | dB |
| INPUT CHARACTERISTICS | | | | | |
| Offset Voltage | $V_{OS,\,dm}$ = $V_{OUT,\,dm}/2$; $V_{DIN+}$ = $V_{DIN-}$ = $+V_S/2$ | −2.5 | ±0.5 | +2.5 | mV |
| | $T_{MIN}$ to $T_{MAX}$ variation | | ±1 | | μV/°C |
| Input Bias Current | | −50 | −30 | −10 | μA |
| | $T_{MIN}$ to $T_{MAX}$ variation | | 0.01 | | μA/°C |
| Input Resistance | Differential | | 6 | | MΩ |
| | Common mode | | 3 | | MΩ |
| Input Capacitance | | | 1 | | pF |
| Input Common-Mode Voltage | | | 0.3 to 1.2 | | V |
| CMRR | $\Delta V_{OUT,\,dm}/\Delta V_{IN,\,cm}$; $\Delta V_{IN,\,cm}$ = ±1 V | −67 | −80 | | dB |
| OUTPUT CHARACTERISTICS | | | | | |
| Output Voltage Swing | Maximum $\Delta V_{OUT}$; single-ended output; $R_F$ = $R_G$ = 10 kΩ | 0.8 | | 2.5 | V |
| Linear Output Current | Per amplifier; $R_{L,\,dm}$ = 20 Ω; f = 10 MHz | | ±47 | | mA |
| Output Balance Error | $\Delta V_{OUT,\,cm}/\Delta V_{OUT,\,dm}$; $\Delta V_{OUT,\,dm}$ = 1 V; f = 10 MHz; see Figure 50 for test circuit | | −61 | | dB |

### $V_{OCM}$ to ±OUT Performance

Table 4.

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{OCM}$ DYNAMIC PERFORMANCE | | | | | |
| −3 dB Bandwidth | | | 440 | | MHz |
| Slew Rate | $V_{IN}$ = 0.9 V to 2.4 V; 25% to 75% | | 900 | | V/μs |
| Input Voltage Noise (RTI) | f = 100 kHz | | 7.5 | | nV/√Hz |
| $V_{OCM}$ INPUT CHARACTERISTICS | | | | | |
| Input Voltage Range | | 1.2 | | 2.1 | V |
| Input Resistance | | | 10 | | kΩ |
| Input Offset Voltage | $V_{OS, cm} = V_{OUT, cm}$; $V_{DIN+} = V_{DIN-}$ = 1.67 V | | 2 | 7.1 | mV |
| Input Bias Current | | | 0.5 | | μA |
| $V_{OCM}$ CMRR | $\Delta V_{OUT, dm}/\Delta V_{OCM}$; $\Delta V_{OCM}$ = ±1 V | −70 | −75 | | dB |
| Gain | $\Delta V_{OUT, cm}/\Delta V_{OCM}$; $\Delta V_{OCM}$ = ±1 V | 0.97 | 0.98 | 1.00 | V/V |
| POWER SUPPLY | | | | | |
| Operating Range | | 3.0 | | 5.25 | V |
| Quiescent Current per Amplifier | Enabled | 36 | 38 | 40 | mA |
| | $T_{MIN}$ to $T_{MAX}$ variation | | 17 | | μA/°C |
| | Powered down | 0.02 | 0.2 | 0.5 | mA |
| Power Supply Rejection Ratio | $\Delta V_{OUT, dm}/\Delta V_S$; $\Delta V_S$ = 1 V | −70 | −90 | | dB |
| POWER-DOWN ($\overline{PD}$) | | | | | |
| $\overline{PD}$ Input Voltage | Powered down | | ≤1 | | V |
| | Enabled | | ≥2 | | V |
| Turn-Off Time | | | 1 | | μs |
| Turn-On Time | | | 200 | | ns |
| $\overline{PD}$ Bias Current per Amplifier | | | | | |
| Enabled | $\overline{PD}$ = 3.3 V | 10 | 20 | 30 | μA |
| Powered Down | $\overline{PD}$ = 0 V | −200 | −120 | −100 | μA |
| OPERATING TEMPERATURE RANGE | | −40 | | +105 | °C |

# ABSOLUTE MAXIMUM RATINGS

**Table 5.**

| Parameter | Rating |
|---|---|
| Supply Voltage | 5.5 V |
| Power Dissipation | See Figure 4 |
| Storage Temperature Range | −65°C to +125°C |
| Operating Temperature Range | −40°C to +105°C |
| Lead Temperature (Soldering, 10 sec) | 300°C |
| Junction Temperature | 150°C |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the device (including exposed pad) soldered to a high thermal conductivity 2s2p circuit board, as described in EIA/JESD51-7.

**Table 6. Thermal Resistance**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 16-Lead LFCSP (Exposed Pad) | 95 | 12.6 | °C/W |
| 24-Lead LFCSP (Exposed Pad) | 67 | 8.78 | °C/W |

### *Maximum Power Dissipation*

The maximum safe power dissipation in the ADA4937-1/ ADA4937-2 packages is limited by the associated rise in junction temperature ($T_J$) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes the properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4937-1/ ADA4937-2. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package ($P_D$) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive. The quiescent power is the voltage between the supply pins ($V_S$) times the quiescent current ($I_S$). The power dissipated due to the load drive depends upon the particular application. The power due to load drive is calculated by multiplying the load current by the associated voltage drop across the device. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation, effectively reducing $\theta_{JA}$. In addition, more metal directly in contact with the package leads/exposed pad from metal traces, through holes, ground, and power planes reduces $\theta_{JA}$.

Figure 4 shows the maximum safe power dissipation in the package vs. the ambient temperature for the ADA4937-1 single 16-lead LFCSP (95°C/W), and the ADA4937-2 dual 24-lead LFCSP (67°C/W) on a JEDEC standard 4-layer board.

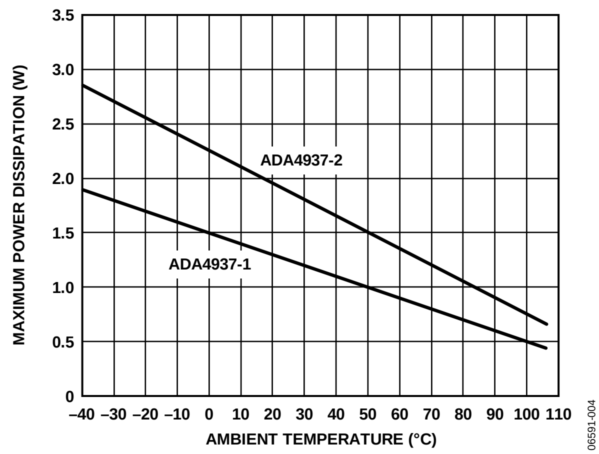
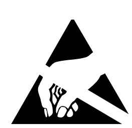



*Figure 4. Maximum Power Dissipation vs. Temperature, 4-Layer Board*

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

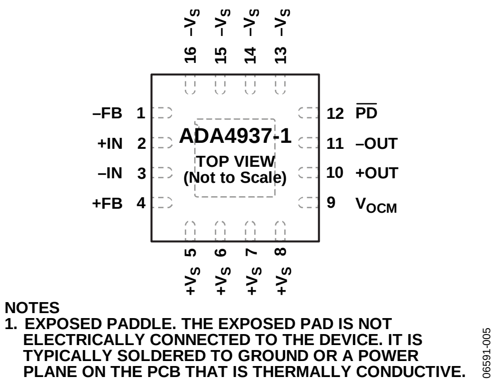



*Figure 5. ADA4937-1 Pin Configuration*

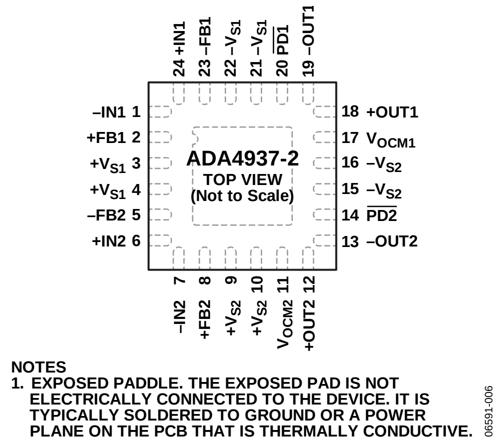



*Figure 6. ADA4937-2 Pin Configuration*

**Table 7. ADA4937-1 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | −FB | Negative Output for Feedback Component Connection. |
| 2 | +IN | Positive Input Summing Node. |
| 3 | −IN | Negative Input Summing Node. |
| 4 | +FB | Positive Output for Feedback Component Connection. |
| 5 to 8 | $+V_S$ | Positive Supply Voltage. |
| 9 | $V_{OCM}$ | Output Common-Mode Voltage. |
| 10 | +OUT | Positive Output for Load Connection. |
| 11 | −OUT | Negative Output for Load Connection. |
| 12 | $\overline{PD}$ | Power-Down Pin. |
| 13 to 16 | $-V_S$ | Negative Supply Voltage. |
| EP | | Exposed Paddle. The exposed pad is not electrically connected to the device. It is typically soldered to ground or a power plane on the PCB that is thermally conductive. |

**Table 8. ADA4937-2 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | −IN1 | Negative Input Summing Node 1. |
| 2 | +FB1 | Positive Output Feedback Pin 1. |
| 3, 4 | $+V_{S1}$ | Positive Supply Voltage 1. |
| 5 | −FB2 | Negative Output Feedback Pin 2. |
| 6 | +IN2 | Positive Input Summing Node 2. |
| 7 | −IN2 | Negative Input Summing Node 2. |
| 8 | +FB2 | Positive Output Feedback Pin 2. |
| 9, 10 | $+V_{S2}$ | Positive Supply Voltage 2. |
| 11 | $V_{OCM2}$ | Output Common-Mode Voltage 2. |
| 12 | +OUT2 | Positive Output 2. |
| 13 | −OUT2 | Negative Output 2. |
| 14 | $\overline{PD2}$ | Power-Down Pin 2. |
| 15, 16 | $-V_{S2}$ | Negative Supply Voltage 2. |
| 17 | $V_{OCM1}$ | Output Common-Mode Voltage 1. |
| 18 | +OUT1 | Positive Output 1. |
| 19 | −OUT1 | Negative Output 1. |
| 20 | $\overline{PD1}$ | Power-Down Pin 1. |
| 21, 22 | $-V_{S1}$ | Negative Supply Voltage 1. |
| 23 | −FB1 | Negative Output Feedback Pin 1. |
| 24 | +IN1 | Positive Input Summing Node 1. |
| EP | | Exposed Paddle. The exposed pad is not electrically connected to the device. It is typically soldered to ground or a power plane on the PCB that is thermally conductive. |

# TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C, $+V_S$ = 5 V, $-V_S$ = 0 V, $V_{OUT,\,dm}$ = 2 V p-p, $V_{OCM}$ = $+V_S/2$, $R_T$ = 61.9 Ω, $R_G$ = $R_F$ = 200 Ω, G = 1, $R_{L,\,dm}$ = 1 kΩ, unless otherwise noted. Refer to Figure 49 for the test setup circuit.

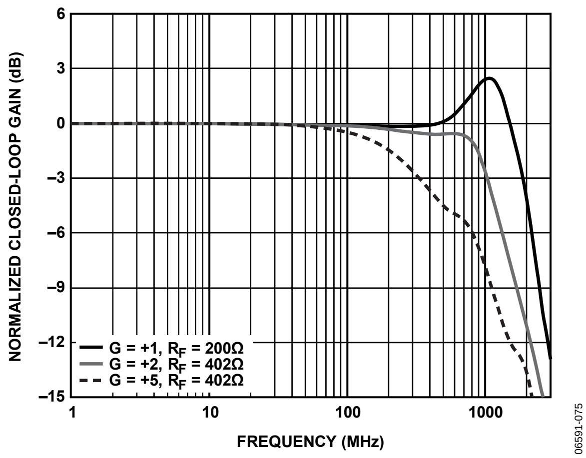



*Figure 7. Small Signal Frequency Response for Various Gains, $V_{OUT,\,dm}$ = 100 mV p-p*

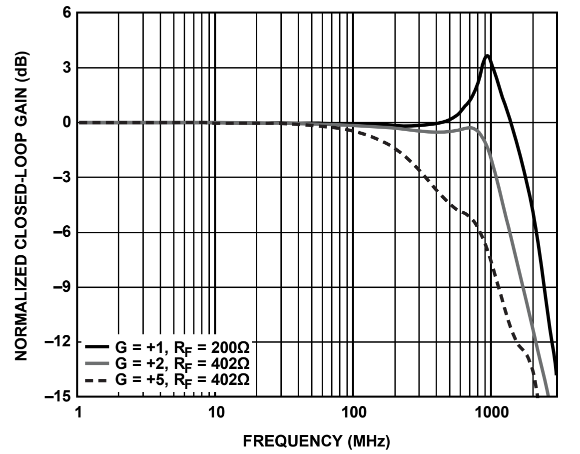



*Figure 10. Large Signal Frequency Response for Various Gains*

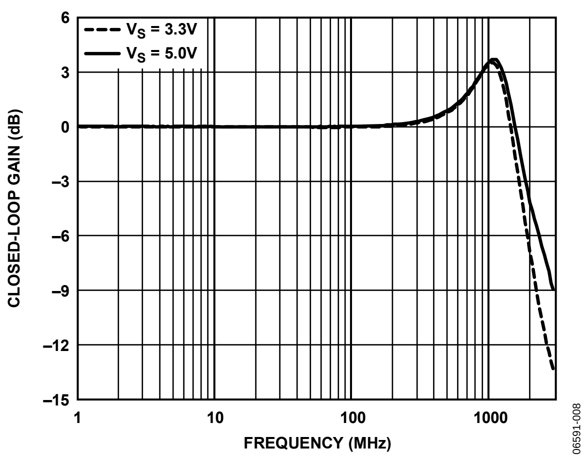



*Figure 8. Small Signal Frequency Response for Various Supplies, $V_{OUT,\,dm}$ = 100 mV p-p*

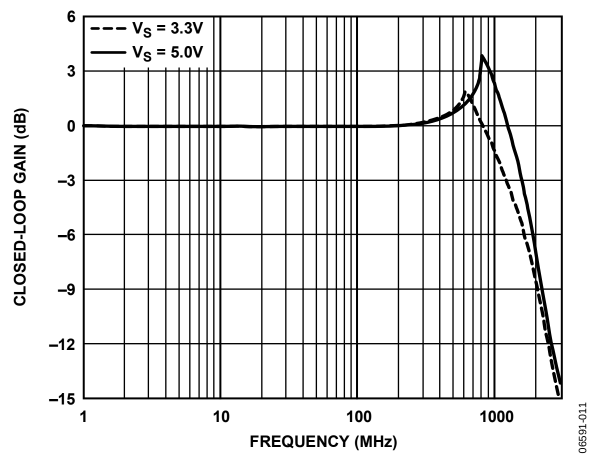



*Figure 11. Large Signal Frequency Response for Various Supplies*

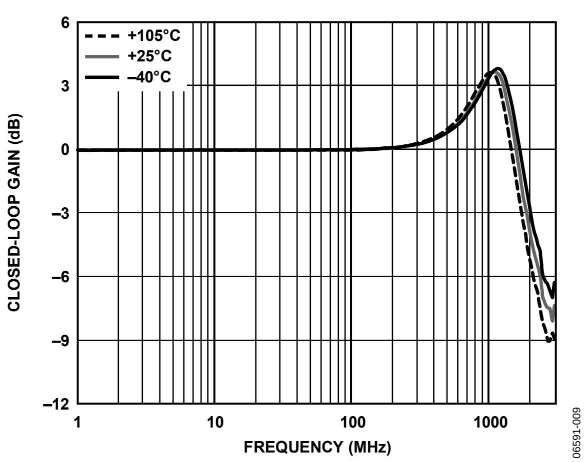



*Figure 9. Small Signal Frequency Response for Various Temperatures, $V_{OUT,\,dm}$ = 100 mV p-p*

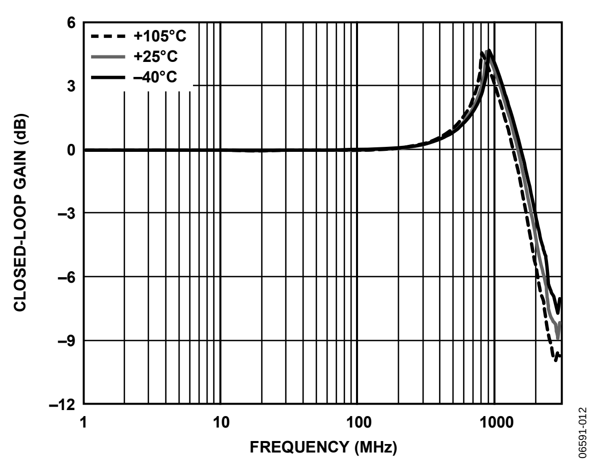



*Figure 12. Large Signal Frequency Response for Various Temperatures*

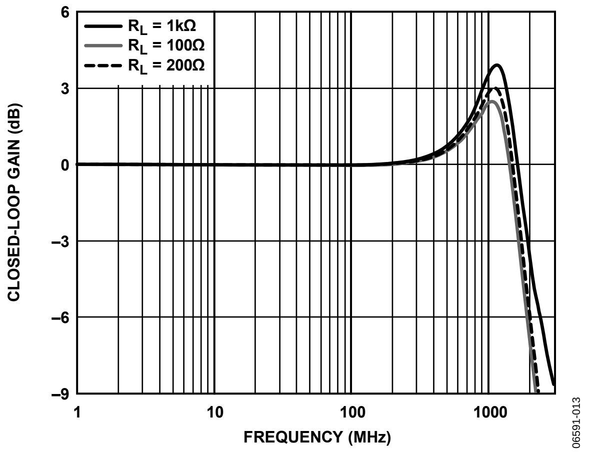



Figure 13. Small Signal Frequency Response for Various Loads, $V_{OUT, dm}$ = 100 mV p-p

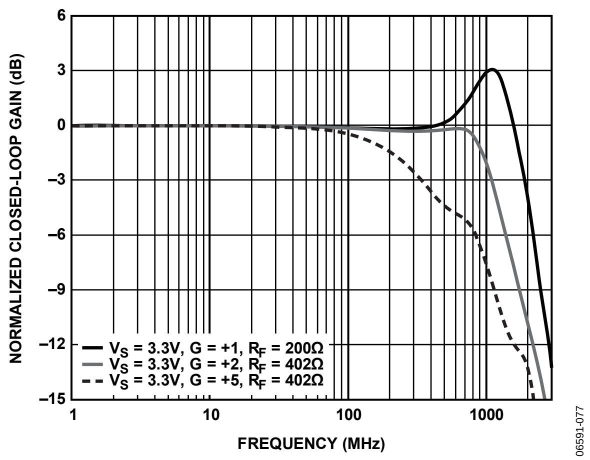



Figure 14. Small Signal Frequency Response for Various Gains, $V_S$ = 3.3 V, $V_{OUT, dm}$ = 100 mV p-p

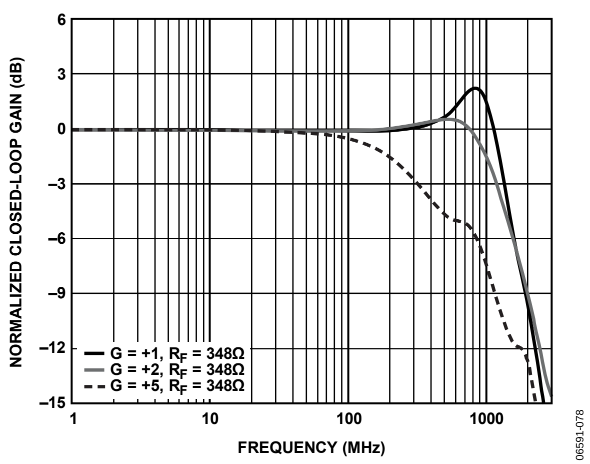



Figure 15. Small Signal Frequency Response for Various Gains, $V_{OUT, dm}$ = 100 mV p-p, $R_F$ = 348 Ω

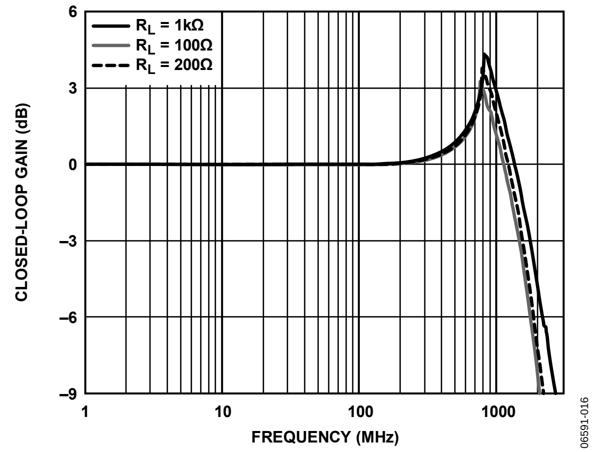



Figure 16. Large Signal Frequency Response for Various Loads

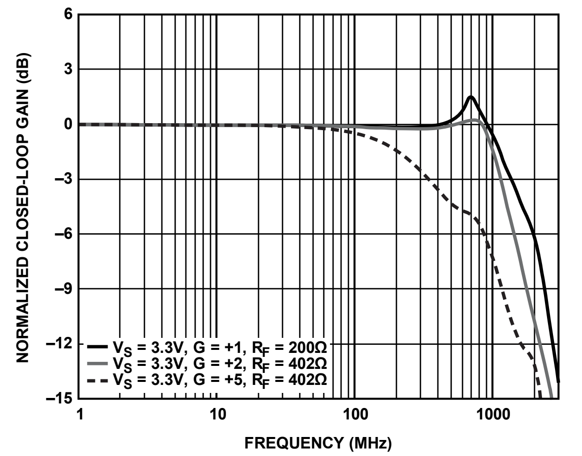



Figure 17. Large Signal Frequency Response for Various Gains, $V_S$ = 3.3 V

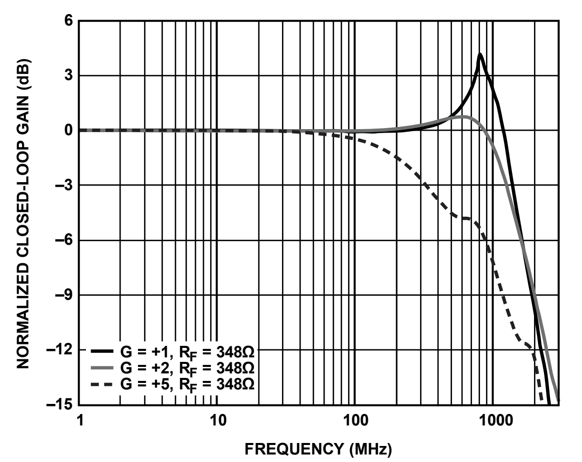



Figure 18. Large Signal Frequency Response for Various Gains, $R_F$ = 348 Ω

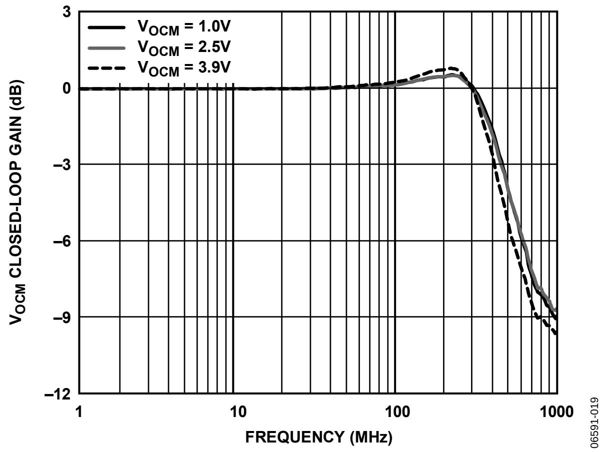


Figure 19. Small Signal Frequency Response for Various $V_{OCM}$

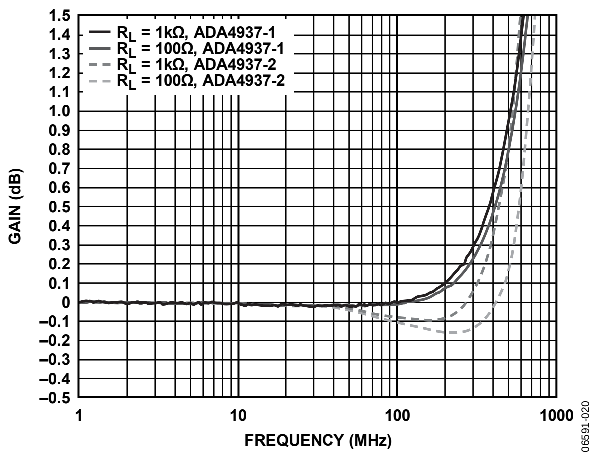


Figure 20. 0.1 dB Flatness Response for Various Loads

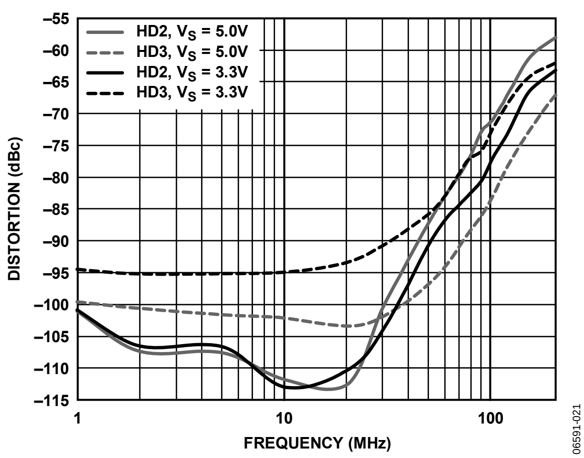


Figure 21. Harmonic Distortion vs. Frequency and Supply Voltage

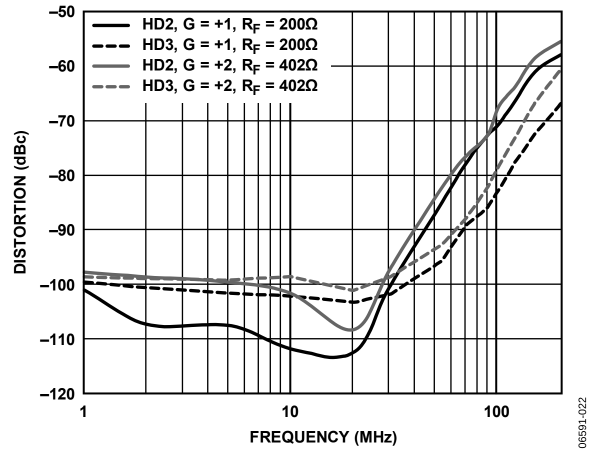


Figure 22. Harmonic Distortion vs. Frequency and Gain

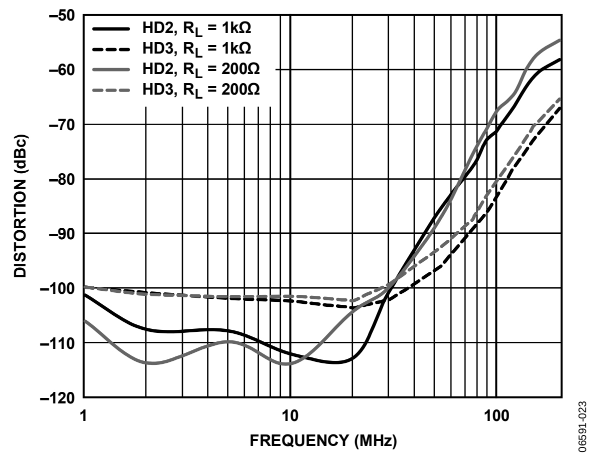


Figure 23. Harmonic Distortion vs. Frequency and Load

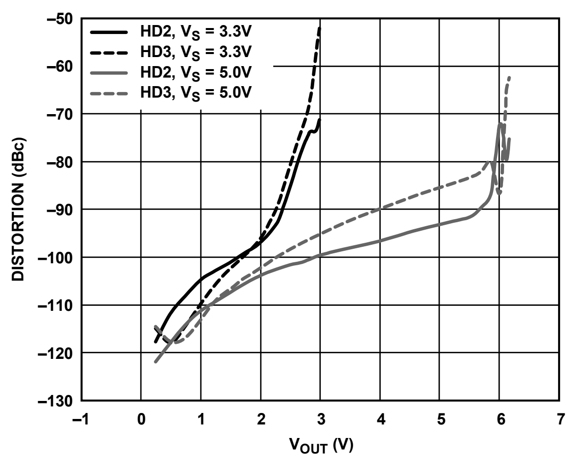


Figure 24. Harmonic Distortion vs. $V_{OUT}$ and Supply Voltage

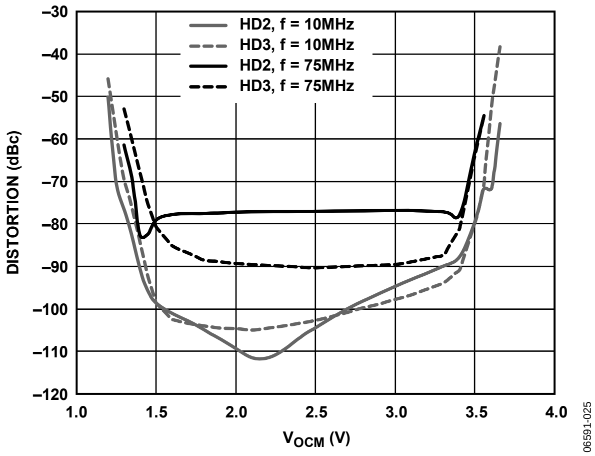



Figure 25. Harmonic Distortion vs. $V_{OCM}$ and Frequency

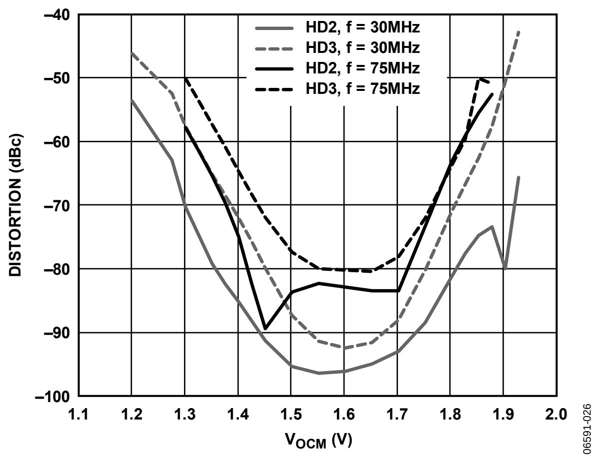



Figure 26. Harmonic Distortion vs. $V_{OCM}$ and Frequency, $V_S$ = 3.3 V

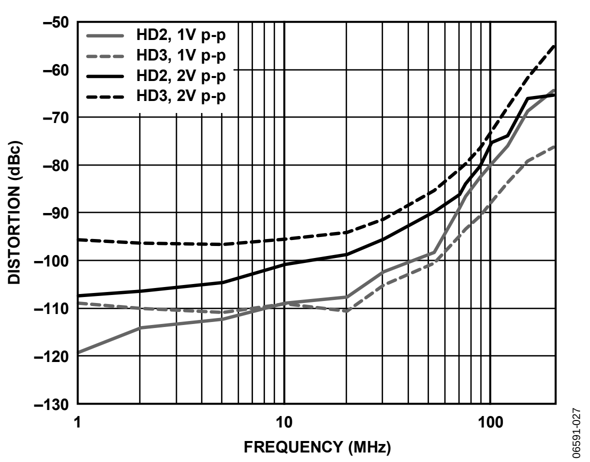



Figure 27. Harmonic Distortion vs. Frequency and $V_{OUT}$, $V_S$ = 3.3 V

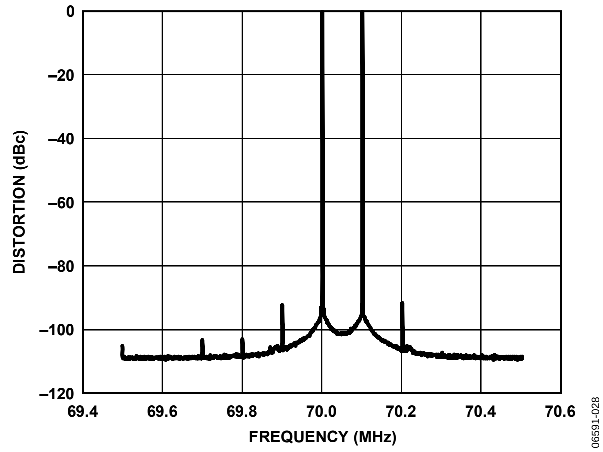



Figure 28. 70 MHz Intermodulation Distortion

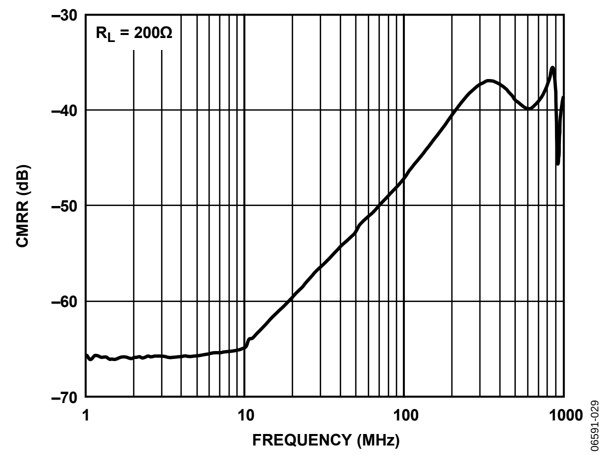



Figure 29. CMRR vs. Frequency

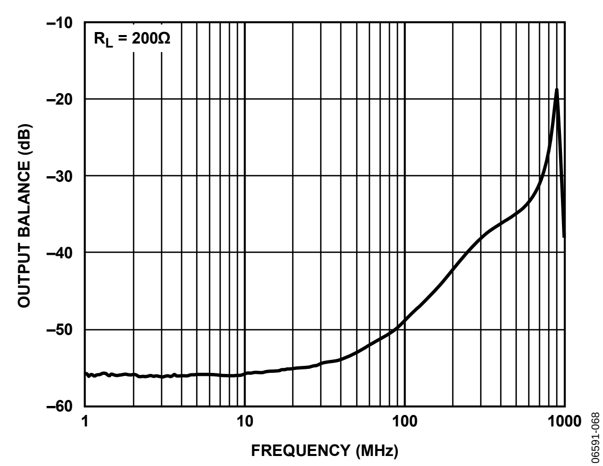



Figure 30. Output Balance vs. Frequency

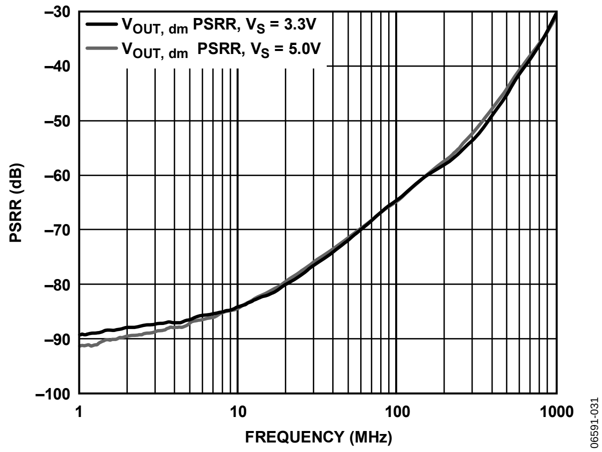



Figure 31. PSRR vs. Frequency, $R_L$ = 200 Ω

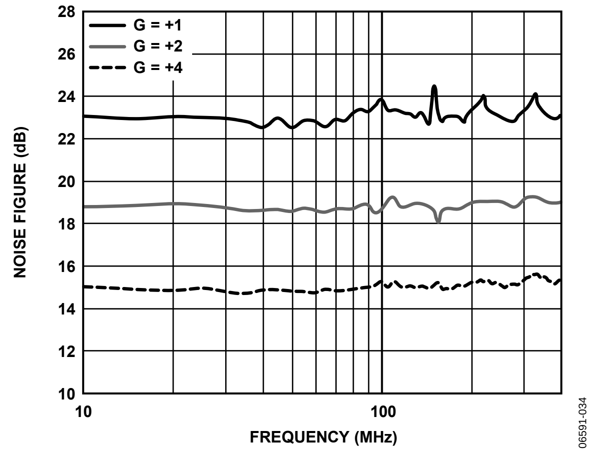



Figure 34. Noise Figure vs. Frequency

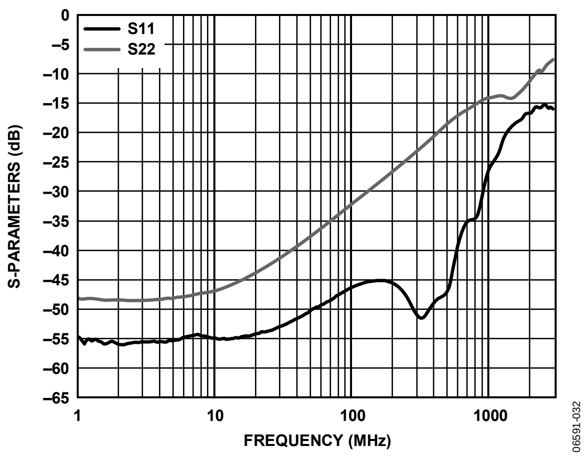



Figure 32. Return Loss (S11, S22) vs. Frequency

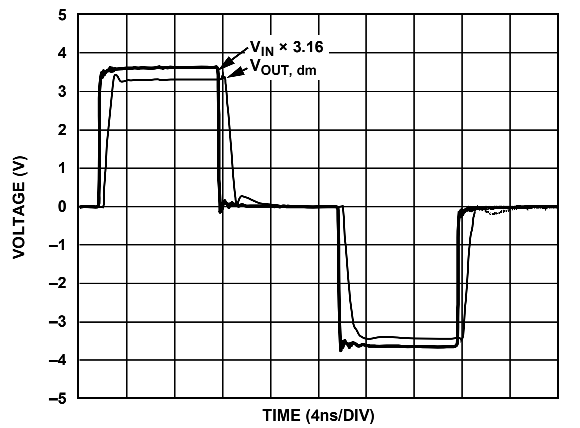



Figure 35. Overdrive Recovery Time (Pulse Input)

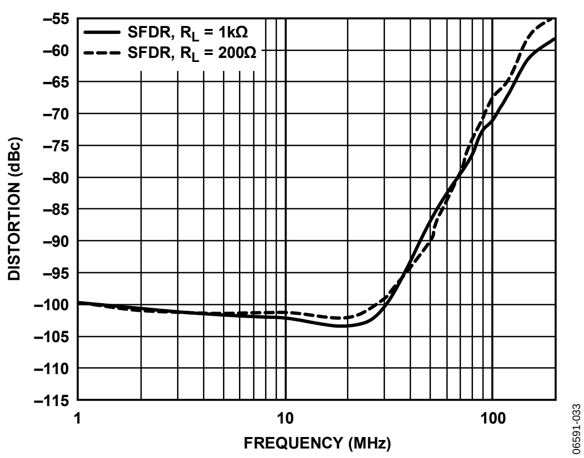



Figure 33. Spurious-Free Dynamic Range vs. Frequency and Load

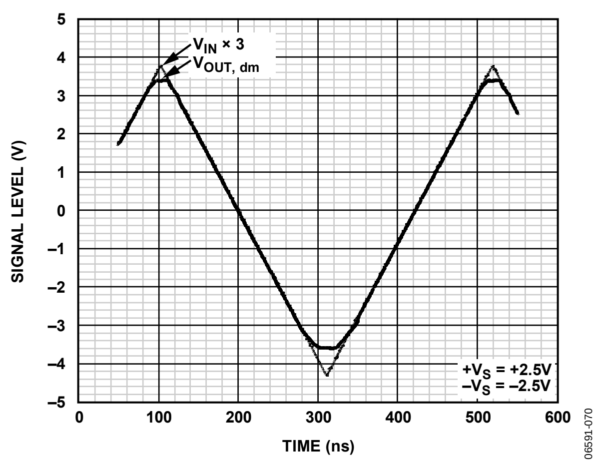



Figure 36. Overdrive Amplitude Characteristics (Triangle Wave Input)

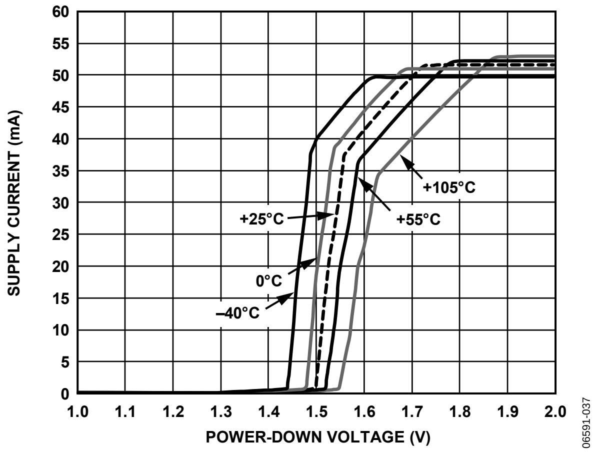



Figure 37. Supply Current vs. $\overline{PD}$ for Various Temperatures

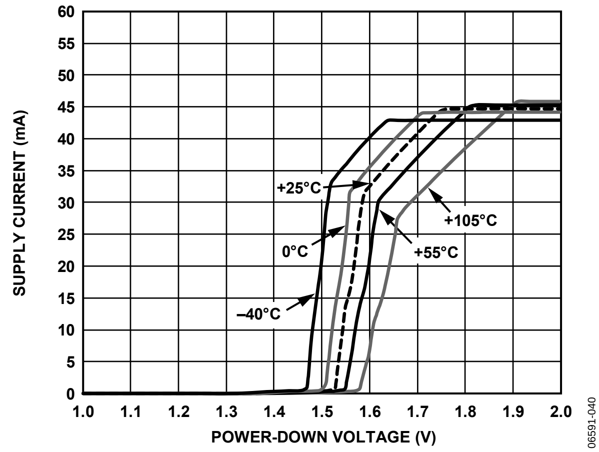



Figure 40. Supply Current vs. $\overline{PD}$ for Various Temperatures, $V_S$ = 3.3 V

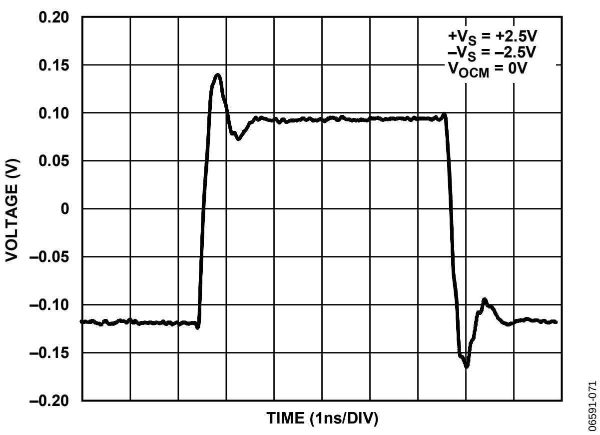



Figure 38. Small Signal Pulse Response

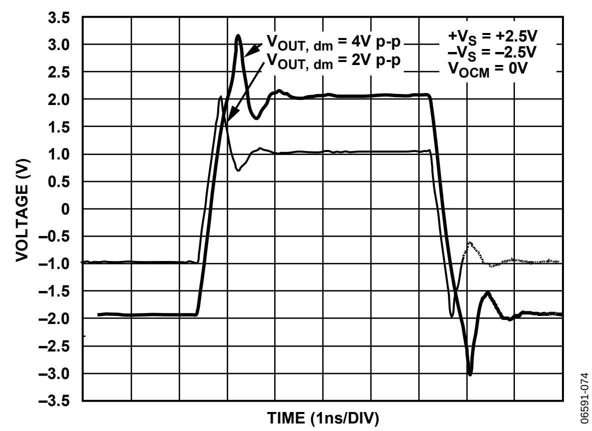



Figure 41. Large Signal Pulse Response

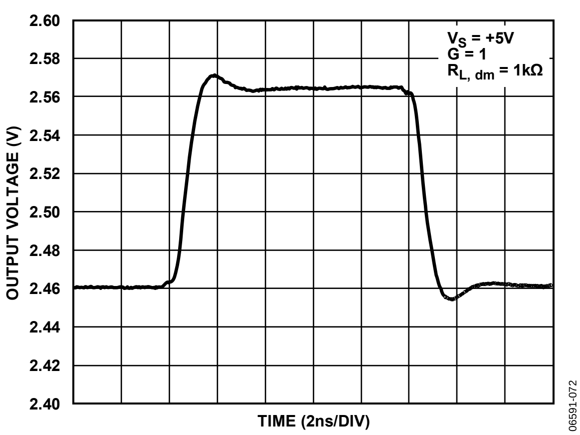



Figure 39. Small Signal $V_{OCM}$ Pulse Response

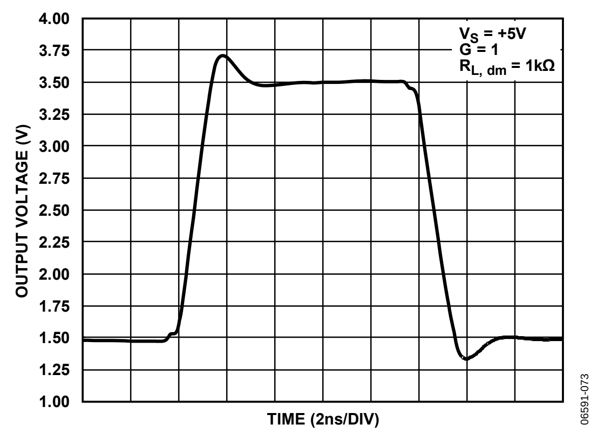



Figure 42. Large Signal $V_{OCM}$ Pulse Response

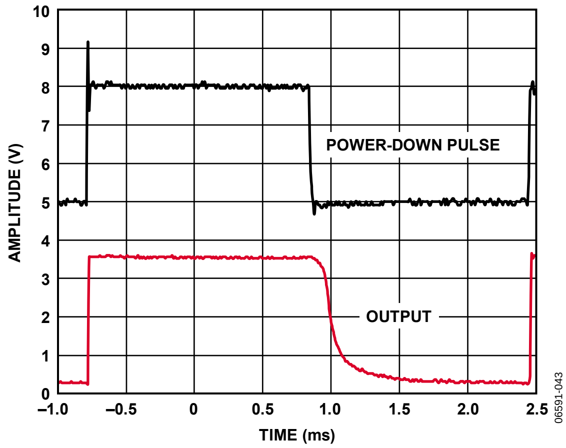



Figure 43. $\overline{PD}$ Response vs. Time

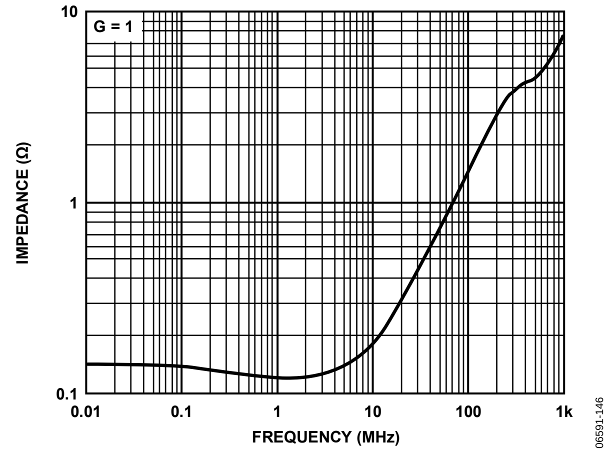



Figure 46. Closed-Loop Output Impedance

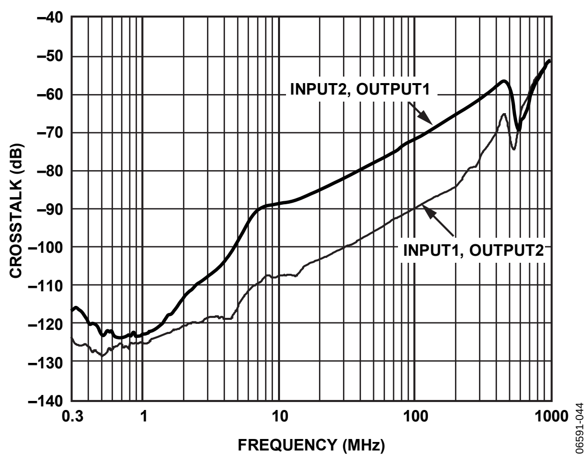



Figure 44. Crosstalk vs. Frequency for ADA4937-2

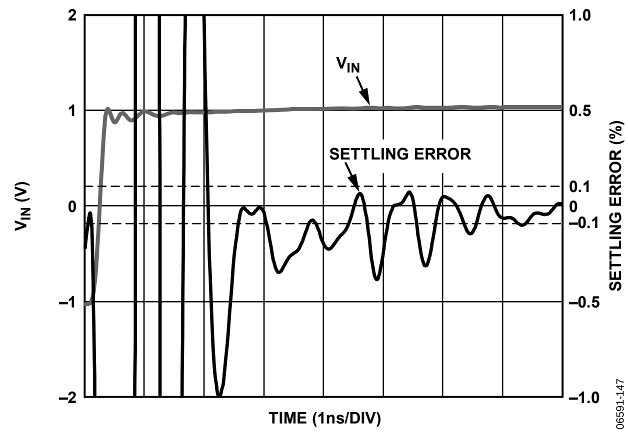



Figure 47. 0.1% Settling Time

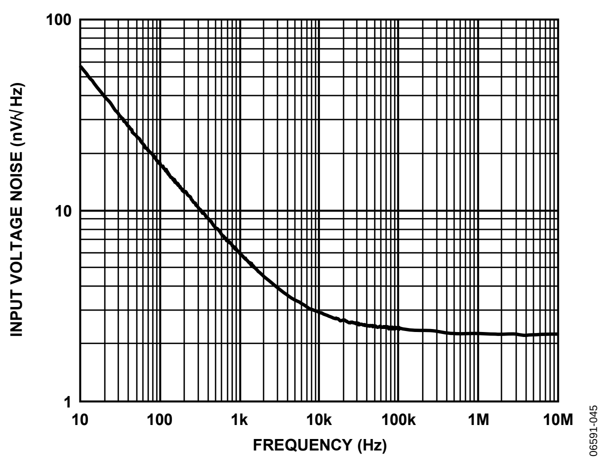



Figure 45. Voltage Spectral Noise Density, RTI

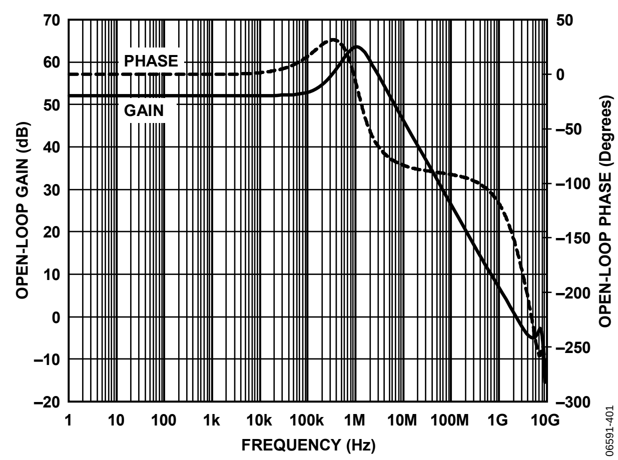



Figure 48. Open-Loop Gain and Phase vs. Frequency

# TEST CIRCUITS

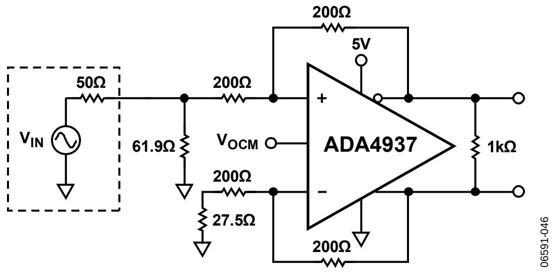



Figure 49. Equivalent Basic Test Circuit

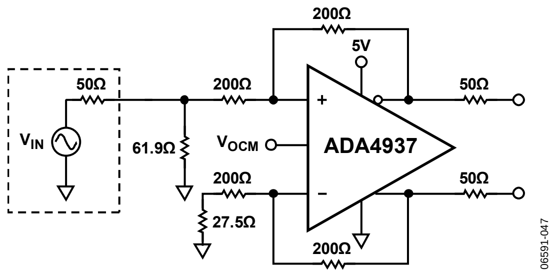



Figure 50. Test Circuit for Output Balance

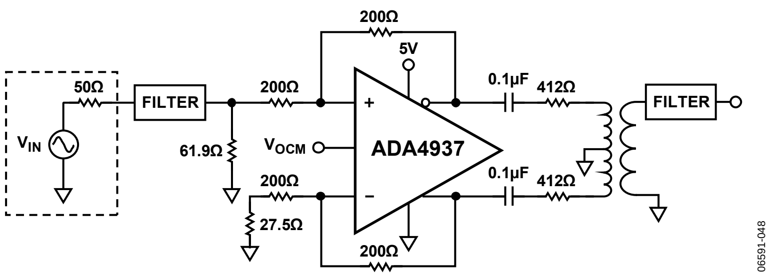



Figure 51. Test Circuit for Distortion Measurements

# TERMINOLOGY

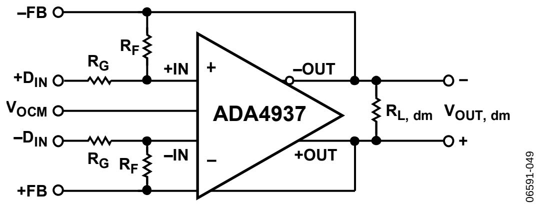



*Figure 52. Circuit Definitions*

**Differential Voltage**

Differential voltage refers to the difference between two node voltages. For example, the output differential voltage (or equivalently, output differential-mode voltage) is defined as

$$V_{OUT,\,dm} = (V_{+OUT} - V_{-OUT})$$

where $V_{+OUT}$ and $V_{-OUT}$ refer to the voltages at the +OUT and −OUT terminals with respect to a common reference.

**Common-Mode Voltage**

Common-mode voltage refers to the average of two node voltages. The output common-mode voltage is defined as

$$V_{OUT,\,cm} = (V_{+OUT} + V_{-OUT})/2$$

**Output Balance**

Output balance is a measure of how close the differential signals are to being equal in amplitude and opposite in phase. Output balance is most easily determined by placing a well-matched resistor divider between the differential voltage nodes and comparing the magnitude of the signal at the midpoint of the divider with the magnitude of the differential signal (see Figure 50). By this definition, output balance is the magnitude of the output common-mode voltage divided by the magnitude of the output differential mode voltage.

$$Output\ Balance\ Error = \left|\frac{V_{OUT,\,cm}}{V_{OUT,\,dm}}\right|$$

# THEORY OF OPERATION

The ADA4937-1/ADA4937-2 differ from conventional operational amplifiers in that they have two outputs whose voltages move in opposite directions. Like an operational amplifier, they rely on open-loop gain and negative feedback to force these outputs to the desired voltages. The ADA4937-1/ADA4937-2 behave much like standard voltage feedback operational amplifiers, which makes it easier to perform single-ended-to-differential conversions, common-mode level shifting, and amplifications of differential signals. Also like an operational amplifier, the ADA4937-1/ADA4937-2 have high input impedance and low output impedance.

Two feedback loops control the differential and common-mode output voltages. The differential feedback loop, set with external resistors, controls only the differential output voltage. The common-mode feedback loop controls only the common-mode output voltage. This architecture makes it easy to set the output common-mode level to any arbitrary value. It is forced, by internal common-mode feedback, to be equal to the voltage applied to the $V_{OCM}$ input without affecting the differential output voltage.

The ADA4937-1/ADA4937-2 architecture results in outputs that are highly balanced over a wide frequency range without requiring tightly matched external components. The common-mode feedback loop forces the signal component of the output common-mode voltage to zero. This results in nearly perfectly balanced differential outputs that are identical in amplitude and are exactly 180° apart in phase.

## ANALYZING AN APPLICATION CIRCUIT

The ADA4937-1/ADA4937-2 use open-loop gain and negative feedback to force their differential and common-mode output voltages in such a way as to minimize the differential and common-mode error voltages. The differential error voltage is defined as the voltage between the differential inputs labeled +IN and −IN (see Figure 52). For most purposes, this voltage can be assumed to be zero. Similarly, the difference between the actual output common-mode voltage and the voltage applied to $V_{OCM}$ can also be assumed to be zero. Starting from these two assumptions, any application circuit can be analyzed.

## SETTING THE CLOSED-LOOP GAIN

The differential-mode gain of the circuit in Figure 52 can be determined by

$$\left|\frac{V_{OUT,dm}}{V_{IN,dm}}\right| = \frac{R_F}{R_G}$$

This assumes that the input resistors ($R_G$) and feedback resistors ($R_F$) on each side are equal.

## ESTIMATING THE OUTPUT NOISE VOLTAGE

To estimate the differential output noise of the ADA4937-1/ADA4937-2 use the noise model in Figure 53. The input-referred noise voltage density, $v_{nIN}$, is modeled as a differential input, and the noise currents, $i_{nIN-}$ and $i_{nIN+}$, appear between each input and ground. The noise currents are assumed to be equal and produce a voltage across the parallel combination of the gain and feedback resistances. $v_{n,cm}$ is the noise voltage density at the $V_{OCM}$ pin. Each of the four resistors contributes $(4kTR_x)^{1/2}$. Table 9 summarizes the input noise sources, the multiplication factors, and the output-referred noise density terms.

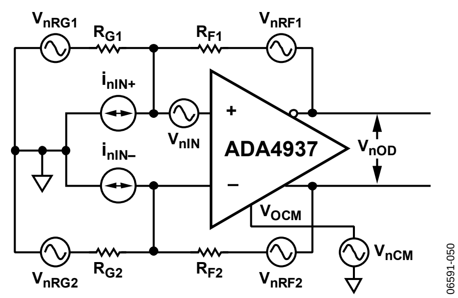



Figure 53. ADA4937-1/ADA4937-2 Noise Model

**Table 9. Output Noise Voltage Density Calculations**

| Input Noise Contribution | Input Noise Term | Input Noise Voltage Density | Output Multiplication Factor | Output Noise Voltage Density Term |
|---|---|---|---|---|
| Differential Input | $v_{nIN}$ | $v_{nIN}$ | $G_N$ | $v_{nO1} = G_N(v_{nIN})$ |
| Inverting Input | $i_{nIN-}$ | $i_{nIN-} \times (R_{G2} \| \| R_{F2})$ | $G_N$ | $v_{nO2} = G_N[i_{nIN-} \times (R_{G2} \| \| R_{F2})]$ |
| Noninverting Input | $i_{nIN+}$ | $i_{nIN+} \times (R_{G1} \| \| R_{F1})$ | $G_N$ | $v_{nO3} = G_N[i_{nIN+} \times (R_{G1} \| \| R_{F1})]$ |
| $V_{OCM}$ Input | $v_{n,cm}$ | $v_{n,cm}$ | $G_N(\beta_1 - \beta_2)$ | $v_{nO4} = G_N(\beta_1 - \beta_2)(v_{n,cm})$ |
| Gain Resistor $R_{G1}$ | $v_{nRG1}$ | $(4kTR_{G1})^{1/2}$ | $G_N(1 - \beta_1)$ | $v_{nO5} = G_N(1 - \beta_1)(4kTR_{G1})^{1/2}$ |
| Gain Resistor $R_{G2}$ | $v_{nRG2}$ | $(4kTR_{G2})^{1/2}$ | $G_N(1 - \beta_2)$ | $v_{nO6} = G_N(1 - \beta_2)(4kTR_{G2})^{1/2}$ |
| Feedback Resistor $R_{F1}$ | $v_{nRF1}$ | $(4kTR_{F1})^{1/2}$ | 1 | $v_{nO7} = (4kTR_{F1})^{1/2}$ |
| Feedback Resistor $R_{F2}$ | $v_{nRF2}$ | $(4kTR_{F2})^{1/2}$ | 1 | $v_{nO8} = (4kTR_{F2})^{1/2}$ |

Similar to the case of a conventional operational amplifier, the output noise voltage densities can be estimated by multiplying the input-referred terms at +IN and −IN by the appropriate output factor, where:

$G_N = \frac{2}{(\beta_1 + \beta_2)}$ is the circuit noise gain.

$\beta_1 = \frac{R_{G1}}{R_{F1} + R_{G1}}$ and $\beta_2 = \frac{R_{G2}}{R_{F2} + R_{G2}}$ are the feedback factors.

When $R_{F1}/R_{G1} = R_{F2}/R_{G2}$, then β1 = β2 = β, and the noise gain becomes

$$G_N = \frac{1}{\beta} = 1 + \frac{R_F}{R_G}$$

Note that the output noise from $V_{OCM}$ goes to zero in this case. The total differential output noise density, $v_{nOD}$, is the root-sum-square of the individual output noise terms.

$$v_{nOD} = \sqrt{\sum_{i=1}^{8} v_{nOi}^2}$$

## IMPACT OF MISMATCHES IN THE FEEDBACK NETWORKS

As previously mentioned in the Setting the Closed-Loop Gain section), even if the external feedback networks ($R_F/R_G$) are mismatched, the internal common-mode feedback loop still forces the outputs to remain balanced. The amplitudes of the signals at each output remain equal and 180° out of phase. The input-to-output differential mode gain varies proportionately to the feedback mismatch, but the output balance is unaffected.

As well as causing a noise contribution from $V_{OCM}$, ratio matching errors in the external resistors result in a degradation of the ability of the circuit to reject input common-mode signals, much the same as for a four-resistor difference amplifier made from a conventional operational amplifier.

In addition, if the dc levels of the input and output common-mode voltages are different, matching errors result in a small differential-mode output offset voltage. When G = 1, with a ground referenced input signal and the output common-mode level set to 2.5 V, an output offset of as much as 25 mV (1% of the difference in common-mode levels) can result if 1% tolerance resistors are used. Resistors of 1% tolerance result in a worst-case input CMRR of approximately 40 dB, a worst-case differential-mode output offset of 25 mV due to 2.5 V level shift, and no significant degradation in output balance error.

## CALCULATING THE INPUT IMPEDANCE FOR AN APPLICATION CIRCUIT

The effective input impedance of a circuit depends on whether the amplifier is being driven by a single-ended or differential signal source. For balanced differential input signals, as shown in Figure 54, the input impedance ($R_{IN,\,dm}$) between the inputs ($+D_{IN}$ and $-D_{IN}$) is simply $R_{IN,\,dm} = 2 \times R_G$.

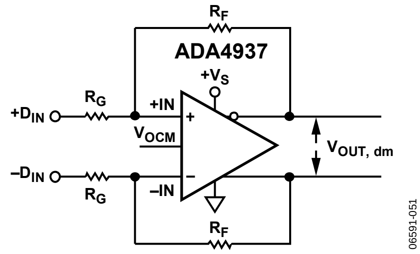



*Figure 54. ADA4937-1/ADA4937-2 Configured for Balanced (Differential) Inputs*

For an unbalanced, single-ended input signal (see Figure 55), the input impedance is

$$R_{IN,\,cm} = \left( \frac{R_G}{1 - \frac{R_F}{2 \times (R_G + R_F)}} \right)$$

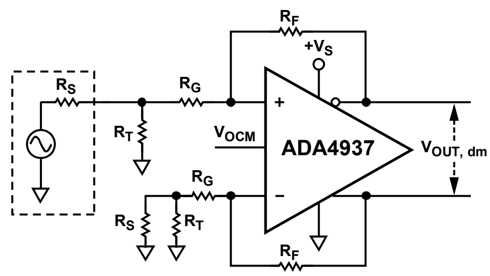



*Figure 55. ADA4937-1/ADA4937-2 Configured for Unbalanced (Single-Ended) Input*

The input impedance of the circuit is effectively higher than it is for a conventional operational amplifier connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the Input Gain Resistor $R_G$.

### *Terminating a Single-Ended Input*

This section explains how to properly terminate a single-ended input to the ADA4937-1/ADA4937-2. Using a simple example with an input source of 2 V and a source resistor of 50 Ω, four simple steps must be followed.

1. The input impedance must be calculated using the formula

$$R_{IN} = \left( \frac{R_G}{1 - \frac{R_F}{2 \times (R_G + R_F)}} \right) = \left( \frac{200}{1 - \frac{200}{2 \times (200 + 200)}} \right) = 267\ \Omega$$

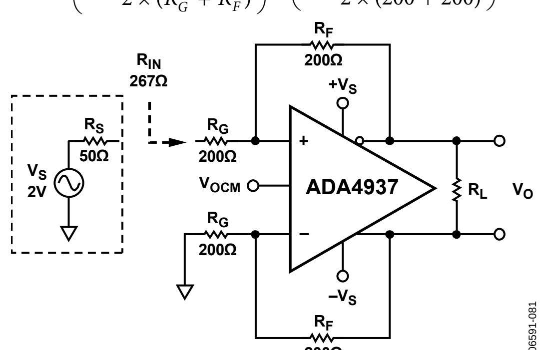



*Figure 56. Single-Ended Input Impedance RIN*

2. For the source termination to be 50 Ω, the termination resistor ($R_T$) is calculated using $R_T||R_{IN}$ = 50 Ω, which makes $R_T$ equal to 61.9 Ω.

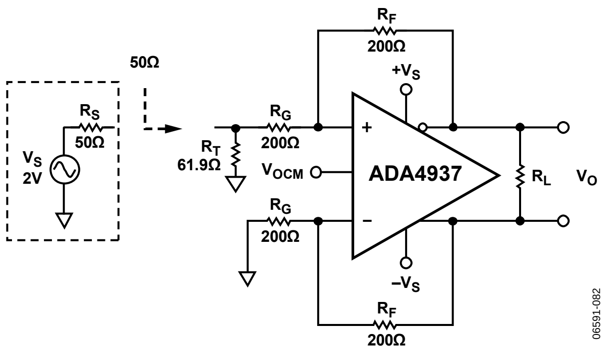



Figure 57. Adding Termination Resistor $R_T$

3. To compensate for the imbalance of the gain resistors, a correction resistor ($R_{TS}$) is added in series with the inverting Input Gain Resistor $R_G$. $R_{TS}$ is equal to the Thevenin equivalent of the Source Resistance $R_S||R_T$.

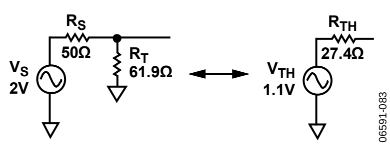



Figure 58. Calculating Thevenin Equivalent

$R_{TS} = R_{TH} = R_S||R_T$ = 27.4 Ω. Note that $V_{TH}$ is not equal to $V_S/2$, which is the case if the termination is not affected by the amplifier circuit.

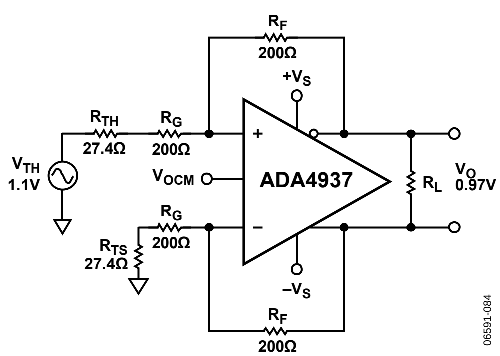



Figure 59. Balancing Gain Resistor $R_G$

4. The feedback resistor is calculated to adjust the output voltage.

   a. To make the output voltage $V_{OUT}$ = 1 V, $R_F$ must be calculated using the following formula:

$$R_F = \left(\frac{V_{OUT} \times (R_G + R_{TS})}{V_{TH}}\right) = \left(\frac{1 \times (200 + 27.4)}{1.1}\right) = 207\,\Omega$$

To make $V_O = V_S$ = 2 V to recover the loss due to the input termination, $R_F$ must be

$$R_F = \left(\frac{V_{OUT} \times (R_G + R_{TS})}{V_{TH}}\right) = \left(\frac{2 \times (200 + 27.4)}{1.1}\right) = 414\,\Omega$$

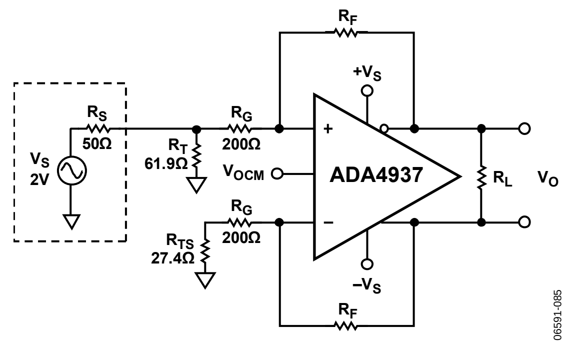



Figure 60. Complete Single-Ended-to-Differential System

## INPUT COMMON-MODE VOLTAGE RANGE IN SINGLE-SUPPLY APPLICATIONS

The ADA4937-1/ADA4937-2 are optimized for level-shifting ground-referenced input signals. As such, the center of the input common-mode range is shifted approximately 1 V down from midsupply. For 5 V single-supply operation, the input common-mode range at the summing nodes of the amplifier is 0.3 V to 3.0 V, and 0.3 V to 1.2 V with a 3.3 V supply. To avoid clipping at the outputs, the voltage swing at the +IN and −IN terminals must be confined to these ranges.

## SETTING THE OUTPUT COMMON-MODE VOLTAGE

The $V_{OCM}$ pin of the ADA4937-1/ADA4937-2 is internally biased at a voltage approximately equal to the midsupply point, $[(+V_S) + (−V_S)]/2$. Relying on this internal bias results in an output common-mode voltage that is within about 100 mV of the expected value.

In cases where more accurate control of the output common-mode level is required, it is recommended that an external source, or resistor divider (10 kΩ or greater resistors), be used. The output common-mode offset listed in Table 2 and Table 4 assumes that the $V_{OCM}$ input is driven by a low impedance voltage source.

It is also possible to connect the $V_{OCM}$ input to a common-mode level (CML) output of an ADC. However, care must be taken to ensure that the output has sufficient drive capability. The input impedance of the $V_{OCM}$ pin is approximately 10 kΩ. If multiple ADA4937-1/ADA4937-2 devices share one reference output, it is recommended that a buffer be used.

Table 10 and Table 11 list several common gain settings, associated resistor values, input impedances, and output noise density values for both balanced and unbalanced input configurations.

## POWER-DOWN OPERATION

The ADA4937-1/ADA4937-2 power-down pin features an internal 25 kΩ pull-up resistor to the positive supply ($+V_S$). This ensures that, with the power-down pin left unconnected (floating), the ADA4937-1/ADA4937-2 turn on. Applying a voltage of ≤1 V turns the ADA4937-1/ADA4937-2 off.

**Table 10. Differential Ground-Referenced Input, DC-Coupled, 1 kΩ Load; See Figure 54**

| Nominal Gain (dB) | $R_F$ (Ω) | $R_G$ (Ω) | $R_{IN, dm}$ (Ω) | Differential Output Noise Density (nV/√Hz) |
|---|---|---|---|---|
| 0 | 200 | 200 | 400 | 5.8 |
| 6 | 402 | 200 | 400 | 9.6 |
| 10 | 402 | 127 | 254 | 12.1 |
| 14 | 402 | 80.6 | 161 | 16.2 |

**Table 11. Single-Ended Ground-Referenced Input, DC-Coupled, $R_S$ = 50 Ω, $R_L$ = 1 kΩ; See Figure 55**

| Nominal Gain (dB) | $R_F$ (Ω) | $R_{G1}$ (Ω) | $R_T$ (Ω) | $R_{IN, cm}$ (Ω) | $R_{G2}$ (Ω)[1] | Differential Output Noise Density (nV/√Hz) |
|---|---|---|---|---|---|---|
| 0 | 200 | 200 | 61.9 | 267 | 226 | 5.5 |
| 6 | 402 | 200 | 60.4 | 301 | 228 | 8.6 |
| 10 | 402 | 127 | 66.5 | 205 | 155 | 10.1 |
| 14 | 402 | 80.6 | 76.8 | 138 | 111 | 12.2 |

[1] $R_{G2} = R_{G1} + (R_S||R_T)$

# LAYOUT, GROUNDING, AND BYPASSING

As high speed devices, the ADA4937-1/ADA4937-2 are sensitive to the PCB environment in which they operate. Realizing their superior performance requires attention to the details of high speed PCB design. This section shows a detailed example of how the design issues of the ADA4937-1 is addressed.

The first requirement is a solid ground plane that covers as much of the board area around the ADA4937-1 as possible. However, the area near the feedback resistors ($R_F$), input gain resistors ($R_G$), and the input summing nodes (Pin 2 and Pin 3) must be cleared of all ground and power planes (see Figure 61). Clearing the ground and power planes minimizes any stray capacitance at these nodes and prevents peaking of the response of the amplifier at high frequencies.

The thermal resistance, $\theta_{JA}$, is specified for the device, including the exposed pad, soldered to a high thermal conductivity 4-layer circuit board, as described in EIA/JESD 51-7.

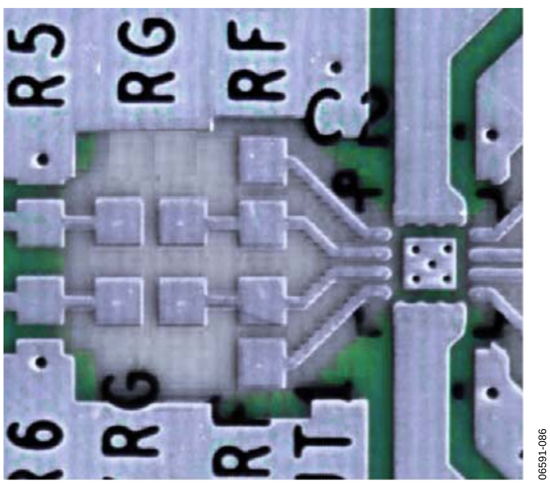



Figure 61. Ground and Power Plane Voiding in Vicinity of $R_F$ and $R_G$

Bypass the power supply pins as close to the device as possible and directly to a nearby ground plane. Use high frequency ceramic chip capacitors. It is recommended that two parallel bypass capacitors (1000 pF and 0.1 μF) be used for each supply with the 1000 pF capacitor placed closer to the device; further away, provide low frequency bypassing using 10 μF tantalum capacitors from each supply to ground.

Signal routing must be short and direct to avoid parasitic effects. Wherever complementary signals exist, provide a symmetrical layout to maximize balanced performance. When routing differential signals over a long distance, keep PCB traces close together and twist any differential wiring to minimize loop area. Doing this reduces radiated energy and makes the circuit less susceptible to interference.

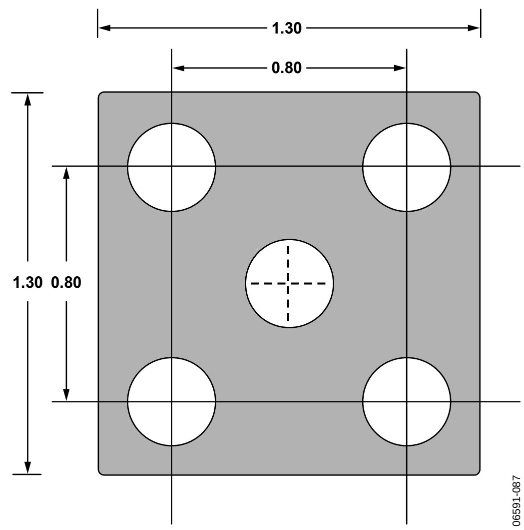



Figure 62. Recommended PCB Thermal Attach Pad Dimensions (mm)

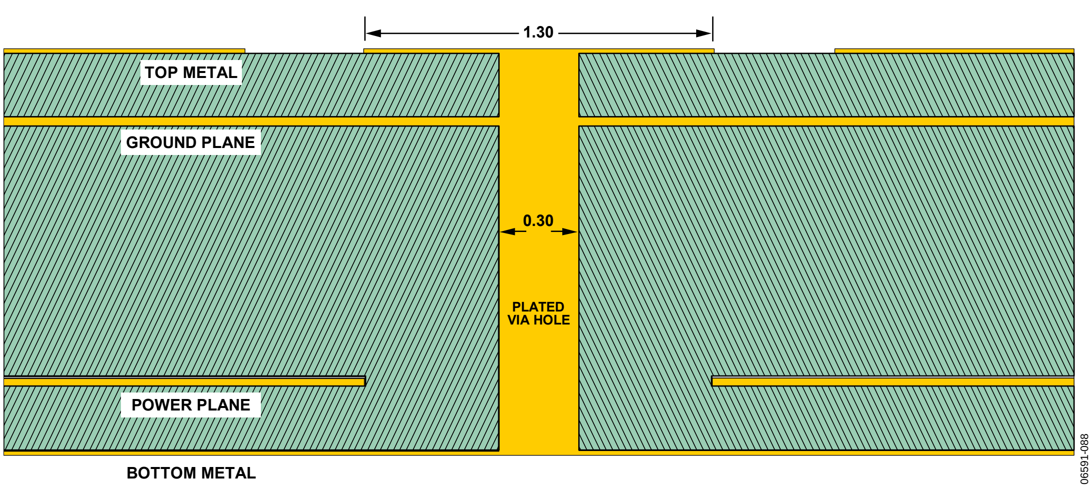



Figure 63. Cross-Section of 4-layer PCB Showing Thermal Via Connection to Buried Ground Plane (Dimensions in mm)

# HIGH PERFORMANCE ADC DRIVING

The ADA4937-1/ADA4937-2 are ideally suited for broadband IF applications. The circuit in Figure 64 shows a front-end connection for an ADA4937-1 driving an AD9445, 14-bit, 105 MSPS ADC. The AD9445 achieves optimum performance when driven differentially. The ADA4937-1/ADA4937-2 eliminate the need for a transformer to drive the ADC and performs a single-ended-to-differential conversion and buffering of the driving signal.

The ADA4937-1/ADA4937-2 are configured with a single 5 V supply and unity gain for a single-ended input to differential output. The 61.9 Ω termination resistor, in parallel with the single-ended input impedance of 267 Ω, provides a 50 Ω termination for the source. The additional 26 Ω (226 Ω total) at the inverting input balances the parallel impedance of the 50 Ω source and the termination resistor driving the noninverting input.

The signal generator has a symmetric, ground-referenced bipolar output. The $V_{OCM}$ pin of the ADA4937-1/ADA4937-2 remains unconnected allowing the internal divider to set the output common-mode voltage at midsupply; one half of the common-mode voltage is fed back to the summing nodes, biasing −IN and +IN at 1.25 V. For a common-mode voltage of 2.5 V, each ADA4937-1/ADA4937-2 output swings between 2.0 V and 3.0 V, providing a 2 V p-p differential output.

The output of the amplifier is ac-coupled to the ADC through a second-order, low-pass filter with a cutoff frequency of 100 MHz. This reduces the noise bandwidth of the amplifier and isolates the driver outputs from the ADC inputs.

The AD9445 is configured for a 2 V p-p full-scale input by connecting the SENSE pin to AGND, as shown in Figure 64.

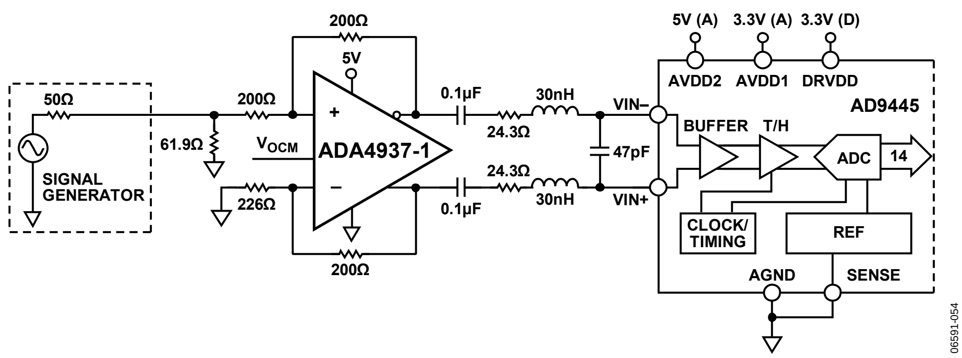



*Figure 64. Driving an AD9445, 14-Bit, 105 MSPS ADC*

The circuit in Figure 66 shows a simplified front-end connection for an ADA4937-1 driving an AD9246, 14-bit, 125 MSPS ADC. The AD9246 achieves optimum performance when driven differentially. The ADA4937-1/ADA4937-2 perform the single-ended-to-differential conversion, eliminating the need for a transformer to drive the ADC.

The ADA4937-1/ADA4937-2 are configured with a single 5 V supply and a gain of ~2 V/V for a single-ended input to differential output. The 76.8 Ω termination resistor, in parallel with the single-ended input impedance of 137 Ω, provides a 50 Ω ac termination for the source. The additional 30 Ω (120 Ω total) at the inverting input balances the parallel ac impedance of the 50 Ω source and the termination resistor driving the noninverting input.

The signal generator has a symmetric, ground-referenced bipolar output. The $V_{OCM}$ pin of the ADA4937-1/ADA4937-2 remains unconnected; therefore, the internal pull-ups set the output common-mode voltage to midsupply. A portion of this is fed back to the summing nodes, biasing −IN and +IN at 0.55 V. For a common-mode voltage of 2.5 V, each ADA4937-1/ADA4937-2 output swings between 2.0 V and 3.0 V, providing a 2 V p-p differential output.

The output is ac-coupled to a single-pole, low-pass filter. This reduces the noise bandwidth of the amplifier and provides some level of isolation from the switched capacitor inputs of the ADC.

The AD9246 is set for a 2 V p-p full-scale input by connecting the SENSE pin to AGND. The inputs of the AD9246 are biased at 1 V by connecting the CML output, as shown in Figure 66.

The circuit was tested with a −1 dBFS signal at various frequencies. Figure 65 shows a plot of the second- and third-order harmonic distortion (HD2/HD3) vs. frequency.

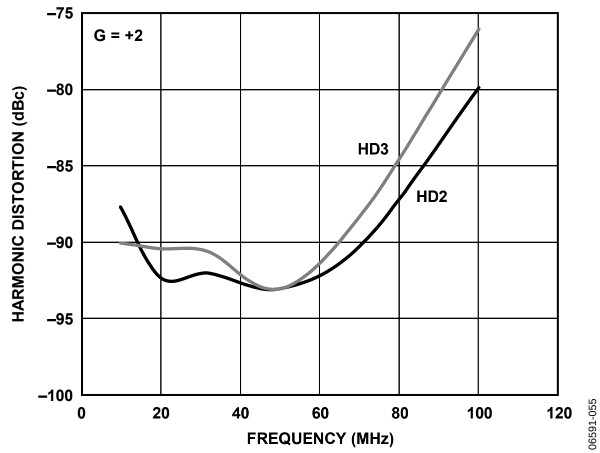



*Figure 65. HD2/HD3 for Combination of ADA4937-1/ADA4937-2 and AD9246 ADC*

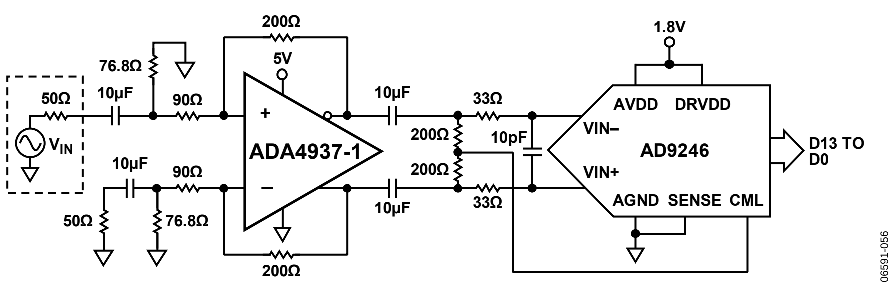



*Figure 66. Driving an AD9246, 14-Bit, 125 MSPS ADC*

### 3.3 V OPERATION

The ADA4937-1/ADA4937-2 provide excellent performance in 3.3 V single-supply applications. Significant power savings can be realized when the ADA4937-1/ADA4937-2 are used in combination with a low voltage ADC.

The circuit in Figure 67 is an example of the ADA4937-1 driving an AD9230, 12-bit, 250 MSPS ADC that is specified to operate with a single 1.8 V supply. The performance of the ADC is optimized when it is driven differentially, making the best use of the signal swing available within the 1.8 V supply. The ADA4937-1/ADA4937-2 perform the single-ended-to-differential conversion, common-mode level-shifting, and buffering of the driving signal.

The ADA4937-1/ADA4937-2 are configured with a single 3.3 V supply and a gain of 2 V/V for a single-ended input to differential output. The 59 Ω termination resistor, in parallel with the single-ended input impedance of 306 Ω, provides a 50 Ω termination for the source. The additional 26 Ω (226 Ω total) at the inverting input balances the parallel impedance of the 50 Ω source and the termination resistor that drives the noninverting input. The signal generator has a symmetric, ground-referenced bipolar output. The $V_{OCM}$ pin is connected to the CML output of the AD9230, and sets the output common mode of the ADA4937-1/ADA4937-2 at 1.4 V. One third of the output common-mode voltage of the amplifier is fed back to the summing nodes, biasing −IN and +IN at ~0.5 V. For a common-mode voltage of 1.4 V, each ADA4937-1/ADA4937-2 output swings between 1.09 V and 1.71 V, providing a 1.25 V p-p differential output.

A third-order, 125 MHz, low-pass filter between the ADA4937-1/ADA4937-2 and the AD9230 reduces the noise bandwidth of the amplifier and isolates the driver outputs from the ADC inputs.

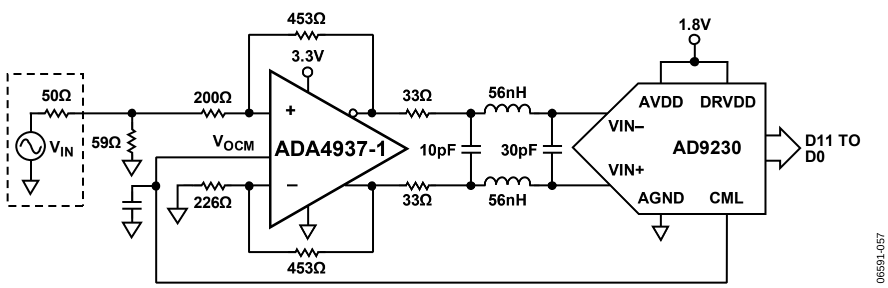



*Figure 67. Driving an AD9230, 12-Bit, 250 MSPS ADC*

# OUTLINE DIMENSIONS

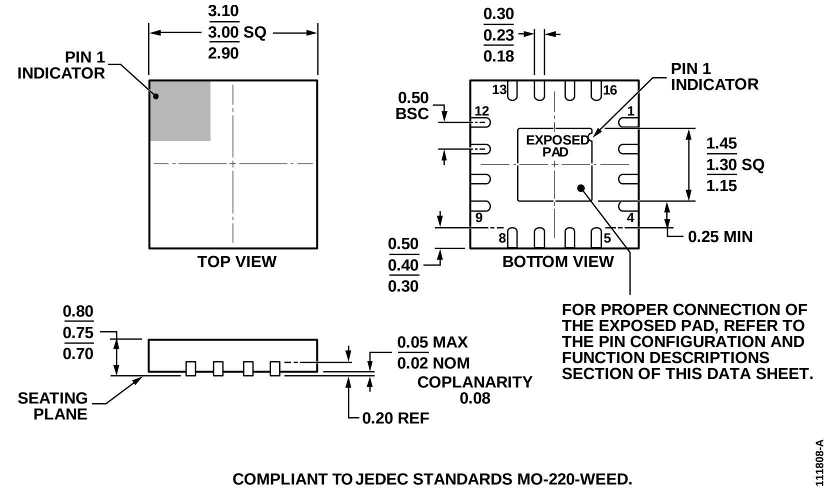



*Figure 68. 16-Lead Lead Frame Chip Scale Package [LFCSP]*
*3 mm × 3 mm Body and 0.75 mm Package Height*
*(CP-16-21)*
*Dimensions shown in millimeters*

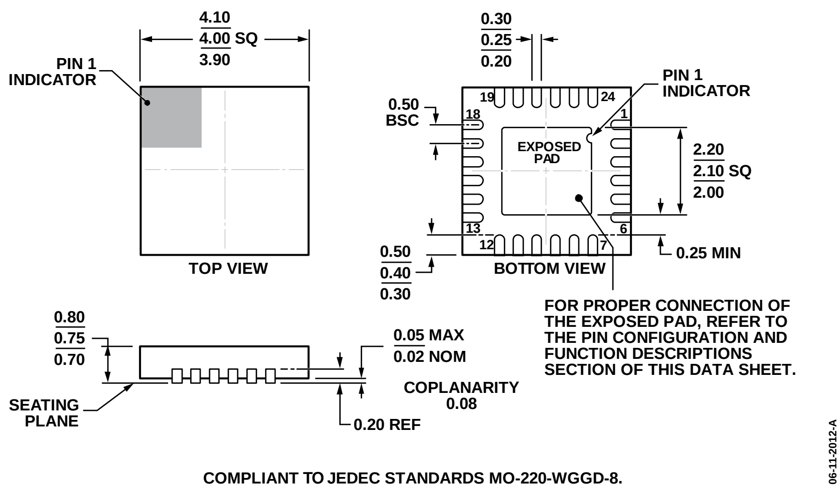



*Figure 69. 24-Lead Lead Frame Chip Scale Package [LFCSP]*
*4 mm × 4 mm Body and 0.75 mm Package Height*
*(CP-24-10)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option | Ordering Quantity | Branding |
|---|---|---|---|---|---|
| ADA4937-1YCPZ-R2 | −40°C to +105°C | 16-Lead LFCSP | CP-16-21 | 250 | H1S |
| ADA4937-1YCPZ-RL | −40°C to +105°C | 16-Lead LFCSP | CP-16-21 | 5,000 | H1S |
| ADA4937-1YCPZ-R7 | −40°C to +105°C | 16-Lead LFCSP | CP-16-21 | 1,500 | H1S |
| ADA4937-2YCPZ-R2 | −40°C to +105°C | 24-Lead LFCSP | CP-24-10 | 250 | |
| ADA4937-2YCPZ-RL | −40°C to +105°C | 24-Lead LFCSP | CP-24-10 | 5,000 | |
| ADA4937-2YCPZ-R7 | −40°C to +105°C | 24-Lead LFCSP | CP-24-10 | 1,500 | |

[1] Z = RoHS Compliant Part.

## NOTES

# NOTES


D06591-0-6/16(F)