AXI BRAM Simulation on PlanAhead

1. **Launch PlanAhead**

2. **Create a new project**
   - ⇨ Specify Project Name.
   - ⇨ Select RTL Sources.
   - ⇨ Add Sources → Skip
   - ⇨ Add Existing IP →Skip
   - ⇨ Add Constraints →Skip
   - ⇨ Default part → I've chosen V6-ML605
   - ⇨ Finish

3. **Add Sources**
   - ⇨ Select Add or Create Embedded Sources

4. **Create File**
   - ⇨ Specify XPS module name "**robot**" (in my example).
   - ⇨ XPS GUI will be launched in "blocking-mode" which means that you have to complete and exit out of XPS in order to switch back to PlanAhead.
   - ⇨ Configure XPS project and Finish. Select File → Exit to exit XPS.

5. **Create Top HDL**
   - ⇨ Right-click and bring up context-sensitive menu and select "**Create Top HDL**"
   - ⇨ This will create "**robot_stub.v**" top level source and will be added to Design Sources.

6. **Create the TestBench**
   - ⇨ Select "**robot**" in the Libraries tab.
   - ⇨ Right Clock and bring up Context-Sensitive menu.
   - ⇨ Select "**Create TestBench**"
   - ⇨ This step will create "**robo_top_tb.v**" testbench source and will be added to Simulation Sources.
   - ⇨ Double-click on this testbench file and replace "robot" with "robot_stub" in order to instantiate the "robot_stub" that was created above:-

   robot

   dut

   With

   robot_stub

   dut

7. **Set Top level module**
   - ⇨ From “Project Settings”, set “Top Module Name” to “**robot_stub”.**

8. **Generate Netlists and Simulation models.**
   - ⇨ Select “**robot**” module, right-click and then click on “**Generate All**”
   - ⇨ This will generate netlists and simulation models for the “**robot**” XPS module and also add the default “bootloops” ELF file to the “Design Sources” and “Simulation-only Sources”.
   - ⇨ Note: If you don’t see these bootloop files (mb_bootloop_le.elf) added to the file sets, then run “Generate All” again. These files should get added this time. If not, then manually add these files from the EDK install area using “Add Sources”.

9. **Verify ELF associations**
   - ⇨ From main menu, click **Tools → ELF File** Associations to bring up the ELF associations dialog box.
   - ⇨ If “Associated ELF file” fields are blank, then click on the – the file browser button to bring-up sub-dialog box for selecting/adding ELF file.
   - ⇨ Select /Add ELF files.
   - ⇨ In this example, I’ve taken a simple “**Hello World**” C project

10. **Run the Behavioral Simulation**
    - ⇨ You can now run the simulation from the “**Run Behavioral Simulation**” button under the “**Project Manager**” on the left window pane.

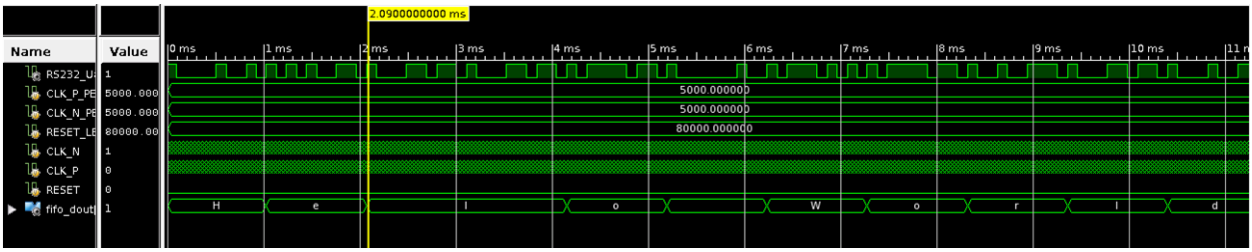

Figure 1: Hello World Simulation on ISIM

In this example I’ve used the Microblaze BRAM controller, the procedure is the same if you wanted to use the DDR. In that case, when making the XPS project firstly, you need to add the DDR peripheral in your project. Also, while generating the linker script from SDK you need to map the sections of the code to DDR.

AXI DDR3 Simulation on PlanAhead

The flow to do this is essentially same as for BRAM mentioned above. Please bear the following in mind

1. Make sure in the XPS project, under project options **Enable External Memory Simulation** is ticked.

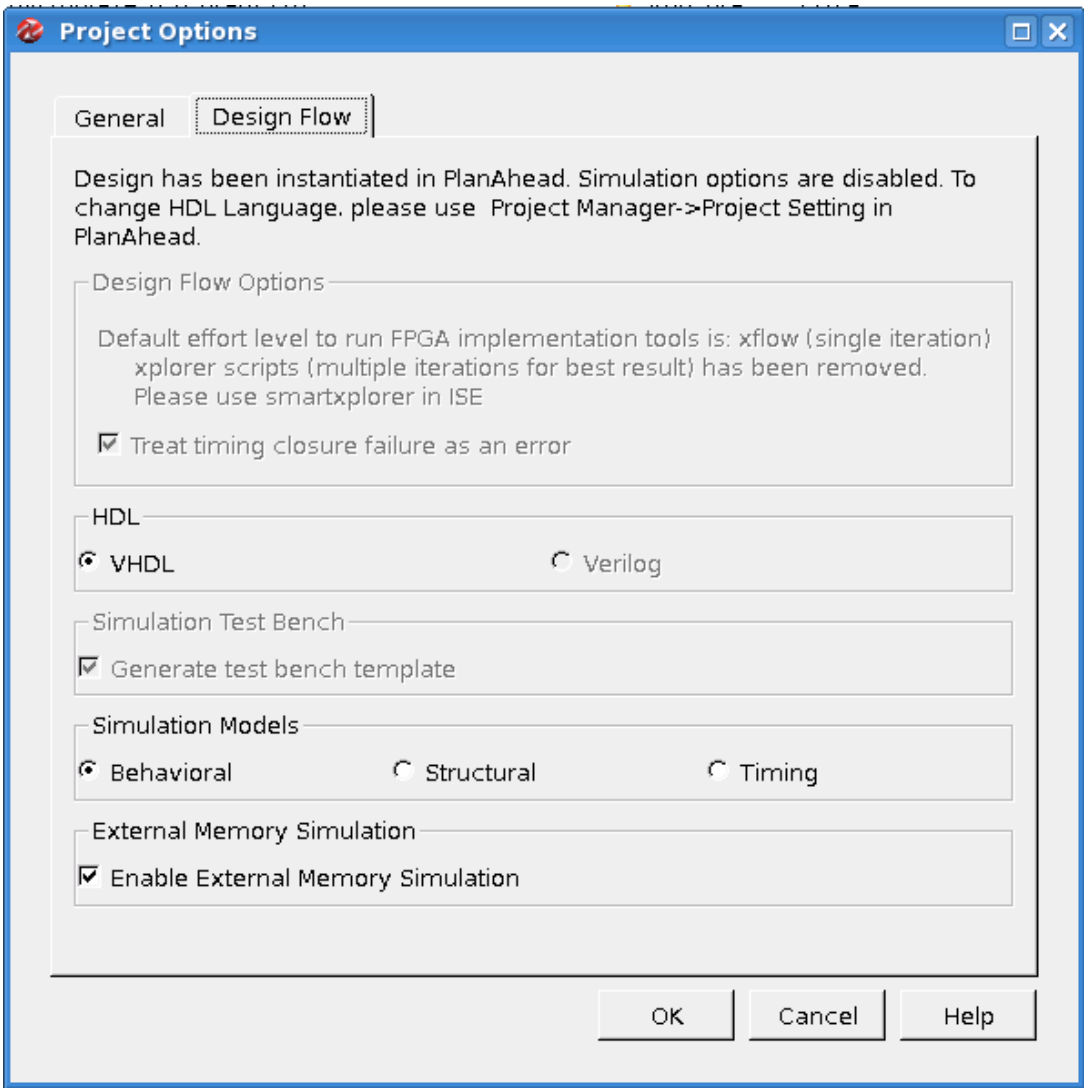

Figure 1: Enable External Memory Simulation

2. When generating the Netlist and Simulation models in PlanAhead, make sure **Enable External Memory Simulation** is checked

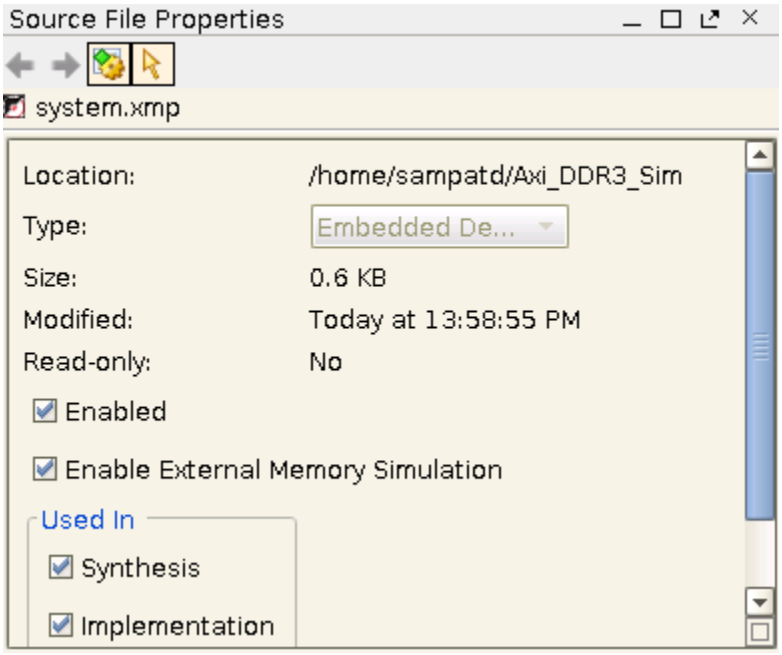

Figure 2: Enable External Memory SImulation in Source File Properties

3. After generating the synthesis and simulation models, add the ddr3 model from **axiddr3.srcs\sources_1\edk\robot__xps\DDR3_SDRAM.** Add the following files –

   a. ddr3_model.v

   b. ddr3_model_parameters.vh

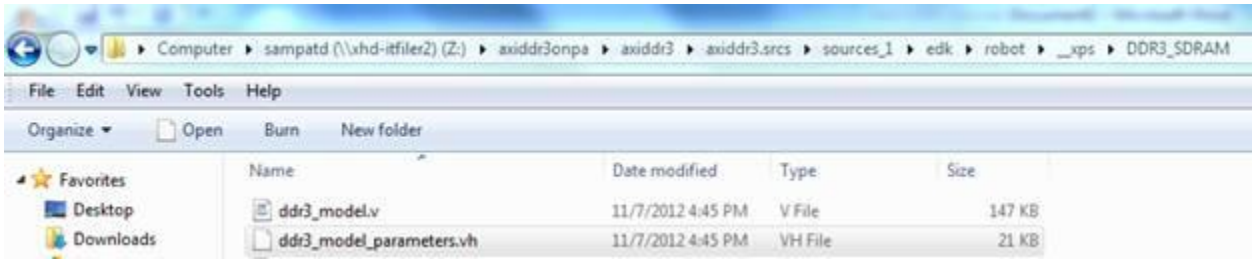

Figure 3: Add the above ddr3 simulation model files to the project

Kindly note that the DDR2/DDR3 memory simulation models are valid only for (Virtex®-6, Kintex®-7 and Virtex-7 DDRx IPs). Please refer to **page 81** of embedded system tools reference manual.

http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_2/est_rm.pdf