Dual, Low Power, 8-/10-/12-/14-Bit TxDAC Digital-to-Analog Converters

AD9714/AD9715/AD9716/AD9717

FEATURES

Power dissipation @ 3.3 V, 2 mA output
- **37 mW @ 10 MSPS**
- **86 mW @ 125 MSPS**

Sleep mode: <3 mW @ 3.3 V
Supply voltage: 1.8 V to 3.3 V
SFDR to Nyquist
- **84 dBc @ 1 MHz output**
- **75 dBc @ 10 MHz output**

AD9717 NSD @ 1 MHz output, 125 MSPS, 2 mA: –151 dBc/Hz
Differential current outputs: 1 mA to 4 mA
2 on-chip auxiliary DACs
CMOS inputs with single-port operation
Output common mode: adjustable 0 V to 1.2 V
Small footprint 40-lead LFCSP RoHS-compliant package

APPLICATIONS

Wireless infrastructures
- **Picocell, femtocell base stations**

Medical instrumentation
- **Ultrasound transducer excitation**

Portable instrumentation
- **Signal generators, arbitrary waveform generators**

GENERAL DESCRIPTION

The AD9714/AD9715/AD9716/AD9717 are pin-compatible, dual, 8-/10-/12-/14-bit, low power digital-to-analog converters (DACs) that provide a sample rate of 125 MSPS. These TxDAC® converters are optimized for the transmit signal path of communication systems. All the devices share the same interface, package, and pinout, providing an upward or downward component selection path based on performance, resolution, and cost.

The AD9714/AD9715/AD9716/AD9717 offer exceptional ac and dc performance and support update rates up to 125 MSPS.

The flexible power supply operating range of 1.8 V to 3.3 V and low power dissipation of the AD9714/AD9715/AD9716/AD9717 make them well-suited for portable and low power applications.

PRODUCT HIGHLIGHTS

1. Low Power.
   DACs operate on a single 1.8 V to 3.3 V supply; total power consumption reduces to 35 mW at 125 MSPS with a 1.8 V supply. Sleep and power-down modes are provided for low power idle periods.
2. CMOS Clock Input.
   High speed, single-ended CMOS clock input supports a 125 MSPS conversion rate.
3. Easy Interfacing to Other Components.
   Adjustable output common mode from 0 V to 1.2 V allows easy interfacing to other components that accept common-mode levels greater than 0 V.

Rev. A
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REVISION HISTORY

3/09—Rev. 0 to Rev. A

8/08—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

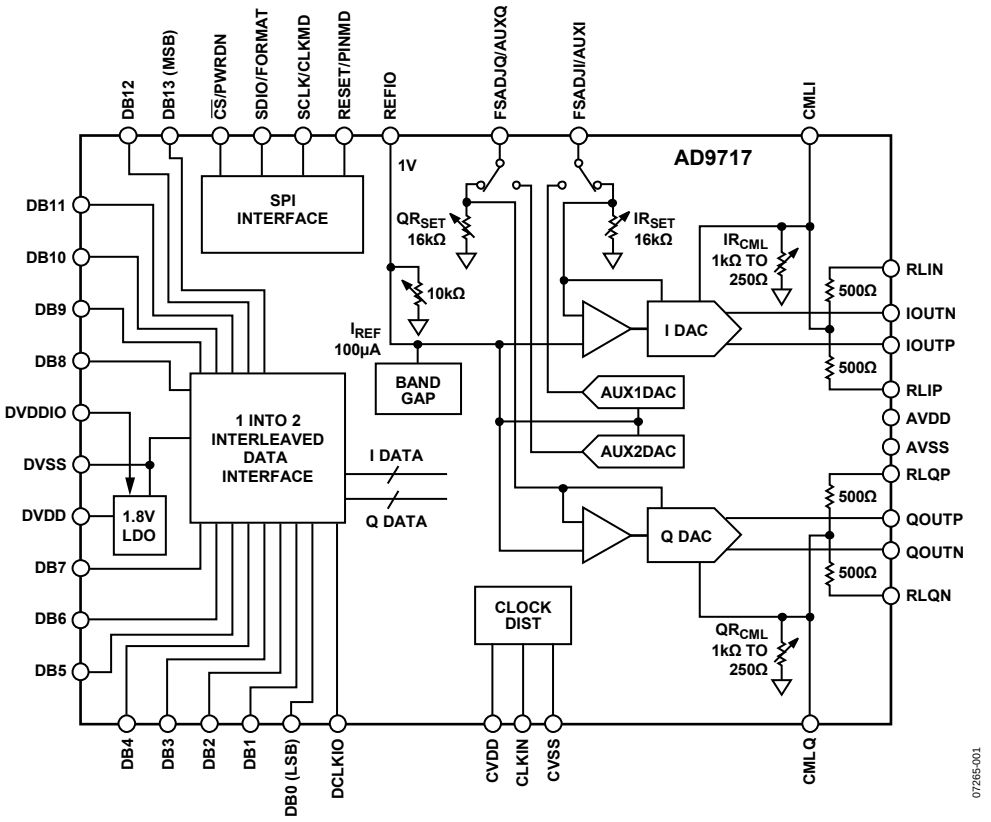


Figure 1.

SPECIFICATIONS

DC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 1.8 V, DVDDIO = 3.3 V, CVDD = 3.3 V, I_{xOUTFS} = 2 mA, maximum sample rate, unless otherwise noted.

Table 1.

	AD9714			AD9715			AD9716			AD9717			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		8			10			12			14		Bits
ACCURACY, AVDD = DVDDIO = CVDD = 3.3 V													
Differential Nonlinearity (DNL)													
Precalibration		±0.02			±0.08			±0.4			±1.7		LSB
Postcalibration		±0.003			±0.01			±0.2			±1.0		LSB
Integral Nonlinearity (INL)													
Precalibration		±0.025			±0.13			±0.4			±1.8		LSB
Postcalibration		±0.01			±0.05			±0.3			±1.3		LSB
ACCURACY, AVDD = DVDDIO = CVDD = 1.8 V													
Differential Nonlinearity (DNL)													
Precalibration		±0.02			±0.08			±0.4			±1.2		LSB
Postcalibration		±0.005			±0.01			±0.2			±1.0		LSB
Integral Nonlinearity (INL)													
Precalibration		±0.025			±0.12			±0.4			±1.5		LSB
Postcalibration		±0.02			±0.05			±0.25			±1.1		LSB
MAIN DAC OUTPUTS													
Offset Error	−1	0	+1	−1	0	+1	−1	0	+1	−1	0	+1	mV
Gain Error													
Internal Reference	−2		+2	−2		+2	−2		+2	−2		+2	% of FSR
Full-Scale Output Current[1]													
AVDD = 3.3 V	1	2	4	1	2	4	1	2	4	1	2	4	mA
AVDD = 1.8 V	1	2	2.5	1	2	2.5	1	2	2.5	1	2	2.5	mA
Output Compliance Range	−0.5	0	+1.2	−0.5	0	+1.2	−0.5	0	+1.2	−0.5	0	+1.2	V
Output Resistance		200			200			200			200		MΩ
Crosstalk, Q DAC to I DAC													
f_{OUT} = 30 MHz		97			97			97			97		dB
f_{OUT} = 60 MHz		78			78			78			78		dB
MAIN DAC TEMPERATURE DRIFT													
Offset		0			0			0			0		ppm/°C
Gain		±40			±40			±40			±40		ppm/°C
Reference Voltage		±25			±25			±25			±25		ppm/°C
AUXDAC OUTPUTS													
Resolution		10			10			10			10		Bits
Full-Scale Output Current (Current Sourcing Mode)		125			125			125			125		µA
Voltage Output Mode	V_{SS}		V_{DD}	V_{SS}		V_{DD}	V_{SS}		V_{DD}	V_{SS}		V_{DD}	V
Output Compliance Range (Sourcing 1 mA)	V_{SS}		V_{DD} − 0.25	V_{SS}		V_{DD} − 0.25	V_{SS}		V_{DD} − 0.25	V_{SS}		V_{DD} − 0.25	V
Output Compliance Range (Sinking 1 mA)	V_{SS} + 0.25		V_{DD}	V_{SS} + 0.25		V_{DD}	V_{SS} + 0.25		V_{DD}	V_{SS} + 0.25		V_{DD}	V
Output Resistance in Current Output Mode, AV_{SS} to 1 V		1			1			1			1		MΩ
AUX DAC Monotonicity Guaranteed		10			10			10			10		Bits
REFERENCE OUTPUT													
Internal Reference Voltage	0.98	1.025	1.08	0.98	1.025	1.08	0.98	1.025	1.08	0.98	1.025	1.08	V
Output Resistance		10			10			10			10		kΩ

Parameter	AD9714 Min	AD9714 Typ	AD9714 Max	AD9715 Min	AD9715 Typ	AD9715 Max	AD9716 Min	AD9716 Typ	AD9716 Max	AD9717 Min	AD9717 Typ	AD9717 Max	Unit
REFERENCE INPUT													
Voltage Compliance													
AVDD = 3.3 V	0.1		1.25	0.1		1.25	0.1		1.25	0.1		1.25	V
AVDD = 1.8 V	0.1		1.0	0.1		1.0	0.1		1.0	0.1		1.0	V
Input Resistance External Reference Mode		1			1			1			1		MΩ
DAC MATCHING													
Gain Matching	−1		+1	−1		+1	−1		+1	−1		+1	% FSR
ANALOG SUPPLY VOLTAGES													
AVDD	1.7		3.5	1.7		3.5	1.7		3.5	1.7		3.5	V
CVDD	1.7		3.5	1.7		3.5	1.7		3.5	1.7		3.5	V
DIGITAL SUPPLY VOLTAGES													
DVDD	1.7		1.9	1.7		1.9	1.7		1.9	1.7		1.9	V
DVDDIO	1.7		3.5	1.7		3.5	1.7		3.5	1.7		3.5	V
POWER CONSUMPTION, AVDD = DVDDIO = CVDD = 3.3 V													
f_{DAC} = 125 MSPS, IF = 12.5 MHz		86			86			86			86		mW
I_{AVDD}		10			10			10			10		mA
$I_{DVDD} + I_{DVDDIO}$		11			11			11			11		mA
I_{CVDD}		3			3			3			3		mA
Power-Down Mode with Clock		50			50			50			50		mW
Power-Down Mode, No Clock		1.5			1.5			1.5			1.5		mW
Power Supply Rejection Ratio		−0.04			−0.04			−0.04			−0.04		% FSR/V
POWER CONSUMPTION, AVDD = DVDDIO = CVDD = 1.8 V.													
f_{DAC} = 125 MSPS, IF = 12.5 MHz		35			35			35			35		mW
I_{AVDD}		10			10			10			10		mA
$I_{DVDD} + I_{DVDDIO}$		8			8			8			8		mA
I_{CVDD}		1.5			1.5			1.5			1.5		mA
Power-Down Mode with Clock		12			12			12			12		mW
Power-Down Mode, No Clock		850			850			850			850		µW
Power Supply Rejection Ratio		−0.001			−0.001			−0.001			−0.001		% FSR/V
OPERATING RANGE	−40	+25	+85	−40	+25	+85	−40	+25	+85	−40	+25	+85	°C

[1] Based on a 10 kΩ external resistor.

DIGITAL SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 1.8 V, DVDDIO = 3.3 V, CVDD = 3.3 V, I_{xOUTFS} = 2 mA, maximum sample rate, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit
DAC CLOCK INPUT (CLKIN)				
V_{IH}	2.1	3		V
V_{IL}		0	0.9	V
Maximum Clock Rate			125	MSPS
SERIAL PERIPHERAL INTERFACE				
Maximum Clock Rate (SCLK)		25		MHz
Minimum Pulse Width High		20		ns
Minimum Pulse Width Low		20		ns
INPUT DATA				
1.8 V Q Channel or DCLKIO Falling Edge				
Setup		0.25		ns
Hold		1.2		ns
1.8 V I Channel or DCLKIO Rising Edge				
Setup		0.13		ns
Hold		1.1		ns
3.3 V Q Channel or DCLKIO Falling Edge				
Setup		−0.2		ns
Hold		1.5		ns
3.3 V I Channel or DCLKIO Rising Edge				
Setup		−0.2		ns
Hold		1.6		ns
V_{IH}	2.1	3		V
V_{IL}		0	0.9	V

AC SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 1.8 V, DVDDIO = 3.3 V, CVDD = 3.3 V, I_{xOUTFS} = 2 mA, maximum sample rate, unless otherwise noted.

Table 3.

	AD9714			AD9715			AD9716			AD9717			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SPURIOUS-FREE DYNAMIC RANGE (SFDR)													
f_{DAC} = 125 MSPS, f_{OUT} = 10 MHz		75			82			83			84		dBc
f_{DAC} = 125 MSPS, f_{OUT} = 50 MHz		60			61			62			63		dBc
TWO TONE INTERMODULATION DISTORTION (IMD)													
f_{DAC} = 125 MSPS, f_{OUT} = 10 MHz		86			87			88			89		dBc
f_{DAC} = 125 MSPS, f_{OUT} = 50 MHz		71			71			71			71		dBc
NOISE SPECTRAL DENSITY (NSD) EIGHT-TONE, 500 kHz TONE SPACING													
f_{DAC} = 125 MSPS, f_{OUT} = 10 MHz		−129			−141			−149			−152		dBc/Hz
f_{DAC} = 125 MSPS, f_{OUT} = 50 MHz		−123			−135			−137			−141		dBc/Hz
W-CDMA ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER													
f_{DAC} = 61.44 MSPS, f_{OUT} = 20 MHz		−71			−71			−71			−71		dBc
f_{DAC} = 122.88 MSPS, f_{OUT} = 30 MHz		−72			−72			−72			−72		dBc

T_{MIN} to T_{MAX}, AVDD = 1.8 V, DVDD = 1.8 V, DVDDIO = 1.8 V, CVDD = 1.8 V, I_{xOUTFS} = 2 mA, maximum sample rate, unless otherwise noted.

Table 4.

	AD9714			AD9715			AD9716			AD9717			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SPURIOUS-FREE DYNAMIC RANGE (SFDR)													
f_{DAC} = 125 MSPS, f_{OUT} = 10 MHz		75			78			79			80		dBc
f_{DAC} = 125 MSPS, f_{OUT} = 50 MHz		55			56			57			58		dBc
TWO TONE INTERMODULATION DISTORTION (IMD)													
f_{DAC} = 125 MSPS, f_{OUT} = 10 MHz		79			80			84			85		dBc
f_{DAC} = 125 MSPS, f_{OUT} = 50 MHz		53			53			53			53		dBc
NOISE SPECTRAL DENSITY (NSD) EIGHT-TONE, 500 kHz TONE SPACING													
f_{DAC} = 125 MSPS, f_{OUT} = 10 MHz		−132			−141			−146			−148		dBc/Hz
f_{DAC} = 125 MSPS, f_{OUT} = 50 MHz		−126			−131			−131			−132		dBc/Hz
W-CDMA ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER													
f_{DAC} = 61.44 MSPS, f_{OUT} = 20 MHz		−68			−68			−68			−68		dBc
f_{DAC} = 122.88 MSPS, f_{OUT} = 30 MHz		−68			−68			−68			−68		dBc

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
AVDD, DVDDIO, CVDD to AVSS, DVSS, CVSS	−0.3 V to +3.9 V
DVDD to DVSS	−0.3 V to +2.1 V
AVSS to DVSS, CVSS	−0.3 V to +0.3 V
DVSS to AVSS, CVSS	−0.3 V to +0.3 V
CVSS to AVSS, DVSS	−0.3 V to +0.3 V
REFIO, FSADJQ, FSADJI, CMLQ, CMLI to AVSS	−0.3 V to AVDD + 0.3 V
QOUTP, QOUTN, IOUTP, IOUTN, RLQP, RLQN, RLIP, RLIN to AVSS	−1.0 V to AVDD + 0.3 V
DBn[1] (MSB) to DB0 (LSB), $\overline{CS}$, SCLK, SDIO, RESET to DVSS	−0.3 V to DVDDIO + 0.3 V
CLKIN to CVSS	−0.3 V to CVDD + 0.3 V
Junction Temperature	125°C
Storage Temperature Range	−65°C to +150°C

[1] n stands for 7 for the AD9714, 9 for the AD9715, 11 for the AD9716, and 13 for the AD9717.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 6.

Package Type	θ_{JA}	θ_{JB}[1]	θ_{JC}[1]	Unit
40-Lead LFCSP (with No Airflow Movement)	29.8	19.0	3.4	°C/W

[1] These calculations are intended to represent the thermal performance of the indicated packages using a JEDEC multilayer test board. Do not assume the same level of thermal performance in actual applications without a careful inspection of the conditions in the application to determine that they are similar to those assumed in these calculations.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

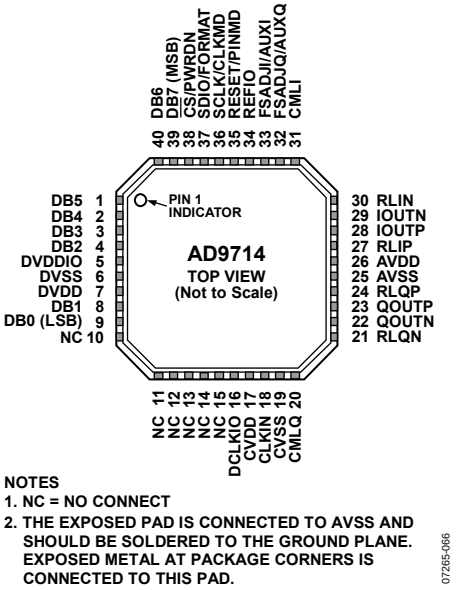


Figure 2. AD9714 Pin Configuration

Table 7. AD9714 Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 4	DB[5:2]	Digital Inputs.
5	DVDDIO	Digital I/O Supply Voltage (1.8 V to 3.3 V Nominal).
6	DVSS	Digital Common.
7	DVDD	Digital Core Supply Voltage (1.8 V). Strap DVDD to DVDDIO at 1.8 V. If DVDDIO > 1.8 V, bypass DVDD with a 1.0 µF capacitor; however, do not otherwise connect it. The LDO should not drive external loads.
8	DB1	Digital Inputs.
9	DB0 (LSB)	Digital Input (LSB).
10 to 15	NC	No Connect. These pins are not connected to the chip.
16	DCLKIO	Data Input/Output Clock. Clock used to qualify input data.
17	CVDD	Sampling Clock Supply Voltage (1.8 V to 3.3 V). CVDD must be ≥ DVDD.
18	CLKIN	LVCMOS Sampling Clock Input.
19	CVSS	Sampling Clock Supply Voltage Common.
20	CMLQ	Q DAC Output Common-Mode Level. When the internal on chip (QR_{CML}) is enabled, this pin is connected to the on-chip QR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on chip (QR_{CML}) is disabled, this pin is the common-mode load for Q DAC and must be connected to AVSS through a resistor (see the Using the Internal Termination Resistors section). The recommended value for this external resistor is 0 Ω.
21	RLQN	Load Resistor (500 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTN externally.
22	QOUTN	Complementary Q DAC Current Output. Full-scale current is sourced when all data bits are 0s.
23	QOUTP	Q DAC Current Output. Full-scale current is sourced when all data bits are 1s.
24	RLQP	Load Resistor (500 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTP externally.
25	AVSS	Analog Common.
26	AVDD	Analog Supply Voltage (1.8 V to 3.3 V).
27	RLIP	Load Resistor (500 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTP externally.
28	IOUTP	I DAC Current Output. Full-scale current is sourced when all data bits are 1s.
29	IOUTN	Complementary I DAC Current Output. Full-scale current is sourced when all data bits are 0s.
30	RLIN	Load Resistor (500 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTN externally.

Pin No.	Mnemonic	Description
31	CMLI	I DAC Output Common-Mode Level. When the internal on chip (IR_{CML}) is enabled, this pin is connected to the on-chip IR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on chip (IR_{CML}) is disabled, this pin is the common-mode load for I DAC and must be connected to AVSS through a resistor (see the Using the Internal Termination Resistors section). The recommended value for this external resistor is 0 Ω.
32	FSADJQ/AUXQ	Full-Scale Current Output Adjust (FSADJQ). When the internal on chip (QR_{SET}) is disabled, this pin is the full-scale current output adjust for Q DAC and must be connected to AVSS through a resistor (see the Theory of Operation section). The nominal value for this external resistor is 16 kΩ for a 2 mA output current. Auxiliary Q DAC Output (AUXQ). When the internal on chip (QR_{SET}) is enabled, this pin is the auxiliary Q DAC output.
33	FSADJI/AUXI	Full-Scale Current Output Adjust (FSADJI). When the internal on chip (IR_{SET}) is disabled, this pin is full-scale current output adjust for I DAC and must be connected to AVSS through a resistor (see the Theory of Operation section). The nominal value for this external resistor is 16 kΩ for a 2 mA output current. Auxiliary I DAC Output (AUXI). When the internal on chip (IR_{SET}) is enabled, this pin is the auxiliary I DAC output.
34	REFIO	Reference Input/Output. Serves as a reference input when the internal reference is disabled. Provides a 1.0 V reference output when in internal reference mode (a 0.1 µF capacitor to AVSS is required).
35	RESET/PINMD	This pin defines the operation mode of the part. A logic low (pull-down to DVSS) sets the part in SPI mode. Pulse RESET high to reset the SPI registers to their default values. A logic high (pull-up to DVDDIO) puts the device into pin mode (PINMD).
36	SCLK/CLKMD	Clock Input for Serial Port (SCLK). In SPI mode, this pin is the clock input for the serial port. Clock Mode (CLKMD). In pin mode, CLKMD determines the phase of the internal retiming clock. When DCLKIO = CLKIN, tie it to 0. When DCLKIO ≠ CLKIN, pulse 0 to 1 to edge trigger the internal retimer (see the Retimer section).
37	SDIO/FORMAT	Serial Port Input/Output (SDIO). In SPI mode, this pin is the bidirectional data line for serial port. Format Pin (FORMAT). In pin mode, FORMAT determines the data format of digital data. A logic low (pull-down to DVSS) selects the binary input data format. A logic high (pull-up to DVDDIO) selects the two complement input data format.
38	$\overline{CS}$/PWRDN	Active Low Chip Select ($\overline{CS}$). In SPI mode, this pin serves as the active low chip select. In pin mode, a logic high (pull-up to DVDDIO) powers down the device, except for the SPI port. Power-Down (PWRDN). In pin mode, PWRDN powers down the device except for the SPI port.
39	DB7 (MSB)	Digital Input (MSB).
40	DB6	Digital Input.
41 (EPAD)	Exposed Pad (EPAD)	The exposed pad is connected to AVSS and should be soldered to the ground plane. Exposed metal at the package corners is connected to this pad.

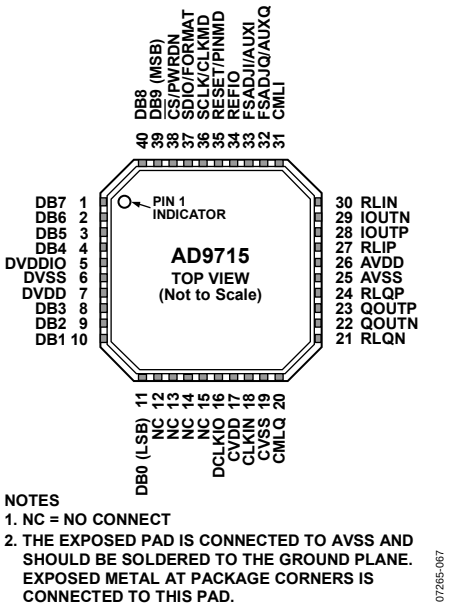


Figure 3. AD9715 Pin Configuration

Table 8. AD9715 Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 4	DB[7:4]	Digital Inputs.
5	DVDDIO	Digital I/O Supply Voltage (1.8 V to 3.3 V Nominal).
6	DVSS	Digital Common.
7	DVDD	Digital Core Supply Voltage (1.8 V). Strap DVDD to DVDDIO at 1.8 V. If DVDDIO > 1.8 V, bypass DVDD with a 1.0 µF capacitor; however, do not otherwise connect it. The LDO should not drive external loads.
8 to 10	DB[3:1]	Digital Inputs.
11	DB0 (LSB)	Digital Input (LSB).
12 to 15	NC	No Connect. These pins are not connected to the chip.
16	DCLKIO	Data Input/Output Clock. Clock used to qualify input data.
17	CVDD	Sampling Clock Supply Voltage (1.8 V to 3.3 V). CVDD must be ≥ DVDD.
18	CLKIN	LVCMOS Sampling Clock Input.
19	CVSS	Sampling Clock Supply Voltage Common.
20	CMLQ	Q DAC Output Common-Mode Level. When the internal on chip (QR_{CML}) is enabled, this pin is connected to the on-chip QR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on chip (QR_{CML}) is disabled, this pin is the common-mode load for Q DAC and must be connected to AVSS through a resistor (see the Using the Internal Termination Resistors section). The recommended value for this external resistor is 0 Ω.
21	RLQN	Load Resistor (500 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTN externally.
22	QOUTN	Complementary Q DAC Current Output. Full-scale current is sourced when all data bits are 0s.
23	QOUTP	Q DAC Current Output. Full-scale current is sourced when all data bits are 1s.
24	RLQP	Load Resistor (500 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTP externally.
25	AVSS	Analog Common.
26	AVDD	Analog Supply Voltage (1.8 V to 3.3 V).
27	RLIP	Load Resistor (500 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTP externally.
28	IOUTP	I DAC Current Output. Full-scale current is sourced when all data bits are 1s.
29	IOUTN	Complementary I DAC Current Output. Full-scale current is sourced when all data bits are 0s.
30	RLIN	Load Resistor (500 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTN externally.

Pin No.	Mnemonic	Description
31	CMLI	I DAC Output Common-Mode Level. When the internal on chip (IR_{CML}) is enabled, this pin is connected to the on-chip IR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on chip (IR_{CML}) is disabled, this pin is the common-mode load for I DAC and must be connected to AVSS through a resistor (see the Using the Internal Termination Resistors section). The recommended value for this external resistor is 0 Ω.
32	FSADJQ/AUXQ	Full-Scale Current Output Adjust (FSADJQ). When the internal on chip (QR_{SET}) is disabled, this pin is the full-scale current output adjust for Q DAC and must be connected to AVSS through a resistor (see the Theory of Operation section). The nominal value for this external resistor is 16 kΩ for a 2 mA output current. Auxiliary Q DAC Output (AUXQ). When the internal on chip (QR_{SET}) is enabled, this pin is the auxiliary Q DAC output.
33	FSADJI/AUXI	Full-Scale Current Output Adjust (FSADJI). When the internal on chip (IR_{SET}) is disabled, this pin is the full-scale current output adjust for I DAC and must be connected to AVSS through a resistor (see the Theory of Operation section). The nominal value for this external resistor is 16 kΩ for a 2 mA output current. Auxiliary I DAC Output (AUXI). When the internal on chip (IR_{SET}) is enabled, this pin is the auxiliary I DAC output.
34	REFIO	Reference Input/Output. Serves as a reference input when the internal reference is disabled. Provides a 1.0 V reference output when in internal reference mode (a 0.1 µF capacitor to AVSS is required).
35	RESET/PINMD	This pin defines the operation mode of the part. A logic low (pull-down to DVSS) sets the part in SPI mode. Pulse RESET high to reset the SPI registers to their default values. A logic high (pull-up to DVDDIO) puts the device into pin mode (PINMD).
36	SCLK/CLKMD	Clock Input for Serial Port (SCLK). In SPI mode, this pin is the clock input for the serial port. Clock Mode (CLKMD). In pin mode, CLKMD determines the phase of the internal retiming clock. When DCLKIO = CLKIN, tie it to 0. When DCLKIO ≠ CLKIN, pulse 0 to 1 to edge trigger the internal retimer (see the Retimer section).
37	SDIO/FORMAT	Serial Port Input/Output (SDIO). In SPI mode, this pin is the bidirectional data line for the serial port. Format Pin (FORMAT). In pin mode, FORMAT determines the data format of digital data. A logic low (pull-down to DVSS) selects the binary input data format. A logic high (pull-up to DVDDIO) selects the twos complement input data format.
38	$\overline{CS}$/PWRDN	Active Low Chip Select ($\overline{CS}$). In SPI mode, this pin serves as the active low chip select. Power-Down (PWRDN). In pin mode, a logic high (pull-up to DVDDIO) powers down the device, except for the SPI port.
39	DB9 (MSB)	Digital Input (MSB).
40	DB8	Digital Input.
41 (EPAD)	Exposed Pad (EPAD)	The exposed pad is connected to AVSS and should be soldered to the ground plane. Exposed metal at the package corners is connected to this pad.

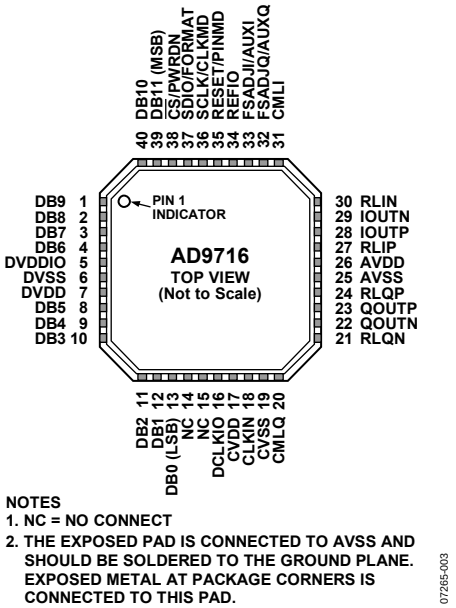


Figure 4. AD9716 Pin Configuration

Table 9. AD9716 Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 4	DB[9:6]	Digital Inputs.
5	DVDDIO	Digital I/O Supply Voltage (1.8 V to 3.3 V Nominal).
6	DVSS	Digital Common.
7	DVDD	Digital Core Supply Voltage (1.8 V). Strap DVDD to DVDDIO at 1.8 V. If DVDDIO > 1.8 V, bypass DVDD with a 1.0 µF capacitor; however, do not otherwise connect it. The LDO should not drive external loads.
8 to 12	DB[5:1]	Digital Inputs.
13	DB0 (LSB)	Digital Input (LSB).
14, 15	NC	No Connect. These pins are not connected to the chip.
16	DCLKIO	Data Input/Output Clock. Clock used to qualify input data.
17	CVDD	Sampling Clock Supply Voltage (1.8 V to 3.3 V). CVDD must be ≥ DVDD.
18	CLKIN	LVCMOS Sampling Clock Input.
19	CVSS	Sampling Clock Supply Voltage Common.
20	CMLQ	Q DAC Output Common-Mode Level. When the internal on chip (QR_{CML}) is enabled, this pin is connected to the on-chip QR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on chip (QR_{CML}) is disabled, this pin is the common-mode load for Q DAC and must be connected to AVSS through a resistor (see the Using the Internal Termination Resistors section). The recommended value for this external resistor is 0 Ω.
21	RLQN	Load Resistor (500 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTN externally.
22	QOUTN	Complementary Q DAC Current Output. Full-scale current is sourced when all data bits are 0s.
23	QOUTP	Q DAC Current Output. Full-scale current is sourced when all data bits are 1s.
24	RLQP	Load Resistor (500 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTP externally.
25	AVSS	Analog Common.
26	AVDD	Analog Supply Voltage (1.8 V to 3.3 V).
27	RLIP	Load Resistor (500 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTP externally.
28	IOUTP	I DAC Current Output. Full-scale current is sourced when all data bits are 1s.
29	IOUTN	Complementary I DAC Current Output. Full-scale current is sourced when all data bits are 0s.
30	RLIN	Load Resistor (500 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTN externally.

Pin No.	Mnemonic	Description
31	CMLI	I DAC Output Common-Mode Level. When the internal on chip (IR_{CML}) is enabled, this pin is connected to the on-chip IR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on chip (IR_{CML}) is disabled, this pin is the common-mode load for I DAC and must be connected to AVSS through a resistor (see the Using the Internal Termination Resistors section). The recommended value for this external resistor is 0 Ω.
32	FSADJQ/AUXQ	Full-Scale Current Output Adjust (FSADJQ). When the internal on chip (QR_{SET}) is disabled, this pin is the full-scale current output adjust for Q DAC and must be connected to AVSS through a resistor (see the Theory of Operation section). The nominal value for this external resistor is 16 kΩ for a 2 mA output current. Auxiliary Q DAC Output (AUXQ). When the internal on chip (QR_{SET}) is enabled, this pin is the auxiliary Q DAC output.
33	FSADJI/AUXI	Full-Scale Current Output Adjust (FSADJI). When the internal on chip (IR_{SET}) is disabled, this pin is the full-scale current output adjust for I DAC and must be connected to AVSS through a resistor (see the Theory of Operation section). The nominal value for this external resistor is 16 kΩ for a 2 mA output current. Auxiliary I DAC Output (AUXI). When the internal on chip (IR_{SET}) is enabled, this pin is the auxiliary I DAC output.
34	REFIO	Reference Input/Output. Serves as a reference input when the internal reference is disabled. Provides a 1.0 V reference output when in internal reference mode (a 0.1 µF capacitor to AVSS is required).
35	RESET/PINMD	This pin defines the operation mode of the part. A logic low (pull-down to DVSS) sets the part in SPI mode. Pulse RESET high to reset the SPI registers to their default values. A logic high (pull-up to DVDDIO) puts the device into pin mode (PINMD).
36	SCLK/CLKMD	Clock Input for Serial Port (SCLK). In SPI mode, this pin is the clock input for the serial port. Clock Mode (CLKMD). In pin mode, CLKMD determines the phase of the internal retiming clock. When DCLKIO = CLKIN, tie it to 0. When DCLKIO ≠ CLKIN, pulse 0 to 1 to edge trigger the internal retimer (see the Retimer section).
37	SDIO/FORMAT	Serial Port Input/Output (SDIO). In SPI mode, this pin is the bidirectional data line for the serial port. Format Pin (FORMAT). In pin mode, FORMAT determines the data format of digital data. A logic low (pull-down to DVSS) selects the binary input data format. A logic high (pull-up to DVDDIO) selects the twos complement input data format.
38	$\overline{CS}$/PWRDN	Active Low Chip Select ($\overline{CS}$). In SPI mode, this pin serves as the active low chip select. Power-Down (PWRDN). In pin mode, a logic high (pull-up to DVDDIO) powers down the device, except for the SPI port.
39	DB11 (MSB)	Digital Input (MSB).
40	DB10	Digital Input.
41 (EPAD)	Exposed Pad (EPAD)	The exposed pad is connected to AVSS and should be soldered to the ground plane. Exposed metal at the package corners is connected to this pad.

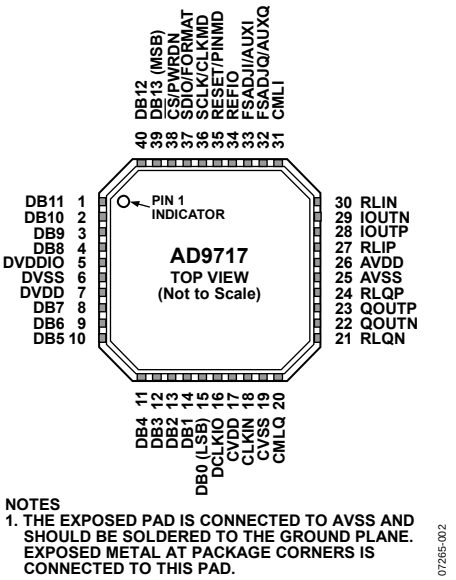


Figure 5. AD9717 Pin Configuration

Table 10. AD9717 Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 4	DB[11:8]	Digital Inputs.
5	DVDDIO	Digital I/O Supply Voltage (1.8 V to 3.3 V Nominal).
6	DVSS	Digital Common.
7	DVDD	Digital Core Supply Voltage (1.8 V). Strap DVDD to DVDDIO at 1.8 V. If DVDDIO > 1.8 V, bypass DVDD with a 1.0 µF capacitor; however, do not otherwise connect it. The LDO should not drive external loads.
8 to 14	DB[7:1]	Digital Inputs.
15	DB0 (LSB)	Digital Input (LSB).
16	DCLKIO	Data Input/Output Clock. Clock used to qualify input data.
17	CVDD	Sampling Clock Supply Voltage (1.8 V to 3.3 V). CVDD must be ≥ DVDD.
18	CLKIN	LVCMOS Sampling Clock Input.
19	CVSS	Sampling Clock Supply Voltage Common.
20	CMLQ	Q DAC Output Common-Mode Level. When the internal on chip (QR_{CML}) is enabled, this pin is connected to the on-chip QR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on chip (QR_{CML}) is disabled, this pin is the common-mode load for Q DAC and must be connected to AVSS through a resistor (see the Using the Internal Termination Resistors section). The recommended value for this external resistor is 0 Ω.
21	RLQN	Load Resistor (500 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTN externally.
22	QOUTN	Complementary Q DAC Current Output. Full-scale current is sourced when all data bits are 0s.
23	QOUTP	Q DAC Current Output. Full-scale current is sourced when all data bits are 1s.
24	RLQP	Load Resistor (500 Ω) to the CMLQ Pin. For the internal load resistor to be used, this pin should be tied to QOUTP externally.
25	AVSS	Analog Common.
26	AVDD	Analog Supply Voltage (1.8 V to 3.3 V).
27	RLIP	Load Resistor (500 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTP externally.
28	IOUTP	I DAC Current Output. Full-scale current is sourced when all data bits are 1s.
29	IOUTN	Complementary I DAC Current Output. Full-scale current is sourced when all data bits are 0s.
30	RLIN	Load Resistor (500 Ω) to the CMLI Pin. For the internal load resistor to be used, this pin should be tied to IOUTN externally.

Pin No.	Mnemonic	Description
31	CMLI	I DAC Output Common-Mode Level. When the internal on chip (IR_{CML}) is enabled, this pin is connected to the on-chip IR_{CML} resistor. It is recommended to leave this pin unconnected. When the internal on chip (IR_{CML}) is disabled, this pin is the common-mode load for I DAC and must be connected to AVSS through a resistor (see the Using the Internal Termination Resistors section). The recommended value for this external resistor is 0 Ω.
32	FSADJQ/AUXQ	Full-Scale Current Output Adjust (FSADJQ). When the internal on chip (QR_{SET}) is disabled, this pin is the full-scale current output adjust for Q DAC and must be connected to AVSS through a resistor (see the Theory of Operation section). The nominal value for this external resistor is 16 kΩ for a 2 mA output current. Auxiliary Q DAC Output (AUXQ). When the internal on chip (QR_{SET}) is enabled, this pin is the auxiliary Q DAC output.
33	FSADJI/AUXI	Full-Scale Current Output Adjust (FSADJI). When the internal on chip (IR_{SET}) is disabled, this pin is the full-scale current output adjust for I DAC and must be connected to AVSS through a resistor (see the Theory of Operation section). The nominal value for this external resistor is 16 kΩ for a 2 mA output current. Auxiliary I DAC Output (AUXI). When the internal on chip (IR_{SET}) is enabled, this pin is the auxiliary I DAC output.
34	REFIO	Reference Input/Output. Serves as a reference input when the internal reference is disabled. Provides a 1.0 V reference output when in internal reference mode (a 0.1 µF capacitor to AVSS is required).
35	RESET/PINMD	This pin defines the operation mode of the part. A logic low (pull-down to DVSS) sets the part in SPI mode. Pulse RESET high to reset the SPI registers to their default values. A logic high (pull-up to DVDDIO) puts the device into pin mode (PINMD).
36	SCLK/CLKMD	Clock Input for Serial Port (SCLK). In SPI mode, this pin is the clock input for the serial port. Clock Mode (CLKMD). In pin mode, CLKMD determines the phase of the internal retiming clock. When DCLKIO = CLKIN, tie it to 0. When DCLKIO ≠ CLKIN, pulse 0 to 1 to edge trigger the internal retimer (see the Retimer section).
37	SDIO/FORMAT	Serial Port Input/Output (SDIO). In SPI mode, this pin is the bidirectional data line for the serial port. Format Pin (FORMAT). In pin mode, FORMAT determines the data format of digital data. A logic low (pull-down to DVSS) selects the binary input data format. A logic high (pull-up to DVDDIO) selects the twos complement input data format.
38	$\overline{CS}$/PWRDN	Active Low Chip Select ($\overline{CS}$). In SPI mode, this pin serves as the active low chip select. Power-Down (PWRDN). In pin mode, a logic high (pull-up to DVDDIO) powers down the device, except for the SPI port.
39	DB13 (MSB)	Digital Input (MSB).
40	DB12	Digital Input.
41 (EPAD)	Exposed Pad (EPAD)	The exposed pad is connected to AVSS and should be soldered to the ground plane. Exposed metal at the package corners is connected to this pad.

TYPICAL PERFORMANCE CHARACTERISTICS

I_{xOUTFS} = 2 mA, maximum sample rate, unless otherwise noted. DVDD is always at 1.8 V.

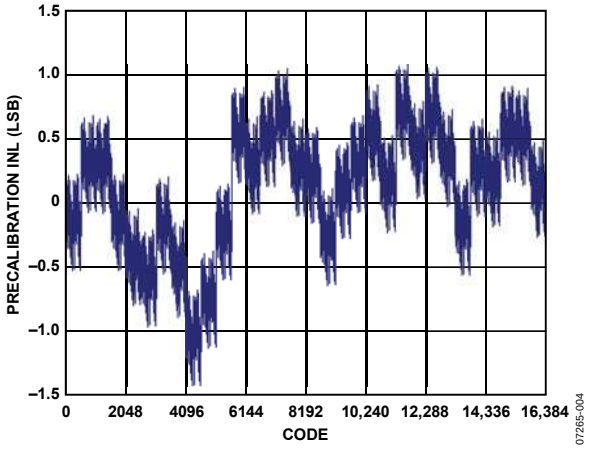


Figure 6. AD9717 Precalibration INL at 1.8 V (DVDD = 1.8 V)

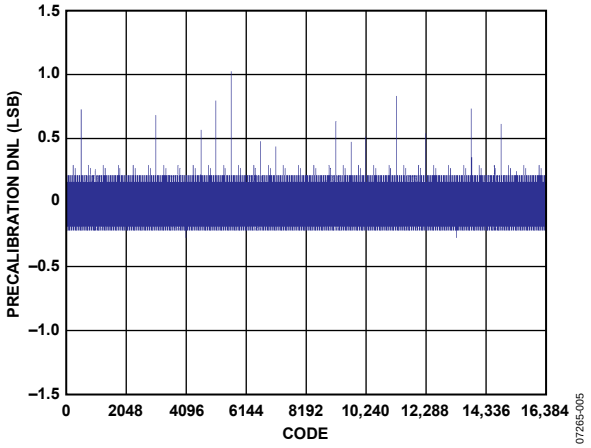


Figure 7. AD9717 Precalibration DNL at 1.8 V (DVDD = 1.8 V)

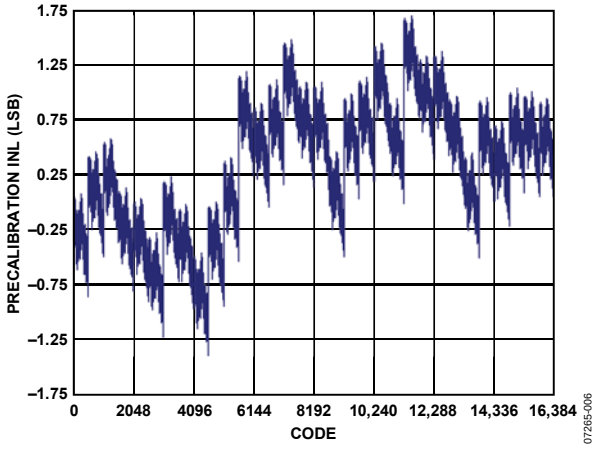


Figure 8. AD9717 Precalibration INL at 3.3 V (DVDD = 1.8 V)

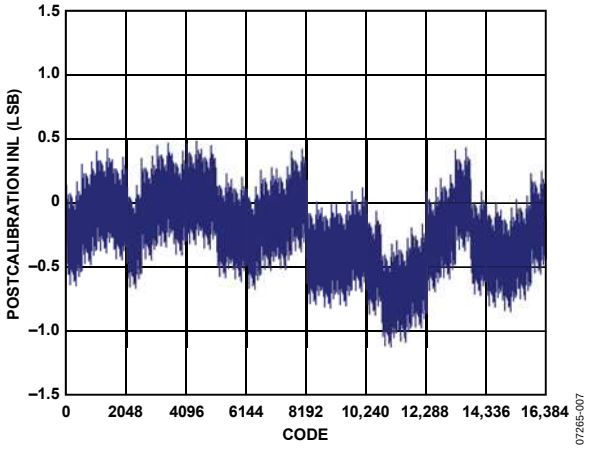


Figure 9. AD9717 Postcalibration INL at 1.8 V (DVDD = 1.8 V)

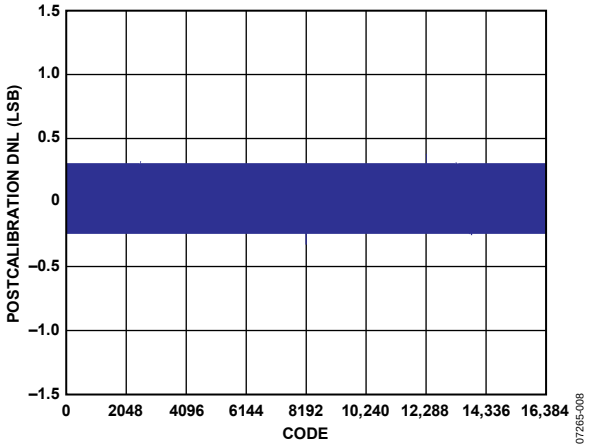


Figure 10. AD9717 Postcalibration DNL at 1.8 V (DVDD = 1.8 V)

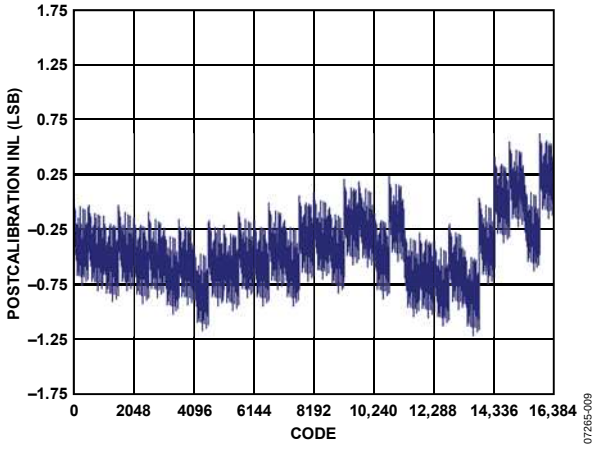


Figure 11. AD9717 Postcalibration INL at 3.3 V (DVDD = 1.8 V)

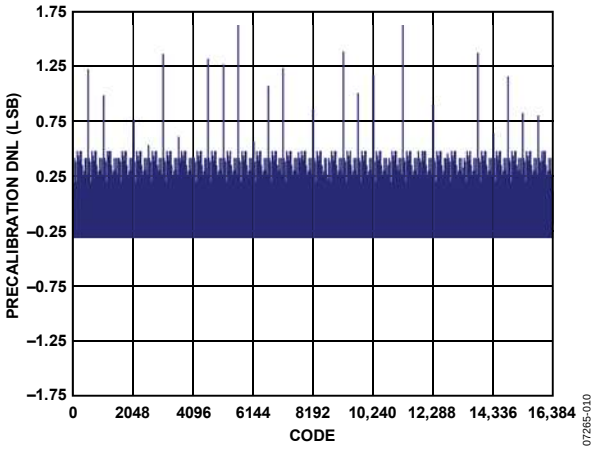


Figure 12. AD9717 Precalibration DNL at 3.3 V

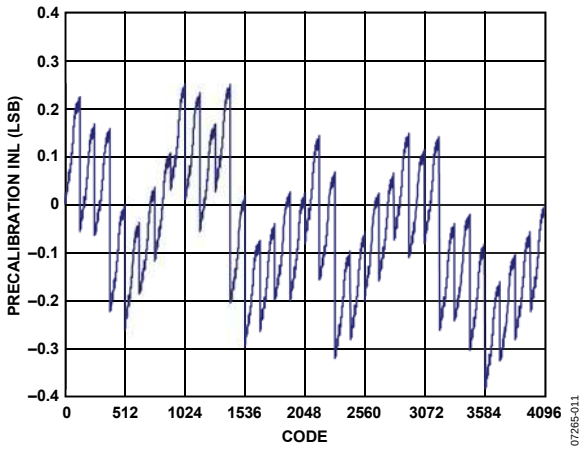


Figure 13. AD9716 Precalibration INL at 1.8 V

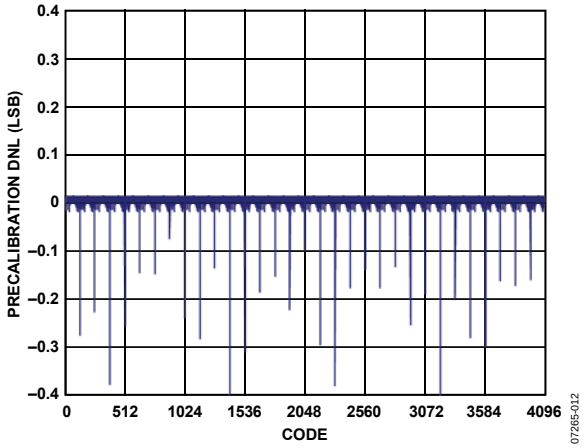


Figure 14. AD9716 Precalibration DNL at 1.8 V

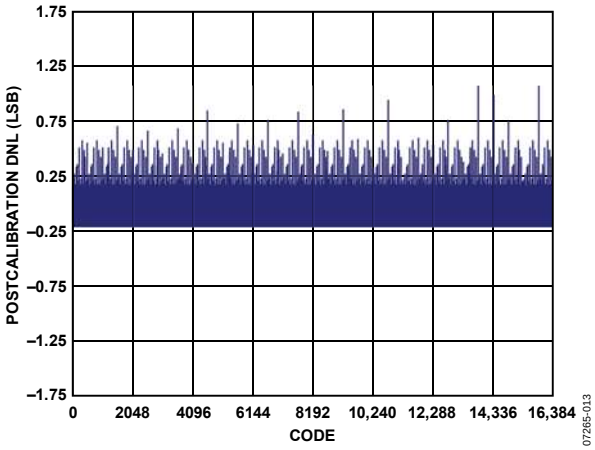


Figure 15. AD9717 Postcalibration DNL at 3.3 V

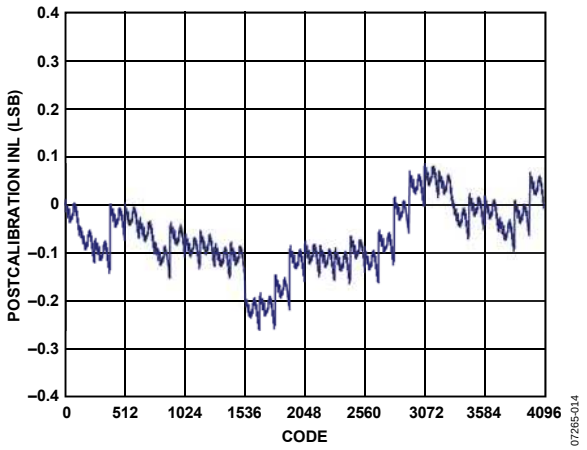


Figure 16. AD9716 Postcalibration INL at 1.8 V

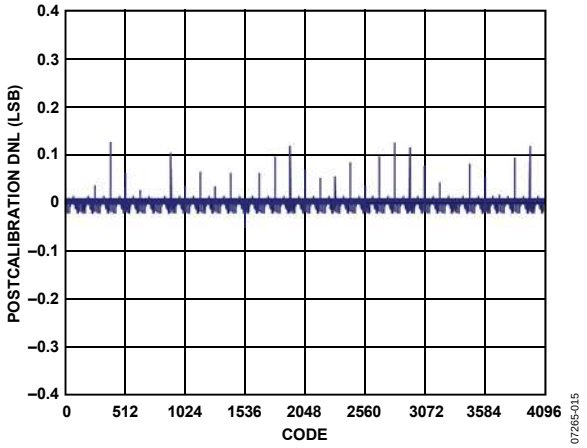


Figure 17. AD9716 Postcalibration DNL at 1.8 V

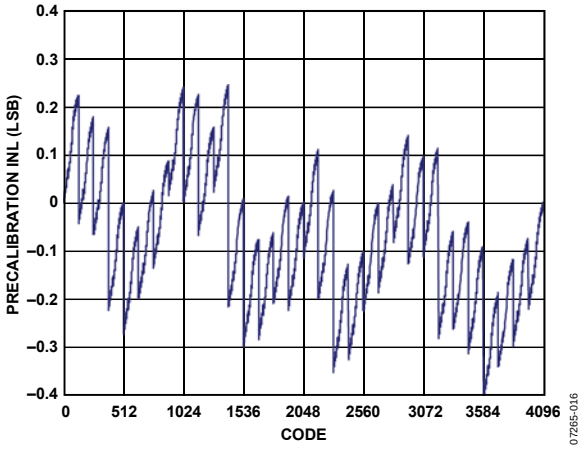


Figure 18. AD9716 Precalibration INL at 3.3 V

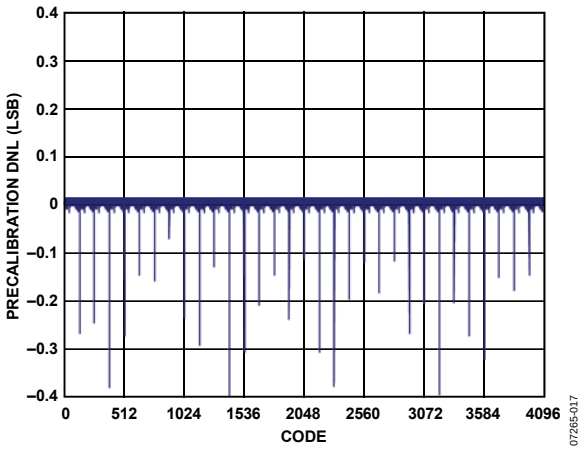


Figure 19. AD9716 Precalibration DNL at 3.3 V

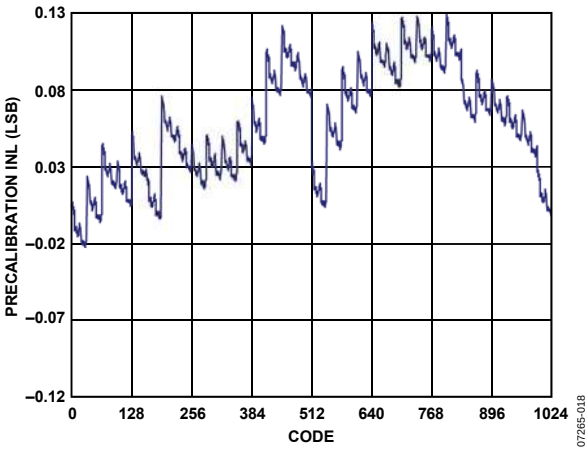


Figure 20. AD9715 Precalibration INL at 1.8 V

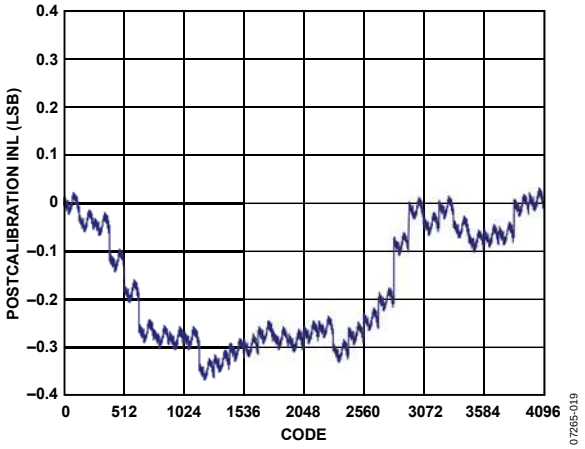


Figure 21. AD9716 Postcalibration INL at 3.3 V

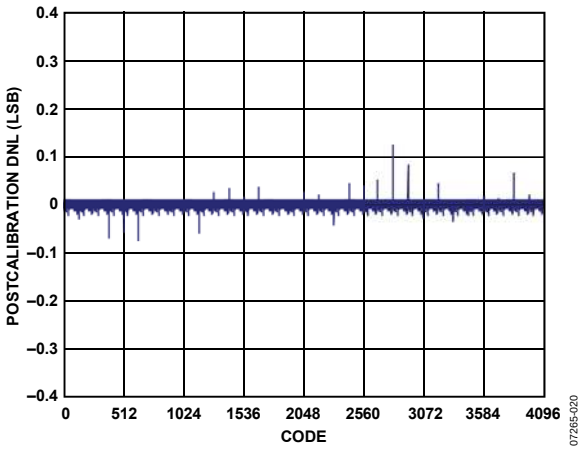


Figure 22. AD9716 Postcalibration DNL at 3.3 V

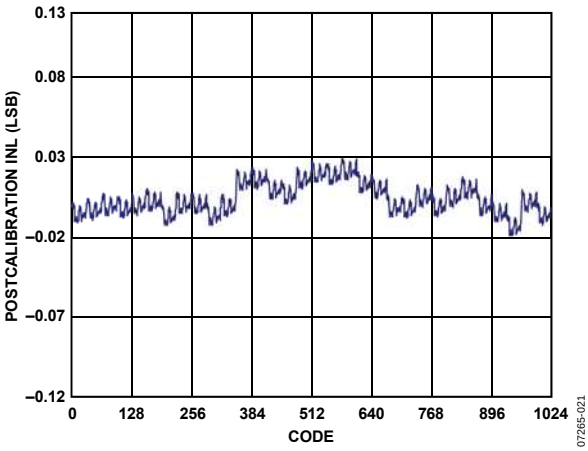


Figure 23. AD9715 Postcalibration INL at 1.8 V

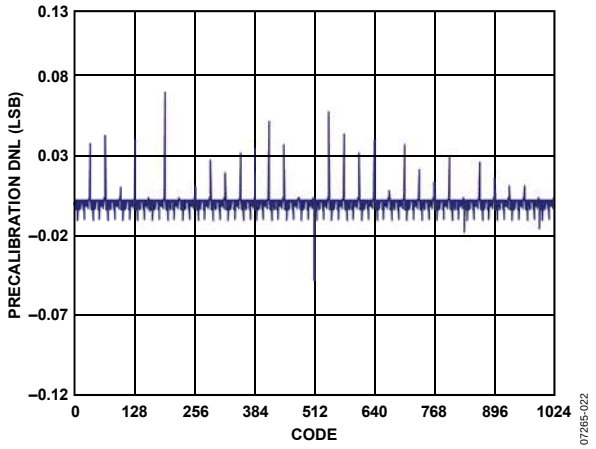


Figure 24. AD9715 Precalibration DNL at 1.8 V

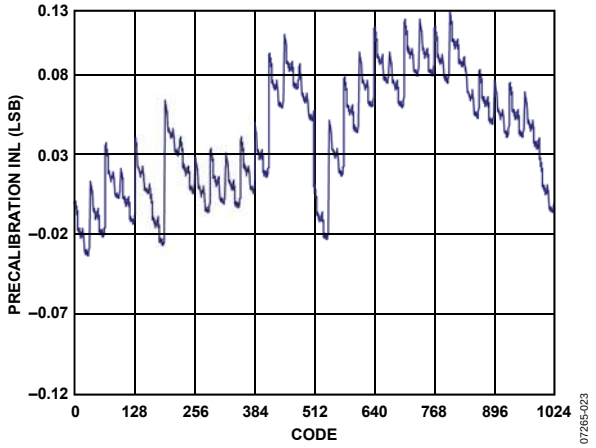


Figure 25. AD9715 Precalibration INL at 3.3 V

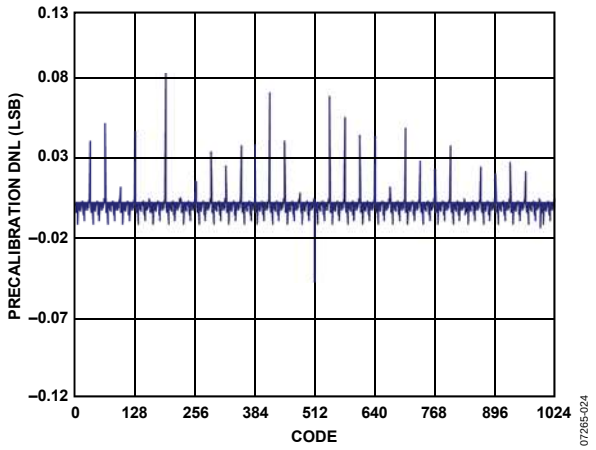


Figure 26. AD9715 Precalibration DNL at 3.3 V

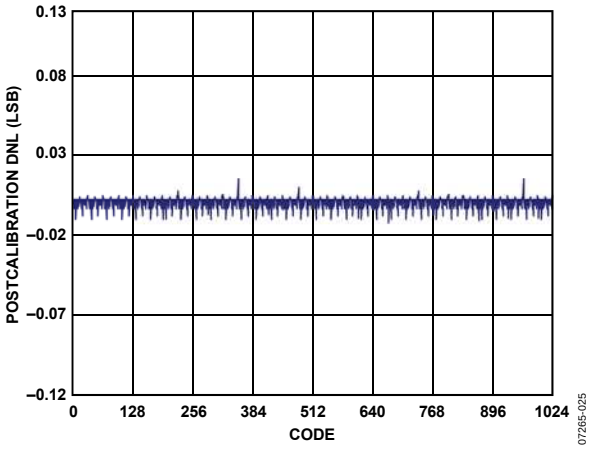


Figure 27. AD9715 Postcalibration DNL at 1.8 V

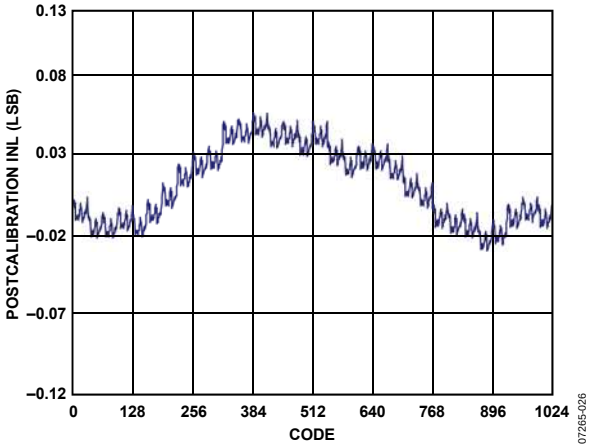


Figure 28. AD9715 Postcalibration INL at 3.3 V

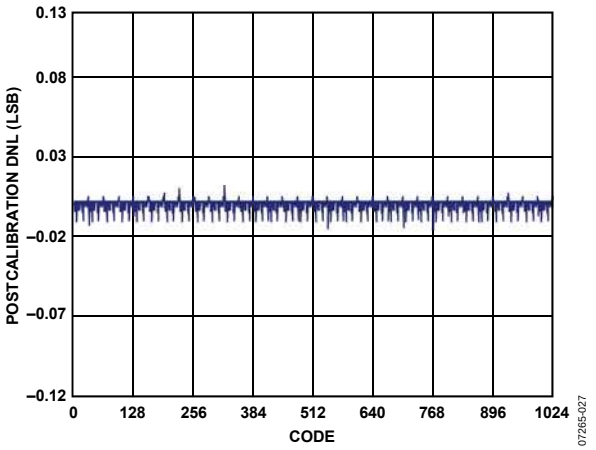


Figure 29. AD9715 Postcalibration DNL at 3.3 V

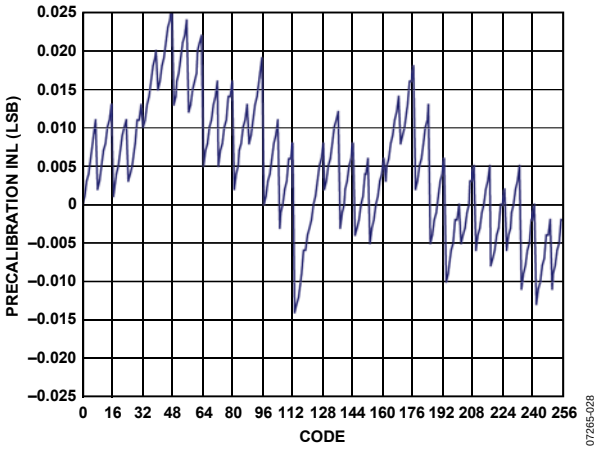


Figure 30. AD9714 Precalibration INL at 1.8 V

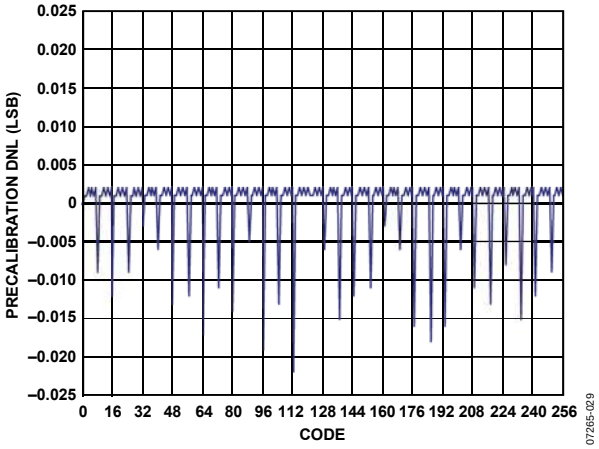


Figure 31. AD9714 Precalibration DNL at 1.8 V

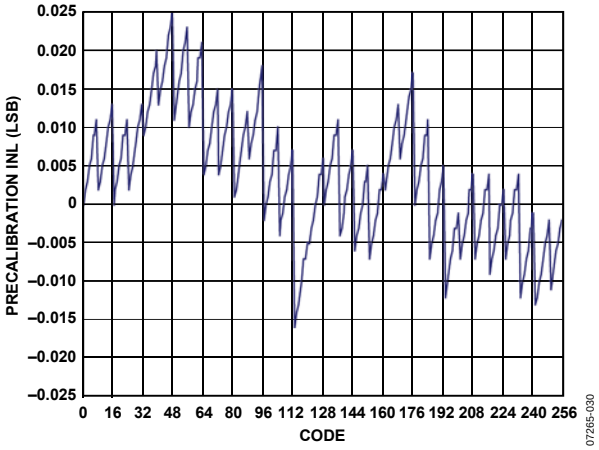


Figure 32. AD9714 Precalibration INL at 3.3 V

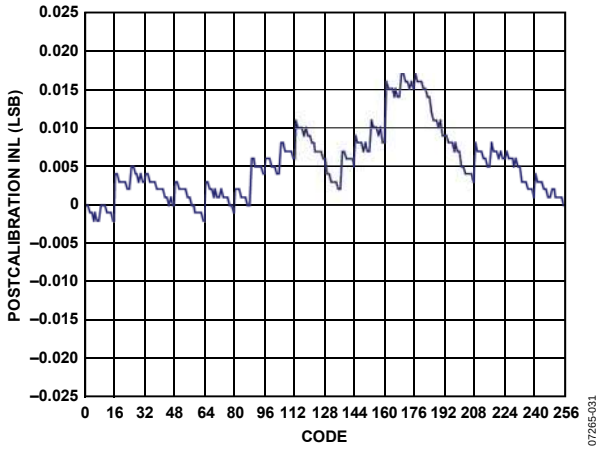


Figure 33. AD9714 Postcalibration INL at 1.8 V

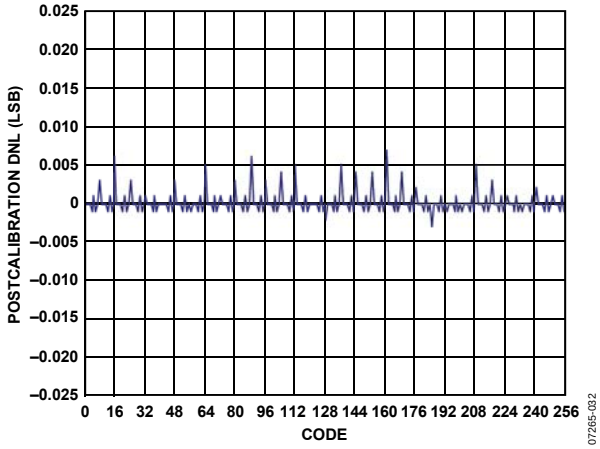


Figure 34. AD9714 Postcalibration DNL at 1.8 V

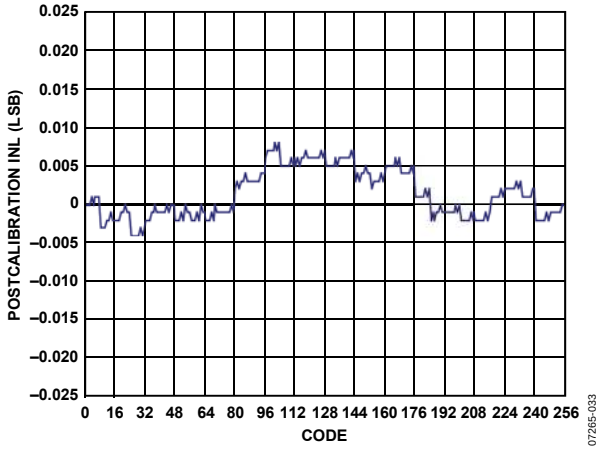


Figure 35. AD9714 Postcalibration INL at 3.3 V

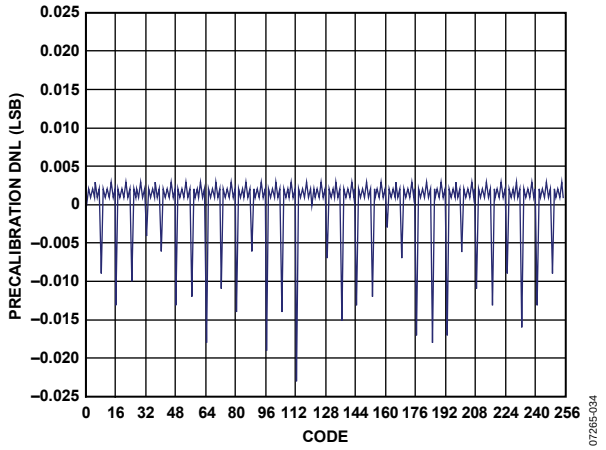


Figure 36. AD9714 Precalibration DNL at 3.3 V

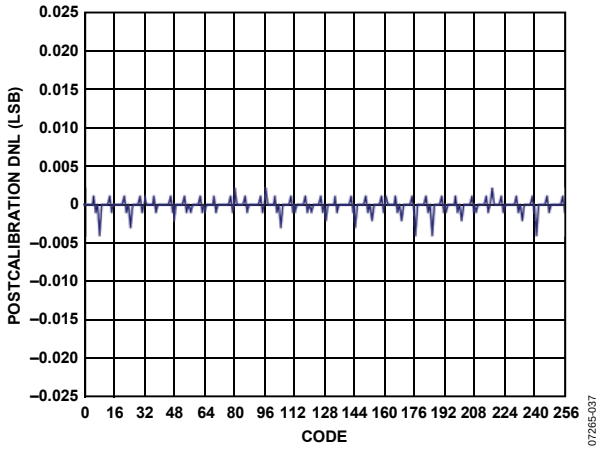


Figure 39. AD9714 Postcalibration DNL at 3.3 V

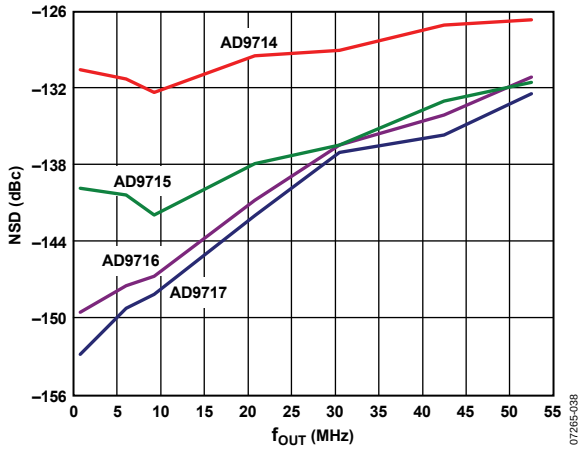


Figure 37. AD9714/AD9715/AD9716/AD9717 Noise Spectral Density at 1.8 V

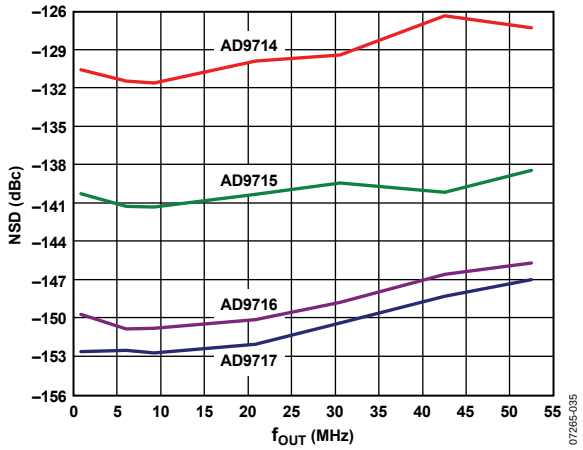


Figure 40. AD9714/AD9715/AD9716/AD9717 Noise Spectral Density at 3.3 V

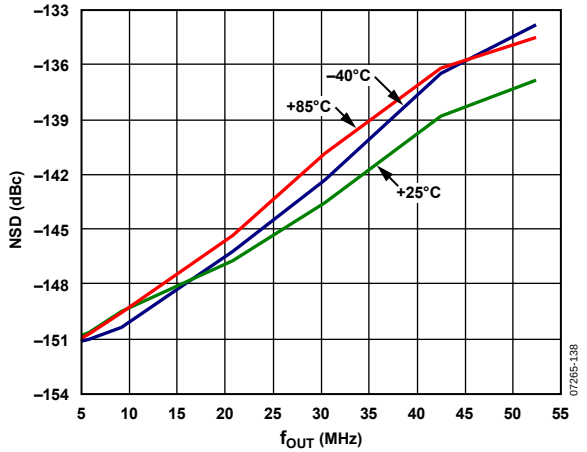


Figure 38. AD9717 Noise Spectral Density at Three Temperatures, 1.8 V

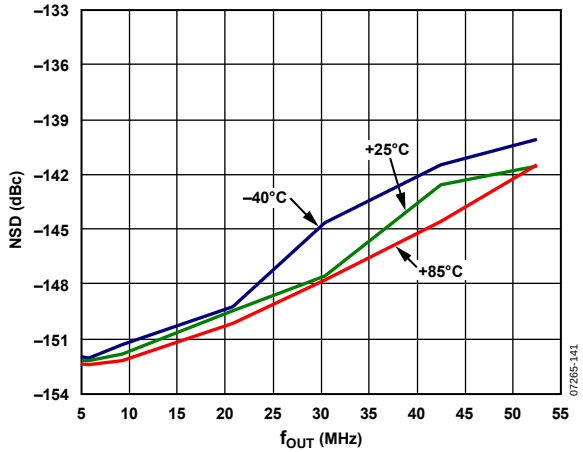


Figure 41. AD9717 Noise Spectral Density at Three Temperatures, 3.3 V

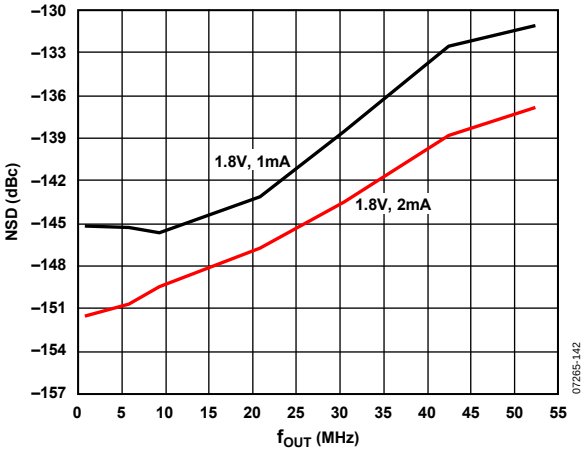


Figure 42. AD9717 Noise Spectral Density at Two Output Currents, 1.8 V

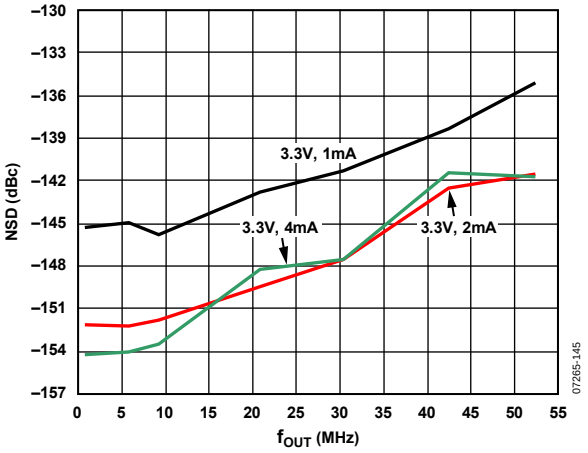


Figure 45. AD9717 Noise Spectral Density at Three Output Currents, 3.3 V

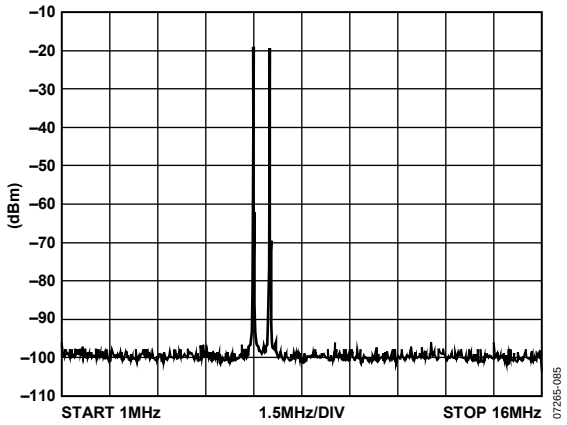


Figure 43. AD9717 Two Tone Spectrum, 1.8 V

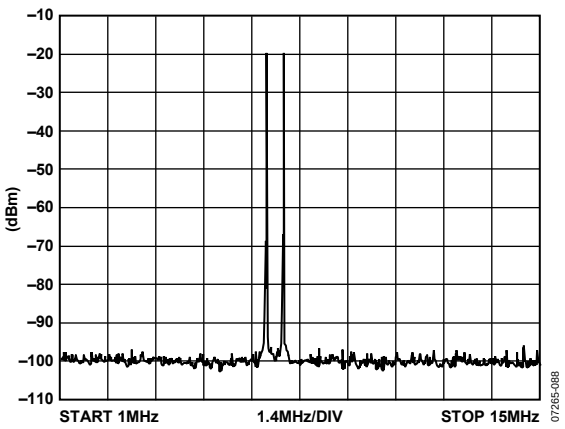


Figure 46. AD9717 Two Tone Spectrum, 3.3 V

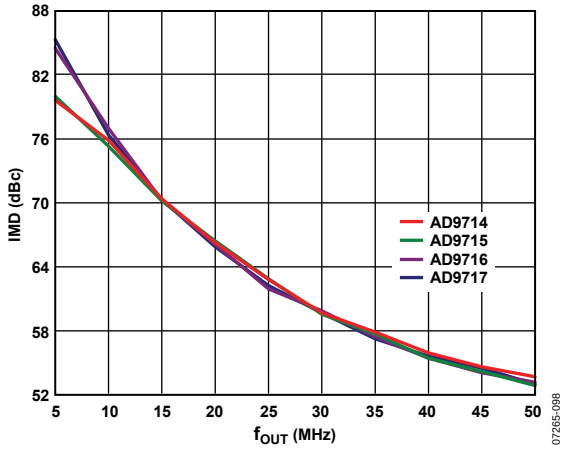


Figure 44. AD9714/AD9715/AD9716/AD9717 IMD at 1.8 V

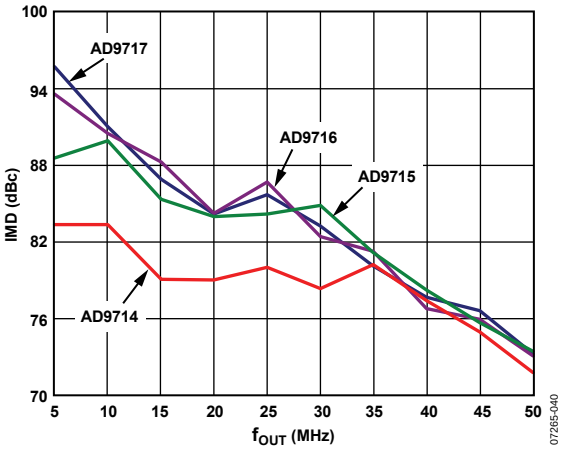


Figure 47. AD9714/AD9715/AD9716/AD9717 IMD at 3.3 V

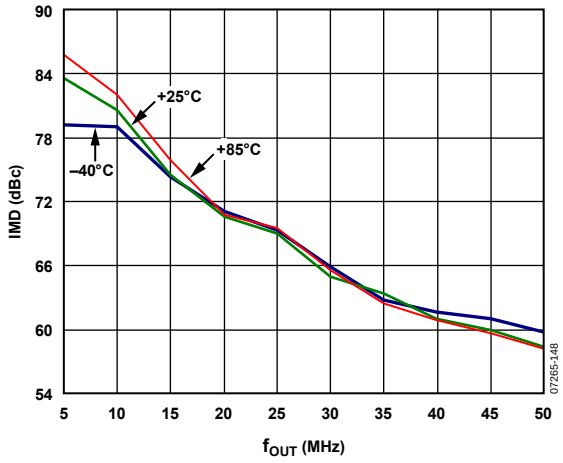


Figure 48. AD9717 IMD at Three Temperatures, 1.8 V

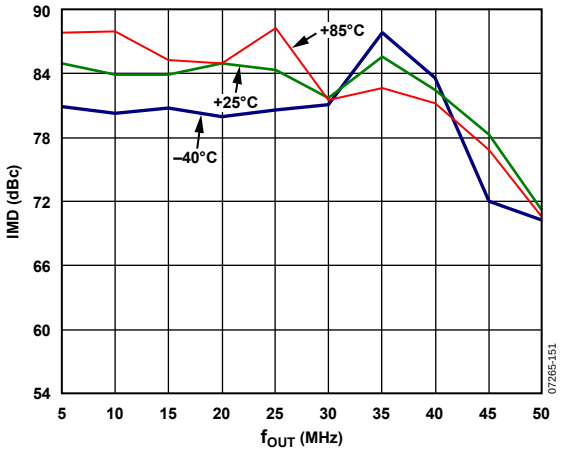


Figure 51. AD9717 IMD at Three Temperatures, 3.3 V

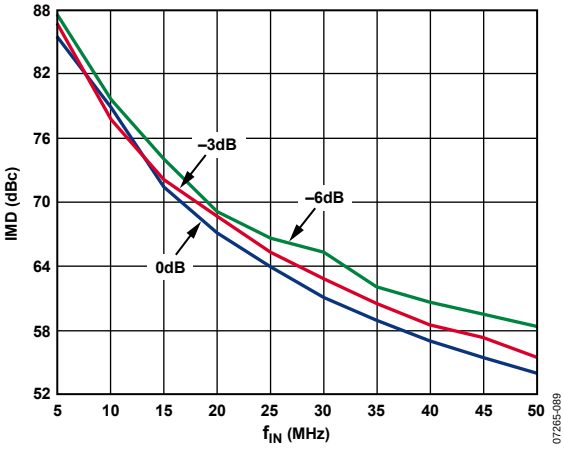


Figure 49. AD9717 IMD at Three Digital Input Levels, 1.8 V

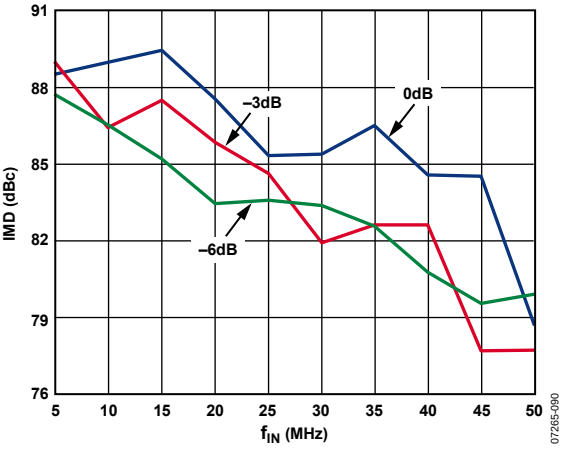


Figure 52. AD9717 IMD at Three Digital Input Levels, 3.3 V

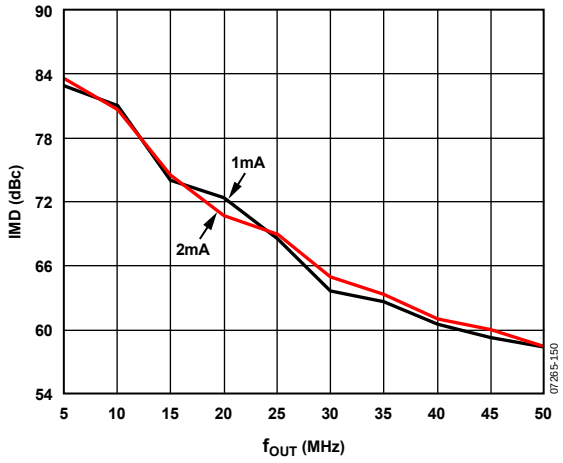


Figure 50. AD9717 IMD at Two Output Currents, 1.8 V

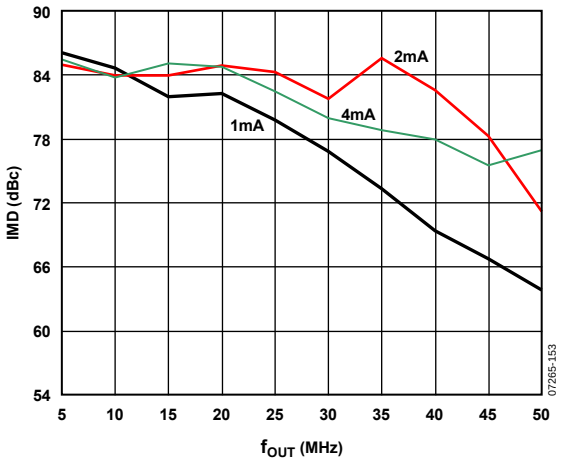


Figure 53. AD9717 IMD at Three Output Currents, 3.3 V

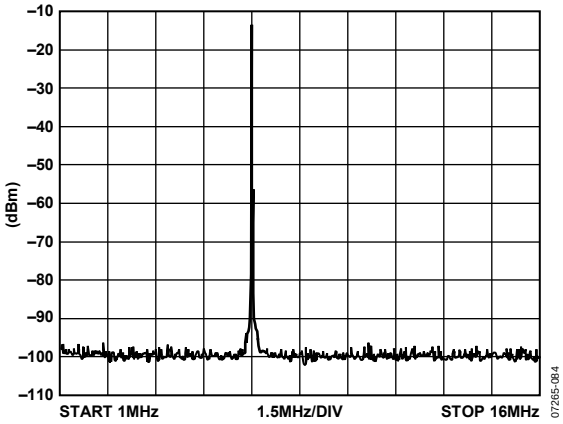


Figure 54. AD9717 Single-Tone Spectrum, 1.8 V

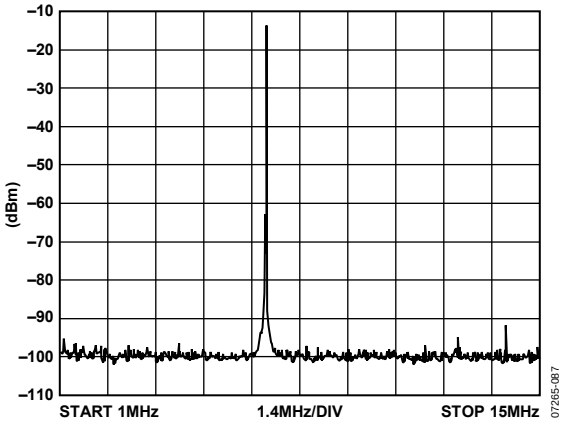


Figure 57. AD9717 Single-Tone Spectrum, 3.3 V

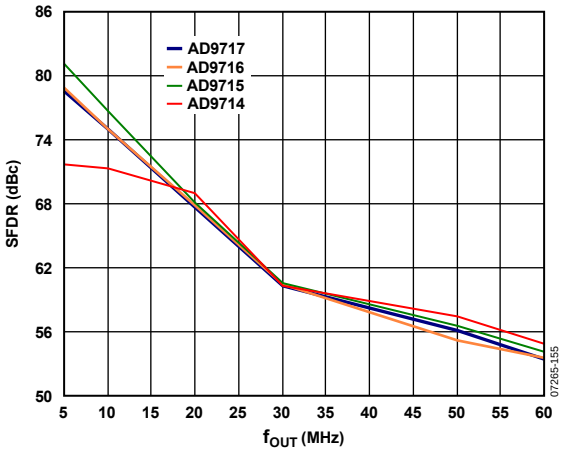


Figure 55. AD9714/AD9715/AD9716/AD9717 SFDR at 1.8 V

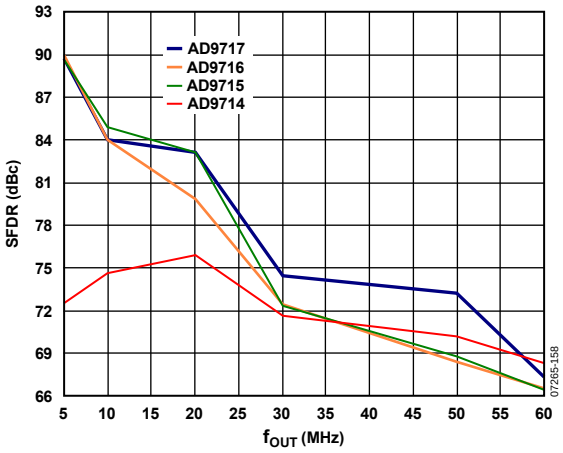


Figure 58. AD9714/AD9715/AD9716/AD9717 SFDR at 3.3 V

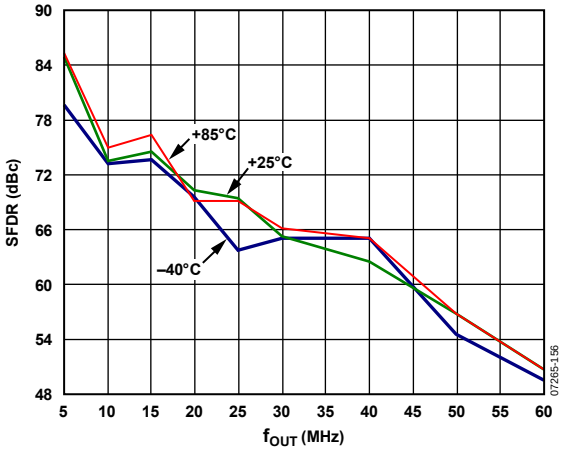


Figure 56. AD9717 SFDR at Three Temperatures, 1.8 V

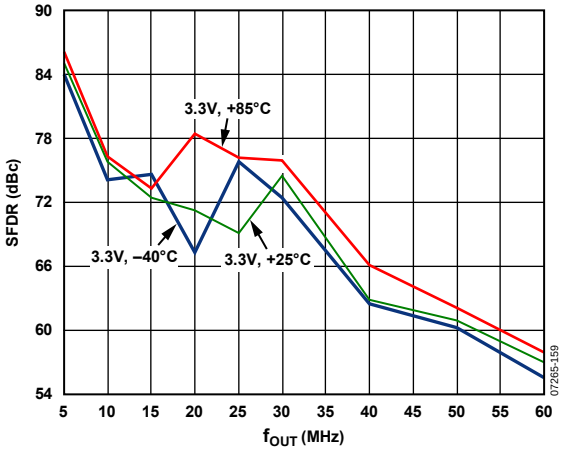


Figure 59. AD9717 SFDR at Three Temperatures, 3.3 V

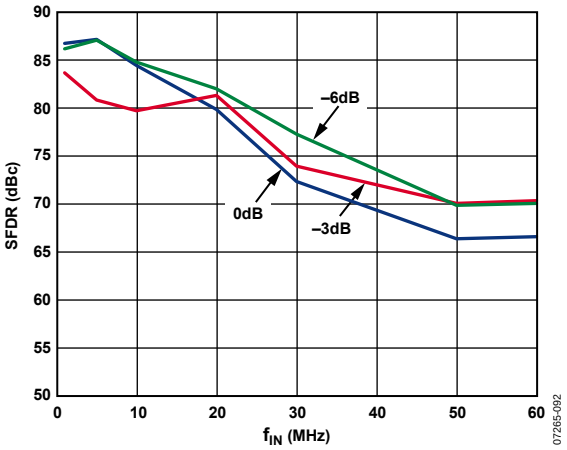


Figure 60. SFDR at Three Digital Input Levels vs. f_{IN}, 1.8 V

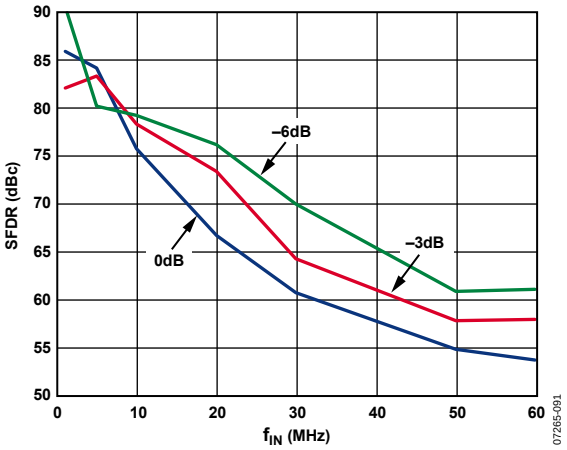


Figure 63. SFDR at Three Digital Input Levels vs. f_{IN}, 3.3 V

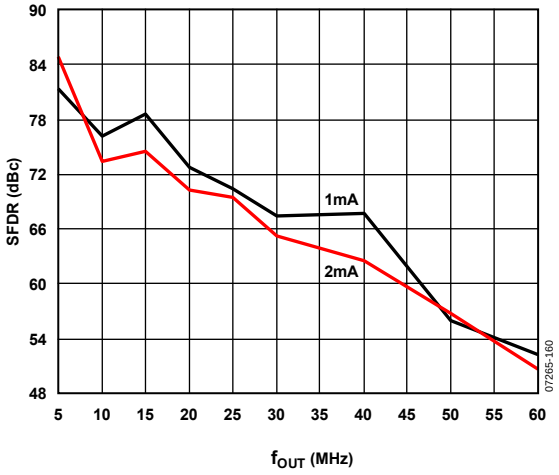


Figure 61. SFDR at Two Output Currents, 1.8 V

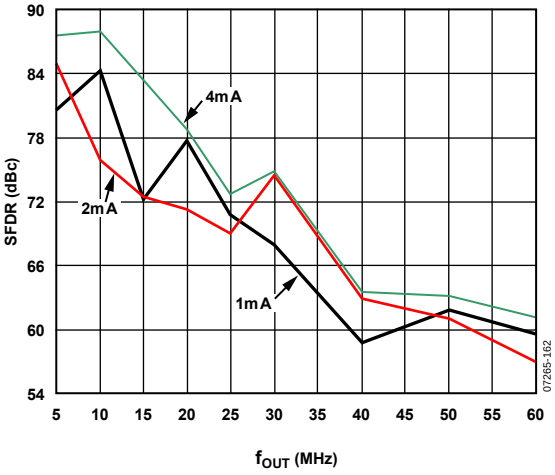


Figure 64. SFDR at Three Output Currents, 3.3 V

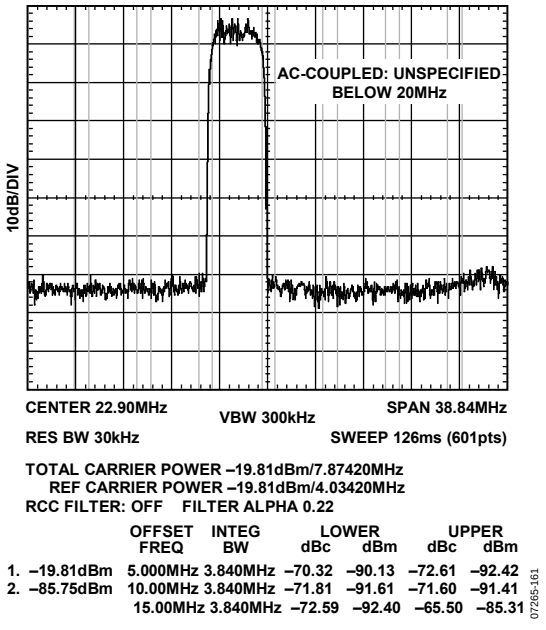


Figure 62. AD9717 One-Carrier ACLR, 1.8 V

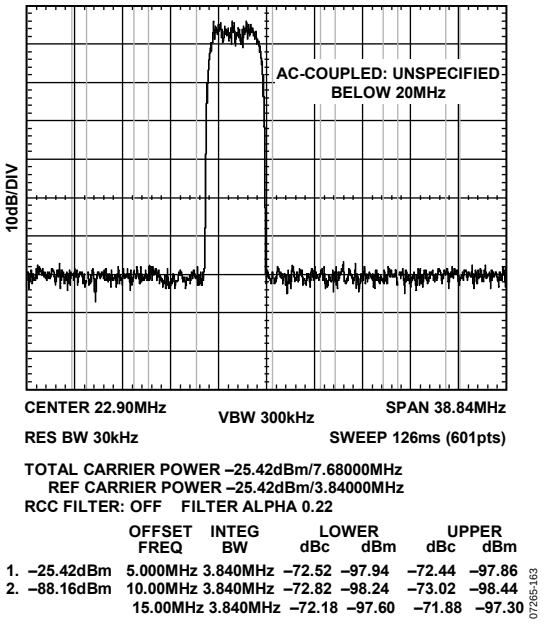


Figure 65. AD9717 One-Carrier ACLR, 3.3 V

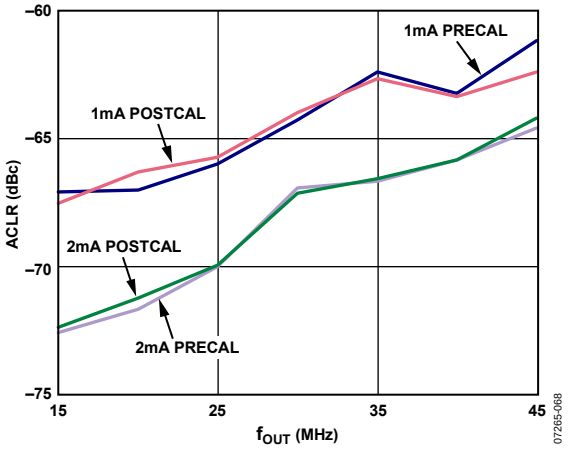


Figure 66. AD9717 One-Carrier W-CDMA First ACLR, 1.8 V

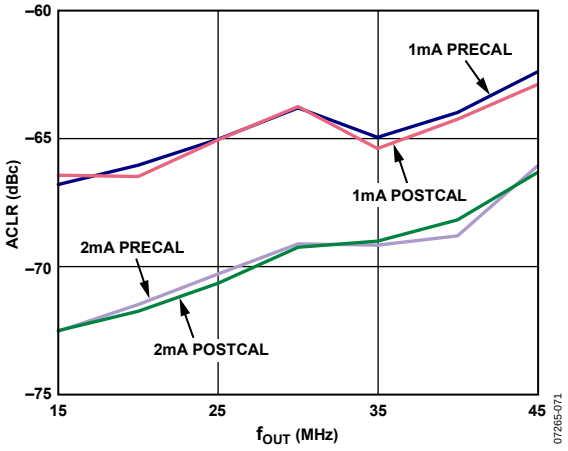


Figure 67. AD9717 One-Carrier W-CDMA Second ACLR, 1.8 V

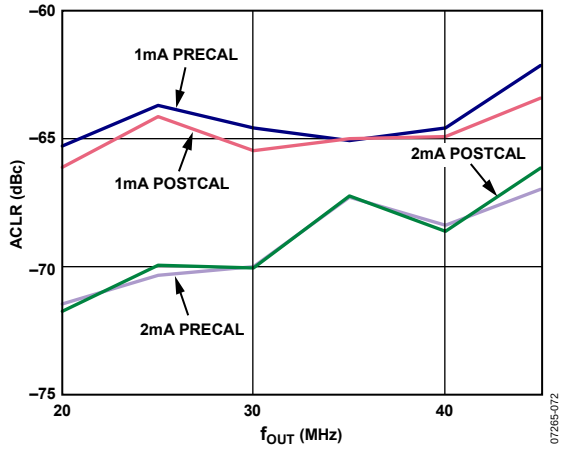


Figure 68. AD9717 One-Carrier W-CDMA Third ACLR, 1.8 V

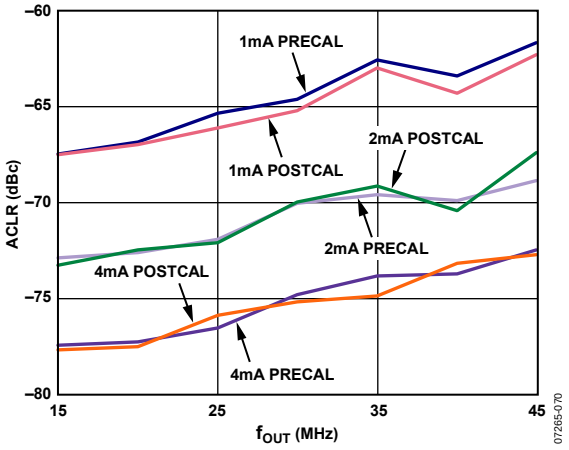


Figure 69. AD9717 One-Carrier W-CDMA First ACLR, 3.3 V

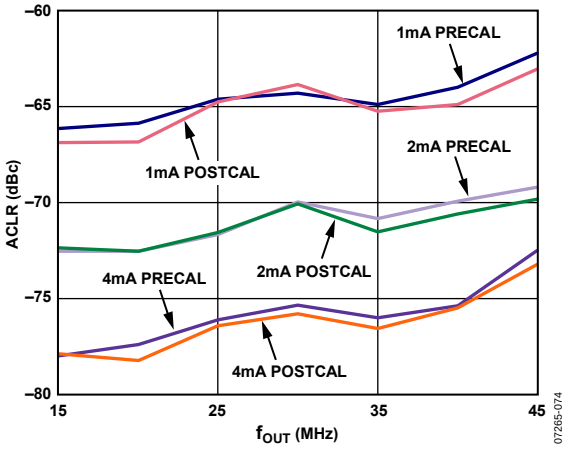
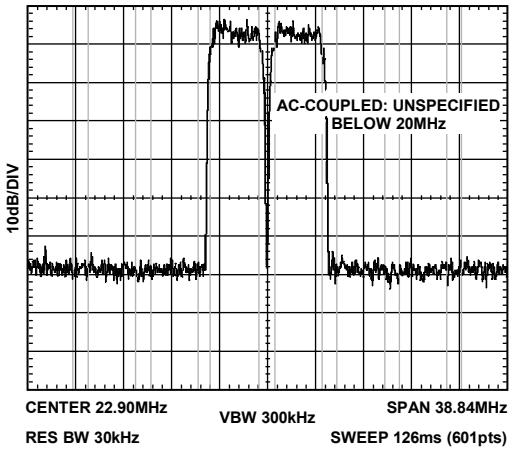


Figure 70. AD9717 One-Carrier W-CDMA Second ACLR, 3.3 V

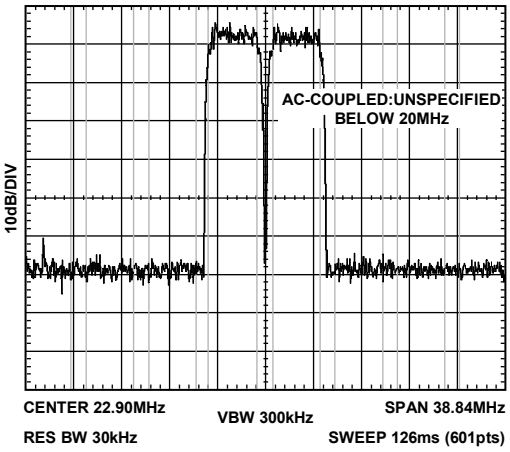
Figure 71. AD9717 One-Carrier W-CDMA Third ACLR, 3.3 V



		OFFSET FREQ	INTEG BW	LOWER dBc	LOWER dBm	UPPER dBc	UPPER dBm
1.	–25.84dBm	5.000MHz	3.840MHz	–65.45	–91.30	–65.63	–91.47
2.	–26.35dBm	10.00MHz	3.840MHz	–67.01	–92.85	–67.05	–92.89
		15.00MHz	3.840MHz	–65.22	–91.06	–65.33	–91.18

07265-164

Figure 72. AD9717 Two-Carrier ACLR, 1.8 V



		OFFSET FREQ	INTEG BW	LOWER dBc	LOWER dBm	UPPER dBc	UPPER dBm
1.	–25.86dBm	5.000MHz	3.840MHz	–66.28	–92.13	–66.68	–92.53
2.	–26.47dBm	10.00MHz	3.840MHz	–68.17	–94.02	–66.93	–92.78
		15.00MHz	3.840MHz	–64.89	–90.73	–65.84	–91.69

07265-165

Figure 75. AD9717 Two-Carrier ACLR, 3.3 V

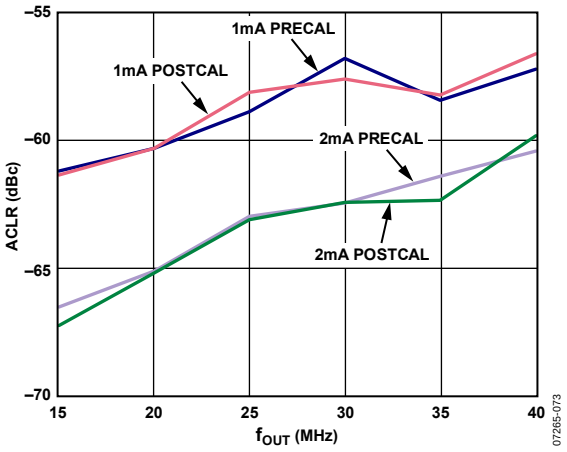


Figure 73. AD9717 Two-Carrier W-CDMA First ACLR, 1.8 V

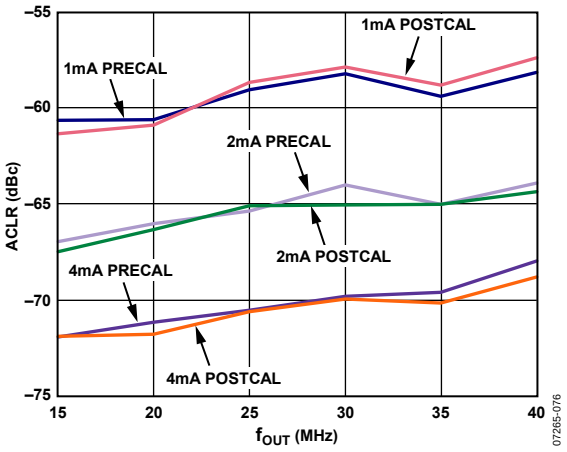


Figure 76. AD9717 Two-Carrier W-CDMA First ACLR, 3.3 V

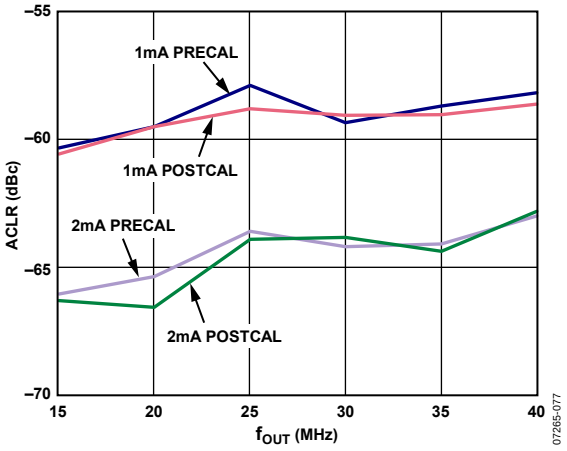


Figure 74. AD9717 Two-Carrier W-CDMA Second ACLR, 1.8 V

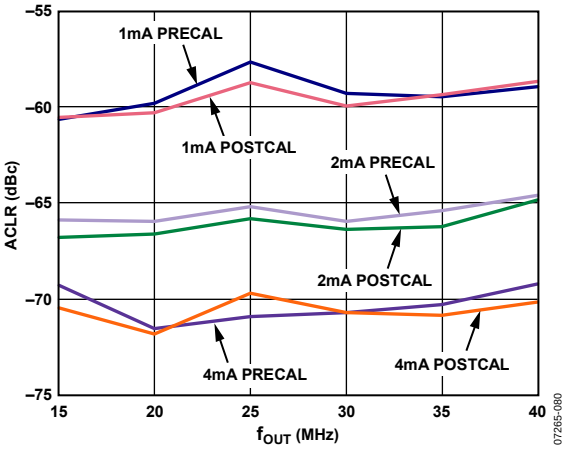


Figure 77. AD9717 Two-Carrier W-CDMA Second ACLR, 3.3 V

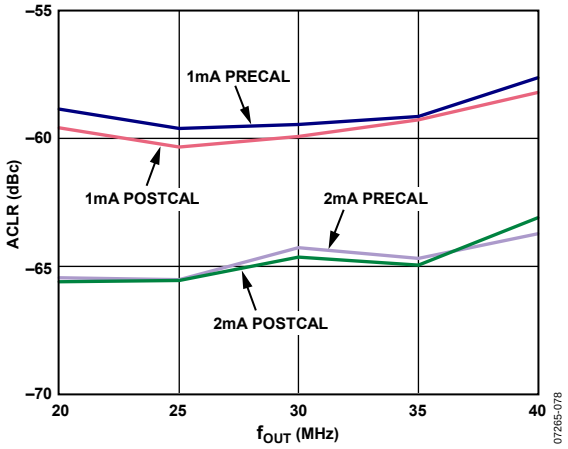


Figure 78. AD9717 Two-Carrier W-CDMA Third ACLR, 1.8 V

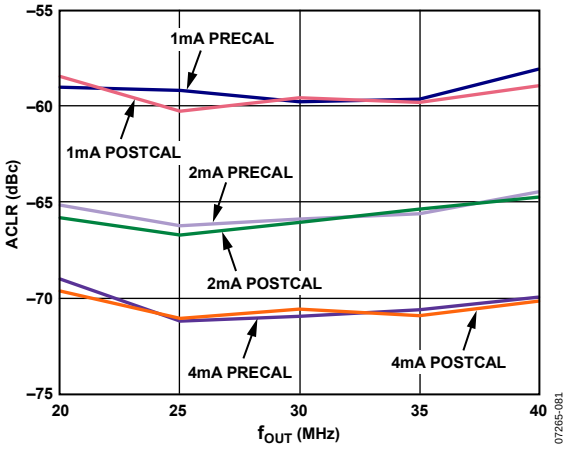


Figure 81. AD9717 Two-Carrier W-CDMA Third ACLR, 3.3 V

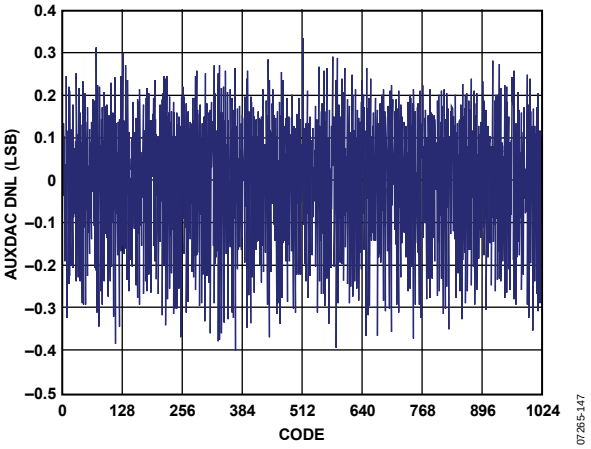


Figure 79. AUXDAC DNL

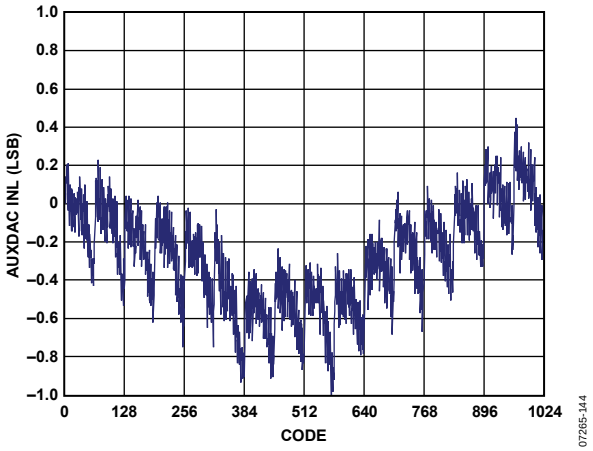


Figure 82. AUXDAC INL

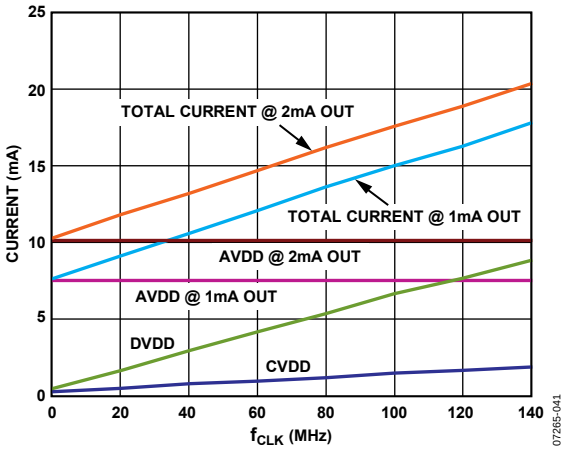


Figure 80. Supply Current vs. Clock Frequency at 1.8 V

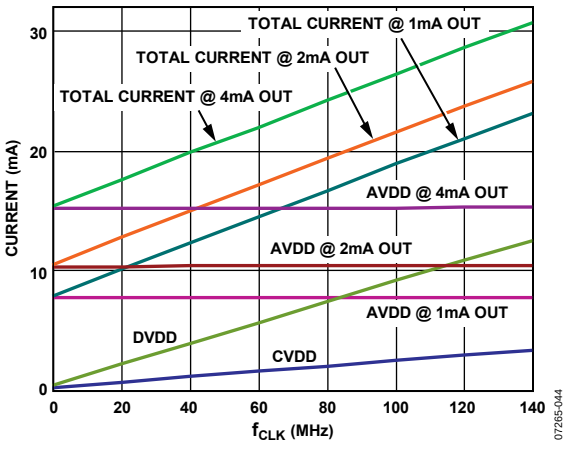


Figure 83. Supply Current vs. Clock Frequency at 3.3 V

TERMINOLOGY

Linearity Error or Integral Nonlinearity (INL)
Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

Differential Nonlinearity (DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A DAC is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
Offset error is the deviation of the output current from the ideal of zero. For I_{OUTP}, 0 mA output is expected when the inputs are all 0. For I_{OUTN}, 0 mA output is expected when all inputs are set to 1.

Gain Error
Gain error is the difference between the actual and the ideal output span. The actual span is determined by the difference between the output when all inputs are set to 1 and the output when all inputs are set to 0.

Output Compliance Range
Output compliance range is the range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits can cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient value (25°C) to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range per degree Celsius (ppm FSR/°C). For reference drift, the drift is reported in parts per million per degree Celsius (ppm/°C).

Power Supply Rejection
Power supply rejection is the maximum change in the full-scale output as the supplies are varied from minimum to maximum specified voltages.

Settling Time
Settling time is the time required for the output to reach and remain within a specified error band around its final value, measured from the start of the output transition.

Spurious Free Dynamic Range (SFDR)
SFDR is the difference, in decibels (dB), between the peak amplitude of the output signal and the peak spurious signal between dc and the frequency equal to half the input data rate.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured fundamental. It is expressed as a percentage or in decibels.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels (dB).

Adjacent Channel Leakage Ratio (ACLR)
ACLR is the ratio in decibels relative to the carrier (dBc) between the measured power within a channel relative to its adjacent channel.

Complex Image Rejection
In a traditional two-part upconversion, two images are created around the second IF frequency. These images have the effect of wasting transmitter power and system bandwidth. By placing the real part of a second complex modulator in series with the first complex modulator, either the upper or lower frequency image near the second IF can be rejected.

THEORY OF OPERATION

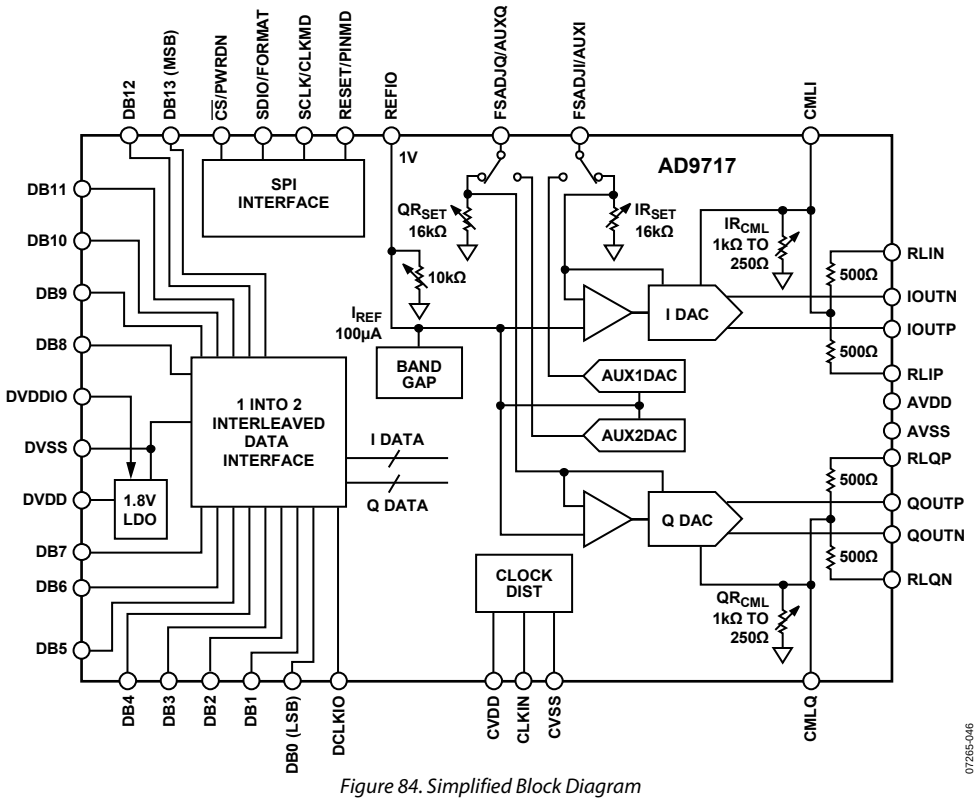


Figure 84. Simplified Block Diagram

Figure 84 shows a simplified block diagram of the AD9714/AD9715/AD9716/AD9717 that consists of two DACs, digital control logic, and a full-scale output current control. Each DAC contains a PMOS current source array capable of providing a nominal full-scale current (I_{xOUTFS}) of 2 mA and a maximum of 4 mA. The arrays are divided into 31 equal currents that make up the five most significant bits (MSBs). The next four bits, or middle bits, consist of 15 equal current sources whose value is 1/16 of an MSB current source. The remaining LSBs are binary weighted fractions of the current sources of the middle bits. Implementing the middle and lower bits with current sources, instead of an R-2R ladder, enhances its dynamic performance for multitone or low amplitude signals and helps maintain the high output impedance of the DACs (that is, >200 MΩ).

All of these current sources are switched to one or the other of the two output nodes (I_{OUTP} or I_{OUTN}) via PMOS differential current switches. The switches are based on the architecture that was pioneered in the AD976x family, with further refinements to reduce distortion contributed by the switching transient. This switch architecture also reduces various timing errors and provides matching complementary drive signals to the inputs of the differential current switches.

The analog and digital I/O sections of the AD9714/AD9715/AD9716/AD9717 have separate power supply inputs (AVDD and DVDDIO) that can operate independently over a 1.8 V to 3.3 V range. The core digital section requires 1.8 V. An optional on-chip LDO is provided for DVDDIO supplies greater than 1.8 V, or the 1.8 V can be supplied directly through DVDD. A 1.0 µF bypass capacitor at DVDD (Pin 7) is required when using the LDO.

The core is capable of operating at a rate of up to 125 MSPS. It consists of edge-triggered latches and the segment decoding logic circuitry. The analog section includes PMOS current sources, associated differential switches, a 1.0 V band gap voltage reference, and a reference control amplifier.

Each DAC full-scale output current is regulated by the reference control amplifier and can be set from 1 mA to 4 mA via an external resistor, xR_{SET}, connected to its full-scale adjust pin (FSADJx).

The external resistor, in combination with both the reference control amplifier and voltage reference, V_{REFIO}, sets the reference current, I_{xREF}, which is replicated to the segmented current sources with the proper scaling factor. The full-scale current, I_{xOUTFS}, is $32 \times I_{xREF}$.

Optional on-chip xR_{SET} resistors are provided that can be programmed between a nominal value of 8 kΩ to 32 kΩ (4 mA to 1 mA I_{xOUTFS}, respectively).

The AD9714/AD9715/AD9716/AD9717 provide the option of setting the output common mode to a value other than AVSS via the output common-mode pins (CMLI and CMLQ). This facilitates directly interfacing the output of the AD9714/AD9715/AD9716/AD9717 to components that require common-mode levels greater than 0 V.

SERIAL PERIPHERAL INTERFACE (SPI)

The serial port of the AD9714/AD9715/AD9716/AD9717 is a flexible, synchronous serial communications port that allows easy interfacing to many industry-standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola SPI and Intel® SSR protocols. The interface allows read/write access to all registers that configure the AD9714/AD9715/AD9716/AD9717. Single or multiple byte transfers are supported, as well as MSB first or LSB first transfer formats. The serial interface port of the AD9714/AD9715/AD9716/AD9717 is configured as a single I/O pin on the SDIO pin.

GENERAL OPERATION OF THE SERIAL INTERFACE

There are two phases to a communications cycle on the AD9714/AD9715/AD9716/AD9717. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9714/AD9715/AD9716/AD9717, coinciding with the first eight SCLK rising edges. In Phase 2, the instruction byte provides the serial port controller of the AD9714/AD9715/AD9716/AD9717 with information regarding the data transfer cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is a read or write, the number of bytes in the data transfer, and the starting register address for the first byte of the data transfer. The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9714/AD9715/AD9716/AD9717.

A Logic 1 on Pin 35 (RESET/PINMD), followed by a Logic 0, resets the SPI port timing to the initial state of the instruction cycle. This is true regardless of the present state of the internal registers or the other signal levels present at the inputs to the SPI port. If the SPI port is in the midst of an instruction cycle or a data transfer cycle, none of the present data is written.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9714/AD9715/AD9716/AD9717 and the system controller. Phase 2 of the communication cycle is a transfer of one, two, three, or four data bytes, as determined by the instruction byte. Using one multibyte transfer is the preferred method. Single-byte data transfers are useful to reduce CPU overhead when register access requires one byte only. Registers change immediately upon writing to the last bit of each transfer byte.

INSTRUCTION BYTE

The instruction byte contains the information shown in Table 11.

Table 11.

MSB							LSB
DB7	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
R/$\overline{W}$	N1	N0	A4	A3	A2	A1	A0

R/$\overline{W}$ (Bit 7 of the instruction byte) determines whether a read or a write data transfer occurs after the instruction byte write. Logic 1 indicates a read operation. Logic 0 indicates a write operation. N1 and N0 (Bit 6 and Bit 5 of the instruction byte) determine the number of bytes to be transferred during the data transfer cycle. The bit decodes are shown in Table 12.

Table 12. Byte Transfer Count

N1	N0	Description
0	0	Transfer 1 byte
0	1	Transfer 2 bytes
1	0	Transfer 3 bytes
1	1	Transfer 4 bytes

A4, A3, A2, A1, and A0 (Bit 4, Bit 3, Bit 2, Bit 1, and Bit 0 of the instruction byte) determine which register is accessed during the data transfer portion of the communications cycle. For multibyte transfers, this address is the starting byte address. The following register addresses are generated internally by the AD9714/AD9715/AD9716/AD9717, based on the LSBFIRST bit (Register 0x00, Bit 6).

SERIAL INTERFACE PORT PIN DESCRIPTIONS

SCLK—Serial Clock

The serial clock pin is used to synchronize data to and from the AD9714/AD9715/AD9716/AD9717 and to run the internal state machines. The SCLK maximum frequency is 20 MHz. All data input to the AD9714/AD9715/AD9716/AD9717 is registered on the rising edge of SCLK. All data is driven out of the AD9714/AD9715/AD9716/AD9717 on the falling edge of SCLK.

$\overline{CS}$—Chip Select

An active low input starts and gates a communications cycle. It allows more than one device to be used on the same serial communications lines. The SDIO/FORMAT pin reaches a high impedance state when this input is high. Chip select should stay low during the entire communications cycle.

SDIO—Serial Data I/O

The SDIO pin is used as a bidirectional data line to transmit and receive data.

MSB/LSB TRANSFERS

The serial port of the AD9714/AD9715/AD9716/AD9717 can support both most significant bit (MSB) first or least significant bit (LSB) first data formats. This functionality is controlled by the LSBFIRST bit (Register 0x00, Bit 6). The default is MSB first (LSBFIRST = 0).

When LSBFIRST = 0 (MSB first), the instruction and data bytes must be written from the most significant bit to the least significant bit. Multibyte data transfers in MSB first format start with an instruction byte that includes the register address of the most significant data byte. Subsequent data bytes should follow in order from a high address to a low address. In MSB first mode, the serial port internal byte address generator decrements for each data byte of the multibyte communications cycle.

When LSBFIRST = 1 (LSB first), the instruction and data bytes must be written from the least significant bit to the most significant bit. Multibyte data transfers in LSB first format start with an instruction byte that includes the register address of the least significant data byte followed by multiple data bytes. The serial port internal byte address generator increments for each byte of the multibyte communication cycle.

The serial port controller data address of the AD9714/AD9715/AD9716/AD9717 decrements from the data address written toward 0x00 for multibyte I/O operations if the MSB first mode is active. The serial port controller address increments from the data address written toward 0x1F for multibyte I/O operations if the LSB first mode is active.

SERIAL PORT OPERATION

The serial port configuration of the AD9714/AD9715/AD9716/AD9717 is controlled by Register 0x00. It is important to note that the configuration changes immediately upon writing to the last bit of the register. For multibyte transfers, writing to this register can occur during the middle of the communications cycle. Care must be taken to compensate for this new configuration for the remaining bytes of the current communications cycle.

The same considerations apply to setting the software reset bit (Register 0x00, Bit 5). All registers are set to their default values except Register 0x00, which remains unchanged.

Use of single-byte transfers or initiating a software reset is recommended when changing serial port configurations to prevent unexpected device behavior.

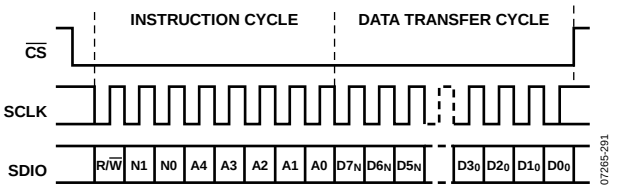


Figure 85. Serial Register Interface Timing, MSB First Write

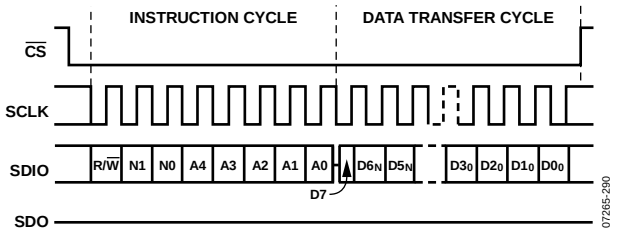


Figure 86. Serial Register Interface Timing, MSB First Read

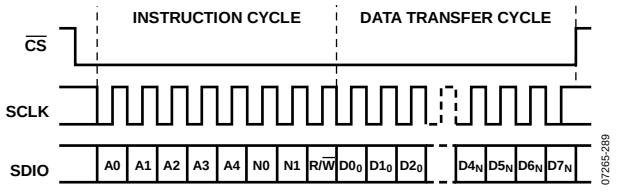


Figure 87. Serial Register Interface Timing, LSB First Write

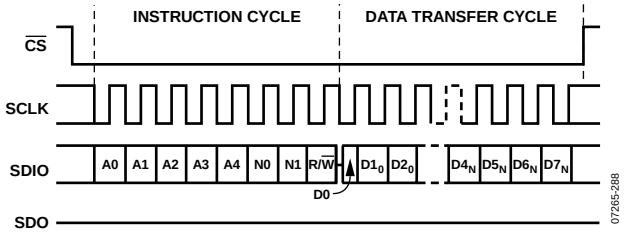


Figure 88. Serial Register Interface Timing, LSB First Read

PIN MODE

The AD9714/AD9715/AD9716/AD9717 can also be operated without ever writing to the serial port. With the RESET/PINMD pin tied high, the SCLK pin becomes CLKMD to provide for clock mode control (see the Retimer section), the SDIO pin becomes FORMAT and selects the input data format, and the $\overline{CS}$/PWRDN pin serves to power down the device.

Operation is otherwise exactly as defined by the default register values in Table 13; therefore, external resistors at FSADJI and FSADJQ are needed to set the DAC currents, and both DACs are active. This is also a convenient quick checkout mode.

DAC currents can be externally adjusted in pin mode by sourcing or sinking currents at the FSADJI/AUXI and FSADJQ/AUXQ pins as desired with the fixed resistors installed. An op amp output with appropriate series resistance is one of many possibilities. This has the same effect as changing the resistor value. Place at least 10 kΩ resistors in series right at the DAC to guard against accidental short circuits and noise modulation. The REFIO pin can be adjusted ±25% in a similar manner, if desired.

SPI REGISTER MAP

Table 13.

Name	Addr	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPI Control	0x00	0x00	Reserved	LSBFIRST	Reset	LNGINS				
Power-Down	0x01	0x40	LDOOFF	LDOSTAT	PWRDN	Q DACOFF	I DACOFF	QCLKOFF	ICLKOFF	EXTREF
Data Control	0x02	0x34	TWOS	Reserved	IFIRST	IRISING	SIMULBIT	DCI_EN	DCOSGL	DCODBL
I DAC Gain	0x03	0x00	Reserved		I DACGAIN[5:0]					
IRSET	0x04	0x00	IRSETEN	Reserved	IRSET[5:0]					
IRCML	0x05	0x00	IRCMLEN	Reserved	IRCML[5:0]					
Q DAC Gain	0x06	0x00	Reserved		Q DACGAIN[5:0]					
QRSET	0x07	0x00	QRSETEN	Reserved	QRSET[5:0]					
QRCML	0x08	0x00	QRCMLEN	Reserved	QRCML[5:0]					
AUXDAC Q	0x09	0x00	QAUXDAC[7:0]							
AUX CTLQ	0x0A	0x00	QAUXEN	QAUXRNG[1:0]		QAUXOFS[2:0]			QAUXDAC[9:8]	
AUXDAC I	0x0B	0x00	IAUXDAC[7:0]							
AUX CTLI	0x0C	0x00	IAUXEN	IAUXRNG[1:0]		IAUXOFS[2:0]			IAUXDAC[9:8]	
Reference Resistor	0x0D	0x00	Reserved		RREF[5:0]					
Cal Control	0x0E	0x00	PRELDQ	PRELDI	CALSELQ	CALSELI	CALCLK	DIVSEL[2:0]		
Cal Memory	0x0F	0x00	CALSTATQ	CALSTATI			CALMEMQ[1:0]		CALMEMI[1:0]	
Memory Address	0x10	0x00	Reserved		MEMADDR[5:0]					
Memory Data	0x11	0x34	Reserved		MEMDATA[5:0]					
Memory R/W	0x12	0x00	CALRSTQ	CALRSTI		CALEN	SMEMWR	SMEMRD	UNCALQ	UNCALI
CLKMODE	0x14	0x00	CLKMODEQ[1:0]			Searching	Reacquire	CLKMODEN	CLKMODEI[1:0]	
Version	0x1F	0x03	Version[7:0]							

SPI REGISTER DESCRIPTIONS

Reading these registers returns previously written values for all defined register bits, unless otherwise noted.

Table 14.

Register	Address	Bit	Name	Description
SPI Control	0x00	6	LSBFIRST	0 (default): MSB first, per SPI standard. 1: LSB first, per SPI standard. Note that the user must always change the LSB/MSB order in single-byte instructions to avoid erratic behavior due to bit order errors.
		5	Reset	Execute software reset of SPI and controllers, reload default register values except Register 0x00. 1: sets software reset; write 0 on the next (or any following) cycle to release reset.
		4	LNGINS	0 (default): the SPI instruction word uses a 5-bit address. 1: the SPI instruction word uses a 13-bit address.
Power-Down	0x01	7	LDOOFF	0 (default): LDO voltage regulator on. 1: turns core LDO voltage regulator off.
		6	LDOSTAT	0: indicates that the core LDO voltage regulator is off. 1 (default) : indicates that the core LDO voltage regulator is on.
		5	PWRDN	0 (default): all analog and digital circuitry and SPI logic are powered on. 1: powers down all analog and digital circuitry except for SPI logic.
		4	Q DACOFF	0 (default): turns on Q DAC output current. 1: turns off Q DAC output current.
		3	I DACOFF	0 (default): turns on I DAC output current. 1: turns off I DAC output current.
		2	QCLKOFF	0 (default): turns on Q DAC clock. 1: turns off Q DAC clock.
		1	ICLKOFF	0 (default): turns on I DAC clock. 1: turns off I DAC clock.
		0	EXTREF	0 (default): turns on internal voltage reference. 1: powers down internal voltage reference (external reference required).
Data Control	0x02	7	TWOS	0 (default): unsigned binary input data format. 1: twos complement input data format.
		5	IFIRST	0: pairing of data—Q first of pair on data input pads. 1 (default): pairing of data—I first of pair on data input pads.
		4	IRISING	0: Q data latched on DCLKIO rising edge. 1 (default): I data latched on DCLKIO rising edge.
		3	SIMULBIT	0 (default): allows simultaneous input and output enable on DCLKIO. 1: disallows simultaneous input and output enable on DCLKIO.
		2	DCI_EN	Controls the use of the DCLKIO pad for data clock input. 0: data clock input disabled. 1 (default): data clock input enabled.
		1	DCOSGL	Controls the use of the DCLKIO pad for data clock output. 0 (default): data clock output disabled. 1: data clock output enabled; regular strength driver.
		0	DCODBL	Controls the use of the DCLKIO pad for data clock output. 0 (default): DCODBL data clock output disabled. 1: DCODBL data clock output enabled; paralleled with DCOSGL for 2× drive current.
I DAC Gain	0x03	5:0	I DACGAIN[5:0]	DAC I fine gain adjustment; alters the full-scale current as shown in Figure 100. Default IDACGAIN = 0x00.

Register	Address	Bit	Name	Description
IRSET	0x04	7	IRSETEN	0 (default): IR_{SET} resistor value for I channel is set by an external resistor connected to the FADJI/AUXI pin. Nominal value for this external resistor is 16 kΩ.
				1: enables the on-chip IR_{SET} value to be changed for I channel.
		5:0	IRSET[5:0]	Changes the value of the on-chip IR_{SET} resistor for I channel; this scales the full-scale current of the DAC in ~0.25 dB steps twos complement (nonlinear); see Figure 99.
				000000 (default): IR_{SET} = 16 kΩ.
				011111: IR_{SET} = 32 kΩ.
				100000: IR_{SET} = 8 kΩ.
				111111: IR_{SET} = 16 kΩ.
IRCML	0x05	7	IRCMLEN	0 (default): IR_{CML} resistor value for the I channel is set by an external resistor connected to the CMLI pin. Recommended value for this external resistor is 0 Ω.
				1: enables on-chip IR_{CML} adjustment for I channel.
		5:0	IRCML[5:0]	Changes the value of the on-chip IR_{CML} resistor for I channel; this adjusts the common-mode level of the DAC output stage.
				000000 (default): IR_{CML} = 250 Ω.
				100000: IR_{CML}= 625 Ω.
				111111: IR_{CML} = 1 kΩ.
Q DAC Gain	0x06	5:0	Q DACGAIN[5:0]	DAC Q fine gain adjustment; alters the full-scale current as shown in Figure 100. Default QDACGAIN = 0x00.
QRSET	0x07	7	QRSETEN	0 (default): QR_{SET} resistor value for Q channel is set by an external resistor connected to the FADJQ/AUXQ pin. Recommended value for this external resistor is 16 kΩ.
				1: enables on-chip QR_{SET} adjustment for Q channel.
		5:0	QRSET[5:0]	Changes the value of the on-chip QR_{SET} resistor for Q channel; this scales the full-scale current of the DAC in ~0.25 dB steps twos complement (nonlinear); see Figure 99.
				000000 (default): QR_{SET} = 16 kΩ.
				011111: QR_{SET} = 32 kΩ.
				100000: QR_{SET} = 8 kΩ.
				111111: QR_{SET} = 16 kΩ.
QRCML	0x08	7	QRCMLEN	0 (default): QR_{CML} resistor value for the Q channel is set by an external resistor connected to CMLQ pin. Recommended value for this external resistor is 0 Ω.
				1: enables on-chip QR_{CML} adjustment for Q channel.
		5:0	QRCML[5:0]	Changes the value of the on-chip QR_{CML} resistor for Q channel; this adjusts the common-mode level of the DAC output stage.
				000000 (default): QR_{CML} = 250 Ω.
				100000: QR_{CML} = 625 Ω.
				111111: QR_{CML} = 1 kΩ.
AUXDAC Q	0x09	7:0	QAUXDAC[7:0]	AUXDAC Q output voltage adjustment word LSBs.
				0x3FF: sets AUXDAC Q output to full scale.
				0x200: sets AUXDAC Q output to midscale.
				0x000 (default): sets AUXDAC Q output to bottom of scale.
AUX CTLQ	0x0A	7	QAUXEN	0 (default): AUXDAC Q output disabled.
				1: enables AUXDAC Q output.
		6:5	QAUXRNG[1:0]	00 (default): sets AUXDAC Q output voltage range to 2 V.
				01: sets AUXDAC Q output voltage range to 1.5 V.
				10: sets AUXDAC Q output voltage range to 1.0 V.
				11: sets AUXDAC Q output voltage range to 0.5 V.
		4:2	QAUXOFS[2:0]	000 (default): sets AUXDAC Q top of range to 1.0 V.
				001: sets AUXDAC Q top of range to 1.5 V.
				010: sets AUXDAC Q top of range to 2.0 V.
				011: sets AUXDAC Q top of range to 2.5 V.
				100: sets AUXDAC Q top of range to 2.9 V.
		1:0	QAUXDAC[9:8]	AUXDAC Q output voltage adjustment word MSBs (default = 00).

Register	Address	Bit	Name	Description
AUXDAC I	0x0B	7:0	IAUXDAC[7:0]	AUXDAC I output voltage adjustment word LSBs. 0x3FF: sets AUXDAC I output to full scale. 0x200: sets AUXDAC I output to midscale. 0x000 (default): sets AUXDAC I output to bottom of scale.
AUX CTLI	0x0C	7	IAUXEN	0 (default): AUXDAC I output disabled. 1: enables AUXDAC I output.
		6:5	IAUXRNG[1:0]	00 (default): sets AUXDAC I output voltage range to 2 V. 01: sets AUXDAC I output voltage range to 1.5 V. 10: sets AUXDAC I output voltage range to 1.0 V. 11: sets AUXDAC I output voltage range to 0.5 V.
		4:2	IAUXOFS[2:0]	000 (default): sets AUXDAC I top of range to 1.0 V. 001: sets AUXDAC I top of range to 1.5 V. 010: sets AUXDAC I top of range to 2.0 V. 011: sets AUXDAC I top of range to 2.5 V. 100: sets AUXDAC I top of range to 2.9 V.
		1:0	IAUXDAC[9:8]	AUXDAC I output voltage adjustment word MSBs (default = 00).
Reference Resistor	0x0D	5:0	RREF[5:0]	Permits an adjustment of the on-chip reference voltage and output at REFIO (see Figure 98) twos complement. 000000 (default): sets the value of R_{REF} to 10 kΩ, V_{REF} = 1.0 V. 011111: sets the value of R_{REF} to 12 kΩ, V_{REF} = 1.2 V. 100000: sets the value of R_{REF} to 8 kΩ, V_{REF} = 0.8 V. 111111: sets the value of R_{REF} to 10 kΩ, V_{REF} = 1.0 V.
Cal Control	0x0E	7	PRELDQ	0 (default): preload Q DAC calibration reference set to 32. 1: preload Q DAC calibration reference set by user (Cal Address 1).
		6	PRELDI	0 (default): preload I DAC calibration reference set to 32. 1: preload I DAC calibration reference set by user (Cal Address 1).
		5	CALSELQ	0 (default): Q DAC self-calibration done. 1: select Q DAC self-calibration.
		4	CALSELI	0 (default): I DAC self-calibration done. 1: select I DAC self-calibration.
		3	CALCLK	0 (default): calibration clock disabled. 1: calibration clock enabled.
		2:0	DIVSEL[2:0]	Calibration clock divide ratio from DAC clock rate. 000 (default): divide by 256. 001: divide by 128. … 110: divide by 4. 111: divide by 2.
Cal Memory	0x0F	7	CALSTATQ	0 (default): Q DAC calibration in progress. 1: calibration of Q DAC complete.
		6	CALSTATI	0 (default): I DAC calibration in progress. 1: calibration of I DAC complete.
		3:2	CALMEMQ[1:0]	Status of Q DAC calibration memory. 00 (default): uncalibrated. 01: self-calibrated. 10: user calibrated.
		1:0	CALMEMI[1:0]	Status of I DAC calibration memory. 00 (default): uncalibrated. 01: self-calibrated. 10: user calibrated.
Memory Address	0x10	5:0	MEMADDR[5:0]	Address of static memory to be accessed.
Memory Data	0x11	5:0	MEMDATA[5:0]	Data for static memory access.

Register	Address	Bit	Name	Description
Memory R/W	0x12	7	CALRSTQ	0 (default): no action. 1: clear CALSTATQ.
		6	CALRSTI	0 (default): no action. 1: clear CALSTATI.
		4	CALEN	0 (default): no action. 1: initiate device self-calibration.
		3	SMEMWR	0 (default): no action. 1: write to static memory (calibration coefficients).
		2	SMEMRD	0 (default): no action. 1: read from static memory (calibration coefficients).
		1	UNCALQ	0 (default): no action. 1: reset Q DAC calibration coefficients to default (uncalibrated).
		0	UNCALI	0 (default): no action. 1: reset I DAC calibration coefficients to default (uncalibrated).
CLKMODE	0x14	7:6	CLKMODEQ[1:0]	Depending on the CLKMODEN bit setting, these two bits reflect the phase relationship between DCLKIO and CLKIN, as described in Table 16. If CLKMODEN = 0, read only; reports the clock phase chosen by the retimer. If CLKMODEN = 1, read/write; value in this register sets Q clock phases; force if needed to better synchronize the DACs (see the Retimer section).
		4	Searching	Data path retimer status bit. 0 (default): clock relationship established. 1: indicates that the internal data path retimer is searching for clock relationship (device output is not usable while this bit is high).
		3	Reacquire	Edge triggered, 0 to 1 causes the retimer to reacquire the clock relationship.
		2	CLKMODEN	0 (default): CLKMODEI/CLKMODEQ values computed by the two retimers and read back in CLKMODEI[1:0] and CLKMODEQ[1:0]. 1: CLKMODE values set in CLKMODEI[1:0] override both I and Q retimers.
		1:0	CLKMODEI[1:0]	Depending on CLKMODEN bit setting, these two bits reflect the phase relationship between DCLKIO and CLKIN as described in Table 16. If CLKMODEN = 0, read only; reports the clock phase chosen by the retimer. If CLKMODEN = 1, read/write; value in this register sets I clock phases; force if needed to better synchronize the DACs (see the Retimer section).
Version	0x1F	7:0	Version[7:0]	Hardware version of the device. This register is set to 0x03 for the latest version of the device.