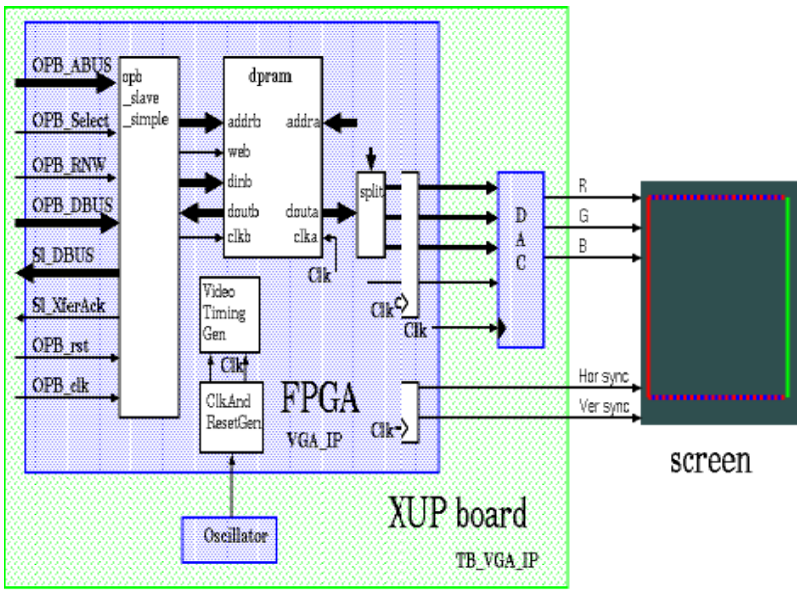
Lab-exercise

Lab6:

VGA_IP

Introduction

In this lab the student compiles a VGA_IP system driving the screen as he did in module4b. Instead of a fixed initialized dual port RAM this time the student will add an interface to the OPB bus. The result of this lab can be used in a consecutive lab as an IP block within a complete system also making use of a PowerPC and CoreConnect busses.



Objectives

- To compile a system in VHDL using existing VHDL units
- To generate a testbench

Knowledge background

Module 4b: driving a screen from a dual port RAM
Module 5a: OPB interface

Classification

Difficulty level (from 1 to 5): 3
Time needed (without support): 2.5 hours

Input

You can find the following folders/files under module6a:

Hardware

- VGA_IP.vhd : vhdl template
- ClkAndResetGen.vhd
- Constants_pack.vhd
- dpram.vhd
- opb_slave_simple.vhd
- VideoTimingGen.vhd

Simulation

- TB_VGA_IP.vhd: testbench template
- General_TB_pack.vhd
- TripleDac.vhd
- dpram.mif

The lab

1. Complete the VHDL of the whole system in Hardware/VGA_IP.vhd.
The easiest method is to copy the system3 system from module4b and complete it with the OPB interface from module5a.
2. Put the opb test procedures from module5a in a separate VHLD package to make them more widely useable.
Copy the opb_write and opb_read procedures from the testbench for opb_slave_simple in module5a and put them in a package called OPB_TB_pack in the file Simulation/OPB_TB_pack.vhd. Compile this package in library OPB_TB_lib.
3. Complete the testbench file TB_VGA_IP.vhd making use of module4b and module5a.
Add the procedures to drive the FPGA system clock and the opb_clk. Use the opb_read and write procedures to send data to and read from the dpram and use CheckPulsWidth and CheckDist to verify the VGA outputs automatically. Make sure the simulation automatically stops after 18 ms.
4. Simulate the complete system. Only the following warnings are allowed.

```
# ** Warning: NUMERIC_STD.">=": metavalue detected, returning
FALSE
# Time: 0 ps Iteration: 0 Instance: /tb_vga_ip/u1/u2
# ** Warning: NUMERIC_STD.">=": metavalue detected, returning
```

```
FALSE
# Time: 0 ps Iteration: 0 Instance: /tb_vga_ip/u1/u2
# ** Warning: NUMERIC_STD."=": metavalue detected, returning
FALSE
# Time: 0 ps Iteration: 0 Instance: /tb_vga_ip/u1/u2
# ** Warning: NUMERIC_STD."<": metavalue detected, returning
FALSE
# Time: 0 ps Iteration: 0 Instance: /tb_vga_ip/u1/u2
# ** Warning: NUMERIC_STD."<": metavalue detected, returning
FALSE
# Time: 0 ps Iteration: 0 Instance: /tb_vga_ip/u1/u2
# ** Warning: NUMERIC_STD.TO_INTEGER: metavalue detected,
returning 0
# Time: 135 ns Iteration: 5 Instance: /tb_vga_ip/u2
# ** Warning: NUMERIC_STD.TO_INTEGER: metavalue detected,
returning 0
# Time: 135 ns Iteration: 5 Instance: /tb_vga_ip/u2
# ** Warning: NUMERIC_STD.TO_INTEGER: metavalue detected,
returning 0
# Time: 135 ns Iteration: 5 Instance: /tb_vga_ip/u2
```