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CS465

HW3

Part 1

1.

a.

Unsigned integer,

0xAD490020 = 10101101010010010000000000100000

Decimal value is 2907242528

b.

Signed integer, flip the binary number above and add 1

Decimal value is -1387724768

c.

This is sw instruction, in particular it looks like:

1011 11, 5 bits, 5 bits, 16 bits

rs rt immediate

1010 1101 0100 1001 0000 0000 0010 0000

AD490020 => sw $t1, 32($t2)

2.

a. This instruction will need to use instruction memory, register file to read register Rd and Rs, then use ALU to add Rd and Rs, access data memory to load value at address Rd + Rs, and then write the value to register Rt.

b. No, all the blocks mentioned above already exist.

c. This instruction only requires changes in the Control unit, so no new signals are needed.

3.

a.

Because only I-Mem and Add are used in a fetch instruction, the clock cycle time will be equal to the longest latency in these two steps. I-Mem has longer latency of 200ps, so clock cycle time 200ps.

b.

The datapath of this instruction include the use of instruction memory, sign-extended and shift-left-2 to get the offset, Add unit to compute the new PC. Then use Mux to select the new value instead of PC + 4. Clock cycle time is 200 + 15 + 10 + 70 + 20 = 315ps

c.

The datapath of this instruction include the use of instruction memory, Registers, Mux, ALU, then Mux again. Clock cycle time is 200 + 90 + 20 + 90 +20 = 420ps

d.

PC-relative branches.

e.

PC-relative unconditional branch instructions. Shift-left-2 is not on the datapath of conditional branches, Also, it is only needed for PC-relative branches.

f.

Of the two instructions BNE and ADD, BNE has a longer critical path so it determines the clock cycle time. Note that every path for ADD is shorter than or equal to the corresponding path for BNE, so changes in unit latency will not affect this. As a result, we focus on how the unit's latency affects the critical path of BNE. This unit is not on the critical path, so the only way for this to become critical is to increase its latency until the path for address computation through sign-extended, shift-left, and branch add becomes longer than the path for PCSrc through registers, Mux, and ALU. The latency of Regs, Mux, and ALU is 200 ps and the latency of sign-extended, shift-left-2, and Add is 95ps, so the latency of shift-left-2 must be increased by 105 ps or more for it to affect clock cycle time.

4.

a.

Sign-extended: 00000000000000000000000000010100

Jump shift-left-2: 00011000100000000000000001010000

b.

ALUOp[1-0] = 00

Instruction[5-0] = 010100

c.

New PC = PC + 4

Datapath is PC to Add (PC + 4) to branch Mux to Jump Mux to PC

d.

WrReg Mux: 2 or 0 (RegDst is X)

ALU Mux : 20

Mem/ALU Mux: X

Branch Mux: PC + 4

Jump Mux: PC + 4

e.

ALU: -3 and 20

Add(PC + 4) : PC and 4

Add(Branch): PC + 4 and 20 * 4

f.

Read Register 1

Read Register 2

Write Register

Write Data

RegWrite