Part2:

Q1:

Address	Binary Pattern	Index	Tag	Hit/Miss	Replacement?
0x018	0000 0001 1000	3	0	Miss	No
0x218	0010 0001 1000	3	8	Miss	Yes
0x2FC	0010 1111 1100	7	11	Miss	No
0x218	0010 0001 1000	3	8	Hit	No
0x018	0000 0001 1000	3	0	Miss	Yes
0x246	0010 0100 0110	0	9	Miss	No
0x180	0001 1000 0000	0	6	Miss	Yes
0x241	0010 0100 0001	0	9	Miss	Yes
0x247	0010 0100 0111	0	9	Hit	No
0x219	0010 0001 1001	3	8	Miss	Yes

Q2:

Address	Binary Pattern	Tag	Hit/Miss	Replacement?	LRU order
0x018	0000 0001 1000	6	Miss	No	6
0x218	0010 0001	134	Miss	No	134,6

	1000				
0x2FC	0010 1111 1100	191	Miss	No	191,134,6
0x218	0010 0001 1000	134	Hit	No	134,191,6
0x018	0000 0001 1000	6	Hit	No	6,134,191
0x246	0010 0100 0110	145	Miss	No	145,6,134,191
0x180	0001 1000 0000	96	Miss	No	96,145,6,134,191
0x241	0010 0100 0001	144	Miss	No	144,96,145,6,134,191
0x247	0010 0100 0111	145	Hit	No	145,144,96,6,134,191
0x219	0010 0001 1001	134	Hit	No	134,145,144,96,6,191

Q3:

a. Clock cycle time = 0.96ns
   Clock rate = 1 / 0.96 = 1.0416GHz

b. Using time units to calculate AMAT:
   Hit time = 0.96ns
   L1 miss penalty = 3.22ns
   L1 miss rate = 11%
   L1, L2 miss penalty = 80ns
   L1, L2 miss rate = 11% * 60% = 6.6%
   AMAT = Hit time + Miss penalty * Miss rate
   = 0.96 + 3.22 * 0.11 + 80 * 0.066
   = 6.5942ns

c. Assuming L1,L2 are both data caches, and we have no instruction misses.
   Base CPI = 1;
   Clock cycle time = 0.96ns
   Using cycle units:
   L1 miss penalty = 3.22/0.96 = 3.354 cycles

L1 miss rate = 11%
L1, L2 miss penalty = 80/0.96 = 83.3 cycles
L1,L2 miss rate = 11% * 60% = 6.6%
Actual CPI = 1 + 0.35*(0.11*3.354+0.066*83.3) = 3.0533

Q4:

				TLB	
Address	Virtual Page	TLB H/M	Valid	Tag	Physical Page
4669	1	TLB miss PT hit PF	1 1 1 1(last access 0)	11 7 3 1	12 4 6 13
2227	0	TLB miss PT hit	1(last access 1) 1 1 1(last access 0)	0 7 3 1	5 4 6 13
13916	3	TLB hit	1(last access 1) 1 1(last access 2) 1(last access 0)	0 7 3 1	5 4 6 13
34587	8	TLB miss PT hit PF	1(last access 1) 1(last access 3) 1(last access 2) 1(last access 0)	0 8 3 1	5 14 6 13
48870	11	TLB miss PT hit	1(last access 1) 1(last access 3) 1(last access 2) 1(last access 4)	0 8 3 11	5 14 6 12
12608	3	TLB hit	1(last access 1) 1(last access 3) 1(last access 5) 1(last access 4)	0 8 3 11	5 14 6 12
49225	12	TLB miss PT miss	1(last access 6) 1(last access 3) 1(last access 5) 1(last access 4)	12 8 3 11	15 14 6 12