Homework #4 Assignment
ECE 2166/1166 Parallel Computer Architecture
Spring Semester 2019

Due: Wednesday, March 20

Consider the cache-coherence protocols, access specs, and access patterns and cited.

Cache-coherence protocols:

1. MSI (with BusUpgr option)
2. MESI (same as #1, plus E state, but no c2c sharing) – *c2c means cache-to-cache*
3. MESI (same as #2, except change M→S downgrade on BusRd to M→I, which will enable the new reader to upgrade as I→E instead of I→S)
4. MESI (same as #2, plus c2c sharing out of M and E states on BusRd)
5. MESI (same as #2, but with maximal c2c sharing, using arbitration as needed)
6. MOESI
7. Dragon (with maximal c2c sharing but no arbitration)

Access patterns: *(to same block by three cache controllers serving their processors)*

1. r1, w1, r2, w2, r3, w3, r1, w1
2. r1, r2, w1, r3, w2, r1, w3, r2, r3

Access specs:

- 1 cycle for cases involving no bus transaction
- 40 cycles for bus transaction involving no block transfer, or just a word transfer
- 80 cycles for bus transaction involving block transfer with peer without arbitration
- 100 cycles for bus transaction involving block transfer with peer with arbitration
- 200 cycles for bus transaction involving block transfer with level below

Part I: Develop and draw the state-transition diagram for each of these 7 protocols; *Note: you may wish to use a computer drawing tool for object design & reuse*.

Part II: Develop and draw the trace table for each protocol with each access pattern; then, for each access pattern, compare the 7 protocols in terms of total cycles; *Note: you may wish to use a computer spreadsheet for table design & reuse*.

Complete assignment and submit as one file (in PDF format).