

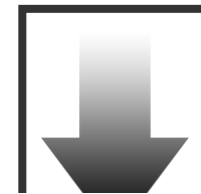
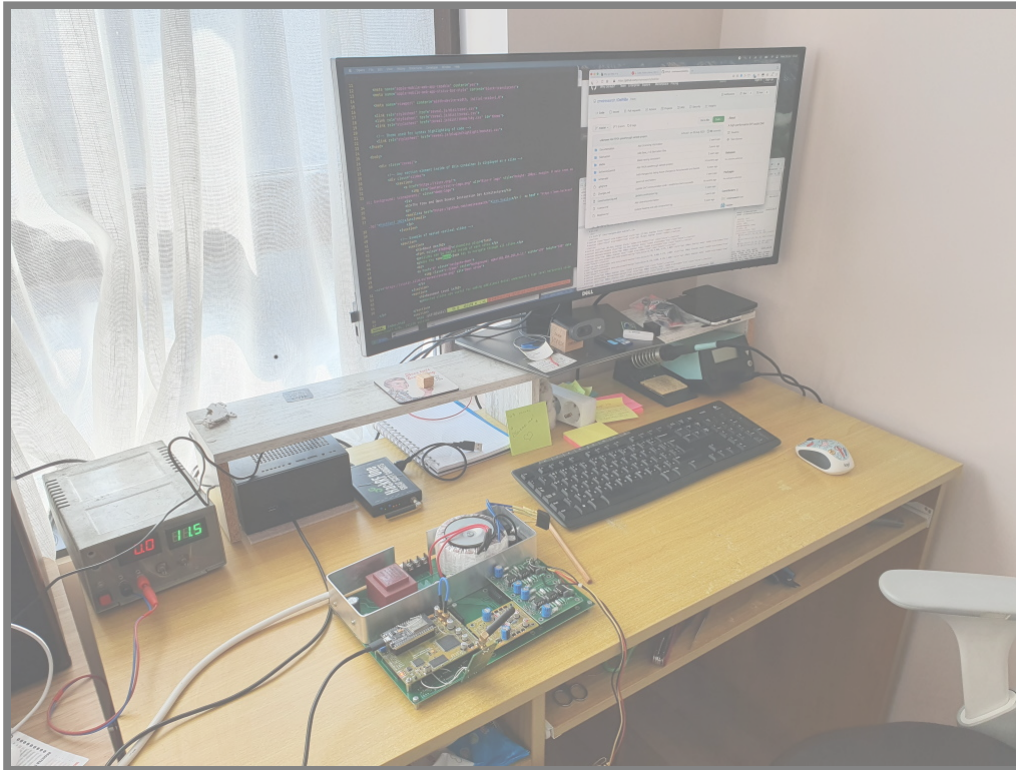


# The Free and Open Source Instruction Set Architecture

Ivan Vasilev @ HackConf 2021

# About me (shameless plug)

... and why I'm here today





# Why do I care about Risc-V?

- Excited
- Believe there is a great potential
- Interesting for others

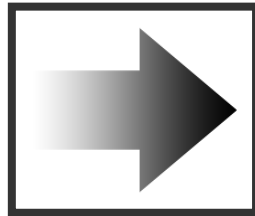
# Objective for today

## Objectives

- Get you interested
- Overview of Risc-V

## Non-Objectives

- Get you scared
- Technical details



# Definitions

# Definitions

- Processor

# Definitions

- Processor
- Microcontroller



# Definitions

- Processor
- Microcontroller
- FPGA

# Definitions

- Processor
- Microcontroller
- FPGA
- ASIC

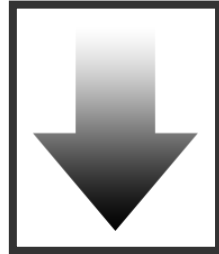
# Definitions

- Processor
- Microcontroller
- FPGA
- ASIC
- RTL

# ISA

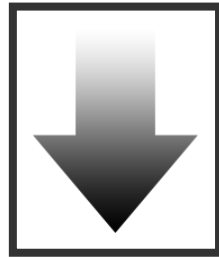
## Instruction Set Architecture

(Simplification)The physical equivalent of an API



# Popular ones

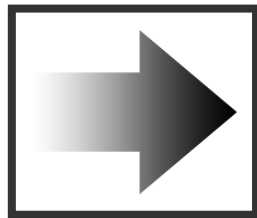
- Intel/AMD x86(64)
- ARM
- MIPS, PowerPC, m68k, etc.



RISC vs CISC

An ISA does not matter  
anymore!

(...except when it does)



# What is RISC-V

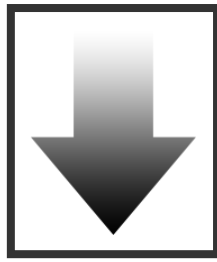
A Free and Open ISA:

*“...Driven through open collaboration*

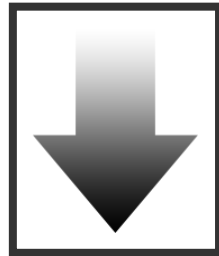
*...Enabling freedom of design across  
all domains and industries*

*...Cementing the strategic foundation  
of semiconductors”*



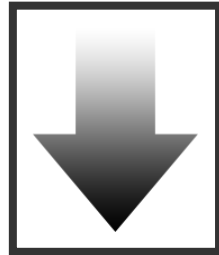


In a little bit more details:



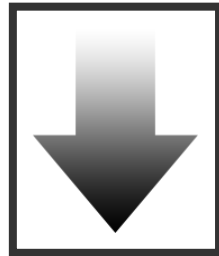
In a little bit more details:

- A set of specifications



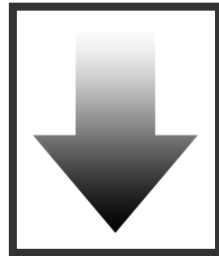
In a little bit more details:

- A set of specifications
- ... targeting 32, 64 and 128-bit processors



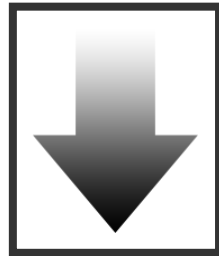
In a little bit more details:

- A set of specifications
- ... targeting 32, 64 and 128-bit processors
- ... at different performance/complexity/cost points



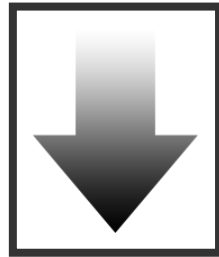
In a little bit more details:

- A set of specifications
- ... targeting 32, 64 and 128-bit processors
- ... at different performance/complexity/cost points
- ... allowing great extensibility and flexibility



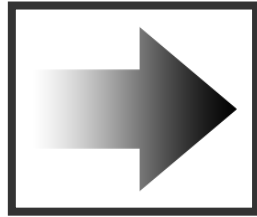
More importantly:

- A vibrant open community
- Backed by commercial vendors
- Overseen by an Non-Profit organization to ensure consistency



...but also:

A growing range of actual devices that you can buy  
and use today.





# RISC-V Implementations: RTL/FPGA

RISC-V Foundation Github lists over 100+ implementation. **Notable mentions:**

- [Western Digital SweRV](#): A set of cores used by Western Digital in their products, open-sourced
- [DarkRISCV](#): BSD-Licensed, implemented in one night, easy to understand, multicore, etc.
- [PicoSoC](#): An open licensed SoC with commercial support

# RISC-V Implementations: Devices

A number of companies offer physical devices:

- SiFive
- NXP
- Allwinner
- GreenWave
- ... and growing

# Why Open source / Open Hardware: Innovation

Allows you to build great products that are otherwise impossible, combining a CPU/MCU with custom blocks/accelerators.

# Why Open source / Open Hardware: Flexibility

Start/prototype with an FPGA, go up or down based on complexity, move to an ASIC if/when needed.

# Why Open source / Open Hardware: Future Proofing

Ability to quickly adapt to changes if needed - e.g.  
semiconductor supply crisis vs Tesla.

# Why Open source / Open Hardware: Security

Be able to inspect/audit the system down to  
transistor/gate level.

# Why Open source / Open Hardware: Learning

Designing a system from the grounds-up is the best  
way to understand it

# Why Open source / Open Hardware: Learning

Designing a system from the grounds-up is the best  
way to understand it

... have lots of fun and experimentation...



# Why Open source / Open Hardware: Learning

Designing a system from the grounds-up is the best  
way to understand it

... have lots of fun and experimentation...

... and the usual "What the..." moments as well

# Random facts:

I've used RISC-V cores in two (semi)commercial products already and love it

# Random facts:

I've used RISC-V cores in two (semi)commercial products already and love it

# Random facts:

I've used RISC-V cores in two (semi)commercial products already and love it

There are open-source projects like [SymbiFlow](#) that enable an end-to-end open toolset, when targeting FPGAs like ones from [Lattice Semiconductor](#)

# Random facts:

Manufacturing an ASIC is (maybe) not that off-the-limits.

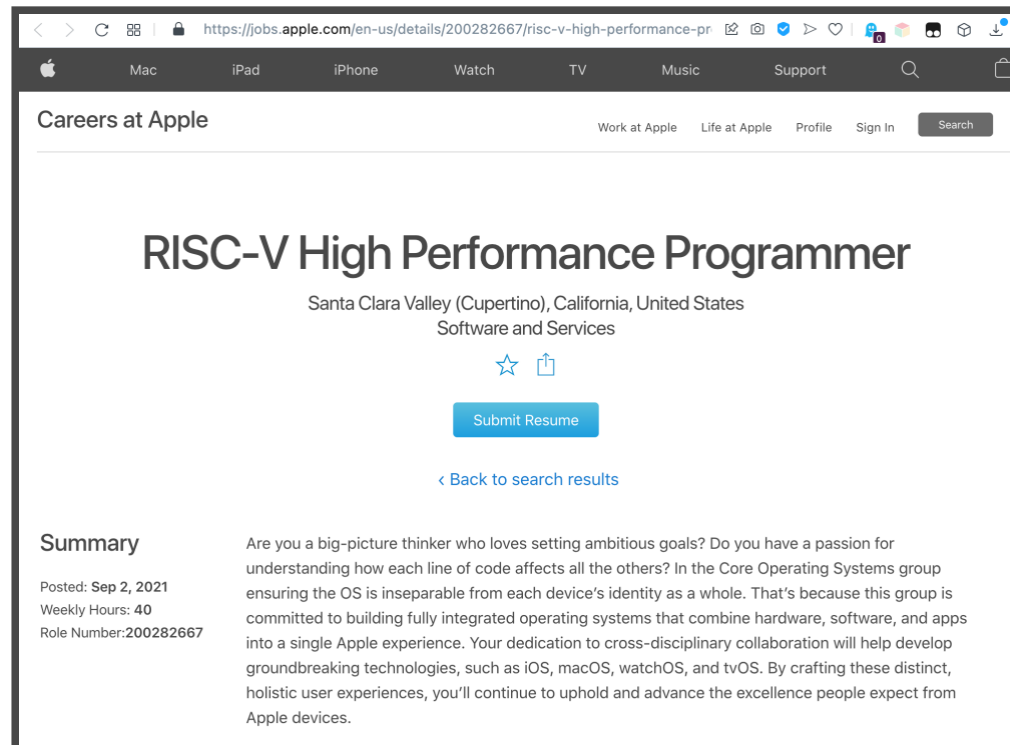
Anecdotal evidence is a design on 130nm process with ~1.5m transistors can be manufactured for less than 100k used. And moving to 180nm (Pentium III-era process) - for less than 10k USD

# Predictions:

- In 10 years, RISC-V will be the preferred platform for smart/IoT devices
- In 5 years, a hyperscaler(My bet - **Microsoft**) will create a high-performance RISC-V chip, rivaling best ones from Intel, AMD, IBM and ARM. /li>

# Predictions:

Apple has some interest too:



The screenshot shows a web browser displaying the Apple Jobs page for a "RISC-V High Performance Programmer" position. The browser's address bar shows the URL: <https://jobs.apple.com/en-us/details/200282667/risc-v-high-performance-pr>. The page features a dark navigation bar with the Apple logo and links to Mac, iPad, iPhone, Watch, TV, Music, and Support. Below the navigation bar, the "Careers at Apple" section includes links for "Work at Apple", "Life at Apple", "Profile", and "Sign In", along with a search bar. The main content area displays the job title "RISC-V High Performance Programmer" in a large, bold font, followed by the location "Santa Clara Valley (Cupertino), California, United States" and the department "Software and Services". There are icons for favoriting and sharing the job, and a blue "Submit Resume" button. A link to "Back to search results" is also present. The "Summary" section on the left provides details about the posting date (Sep 2, 2021), weekly hours (40), and role number (200282667). The main text describes the role as a big-picture thinker in the Core Operating Systems group, responsible for ensuring the OS is inseparable from each device's identity as a whole, and mentions the group's commitment to building fully integrated operating systems that combine hardware, software, and apps into a single Apple experience.

Careers at Apple

Work at Apple Life at Apple Profile Sign In Search

## RISC-V High Performance Programmer

Santa Clara Valley (Cupertino), California, United States

Software and Services

☆ ↗

Submit Resume

[Back to search results](#)

### Summary

Posted: Sep 2, 2021  
Weekly Hours: 40  
Role Number: 200282667

Are you a big-picture thinker who loves setting ambitious goals? Do you have a passion for understanding how each line of code affects all the others? In the Core Operating Systems group ensuring the OS is inseparable from each device's identity as a whole. That's because this group is committed to building fully integrated operating systems that combine hardware, software, and apps into a single Apple experience. Your dedication to cross-disciplinary collaboration will help develop groundbreaking technologies, such as iOS, macOS, watchOS, and tvOS. By crafting these distinct, holistic user experiences, you'll continue to uphold and advance the excellence people expect from Apple devices.

# Thanks!

This presentation has been created using open-source tools only and is available in full under CC BY 4.0 license @ : [HackConf2021\\_Why-Go-Risc-V-y](#)