**实验七 触发器及其应用（1）**

**一、实验数据记录**

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| **实验名称** | **实验七&八 触发器及其应用** | | | |
| **器件** |  | | | |
| 1. **实验任务（1）：测试D触发器的逻辑功能（必做）** 2. **实验任务（2）：用D触发器设计一个异步八进制计数器（必做）**  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | **1.D触发器逻辑功能测试 2.8进制计数器状态表：**   |  |  |  |  |  | | --- | --- | --- | --- | --- | | 序号 | CLK | Q2 | Q1 | Q0 | | 1 | ↑ | 0 | 0 | 0 | | 2 | ↑ | 0 | 0 | 1 | | 3 | ↑ | 0 | 1 | 0 | | 4 | ↑ | 0 | 1 | 1 | | 5 | ↑ | 1 | 0 | 0 | | 6 | ↑ | 1 | 0 | 1 | | 7 | ↑ | 1 | 1 | 0 | | 8 | ↑ | 1 | 1 | 1 |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | | CLK | D | PRN | CLRN | Q | 触发器状态 | | ↑ | 0 | 0 | 1 | 1 |  | | ↑ | 0 | 1 | 0 | 0 |  | | ↑ | 0 | 1 | 1 | 0 |  | | ↑ | 1 | 0 | 1 | 1 |  | | ↑ | 1 | 1 | 0 | 0 |  | | ↑ | 1 | 1 | 1 | 1 |  | | | **实验任务（2）异步八进制计数器设计思路：** | | **电路及波形仿真结果：（请分析结果现象）**      **在每次CP信号出现上升沿时，输出Q加1，当Q输出为7（译码为111）时，CP信号出现上升沿，Q置0。** |  1. **实验任务（3）：**用D触发器设计一个异步六进制计数器**（选做）** | | | | |
| **设计思路：**  **当Q输出6（译码为110）时，需要对计数器进行复位，使之输出0。将Q2、Q1的输出格外用一个与非门连接，用于产生复位信号。同时加入一个RS锁存器对复位信号进行锁存，防止元件中的二进制计数器复位不同步带来的影响。**  **电路图：** | | | | |
| **电路及波形仿真结果：（请分析结果现象）**    **当Q将要变为110时，输出复位信号，reset端输出0（低电平有效），计数器重置为000。** | | | | |
| **故障记录（记录实验过程中的故障现象及解决方案）** | | | | |
| **实验成绩** | |  | **指导老师签字** |  |