

2023 超大型積體電路電腦輔助設計概論

2023 Introduction to VLSI CAD

Lab 11

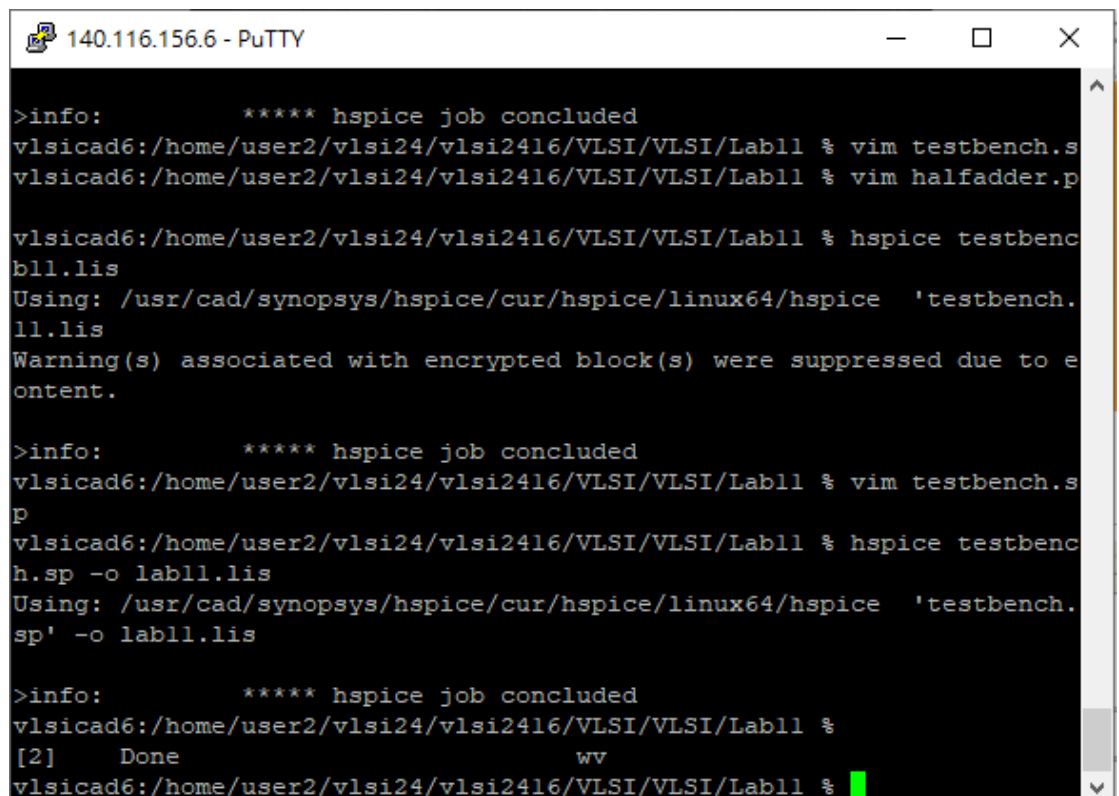
學號：E14102305

姓名：簡笠恩

※作業要求的圖請使用**電腦截圖程式**截取，請勿用手機拍照的方式繳交

※Report 檔請以 pdf 的格式繳交

- HA
 - Presim
 - 請截取 terminal 顯示 job concluded 的圖



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140.116.156.6 - PuTTY

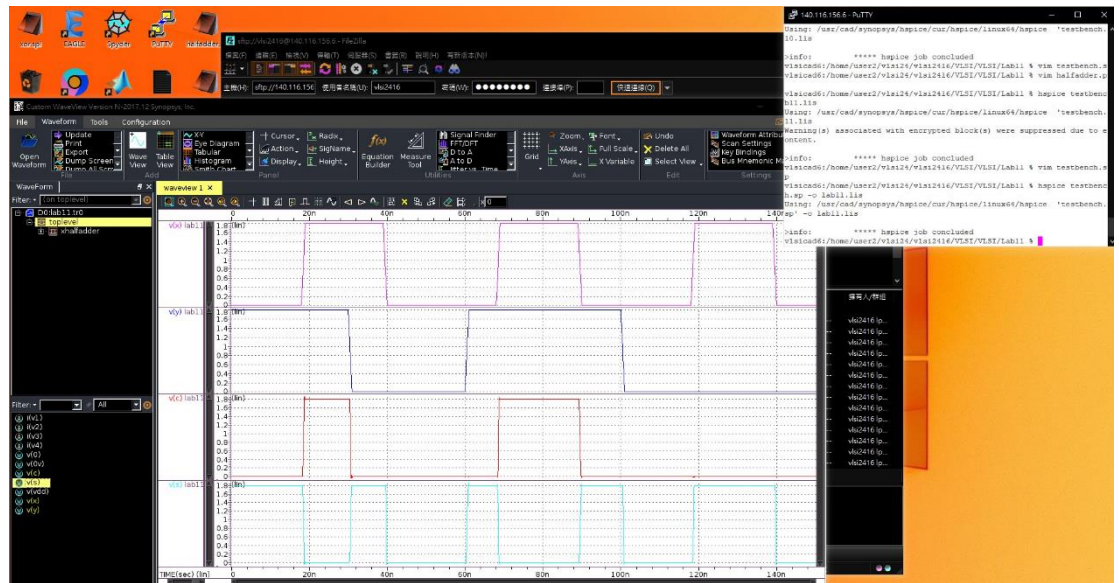
>info:          ***** hspice job concluded
vlsicad6:/home/user2/vlsi24/vlsi2416/VLSI/VLSI/Lab11 % vim testbench.s
vlsicad6:/home/user2/vlsi24/vlsi2416/VLSI/VLSI/Lab11 % vim halfadder.p

vlsicad6:/home/user2/vlsi24/vlsi2416/VLSI/VLSI/Lab11 % hspice testbenc
b11.lis
Using: /usr/cad/synopsys/hspice/cur/hspice/linux64/hspice 'testbench.
11.lis
Warning(s) associated with encrypted block(s) were suppressed due to e
ontent.

>info:          ***** hspice job concluded
vlsicad6:/home/user2/vlsi24/vlsi2416/VLSI/VLSI/Lab11 % vim testbench.s
p
vlsicad6:/home/user2/vlsi24/vlsi2416/VLSI/VLSI/Lab11 % hspice testbenc
h.sp -o lab11.lis
Using: /usr/cad/synopsys/hspice/cur/hspice/linux64/hspice 'testbench.
sp' -o lab11.lis

>info:          ***** hspice job concluded
vlsicad6:/home/user2/vlsi24/vlsi2416/VLSI/VLSI/Lab11 %
[2] Done wv
vlsicad6:/home/user2/vlsi24/vlsi2416/VLSI/VLSI/Lab11 %
```

- 請截取 WaveView 中的波形



- Post-sim
- 請截取 terminal 顯示 job concluded 的圖

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140.116.156.6 - PuTTY

>info:          ***** hspice job concluded
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vlsicad6:/home/user2/vlsi24/vlsi2416/VLSI/VLSI/Lab11 % vim halfadder.p

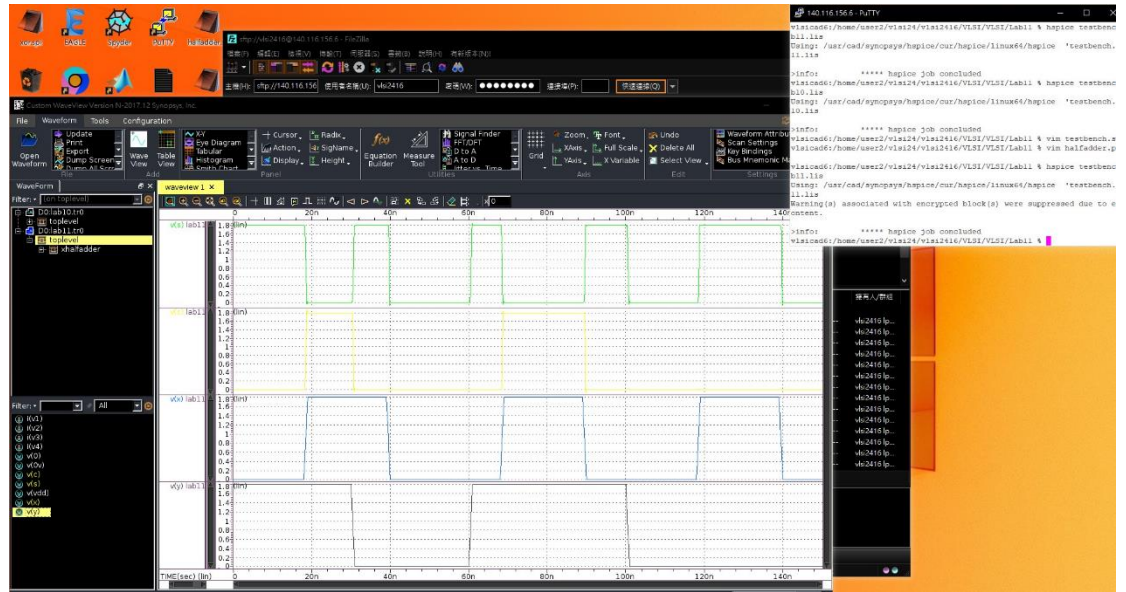
vlsicad6:/home/user2/vlsi24/vlsi2416/VLSI/VLSI/Lab11 % hspice testbenc
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Using: /usr/cad/synopsys/hspice/cur/hspice/linux64/hspice 'testbench.
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vlsicad6:/home/user2/vlsi24/vlsi2416/VLSI/VLSI/Lab11 %
[2]      Done                                wv
vlsicad6:/home/user2/vlsi24/vlsi2416/VLSI/VLSI/Lab11 %

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- 請截取 WaveView 中的波形



DRC/LVS 結果



- DFF

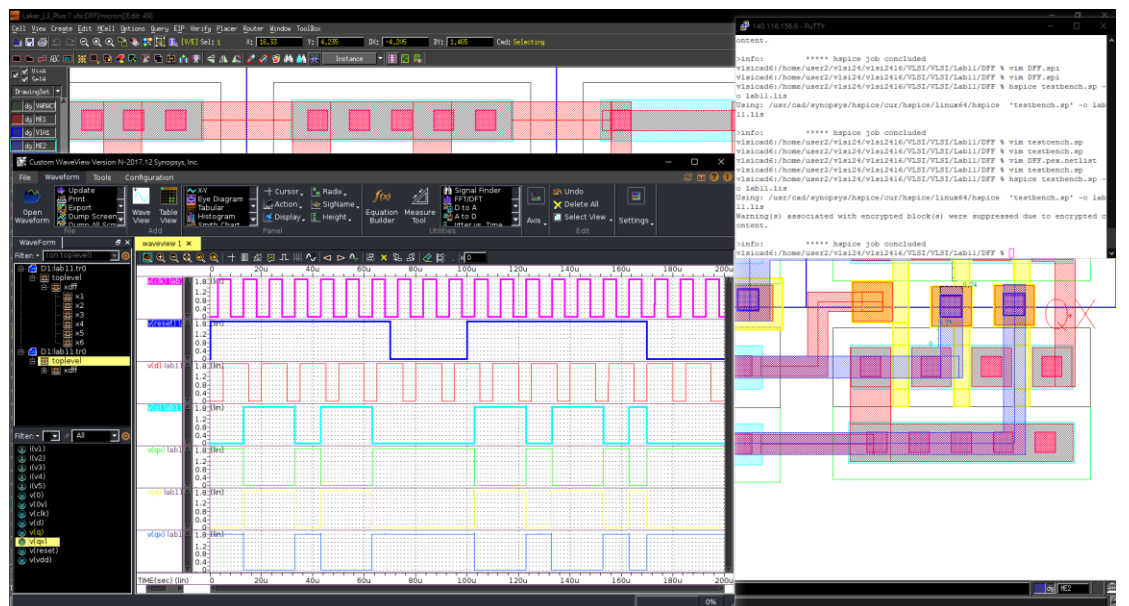
- Presim

- 請截取 terminal 顯示 job concluded 的圖

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vlsicad6:/home/user2/vlsi24/vlsi2416/VLSI/VLSI/Lab11/DFF % vim testcench.sp
vlsicad6:/home/user2/vlsi24/vlsi2416/VLSI/VLSI/Lab11/DFF % vim testbench.sp
vlsicad6:/home/user2/vlsi24/vlsi2416/VLSI/VLSI/Lab11/DFF % vim DFF.pex.netlist
vlsicad6:/home/user2/vlsi24/vlsi2416/VLSI/VLSI/Lab11/DFF % vim testbench.sp
vlsicad6:/home/user2/vlsi24/vlsi2416/VLSI/VLSI/Lab11/DFF % hspice testbench.sp -o lab11.lis
Using: /usr/cad/synopsys/hspice/cur/hspice/linux64/hspice 'testbench.sp' -o lab11.lis
Warning(s) associated with encrypted block(s) were suppressed due to encrypted content.

>info: ***** hspice job concluded
```

- 請截取 WaveView 中的波形



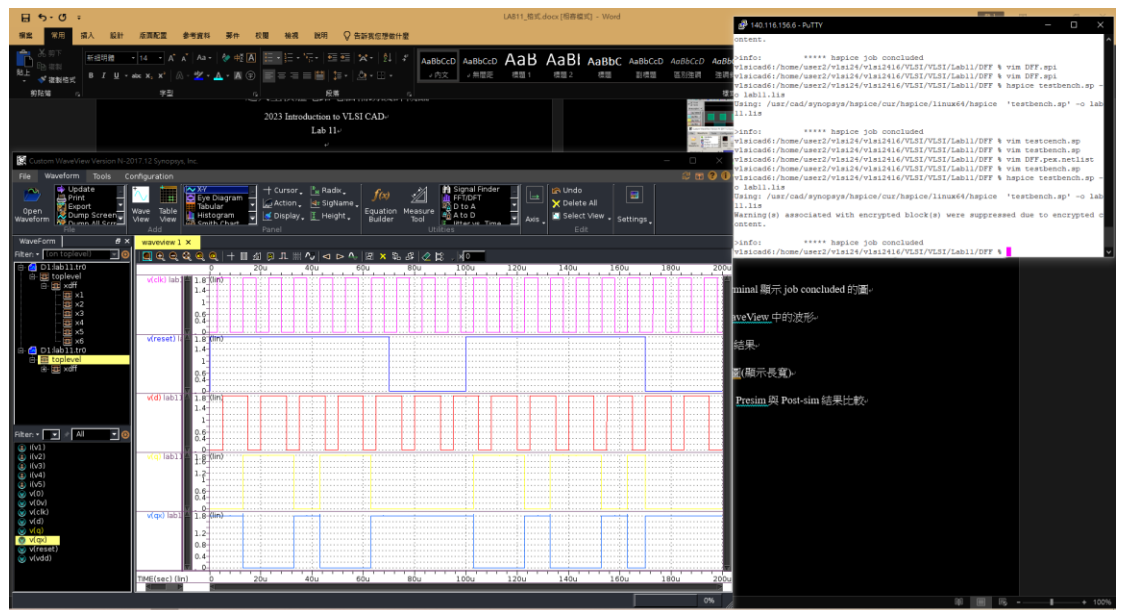
- Post-sim

- 請截取 terminal 顯示 job concluded 的圖

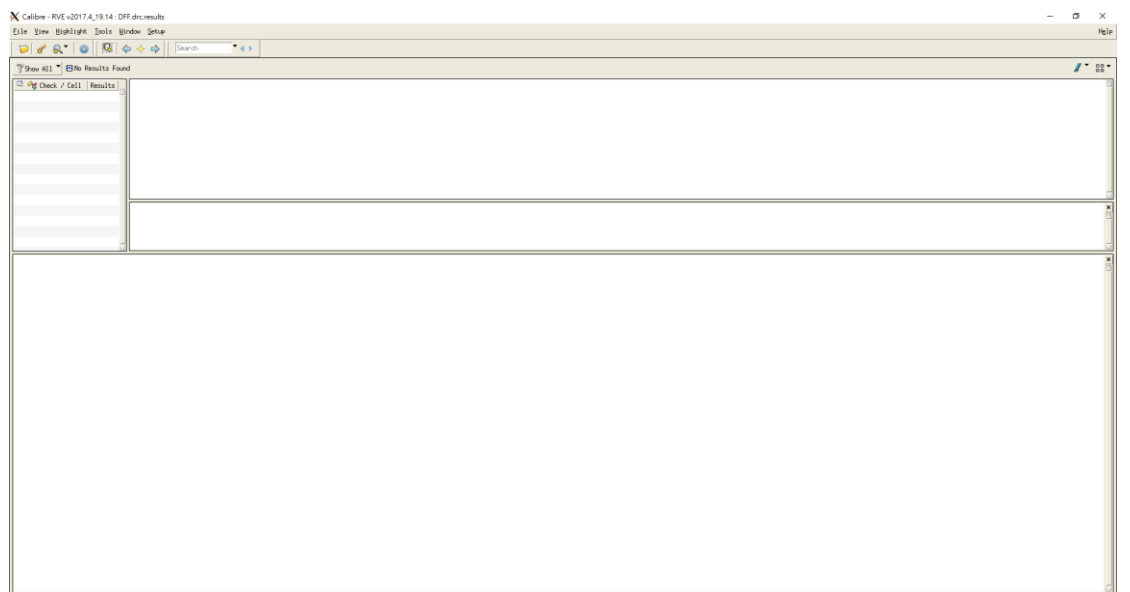

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vlsicad6:/home/user2/vlsi24/vlsi2416/VLSI/VLSI/Lab11/DFE % vim testcench.sp
vlsicad6:/home/user2/vlsi24/vlsi2416/VLSI/VLSI/Lab11/DFE % vim testbench.sp
vlsicad6:/home/user2/vlsi24/vlsi2416/VLSI/VLSI/Lab11/DFE % vim DFF.pex.netlist
vlsicad6:/home/user2/vlsi24/vlsi2416/VLSI/VLSI/Lab11/DFE % vim testbench.sp
vlsicad6:/home/user2/vlsi24/vlsi2416/VLSI/VLSI/Lab11/DFE % hspice testbench.sp -o lab11.lis
Using: /usr/cad/synopsys/hspice/cur/hspice/linux64/hspice 'testbench.sp' -o lab11.lis
Warning(s) associated with encrypted block(s) were suppressed due to encrypted content.

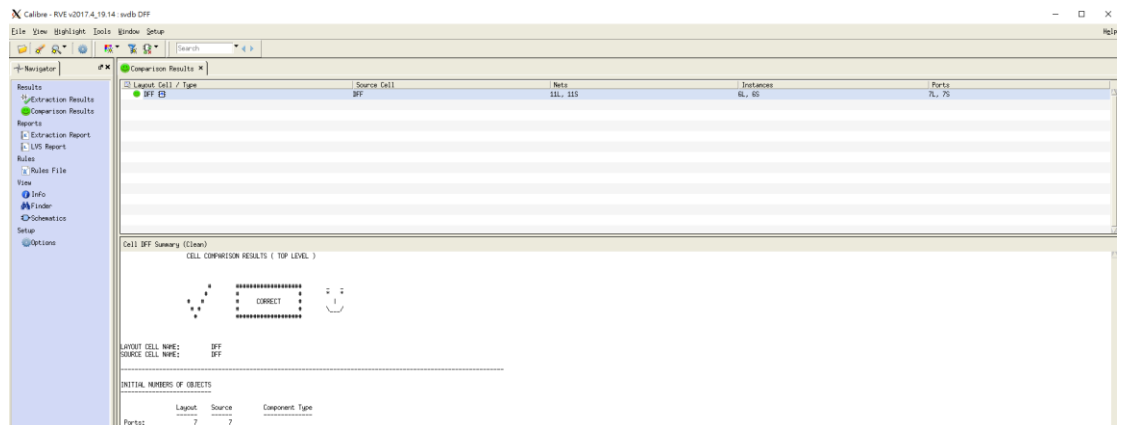
>info: ***** hspice job concluded
```

- 請截取 WaveView 中的波形

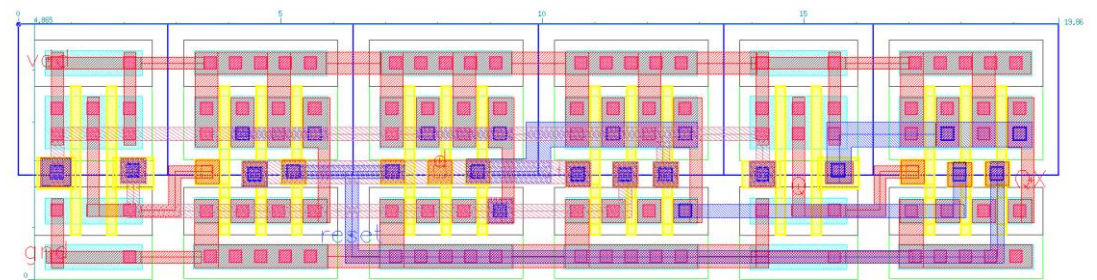


- DRC/LVS 結果





- Layout 截圖(顯示長寬)



AREA:96.619

- 嘗試簡單說明 Presim 與 Post-sim 結果比較
- Presim 和 possim 基本上會一樣，會差的只可能會是延遲或電壓，主要看自己的 layout 如何規劃!
- 心得討論
- 這次我們實作了 halfadder 和 DFF 真的是一個特別的經驗，因為我們數位的最後兩個 lab 有用到 ram 裡面就有運用到 DFF，可以說更了解 DFF 的內部，在經過我的努力完成了這次 lab，水水水!