National Cheng Kung University

Department of Electrical Engineering

Introduction to VLSI CAD (Spring 2024)

Lab Session 3

Design of ALU and Multiplication Using Verilog Coding

Name	Student ID	
簡笠恩	E14102305	
Practical Sections:	Points	Marks
Prob A	30	
Prob B	30	
Prob C	20	
Report	15	
File hierarchy, naming…etc.	5	
Notes		

Due Date: 15:00, March 13, 2024 @ moodle

Deliverables

1) All Verilog codes including testbenches for each problem should be uploaded.
   NOTE: Please **DO NOT** include source code in the paper report!
2) All homework requirements should be uploaded in this file hierarchy or you will not get the full credit.
   NOTE: Please **DO NOT** upload waveforms!
3) Important! TA will use the command in Appendix A to check your design under SoC Lab environment, if your code can not be recompiled by TA successfully using the commands, you will not get the full credit.
4) If you upload a dead body which we can't even compile you will get **NO** credit!
5) All Verilog file should get at least 90% superLint Coverage.
6) File hierarchy should not be changed; it may cause your code can not be recompiled by TA successfully using the autograding commands

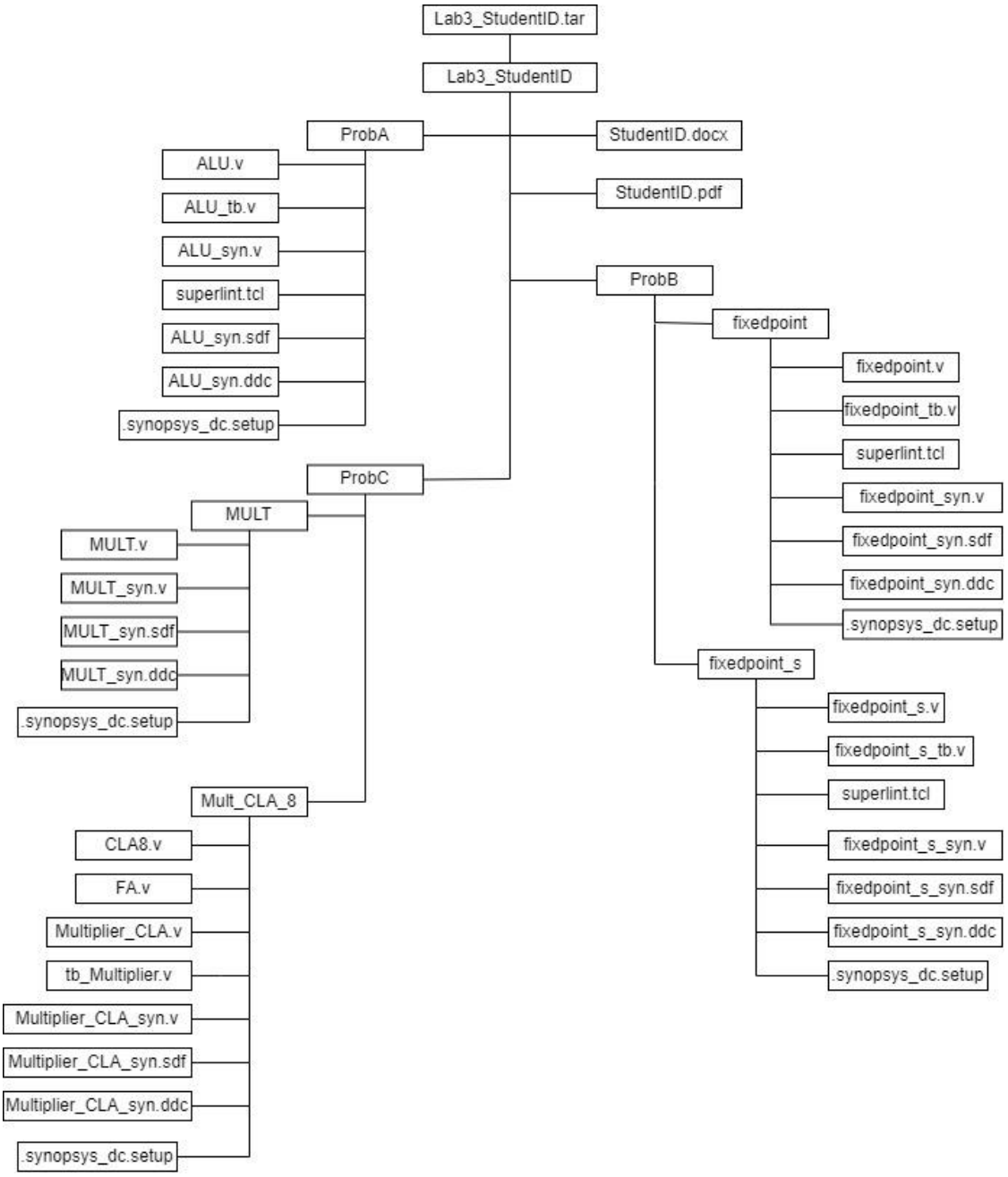
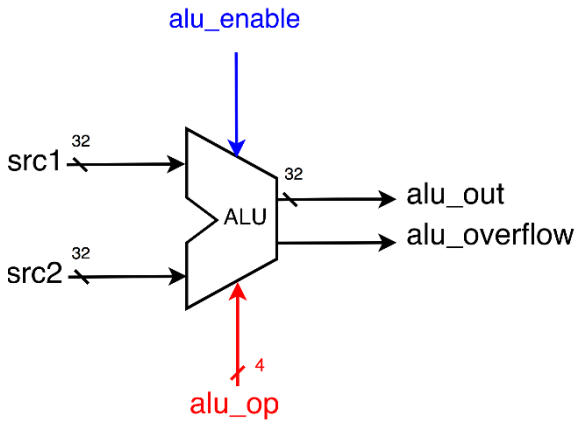


Fig.1 File hierarchy for Homework submission

Prob A: Arithmetic Logic Unit

Design your Verilog code with the following specifications:



1. Based on the reference code, please implement the following operations.

alu_op	Operation	Description
00000	ADD	$src1_{signed}$ + $src2_{signed}$
00001	SUB	$src1_{signed}$ - $src2_{signed}$
00010	OR	src1 or src2
00011	AND	src1 and src2
00100	XOR	src1 xor src2
00101	NOT	Invertion of src1
00110	NAND	src1 nand src2
00111	NOR	src1 nor src2

alu_op	Operation	Description
01011	SLT	alu_out = (src1 signed < src2 signed) ? 32'd1 : 32'd0
01100	SLTU	alu_out = (src1 unsigned < src2 unsigned) ? 32'd1 : 32'd0
01101	SRA	alu_out = src1 signed >>> src2 unsigned
01110	SLA	alu_out = src1 signed <<< src2 unsigned
01111	SRL	alu_out = src1 unsigned >> src2 unsigned
10000	SLL	alu_out = src1 unsigned << src2 unsigned
10001	ROTR	alu_out = src1 rotate right by "src2 bits"
10010	ROTL	alu_out = src1 rotate left by "src2 bits"
10011	MUL	alu_out = lower 32 bits of (src1 * src2)
10100	MULH	alu_out = upper 32 bits of (src1 signed * src2 signed)
10101	MULHSU	alu_out = upper 32 bits of (src1 signed * src2 unsigned)
10110	MULHU	alu_out = upper 32 bits of (src1 unsigned * src2 unsigned)

a. The frame code and testbench are given. Follow the frame code to finish this homework. The decimal part should be rounded.
b. Follow the PPT file to synthesize your code.

After you synthesize your design, you may have some information about the circuit. Fill in the following form.

Timing (slack)	Area (total cell area)	Power (total)
18.04	**4127.967**	**4.2602(mW)**

Please attach your design waveforms.

Your simulation result on the terminal.

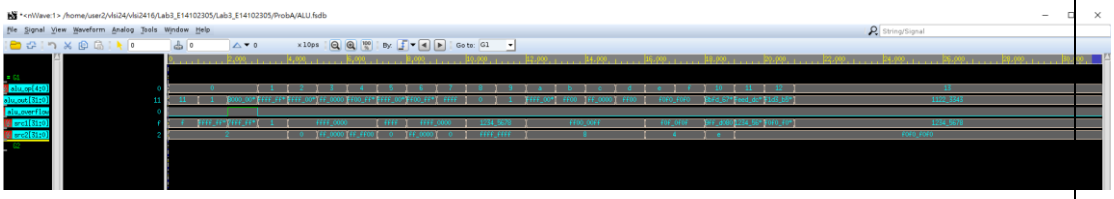
RTL

SYN

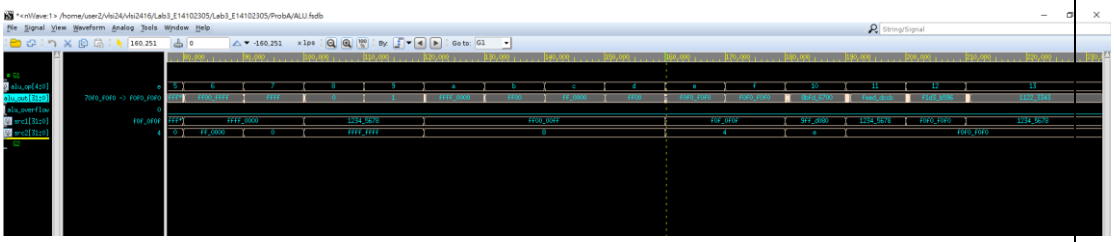
```
223343, alu_overflow = 0



        ****************************
        **                        **       |\__||
        **  Congratulations !!    **      / O.O  |
        **                        **    /_____   |
        **  Simulation PASS!!     **   /^ ^ ^ \  |
        **                        **  |^ ^ ^ ^ |w|
        ****************************   \m___m__|_|


$finish called from file "ALU_tb.v", line 315.
$finish at simulation time                310000
           V C S   S i m u l a t i o n   R e p o r t
Time: 310000 ps
CPU Time:      1.100 seconds;       Data structure size:   3.3Mb
Mon Mar 18 18:49:28 2024
CPU time: 13.550 seconds to compile + 1.100 seconds to elab + .899 seconds to li
nk + 1.141 seconds in simulation
vlsicad6:/home/user2/vlsi24/vlsi2416/Lab3_E14102305/Lab3_E14102305/ProbA %
```

Your waveform (RTL & Synthesis) :

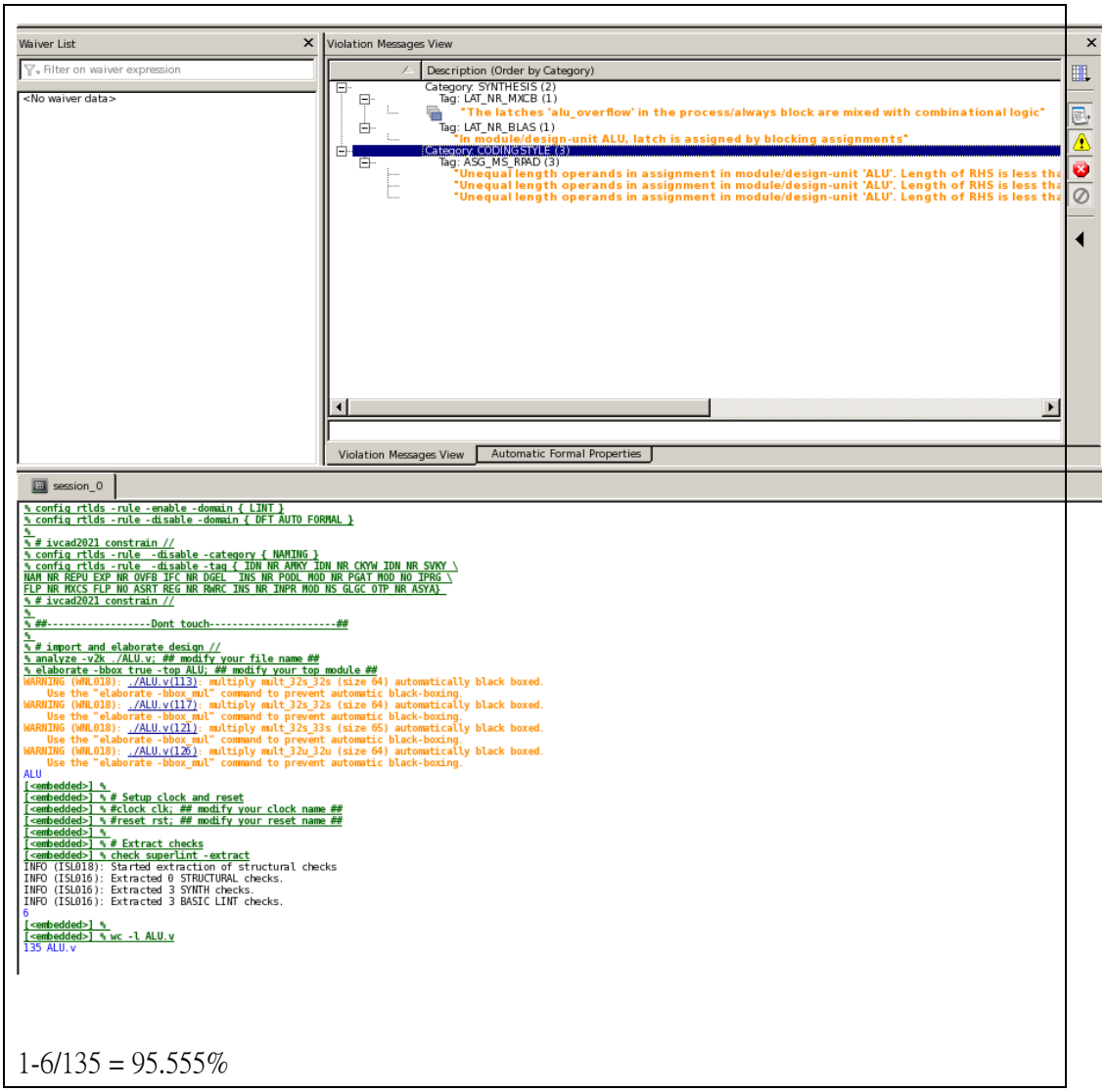
RTL



SYn



SuperLint Coverage



Prob B-1: Practice fixed point

Design your Verilog code with the following specifications: Number format: unsigned numbers.

c. The frame code and testbench are given. Follow the frame code to finish this homework. The decimal part should be rounded.

d. Follow the PPT file to synthesize your code.

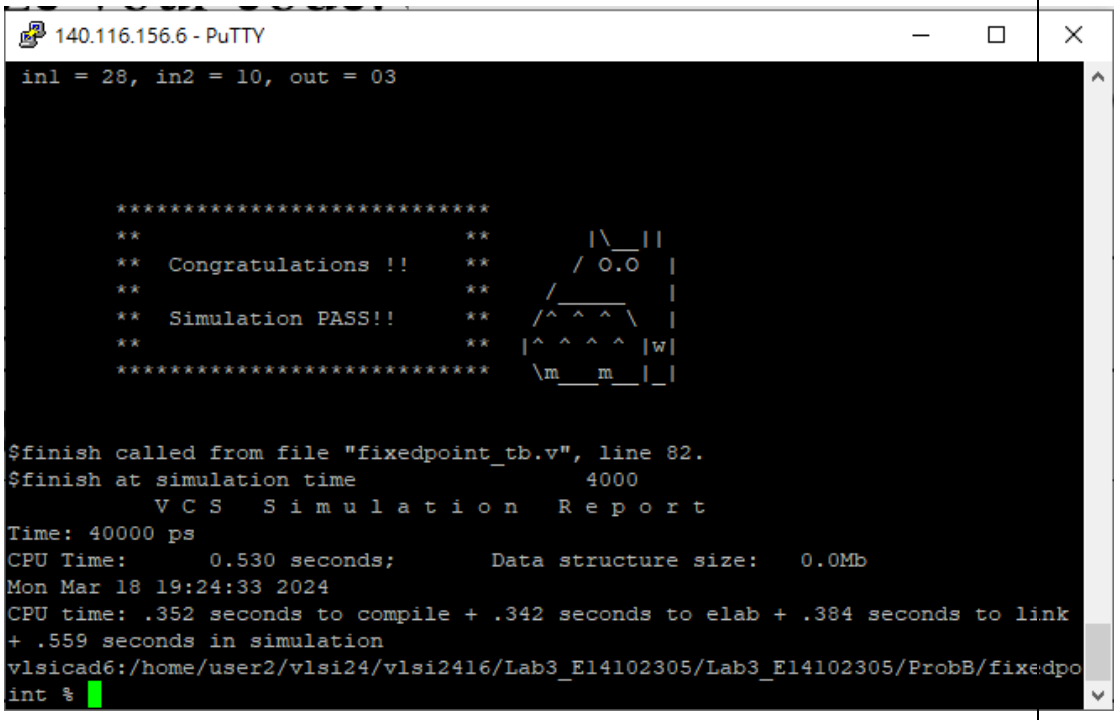
After you synthesize your design, you may have some information about the circuit. Fill in the following form.

Timing (slack)	Area (total cell area)	Power (total)
19.53	70.088	4.7329e-02 mW

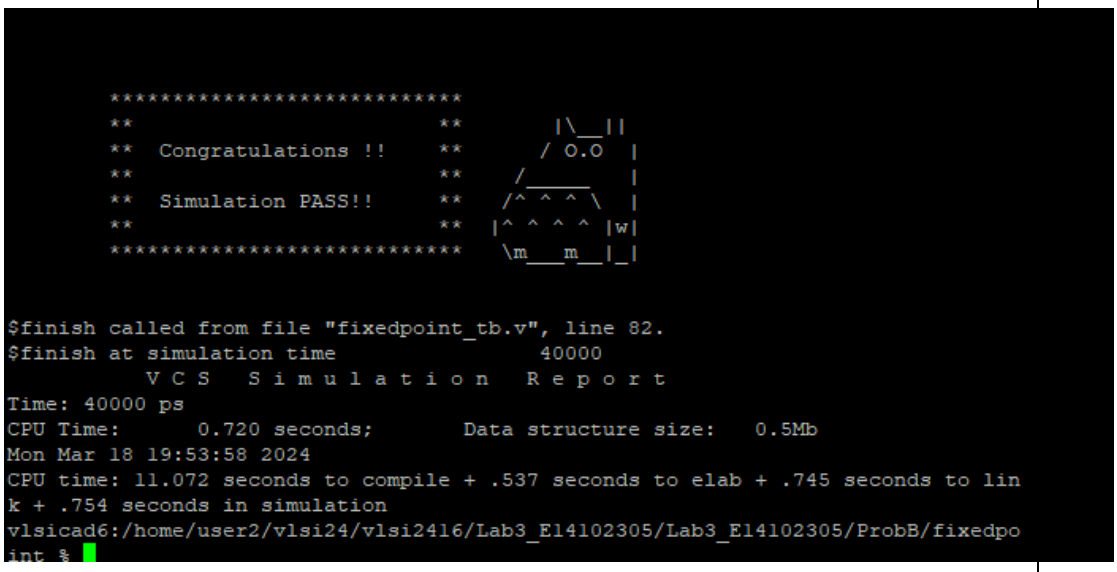
Please attach your design waveforms.

Your simulation result on the terminal.

RTL

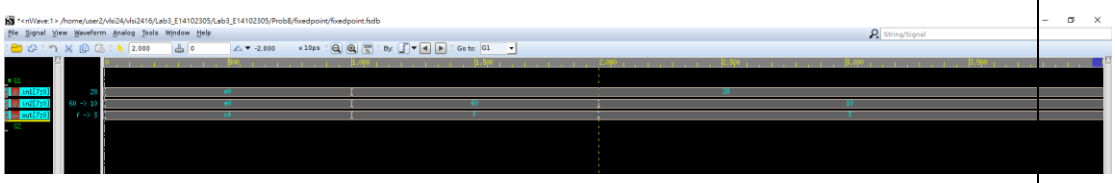


SYN

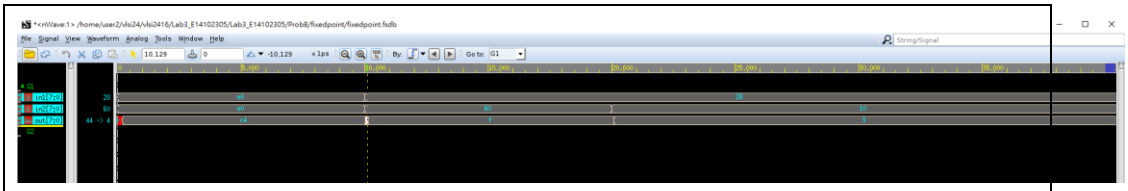


Your waveform (RTL & Synthesis) :

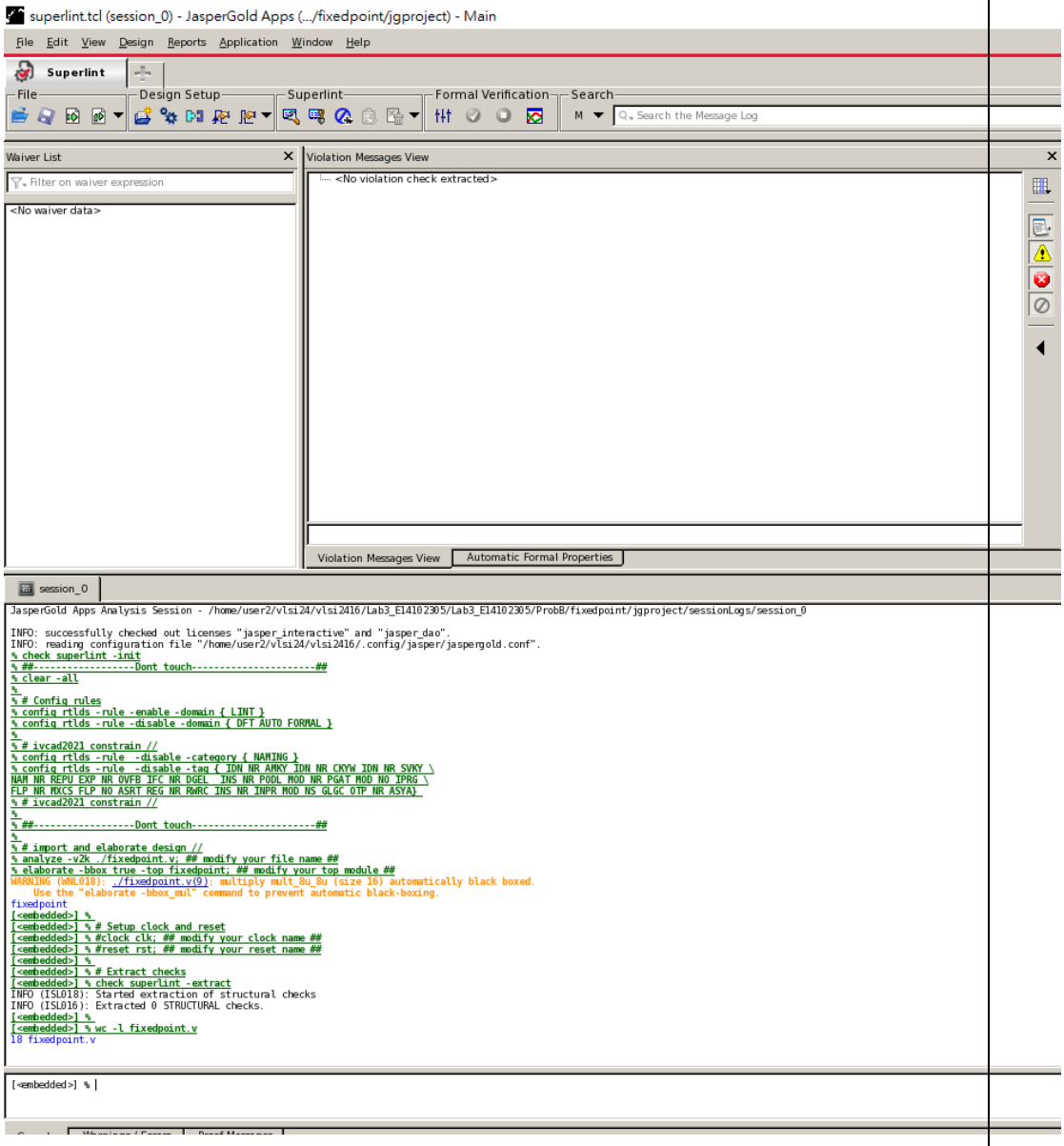
RTL



SYN



SuperLint Coverage



0 → 100%

Prob B-2: Practice fixed point (signed)

Design your Verilog code with the following specifications: Number format: signed numbers.

a. The frame code and testbench are given. Follow the frame code to finish this homework. The decimal part should be rounded.

b. Follow the PPT file to synthesize your code.

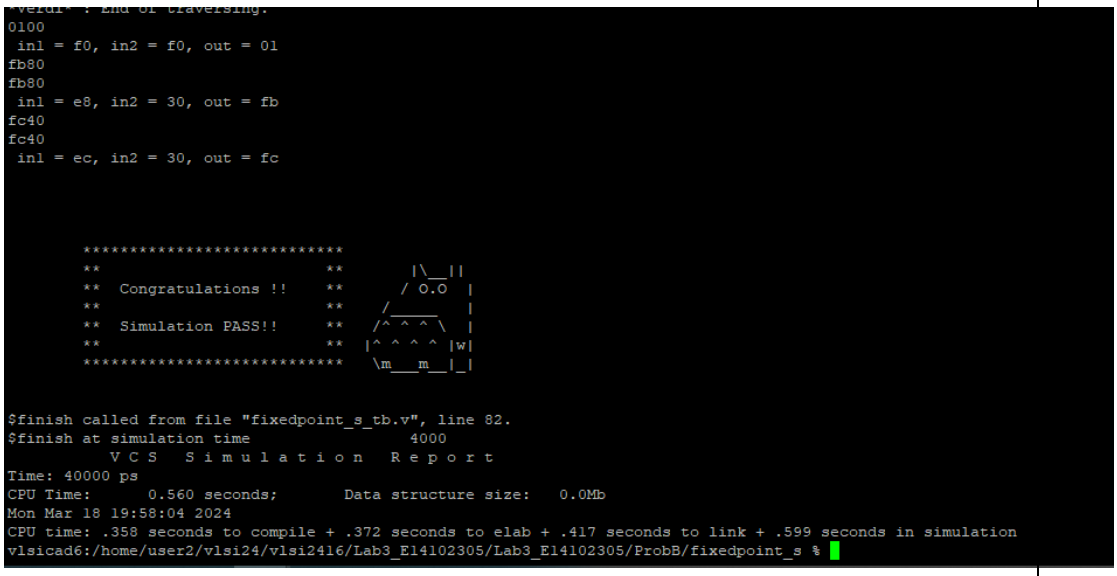
After you synthesize your design, you may have some information about the circuit. Fill in the following form

Timing (slack)	Area (total cell area)	Power (total)
19.5	77.915522	6.2067e-02 mW

Please attach your design waveforms.

Your simulation result on the terminal.

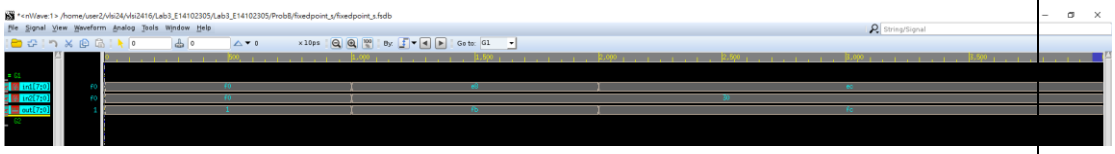
RTL



SYN

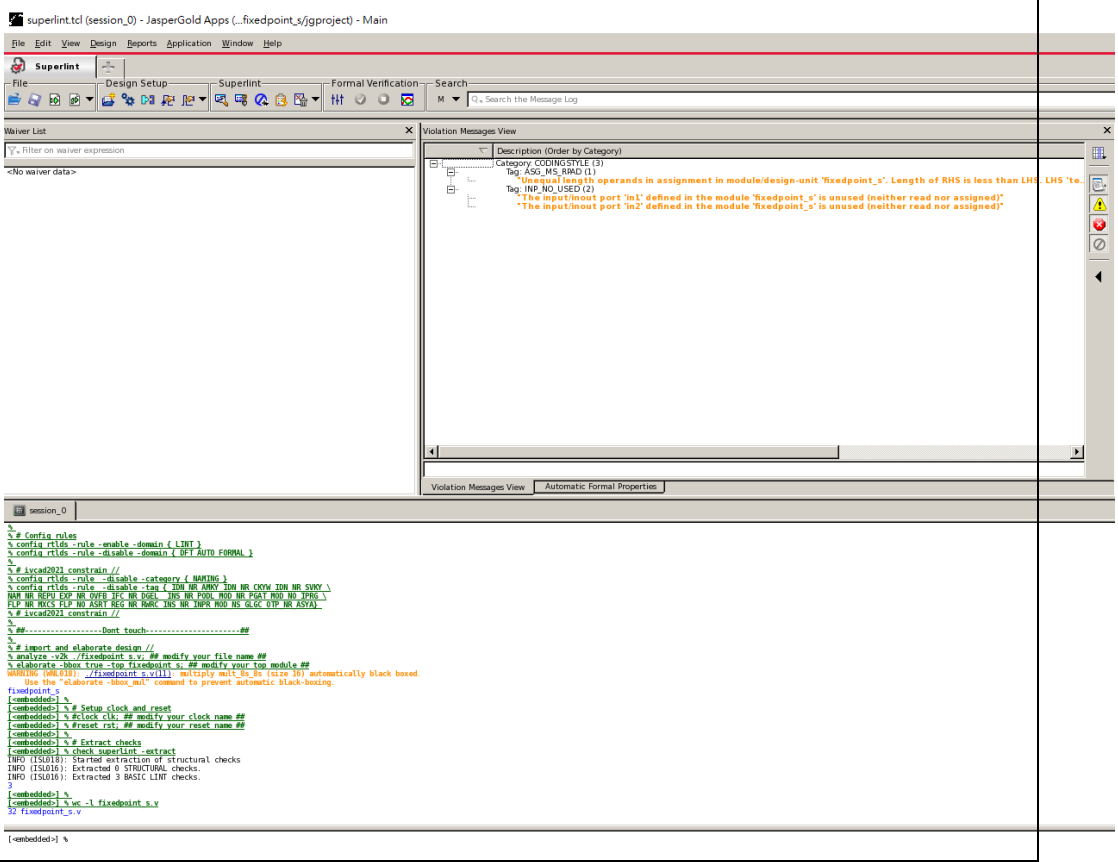
Your waveform (RTL & Synthesis) :

RTL



SYN

SuperLint Coverage



1-3/32 = 90.63%

Prob C: Performance comparison

Synthesize the 8*8-bit CLA multiplier implemented in Lab2 and the given 8*8-bit multiplier separately.

You should answer the following questions:

1. Determine the lowest achievable clock period for both, along with the corresponding area and power consumption.

	Clock period	**Timing (slack)**	**Area (total cell area)**	**Power (total)**
CLA multiplier	**.5**	**0**	**213.995525**	**0.1263 mW**
“*”operator	**0.17**	**0**	**151.735682**	**9.7272e-02 mW**

2. Considering clock period and area, which structure has the better performance.

在 **POWER** 的部分可以知道，下面那個會比較好，所以我們可以以此推論，**CLOCK PERIODE AND AREA** 越小越好

At last, please write the lessons learned from this lab session, or some suggestions for this lab session. Thank you.

太美了，這麼棒的課，可以督促自己專研硬體描述語言，還可以順練耐心，者麼棒的課我會推給學弟妹們上的，沒有一個跑得掉。

Problem		Command
ProbA	Compile	% vcs -R ALU.v -full64
	Simulate	% vcs -R ALU_tb.v -debug_access+all -full64 +define+FSDB
	Synthesis	% vcs -R ALU_tb.v -debug_access+all -full64 +define+FSDB+syn
ProbB-1	Compile	% vcs -R fixedpoint.v -full64
	Simulate	% vcs -R fixedpoint_tb.v -debug_access+all -full64 +define+FSDB
	Synthesis	% vcs -R fixedpoint_tb.v -debug_access+all -full64 +define+FSDB+syn
ProbB-2	Compile	% vcs -R fixedpoint_s.v -full64
	Simulate	% vcs -R fixedpoint_s_tb.v -debug_access+all -full64 +define+FSDB
	Synthesis	% vcs -R fixedpoint_s_tb.v -debug_access+all -full64 +define+FSDB+syn

Appendix A : Commands we will use to check your homework