2024 超大型積體電路電腦輔助設計概論

2024 Introduction to VLSI CAD

Lab 9

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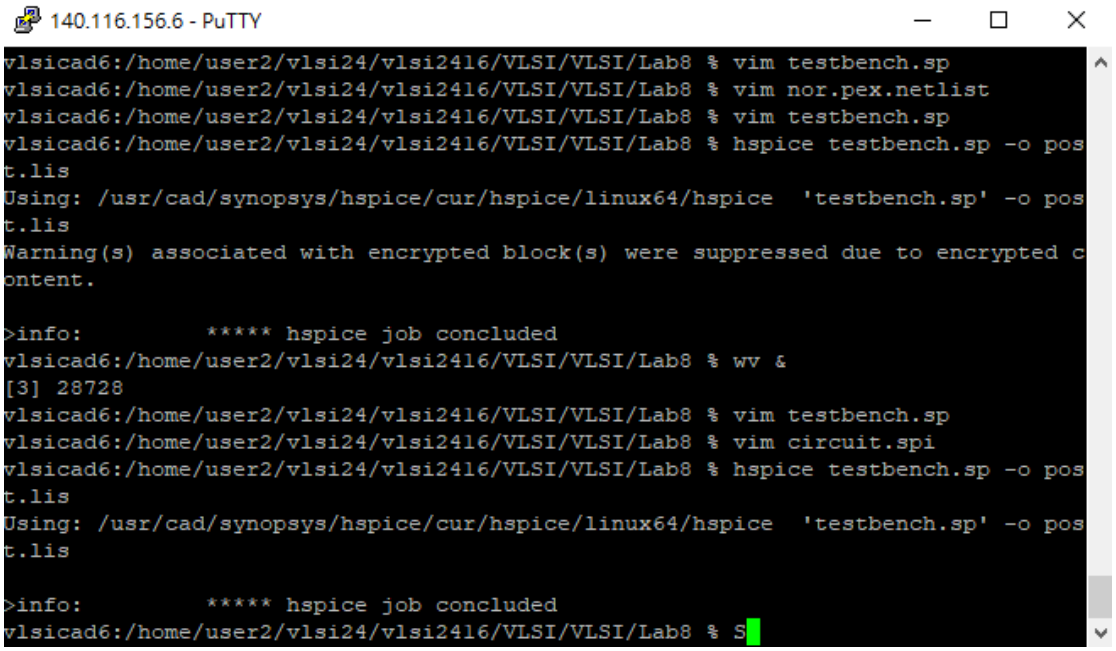
※作業要求的圖請使用**電腦截圖程式**截取，請勿用手機拍照的方式繳交

※Report 檔請以 pdf 的格式繳交

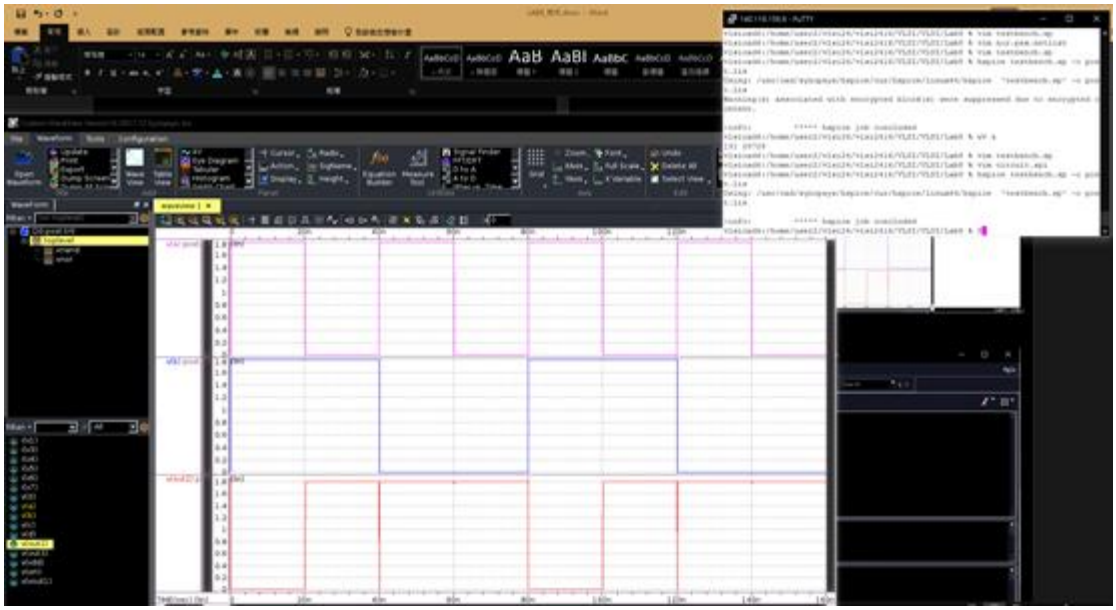
A. NAND

1. Presim

i. 請截取 terminal 顯示 job concluded 的圖

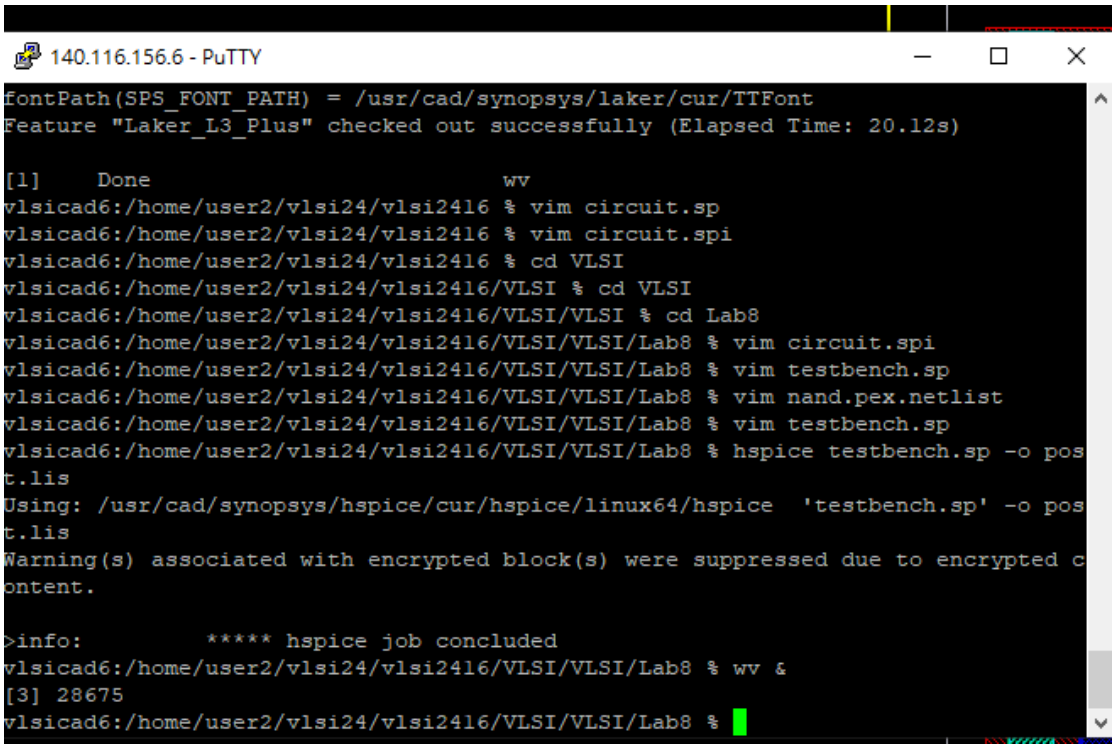


ii. 請截取 WaveView 中的波形

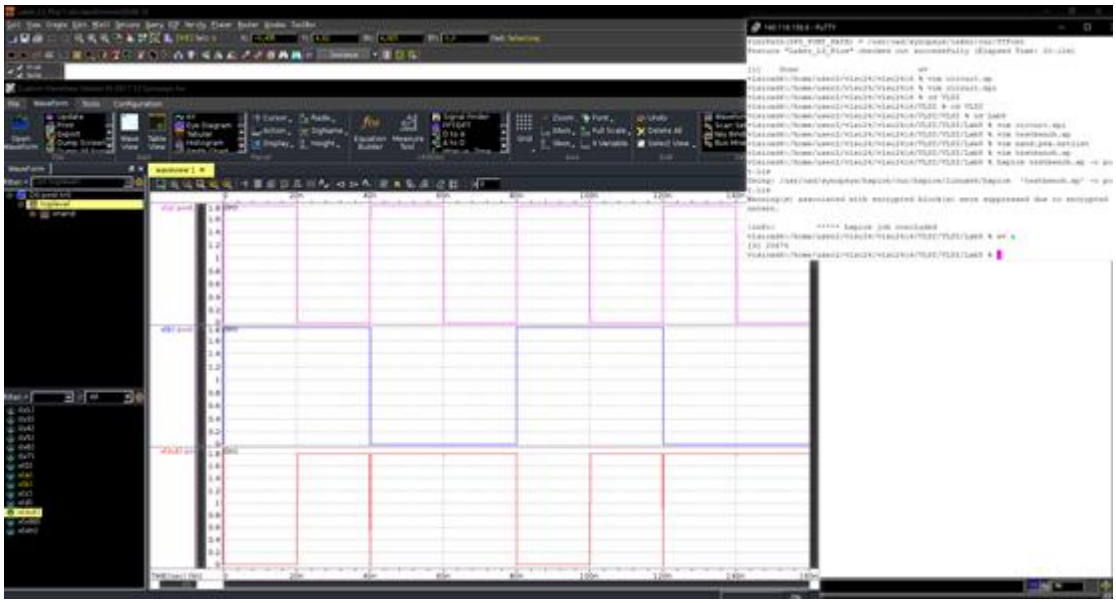


2. Post-sim

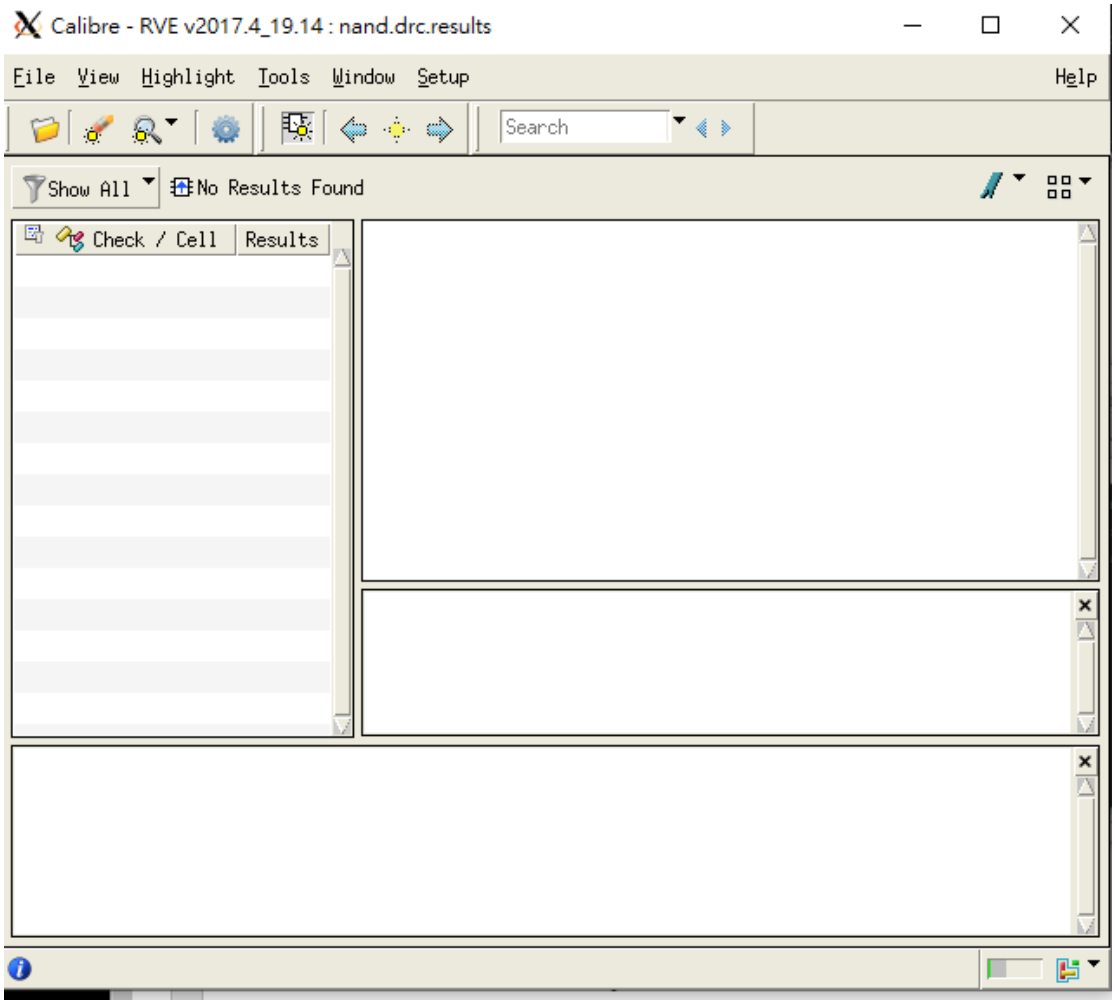
i. 請截取 terminal 顯示 job concluded 的圖

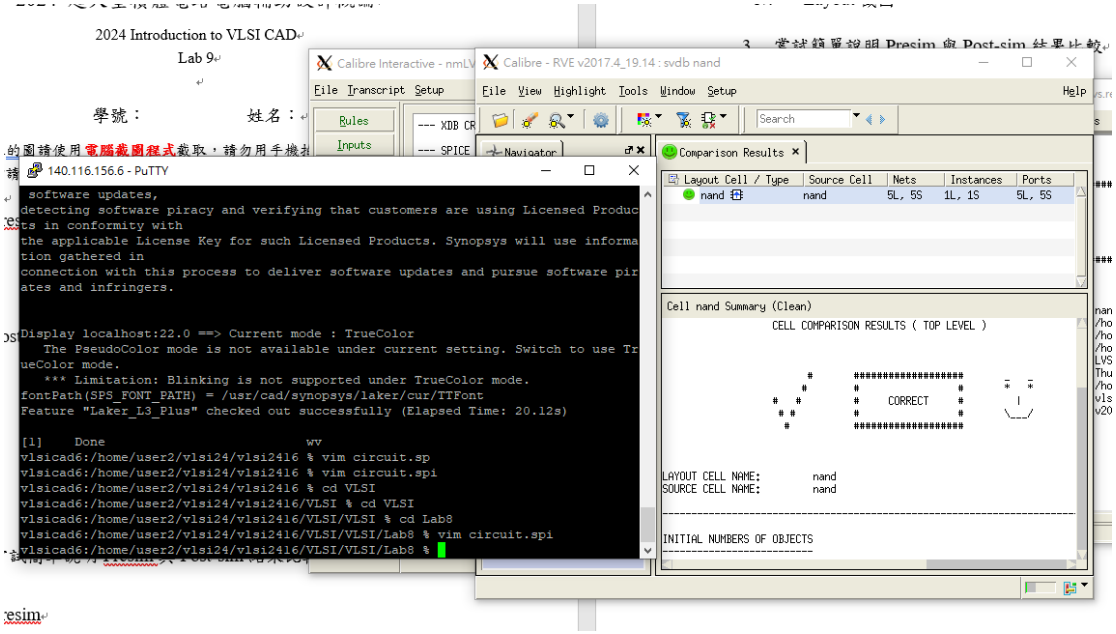


ii. 請截取 WaveView 中的波形



iii. DRC/LVS 結果

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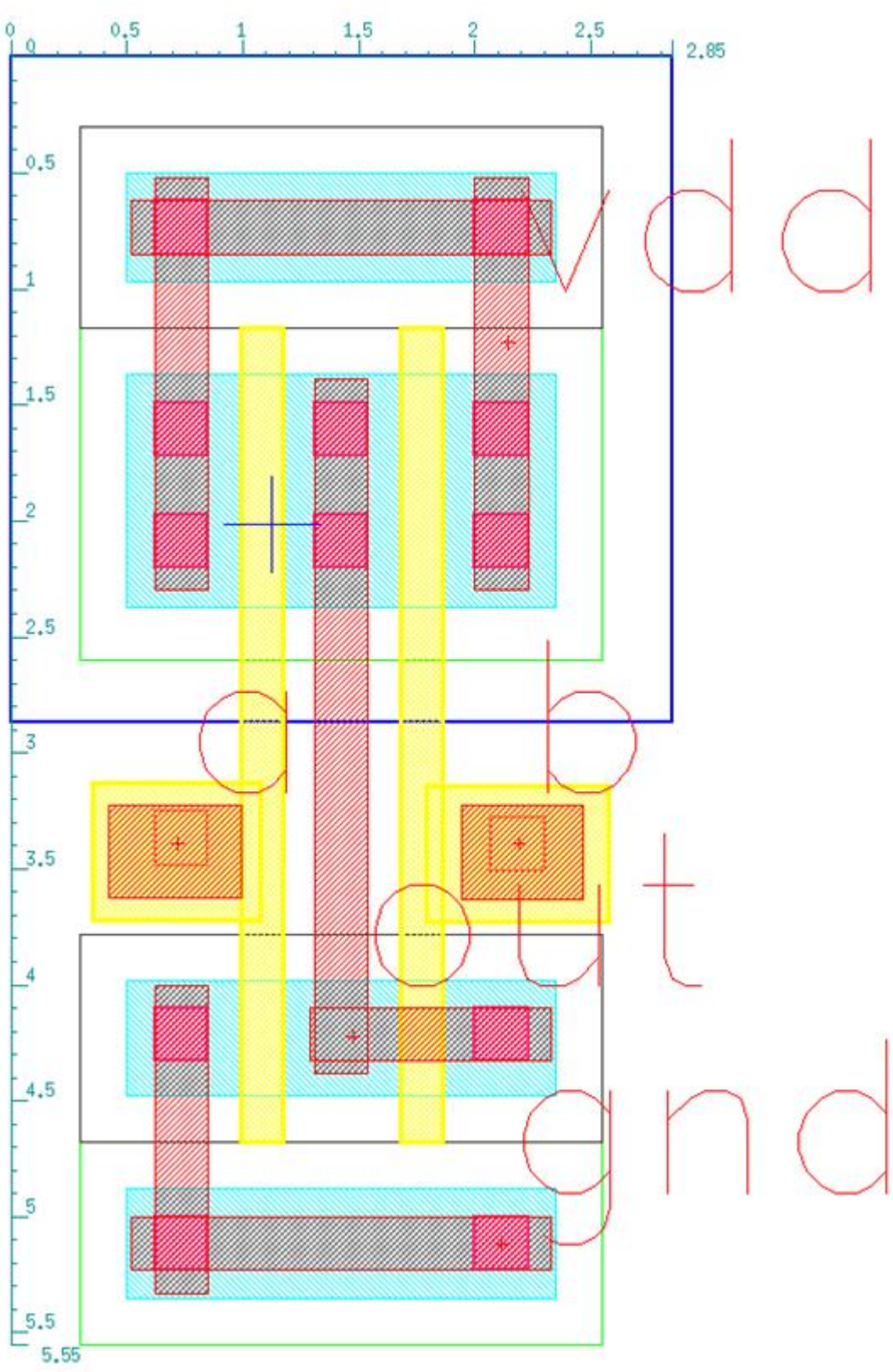
學號：
姓名：
Calibre Interactive - nmLV
File Transcript Setup
Rules
Inputs
--- XDB CR
--- SPICE
Calibre - RVE v2017.4_19.14 : svdb nand
File View Highlight Tools Window Setup
Help
Search
Navigator
Comparison Results
Layout Cell / Type
Source Cell
Nets
Instances
Ports
nand
nand
5L, 5S
1L, 1S
5L, 5S
140.116.156.6 - PuTTY
software updates,
detecting software piracy and verifying that customers are using Licensed Products in conformity with
the applicable License Key for such Licensed Products. Synopsys will use information gathered in
connection with this process to deliver software updates and pursue software pirates and infringers.
Display localhost:22.0 ==> Current mode : TrueColor
The PseudoColor mode is not available under current setting. Switch to use TrueColor mode.
*** Limitation: Blinking is not supported under TrueColor mode.
fontPath(SPS_FONT_PATH) = /usr/cad/synopsys/laker/cur/TTFont
Feature "Laker_L3_Plus" checked out successfully (Elapsed Time: 20.12s)
[1] Done wv
vlsicad6:/home/user2/vlsi24/vlsi2416 % vim circuit.sp
vlsicad6:/home/user2/vlsi24/vlsi2416 % vim circuit.spi
vlsicad6:/home/user2/vlsi24/vlsi2416 % cd VLSI
vlsicad6:/home/user2/vlsi24/vlsi2416/VLSI % cd VLSI
vlsicad6:/home/user2/vlsi24/vlsi2416/VLSI/VLSI % cd Lab8
vlsicad6:/home/user2/vlsi24/vlsi2416/VLSI/VLSI/Lab8 % vim circuit.spi
vlsicad6:/home/user2/vlsi24/vlsi2416/VLSI/VLSI/Lab8 %
Cell nand Summary (Clean)
CELL COMPARISON RESULTS (TOP LEVEL)
CORRECT
LAYOUT CELL NAME: nand
SOURCE CELL NAME: nand
INITIAL NUMBERS OF OBJECTS

iv. Layout 截圖



3. 嘗試簡單說明 Presim 與 Post-sim 結果比較

可以發現我們 pre-sim 和 post-sim 的結果是相像的，這是因

為我們 pre-sim 是以參數去模擬我們的電路，而 layout 就是

將真實樣貌畫在 board 上。所以結果相像我認為是應該的。

B. NOR

1. Presim

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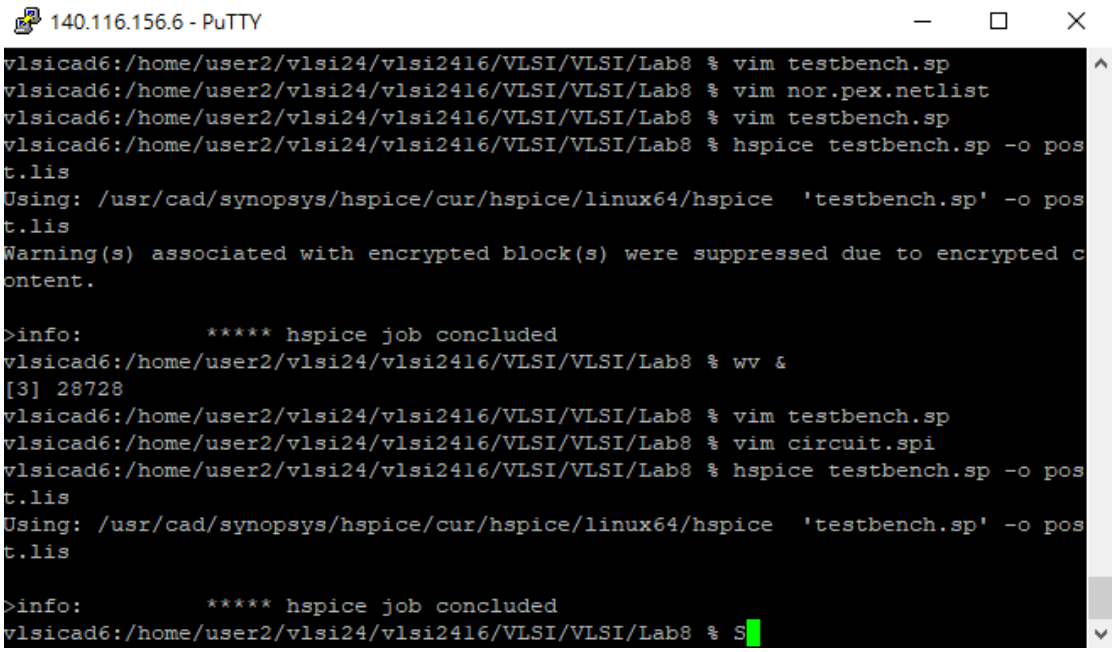

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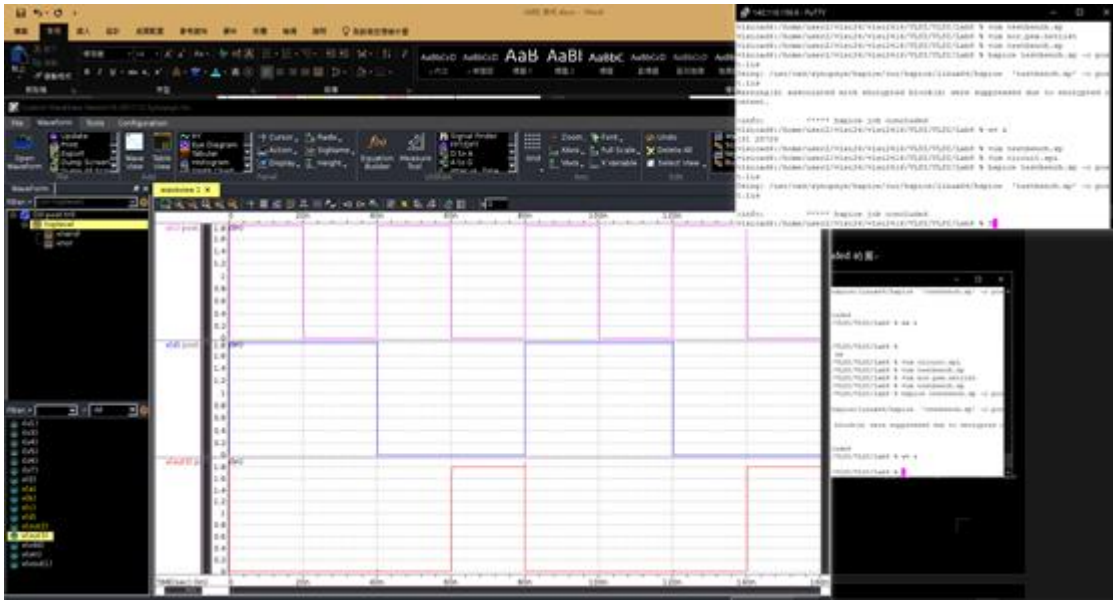

2. Post-sim

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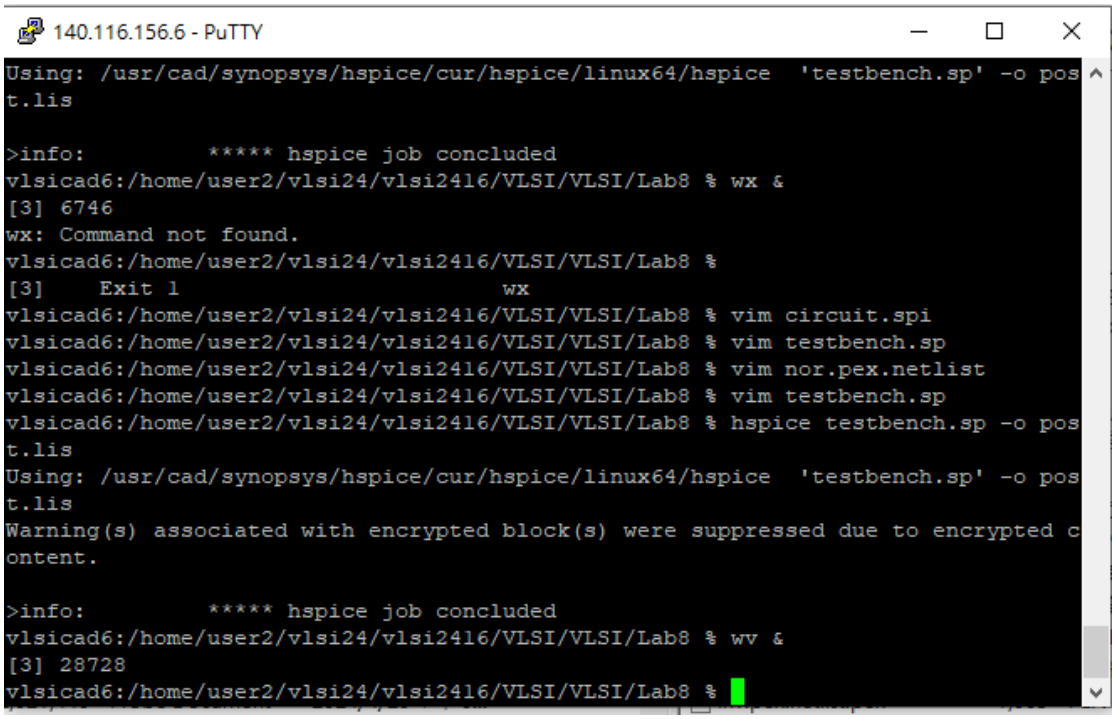

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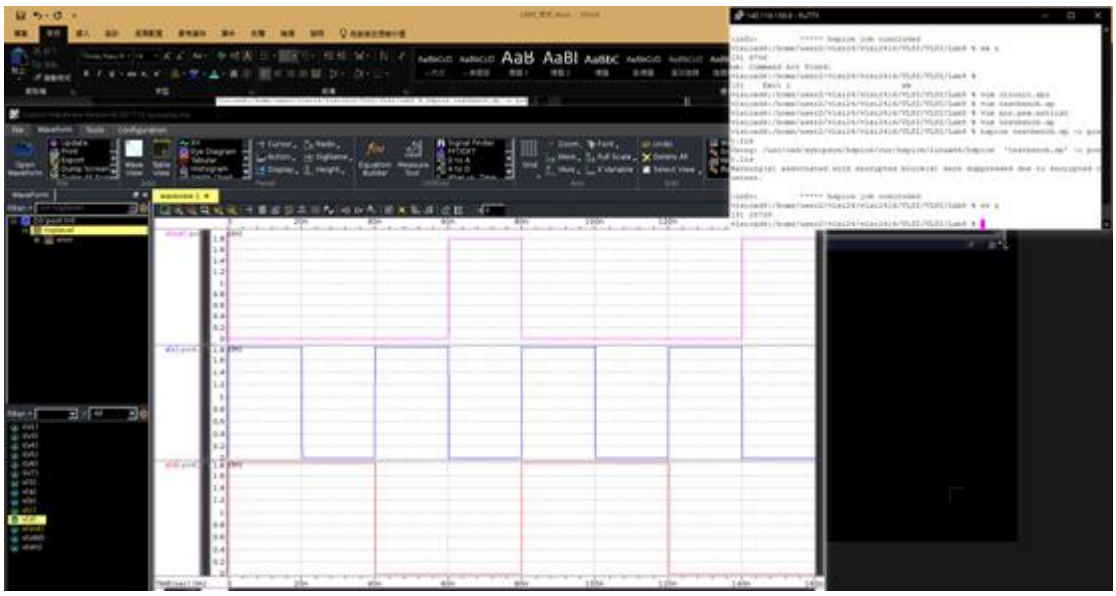

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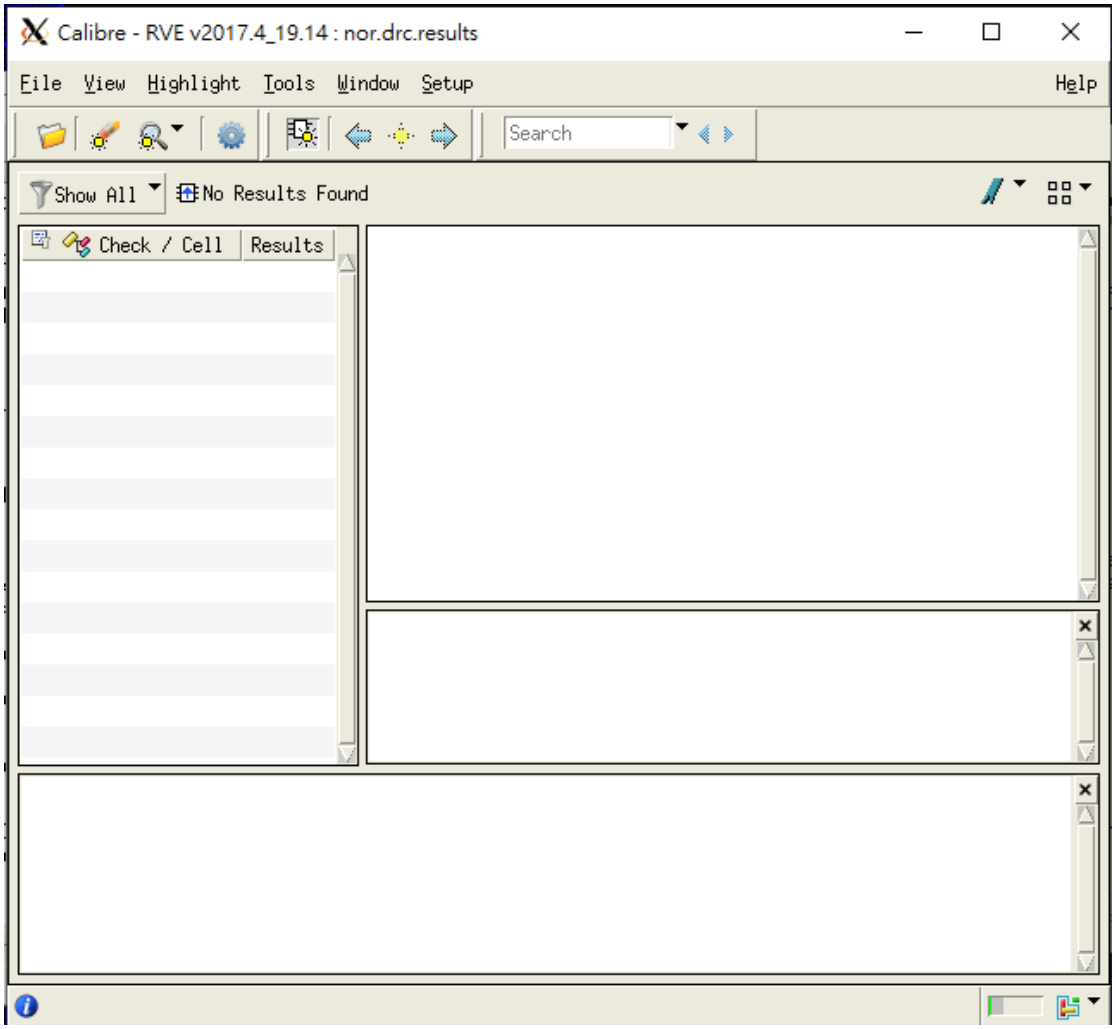
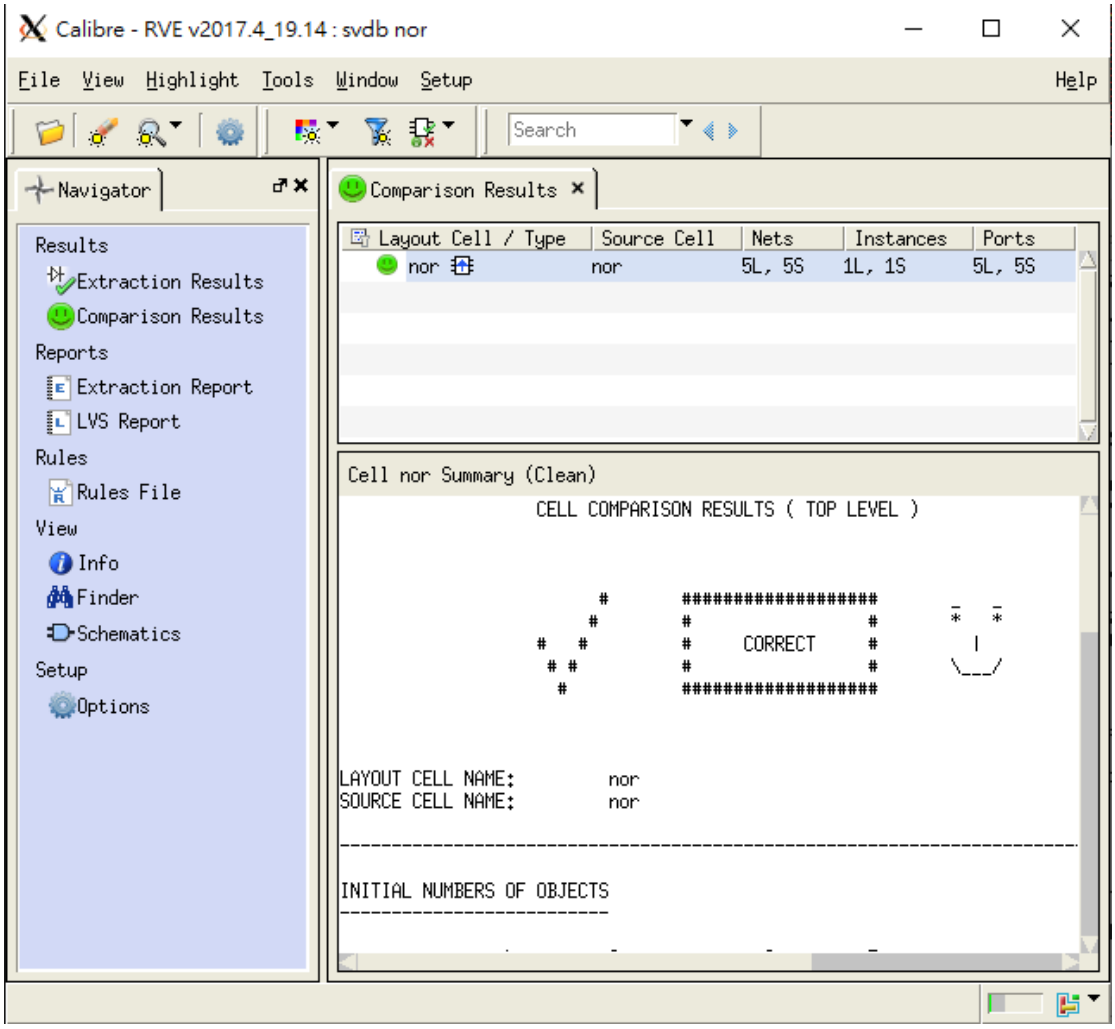

Calibre - RVE v2017.4_19.14 : nor.drc.results
File View Highlight Tools Window Setup Help
Search
Show All
No Results Found
Check / Cell
Results


Calibre - RVE v2017.4_19.14 : svdb nor
File View Highlight Tools Window Setup Help
Search
Navigator
Results
Extraction Results
Comparison Results
Reports
Extraction Report
LVS Report
Rules
Rules File
View
Info
Finder
Schematics
Setup
Options
Comparison Results
Layout Cell / Type
Source Cell
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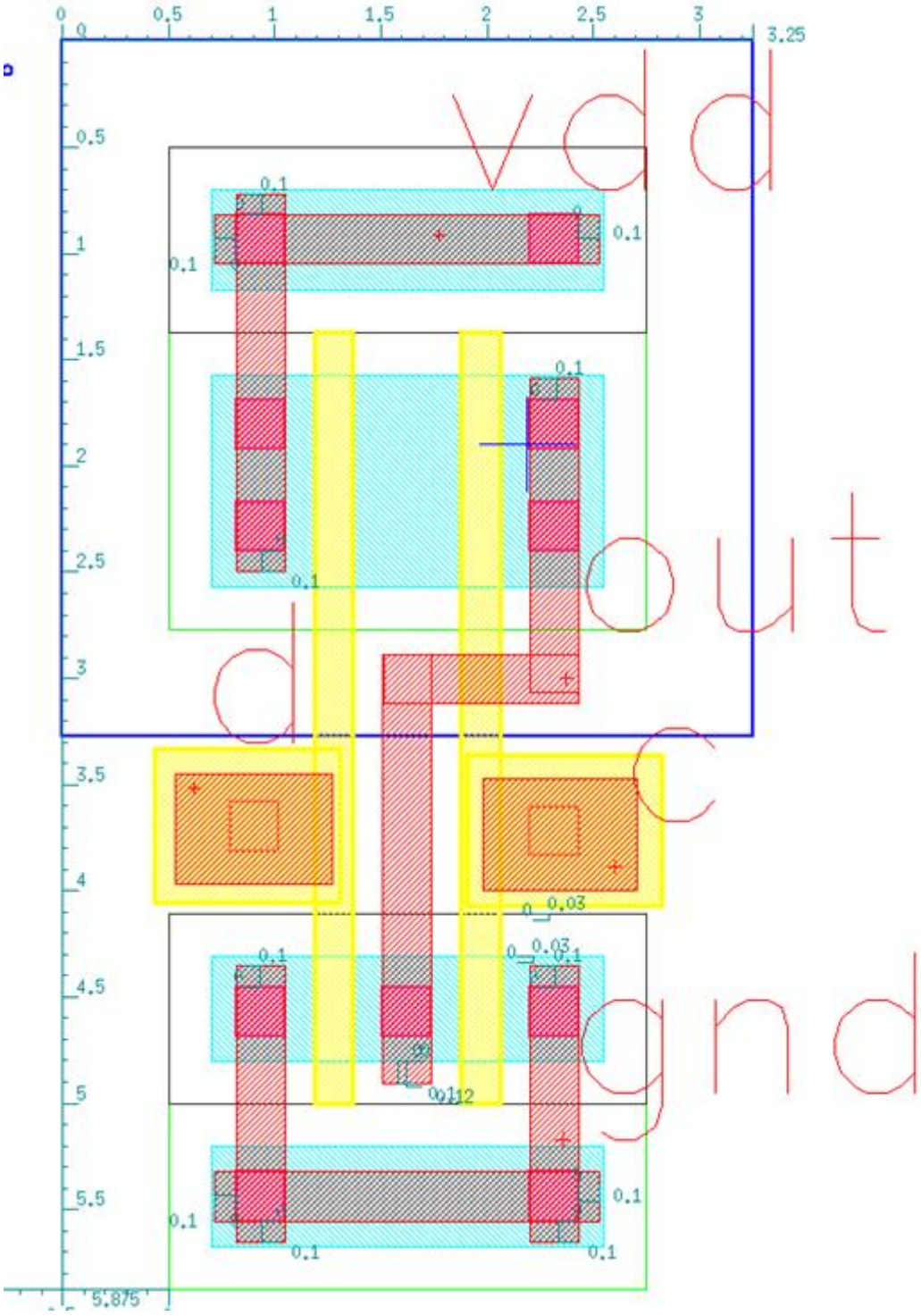

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D. 心得討論

這次 lab 是第一次畫 layout，我是從 inverter 先下手的，一開始沒有熟記裡面的規則可以說是碰到重重困難，還好的是什麼沒有，我的耐心和時間巨多，所以在我努力不懈下，我順利地畫完 inverter 而有了這個經驗後，我在畫這次 lab 時就非常順利的完成了。