**National Cheng Kung University**

**Department of Electrical Engineering**

***Introduction to VLSI CAD (Spring 2024)***

**Lab Session 3**

**Design of ALU and Multiplication Using Verilog Coding**

|  |  |  |  |
| --- | --- | --- | --- |
| Name | Student ID | | |
| 簡笠恩 | E14102305 | | |
| Practical Sections: | | Points | Marks |
| Prob A | | 30 |  |
| Prob B | | 30 |  |
| Prob C | | 20 |  |
| Report | | 15 |  |
| File hierarchy, naming…etc. | | 5 |  |
| Notes | | | |

**Due Date: 15:00, March 13, 2024 @ moodle**

**Deliverables**

1. All Verilog codes including testbenches for each problem should be uploaded.

NOTE: Please **DO NOT** include source code in the paper report!

1. All homework requirements should be uploaded in this file hierarchy or you will not get the full credit.

NOTE: Please **DO NOT** upload waveforms!

1. Important! TA will use the command in Appendix A to check your design under SoC Lab environment, if your code can not be recompiled by TA successfully using the commands, you will not get the full credit.
2. **If you upload a dead body which we can’t even compile you will get NO credit!**
3. **All Verilog file should get at least 90% superLint Coverage.**
4. **File hierarchy should not be changed; it may cause** your code can not be recompiled by TA successfully using the autograding commands

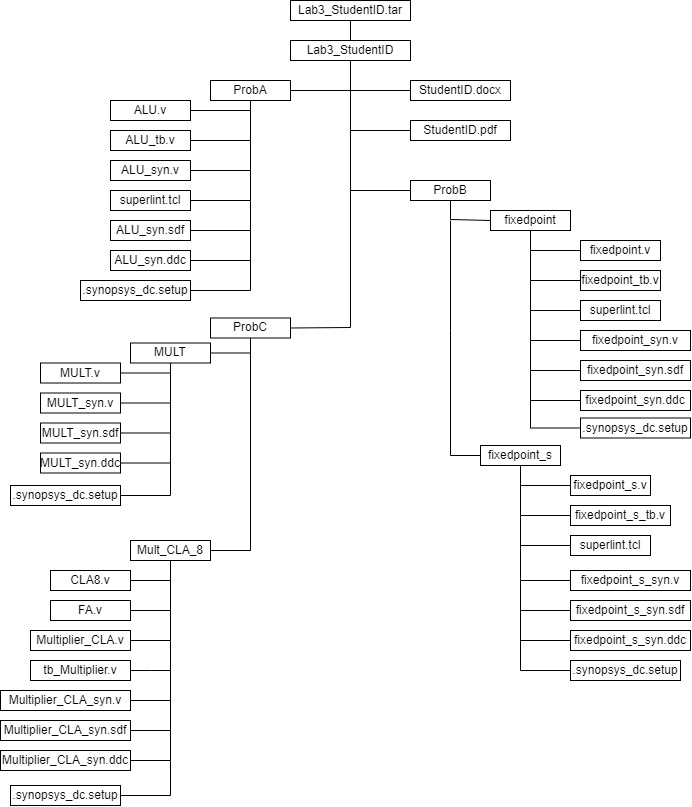
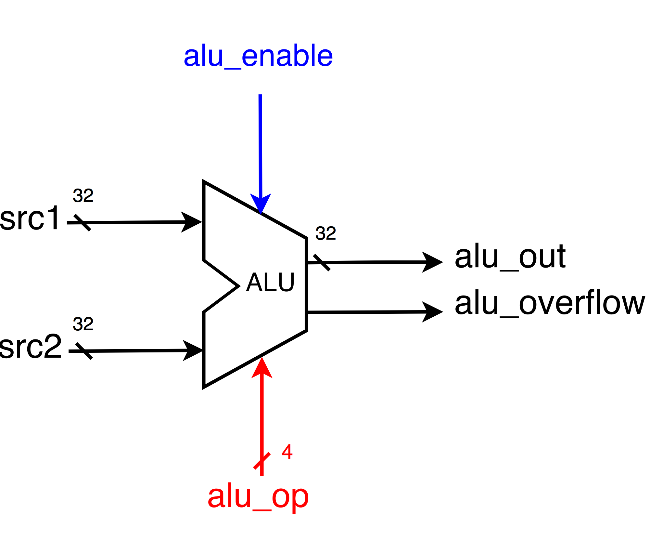


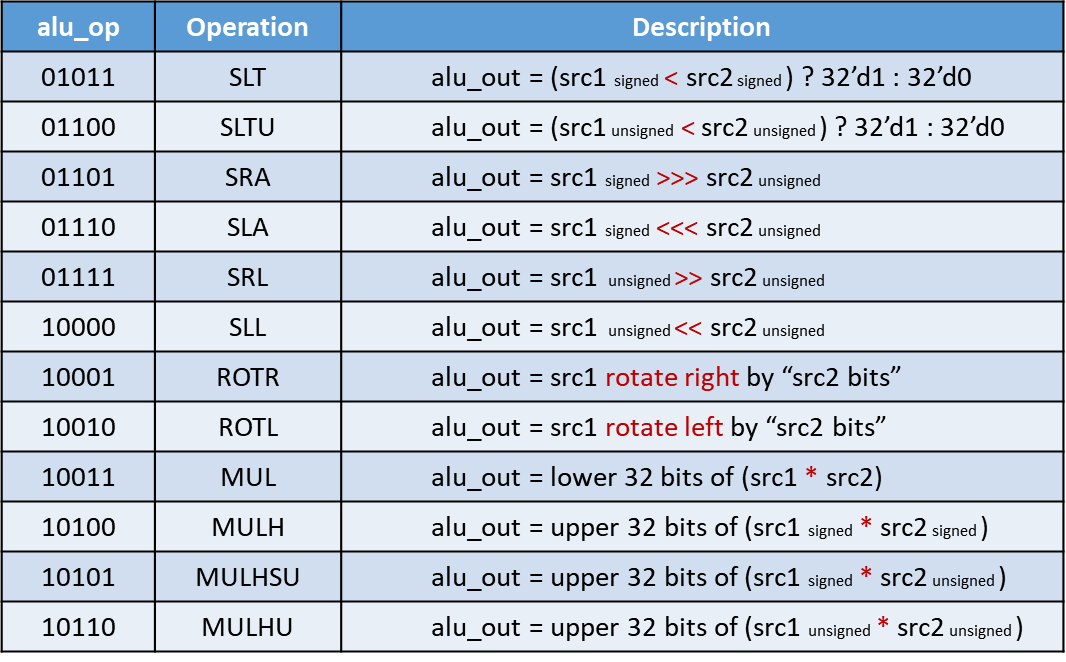
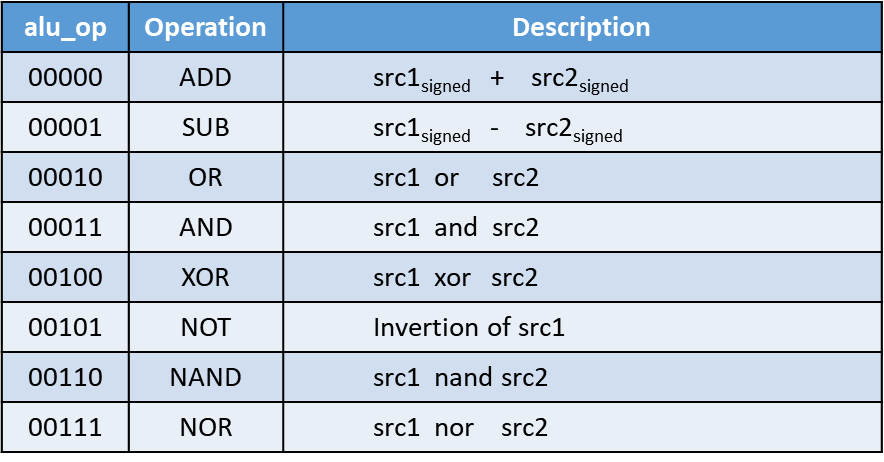
Fig.1 File hierarchy for Homework submission

Prob A: Arithmetic Logic Unit

**Design your Verilog code with the following specifications:**



1. Based on the reference code, please implement the following operations.



* 1. The frame code and testbench are given. Follow the frame code to finish this homework. The decimal part should be rounded.
  2. Follow the PPT file to synthesize your code.

**After you synthesize your design, you may have some information about the circuit. Fill in the following form.**

|  |  |  |
| --- | --- | --- |
| **Timing (slack)** | **Area (total cell area)** | **Power (total)** |
| **18.04** | **4127.967** | **4.2602(mW)** |

**Please attach your design waveforms.**

|  |
| --- |
| Your simulation result on the terminal. |
| RTL    SYN |
| Your waveform (RTL & Synthesis) : |
| RTL  SYn |
| SuperLint Coverage |
| 1-6/135 = 95.555% |

Prob B-1: Practice fixed point

**Design your Verilog code with the following specifications:** Number format: unsigned numbers.

* 1. The frame code and testbench are given. Follow the frame code to finish this homework. The decimal part should be rounded.
  2. Follow the PPT file to synthesize your code.

**After you synthesize your design, you may have some information about the circuit. Fill in the following form.**

|  |  |  |
| --- | --- | --- |
| **Timing (slack)** | **Area (total cell area)** | **Power (total)** |
| **19.53** | **70.088** | **4.7329e-02 mW** |

**Please attach your design waveforms.**

|  |
| --- |
| Your simulation result on the terminal. |
| RTL  SYN |
| Your waveform (RTL & Synthesis) : |
| RTL  SYN |
| SuperLint Coverage |
| 0 🡪 100% |

Prob B-2: Practice fixed point (signed)

**Design your Verilog code with the following specifications:** Number format: signed numbers.

1. The frame code and testbench are given. Follow the frame code to finish this homework. The decimal part should be rounded.
2. Follow the PPT file to synthesize your code.

**After you synthesize your design, you may have some information about the circuit. Fill in the following form**

|  |  |  |
| --- | --- | --- |
| **Timing (slack)** | **Area (total cell area)** | **Power (total)** |
| **19.5** | **77.915522** | **6.2067e-02 mW** |

**Please attach your design waveforms.**

|  |
| --- |
| Your simulation result on the terminal. |
| RTL  SYN |
| Your waveform (RTL & Synthesis) : |
| RTL  SYN |
| SuperLint Coverage |
|  |
| 1-3/32 = 90.63% |

Prob C: Performance comparison

**Synthesize the 8\*8-bit CLA multiplier implemented in Lab2 and the given 8\*8-bit multiplier separately.**

You should answer the following questions:

**1. Determine the lowest achievable clock period for both, along with the corresponding area and power consumption.**

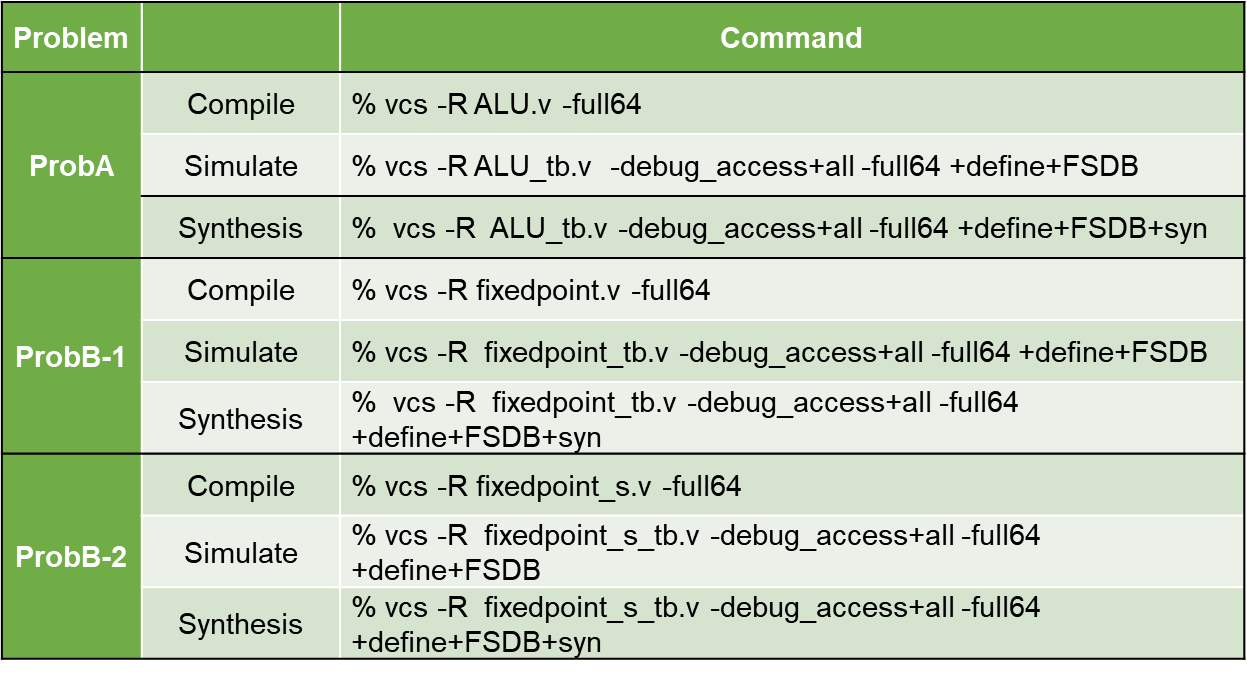
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **Clock period** | **Timing (slack)** | **Area (total cell area)** | **Power (total)** |
| **CLA multiplier** | **.5** | **0** | **213.995525** | **0.1263 mW** |
| **“\*”operator** | **0.17** | **0** | **151.735682** | **9.7272e-02 mW** |

**2. Considering clock period and area, which structure has the better performance.**

**在POWER的部分可以知道，下面那個會比較好，所以我們可以以此推論，CLOCK PERIODE AND AREA 越小越好**

**At last, please write the lessons learned from this lab session, or some suggestions for this lab session. Thank you.**

**太美了，這麼棒的課，可以督促自己專研硬體描述語言，還可以順練耐心，這麼棒的課我會推給學弟妹們上的，沒有一個跑得掉。意思是我覺得這是一門可增進個人實力的課，我覺得大家都可以修。**



Appendix A : Commands we will use to check your homework