**National Cheng Kung University**

**Department of Electrical Engineering**

***Introduction to VLSI CAD (Spring 2024)***

**Lab Session 4**

**Register Files, Manhattan Distance and LFSR**

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| --- | --- | --- |
| Name | Student ID | |
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| **Practical Sections** | **Points** | **Marks** |
| Prob A | 30 |  |
| Prob B | 30 |  |
| Prob C | 20 |  |
| Report | 15 |  |
| File hierarchy, naming…etc. | 5 |  |
| Notes: | | |

**Due Date: 15:00, March 27, 2024 @ moodle**

**Deliverables**

1. All Verilog codes including testbenches for each problem should be uploaded.

NOTE: Please **DO NOT** include source code in the paper report!

1. All homework requirements should be uploaded in this file hierarchy or you will not get the full credit.

NOTE: Please **DO NOT** upload waveforms!

1. Important! TA will use the command in Appendix A to check your design under SoC Lab environment, if your code can not be recompiled by TA successfully using the commands, you will not get the full credit.
2. **If you upload a dead body which we can’t even compile you will get NO credit!**
3. **All Verilog file should get at least 90% superLint Coverage.**
4. **File hierarchy should not be changed; it may cause** your code can not be recompiled by TA successfully using the autograding commands

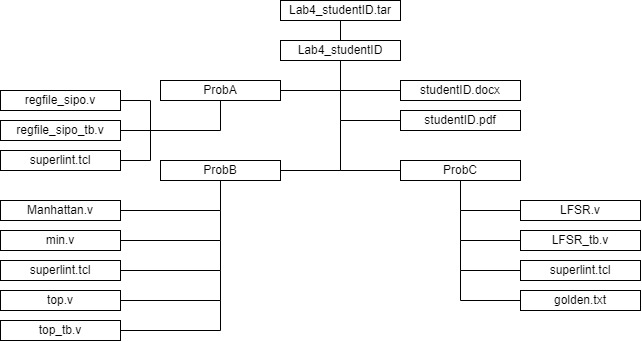


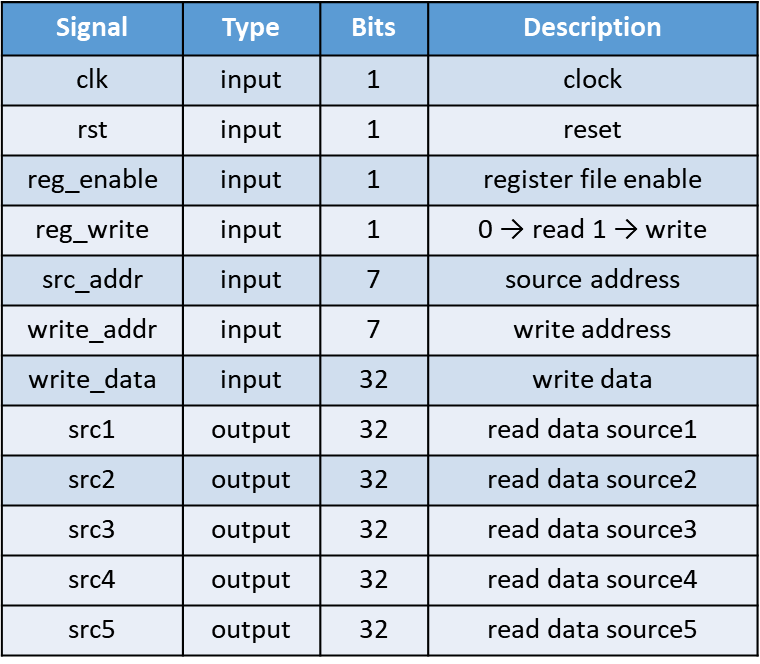
Fig.1 File hierarchy for Homework submission

Prob A: SIPO Register File

一張含有 文字, 圖表, 數字, 字型 的圖片

自動產生的描述

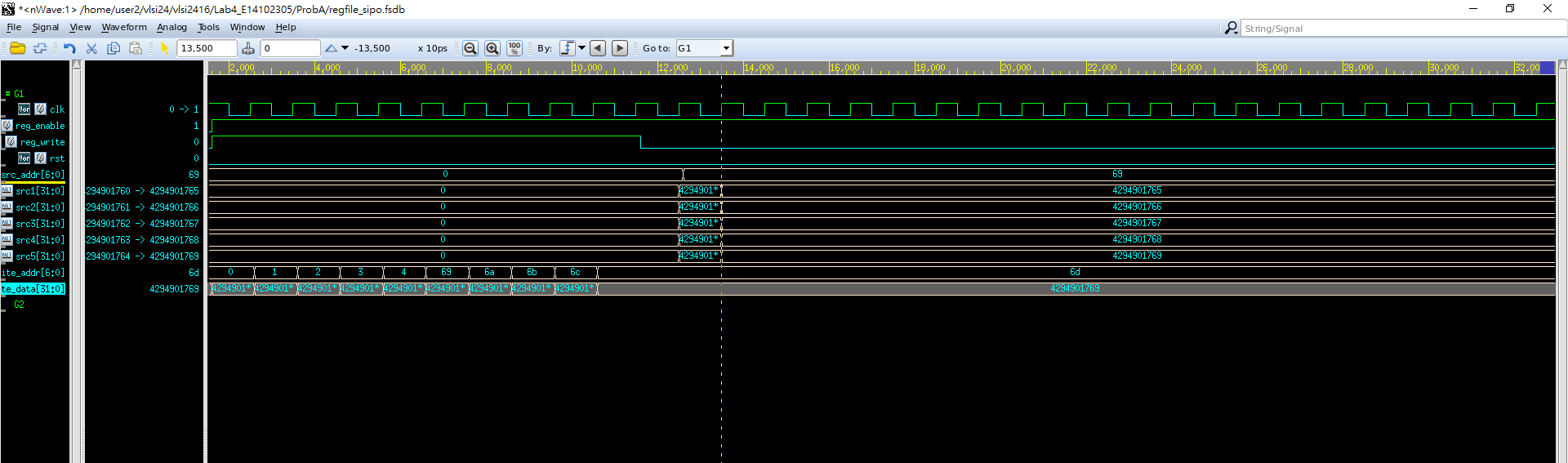
1. Based on the SIPO register file structure in LabA, please design a 128 x 32 SIPO register file with 5 output ports.
2. Port list



1. Show the simulation result on the terminal.



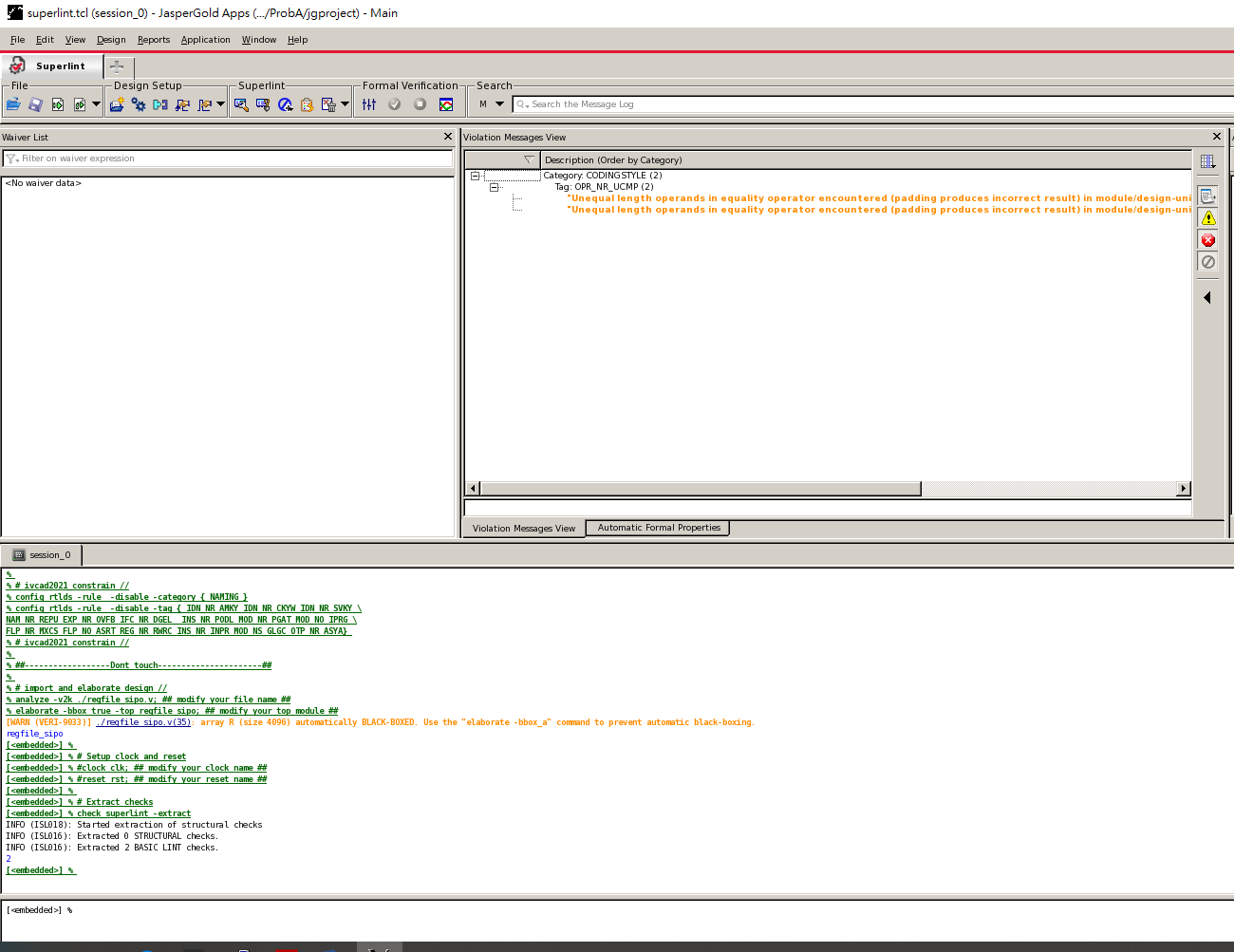
1. Show waveforms to explain that your register work correctly when read and write.



從此圖可知reg\_write = 0 為read模式故

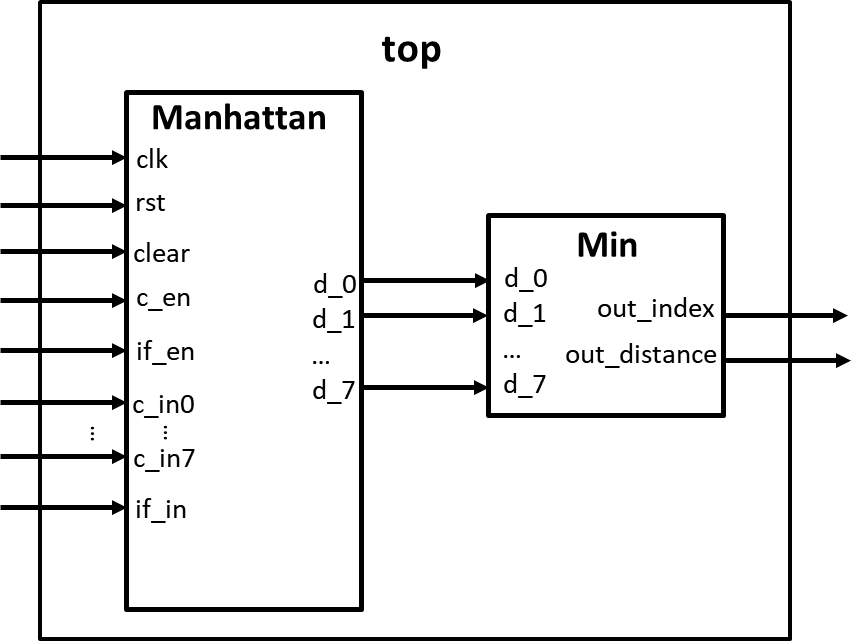
我們第一個要讀的是69暫存器所以src1為其內的值，後面四個為6a,6b,6c,6d的值，src5會是69結尾，如圖所示，前面四個也是如此。

1. Show SuperLint coverage



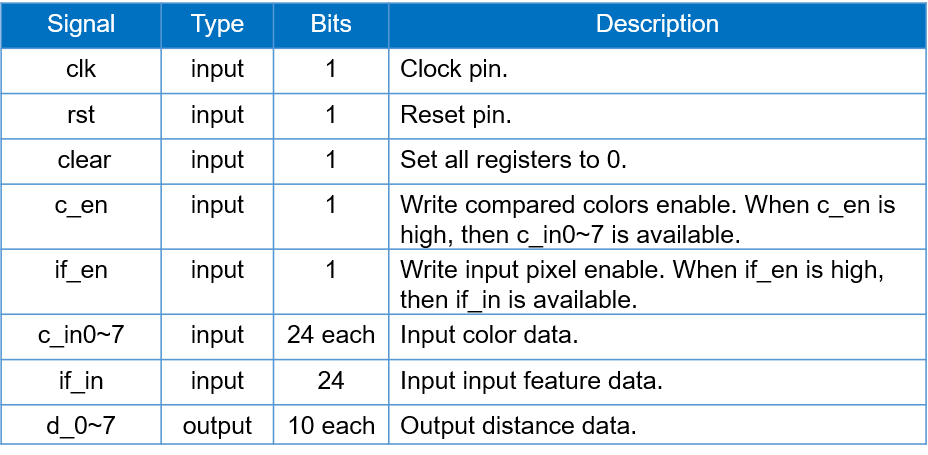
1 – 2/69 = 97%

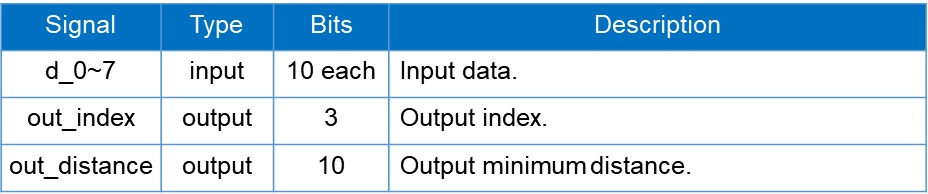
Prob B: Finding Smallest Distance



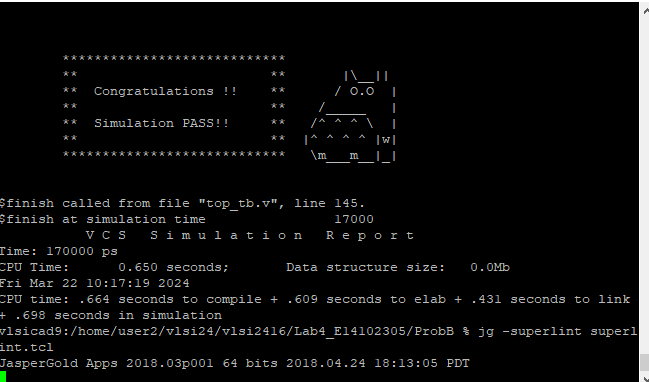
1. Please design a circuit that will find the smallest distance between the input feature and input colors, based on the structure given in the LAB4 slide.
2. Port list

Manhattan:

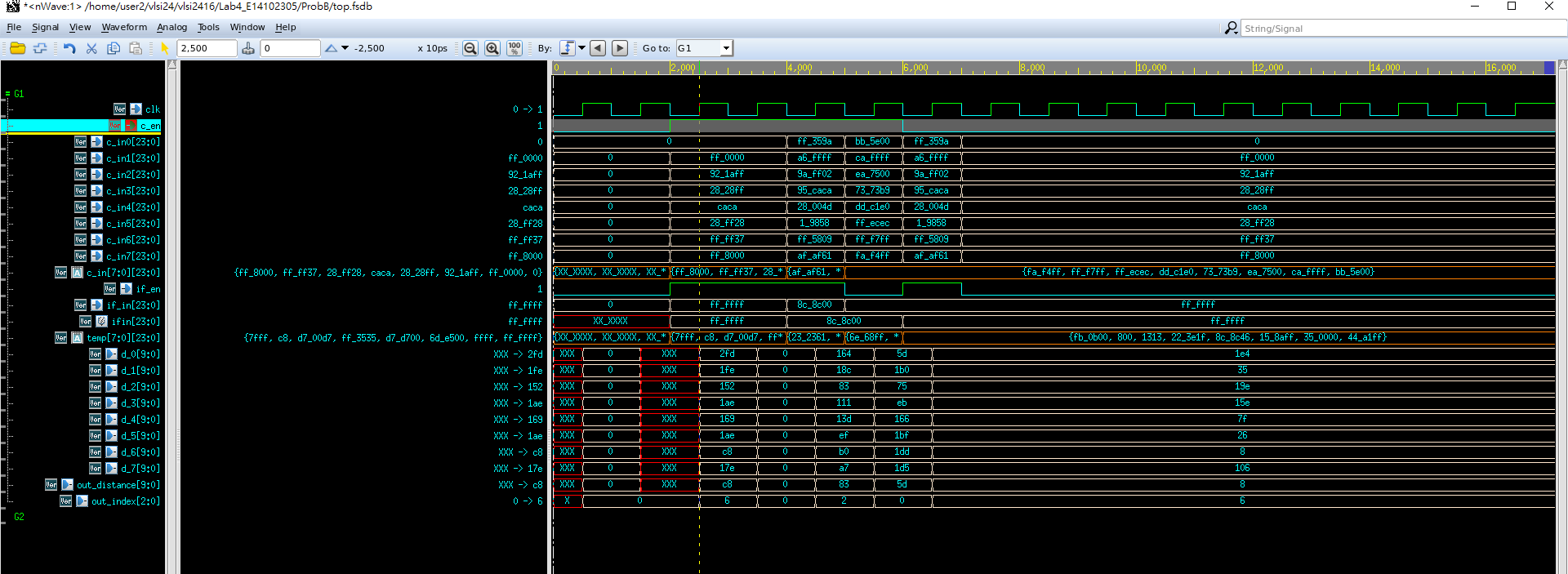
Min:



1. Show the simulation result on the terminal.

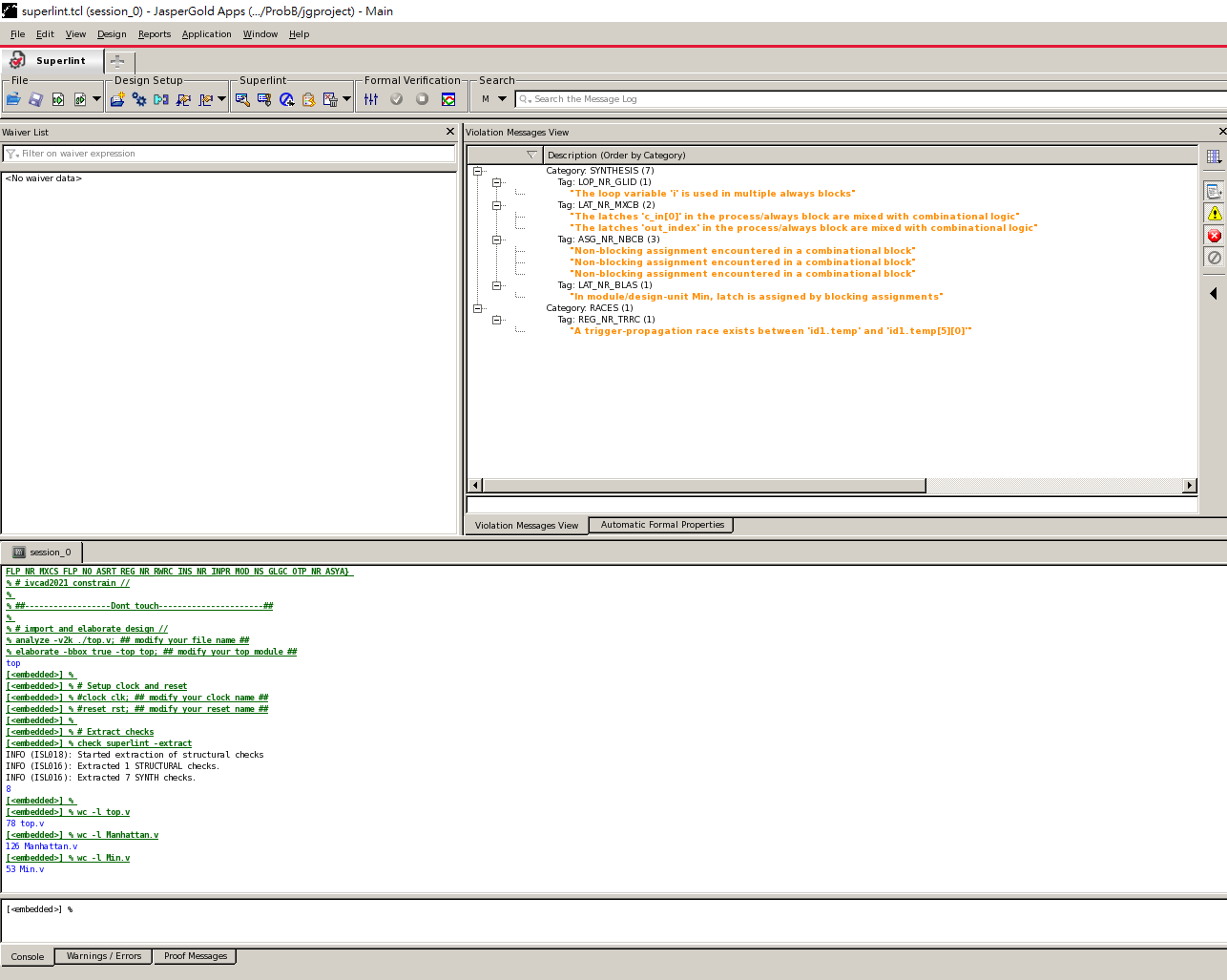


1. Show waveforms to explain that your design works correctly.



我們已第一題來說，當在c\_en升起，會將每個c\_in的值存入自製暫存器，而input\_feature也是如此，且在他們值有變化時temp就會去計算他們之間的最小路徑的3個part(RGB)並存在temp裡，然後會在時脈正源時，將temp的RGB相加存入個別的d裡，並且送入min裡判斷最小值是誰，最後將最小值送回去output\_distance裡，並且判斷他是哪個C\_in。

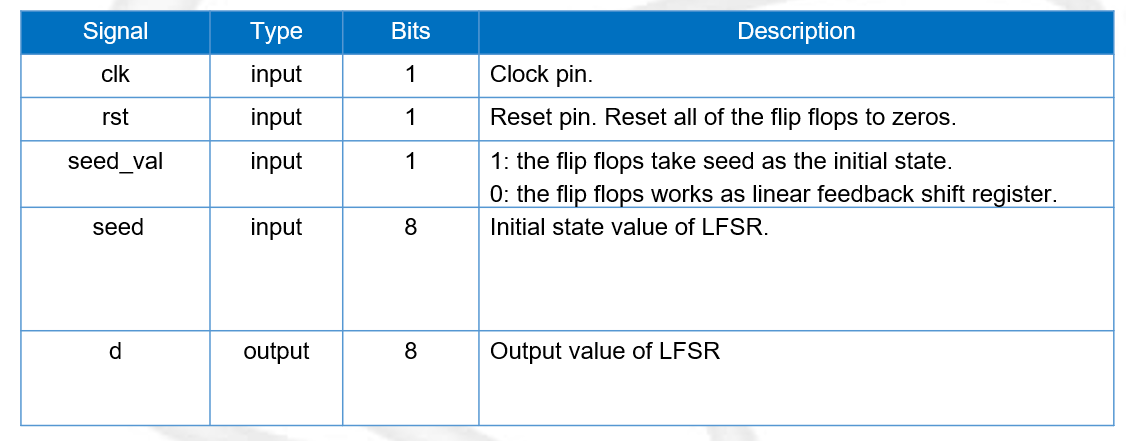
1. Show SuperLint coverage



1-8/78+126+53 = 96.89%

Prob C: LFSR

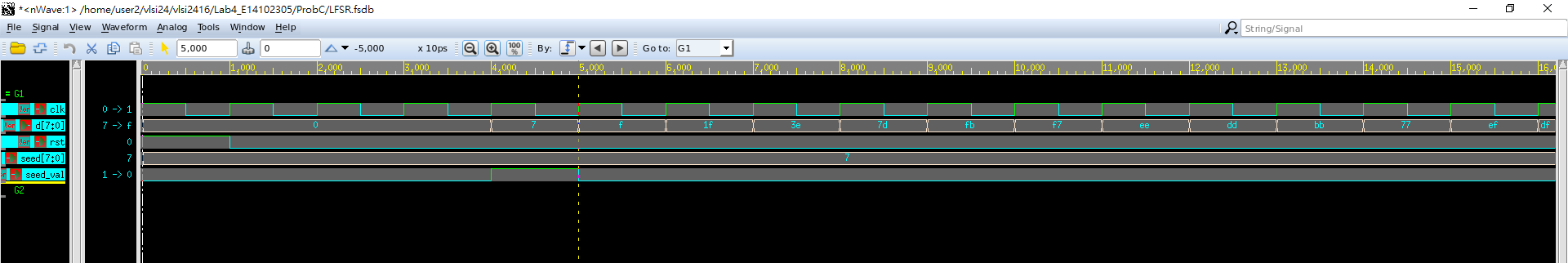
1. Please design an 8-bit-LFSR, with the given feedback function in the LAB4 slide.
2. Port list



1. Feedback function

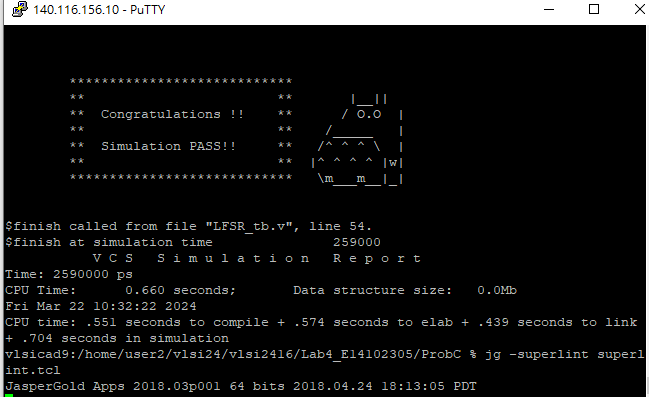
***d[0] = ( d[7] ^ d[5] ) ^ ( d[4] ^ d[2] )***

1. Show waveforms to explain that your LFSR module works correctly.

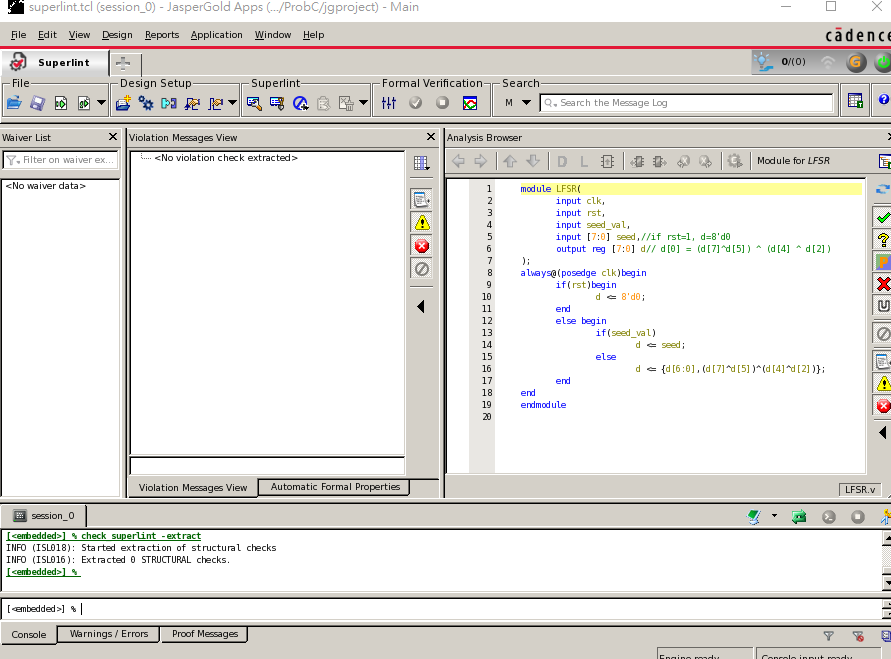


在seed\_val=1時，會將output d存入seed值故為7，在下一個時脈正源，因為seed\_val=0，故開始線性回饋，起始7為8’b00000111，經過線性F🡪d[0] = (0^0)^(0^1)🡪0^1🡪1，故會變成8’b00001111即為0f。

1. Show the simulation result on the terminal.



1. Show SuperLint coverage



100%

At last, please write the lesson you learned from Lab4

我覺得學到了關於sequential的寫法，且更了解暫存器的運作，還有non-blocking與blocking的區別，還有for迴圈的運用會使得程式較為簡化。

老話一句，好課一生推。

Appendix A : Commands we will use to check your homework

