RGB-to-VGA 1.0 IP Core User Guide

Revised April 23, 2015; Author Elod Gyorgy

1 Overview

This user guide describes the Digilent RGB-to-VGA Intellectual Property. This IP accepts a Xilinx vid_io input and outputs an independently customizable color depth, properly blanked RGB pixel bus to connect to a VGA DAC. On Digilent boards the outputs directly connect to the on-board resistor ladder that serves as VGA DAC. The supported color depth varies between boards and the IP should be configured to match it.

2 Performance

The IP itself does not include timing constrains. PixelClk is still expected to be period-constrained from outside.

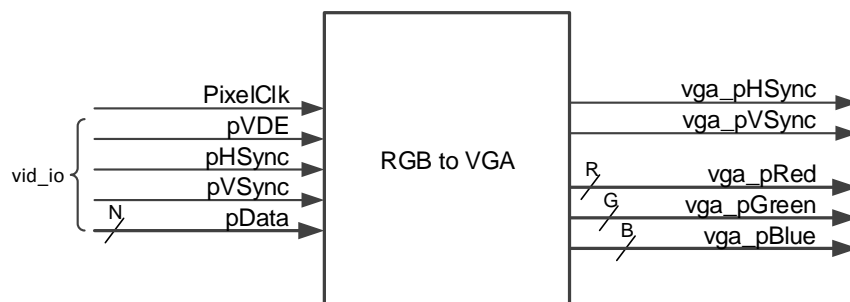| IP quick facts	
Supported device families	Zynq®-7000, 7 series
Supported user interfaces	Xilinx: vid_io
Provided with core	
Design files	VHDL
Simulation model	VHDL Behavioral
Constraints file	N/A
Software driver	N/A
Tested design flows	
Design entry	Vivado™ Design Suite 2014.4
Synthesis	Vivado Synthesis 2014.4

3 Port descriptions

Figure 1. IP top-level diagram.

The signals of the RGB-to-VGA Core are listed and described in Table 1.

Signal Name	Interface	Signal Type	Init State	Description
PixelClk	-	I	N/A	Pixel clock.
pVDE	vid_io	I	N/A	Video data valid: • 1 = Active video. • 0 = Blanking period.
pHSync	vid_io	I	N/A	Horizontal synchronization video timing signal.
pVSync	vid_io	I	N/A	Vertical synchronization video timing signal.
pData(N-1:0)	vid_io	I	N/A	Packed RGB data.
vga_pRed (R-1:0)	-	O	N/A	Blanked red color data.
vga_pGreen (G-1:0)	-	O	N/A	Blanked green color data.
vga_pBlue (B-1:0)	-	O	N/A	Blanked blue color data.
vga_pHSync	-	O	N/A	Output horizontal sync.
vga_pVSync	-	O	N/A	Output vertical sync.

Table 1. Port descriptions.

4   Designing with the core

4.1   Customization

Provide the width of the input pixel bus and the output pixel buses. The output color depth should match the on-board VGA DAC solution.