Email: harry021633@gmail.com 陳昕佑 Mobile: (+886) 901-020-267

SUMMARY

A system software engineer respecting performance and efficiency are brought by seamless integration between software and hardware. 1+ years of experience in IC verification, platform performance enhancement and memory utilization reduction.

Professional skills

TODO

Professional Experience

Airoha

Hsinchu, Taiwan Feb 2022 - Present

System Software Engineer @ Ethernet SoC team

- FreeRTOS SDK Implementation: Refine the GPIO and I2C driver, eliminating the database to reduce memory usage approximate 10%.
- Linux SDK Implementation: Integrated the I2C and GPIO driver with a standard Linux subsystem, enabling it to utilize Linux-provided APIs. Additionally, I implemented a kernel module ioctl interface to reduce the frequency of user space to kernel space transitions, enhancing the boot-up speed of the program within the SDK 40%.
- SDK Integration: Redesigned and consolidated multiple SDK architectures into a single repository for enhanced maintainability and reduced development complexity. Furthermore, I refine the Makefile and redesign the compilation procedure, improving the compilation speed about 7 times.
- IC Verification: Verify CPU peripherals, including I2C, GPIO, pinmux, CPU Bus.
- Auto Test Development: Verify CPU peripherals, including I2C, GPIO, pinmux, CPU Bus.
- System Level Testing Software Development: Verify CPU peripherals, including I2C, GPIO, pinmux, CPU Bus.

• Side Projects Taipei, Taiwan

- Vector ISA: Research on conventional and modern vector architectures, including Cray vector supercomputers, RISC-V Vector Extension and ARM Scalable Vector Extension.
- Vector Microarchitecture: Design a Cray-like vector core and construct a performance model on it. Evaluate the impact of vector chaining on several processor configurations.
- o Code Optimization for Vector: Research on effective code optimization techniques, such as loop transforms and instruction scheduling, on different vector core configurations.
- Application Profiling and Performance Projection: Extract vectorizable parts of program by using LLVM, including SPEC2017fp and Darknet, and give an estimated evaluation on our vector core.

• Andes Technology Corporation

Hsinchu, Taiwan

Summer Intern @ RD/Architecture team

Jul 2018 - Aug 2018

- Branch Prediction Performance Modeling: Collaborating with VLSI team, evaluate the impact of different branch prediction policies on the high-end Andes RISC-V processor.
- o Benchmark automatic flow development: Develop an automatic benchmarking suite, including SPEC2006 and EEMBC, for performance analysis of Andes processors.

EDUCATION

• National Cheng Kung University

Tainan, Taiwan

Master of Mechanical Engineering

Sep. 2020 - Aug. 2022

• National Central University

Taoyuan, Taiwan

Bachelor of Mechanical Engineering

Sep. 2016 – Jun. 2020