

Lab Report - 01

Course No: 206

Course Title: Digital Logic Design

Submitted To:

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Dept: CSE

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Section: 07

Dept: CSE

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	nilization					,	. On prote	
		belove :	0	1.	T.	Experien	worf Equipm	un:
@ OR_	,		eutpu			Logic p		
@ AND		Garle	Not	P	able c	Logic 3		
3 NOT	Gate	4				V		
9 NOR	Gate	,			Ã:X	A	A =X	
3 NAND	Gate	•	A		1	0		
6 x-0R					0			
(₹) X-NO	e Ga	te. Table Touth a Di	le for R Gat	es				
		~~~	input	U	ulpul			
X= A+	B	A	G		X			

inp	input					
A	G	× .				
0	0	0				
D	1	1				
7	0	4				
1	7	1				

A X= A+B

(P)

# Truth table for AND Grates

X = A.B

Impl	ν <b>1</b>	1 2 2
A	B	X=A.B
0	0	0
0	1	0
1	O	0
1	1	1
		outp

 $A = A \cdot B$ 

Truth table of NOT Gates

X= A

A	X2Ā
Ô	1
1	D

DNOR GATE

SX-0R

Gate

A

Conference

Con

## Truth Table for NOR Grates

3

X >	A+B

A	В	AIB	AIB	14	A	1	A+B XOFHE
0	0	0	2	>_	B		AD 1-4101 =
0	1	1	0	1.	1		
1	0	4	0	)	A -	10	x = A+B
1	1	01	0		В		

## Truth dable for NAND GATE

X2 A.B

	A	B	AIB	AIB	0		AB X
	0.	٥	. 0	1	· B		
4:9	0	1	0	1	d	П	38.00
1_	1	0	0	1	A	0	To A.B
٥.	i âi.	1	Ŀ	0	8-	Ü	
	0	U	1	4.0	0	1_	
1	0	1	U	U	1	L.	

RUPBET AB

# Truth Pable for x-or Gate

X= ADB, and = AB+AB

						_	
⊕B, AIA	A	В	A	B	AB	AB	AB+AB
B+AB	0	0	1	= 10	0	D	0
	0	1	1	10	1	0	1
8 1. 1. 1. 1. B	1	O A	0	15	0	1	1
	1	. 10	0	00	0	0	D

JUAN GHAIN mot

Truth Pable for X-NOR Gates

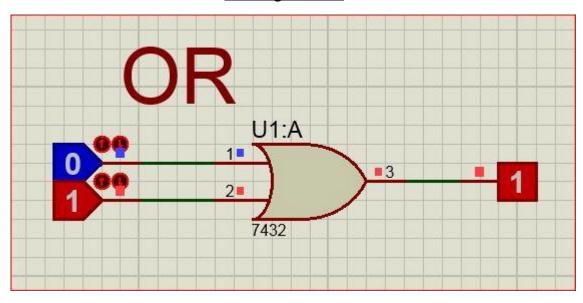
AIB AIB

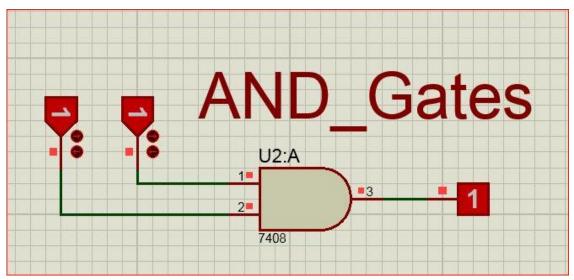
> AB+AB

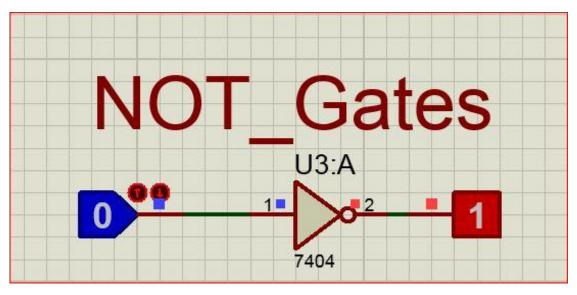
			-0			
A	B	Ā	B	AB	ĀĒ	ABTĀB
0	0	1	1	D	1	_1
D	19	10	0	0	Oc.	0
1	0	0	1	0	0	0
1	1	0	0	1	0	1

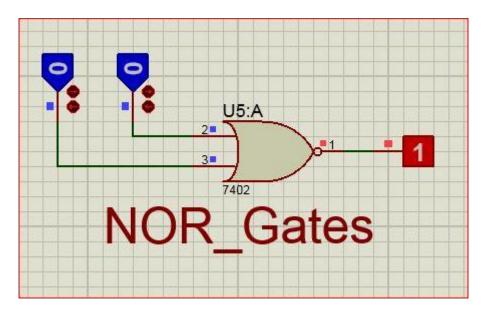
AB+AB

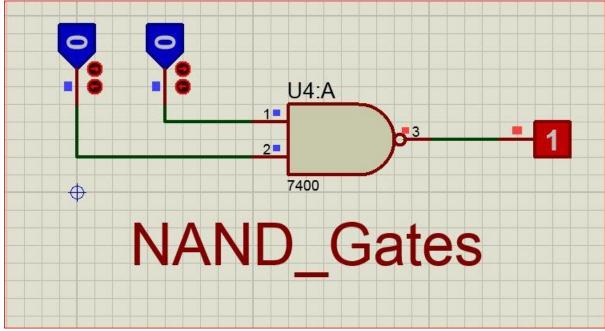
#### All Logic Gates

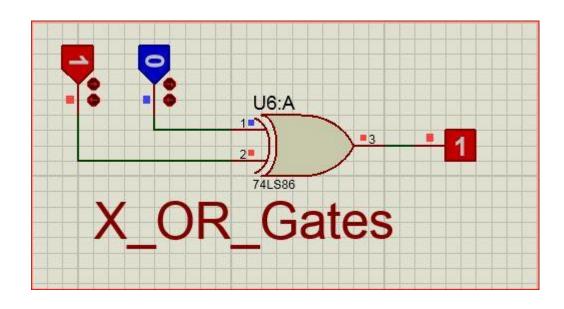


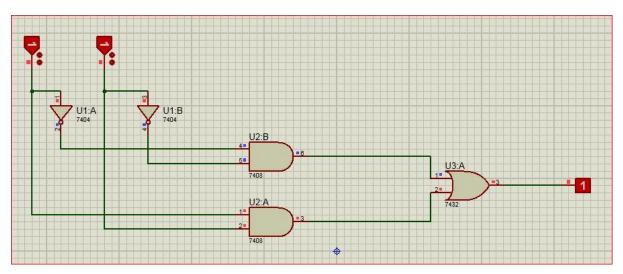












Picture of X_NOR Gates

#### Conclusion +

in profess software.

2: we have understand the digit simulation of any cineuit in the software.

3. we have verified the truth table for each imput/output combination.

4. we repeated the process for all others logic gates.

Thereits in proteus softwere.

5. Lasty we understant the MIND on 15th.