

Lab Report - 04

Course No: 206

Course Title: Digital Logic Design

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Section: 07

Dept: CSE

Lab Report > 04

Name of Experiment:

Construct and test various adders and sub-tractor cincuit.

Equipment :

1: 2 imput AND Grates

2. 3 input AND Godes

3. 2 input or Godes

4. 4 input OR Grates

5. X-OR Gates

6. Not Gate

7.3 input OR Gate

Description:
Am adders is a digital circuit that perstroms addition of numbers. In many computeres and others kinds of processons adderes are used in the arithmetic Logic units on other signed numbers representations require mone logic around the basic adders. There are two types of adders; Of Half adders

(2) full adder.

Half adders: The half adders cineuit has food imputs (ne and) which add two imput digit and generates a carry and a sum.

Hulf adders cincuit doesn't considers

the previous carry.

full adders;— The full adders cineuif has theree imput (n, y and 2) where z is a prievous coory and (n andy) are a literal. The full adders generate a carry and sum.

Halso considers the prievous coory.

This is the truth table of Half adders

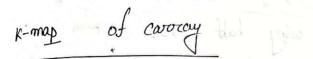
		- 1	
20	7	C	5
0	0	0	0
D	1	D	1
1	0	0	1
1	1	1	0

This is the touth table of Full adders

	-	and the same			
2	y	2	C	5	
0	0	0	0	0	
0	0	1	0	1	
0.0	100	0	0	1	
0	1	1	1	0	
T	0	0	0	1	
1	0	In	10	0	
1 2	rollint	0	11	0	
1	1	1	1	1	
				-	

ves of addies; Whalf added

moses I do many computer as



147	2			M. 500	0 + 7 K20 + 3 Lynn : 5 Lynn
24	00	OT	11	10	0
D	٥	0	1	0	= = 100 + 100 + 2 (dy + .
1	0	I	1	1	
	7		- 7		= 2'(RD2) + 2 (RD2)' =

C= xx +xy+yz out indmod (30) 00

k-map of Sum

5= 26y'z + 2/42' + 2y'z' + 2yz

[(R+12) 20 + 26, x. + P.

75 (4+4) + WS

1, Rock 7 Bro + 2 Bro + Bro

cincuit of full adders using half adders;

Equipment

- 1 2 AND Gate
- 2 2 xOR Gate
- 3 OR Gate

i) is input no hade

T - 5

Part, 2 Bio +, 7 By + 2 Ryo =

Simplification Full adders using half adders

1.12550150361

= my (1+2) + my z + my 2

= my + my 2 + xy'z

2 my + 2 (x'y + my) bornon who admin and assess

= my + 2 (n) [combine two half adders]

Last address. and I wonder make with two

inputs and -two outputs, this cinewit is well to subtract two outputs to this cinewit is well as subtracts out the cond is to bornow oute to confer states at half subtractor.

Tull Subtract Sut

the full subtraction is used into subtract three 1-bit numbers 11, 13, and e, which are animosed customakind and bournous wregarding the full subtraction has three input states and two autputs states subtraction

Full adder using Basic Gades

Equipment :

i) 3 imput AND Gate

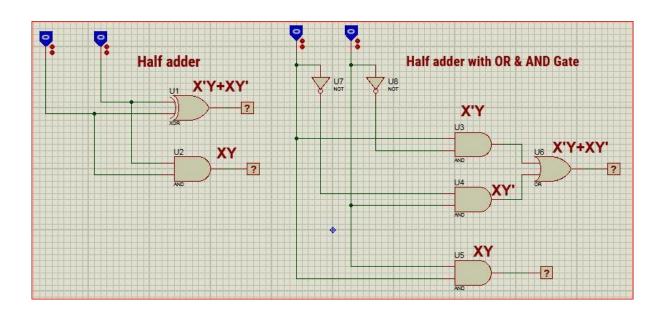
ii) 3 input or Grafe

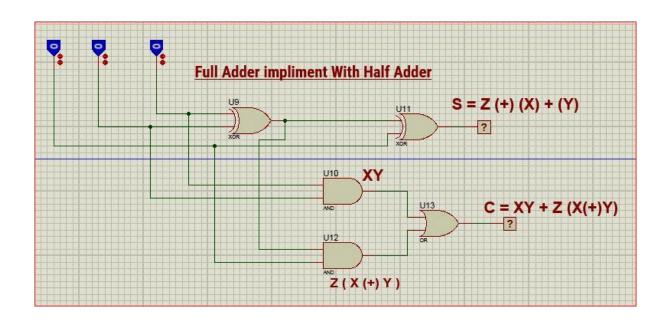
ii) 4 input of Grade

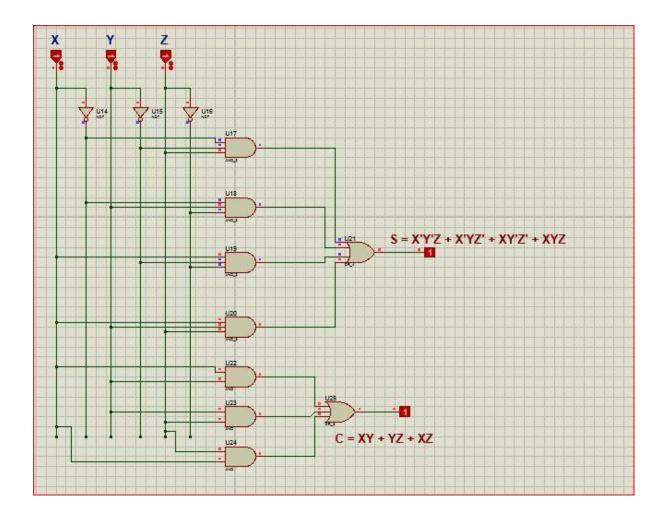
in) 2 input AND Grates

CP Sado

v) Not Gate (5010) (1)5 my+ Intyz 50 2/2+2/22/+ my/2/+my/2







Full Adder Using Basic Gates

Balt 2 (211) B.

Description:

A subtraction logic circuit for colculating the difference between two numbers. The minuena and the numbers to be subtracted.

Jange: Any con: rigines] (R. Dr.) 2 + R.

Half Subtructor:

The half subtraction is also a building block for subtracting two binary numbers. It has two imputs and two outputs, this cineuit is used to subtract two single bit binary numbers A and B. The D= sub and B= bonnow ource.

Two Dutput states of half subtractor.

Full Subtraction:

The full subtraction is used to subtract three 1-bit numbers A, B, and C, which are minused subtrahind and bonnous respectivly. The full subtraction has three input states and two outputs State. Sub := 0 and bonnow = B

Int Subling tun

Half Subtractors

				Ching	0 20	U		
А	B	Bn	D	L	1	1		
0	0	0	D		1	i		Ü
0	1	1	1	1-14	1. 4			- 0
7	0	0	1		0.	U	ú	L
1	1	0	0		0-	1	- 0	1

Half Subtractor implement with Kmap of Bonnous

20	0	. 1
0	0	国
긔	0	0

B= AB

losoli - (a,A)

C - Previous Bannows

0 0 1 1

Half Subtraction implement with k-map of (1)

D= 78 + AB = ABB

Full Subfracton

A	B	C	Bm	D	_
0	D	D	0	0.	70.
0	0	1	1	1,4	d ord
0	. 1	0	10	1	
0	1	L	1	O.	1
1	0	0	0	1	U
1	0	. 1	0	0	0.0
1	T	0	O'	0	1 1 1 1
C. Ha	1 40	L	1	1.4	In company

(A,B) -> litoral

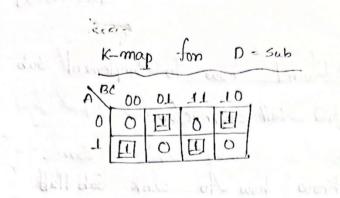
000

€ → Anerious Bonnous

K-map for Borrow

0 0	ann-	4	11100	Loron
A	DD	OT	11	70
Ō	0	I	1	工
1	0	0	1	O

Bormow = A'C + BC + A'B AA + BA & G

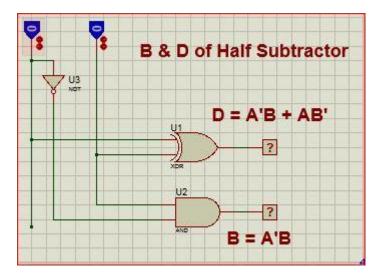


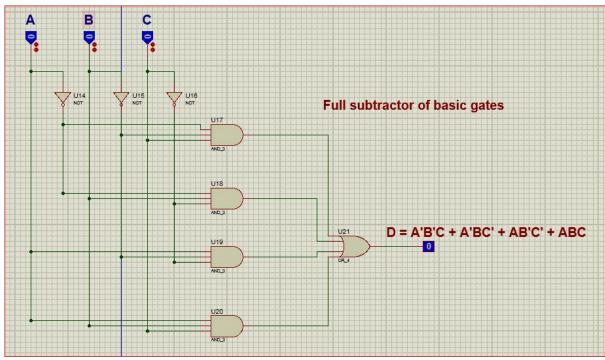
D = A'B'C + A'BC' + AB'C' + ABC

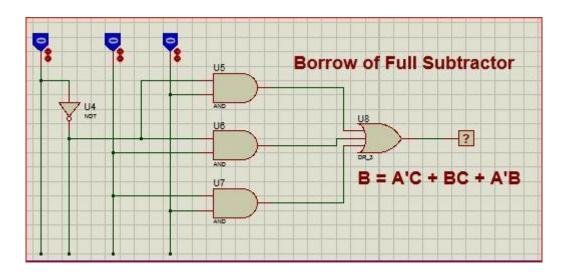
which adds two throng chipts tojethere.

we also learn't that submarks is used for a confice of combinational circuit which is used to predomine the predominant which is used to predomine the submarks of the folia.

5. he also know the implements light addoc, but added, and state subtraction and toll subtraction dealing in produce de bullmans.







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Conclusion;

- 1. We have leaven't how to implement sub tractor and Full Subtractor.
- 2. we also know how to work Half adders and how to get full adders from thou half adders.
- 3. We leavon't that, Half adders is an adders which adds two binary digits togethers, viesulting in a sum and carray.
- 4. we also learn't Half subtraction is another type of combinational cincuit which is wed to personal subtraction at two bits.
- 5. We also know, How to implements Half adder, full adders, and Half subtraction and full subtraction desing in protues software.