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ECE445
May 8, 2025

Lab Notebook

Week 1:

- 2/3/2025: Brainstorm project ideas
    - Looked into embedded system projects which are applicable to grading rubric
    - EDIT: Finalized project brainstorming to Portable Offline Translator because of the open-source AI models available
- 2/11/2025: First TA meeting
    - Received outline of class, objectives, and deliverables for the week

Week 2:

- 2/18/2025: Project Proposal
    - Feedback:
        - Software heavy project, very complex, room for failure if software is not delivered
        - Discussion of possible on board peripherals: Power Subsystem, I/O circuits, MCU, and header pins
- 2/19/2025: Look at PCB Examples and Part selection/availability:
    - Found possible Audio Amplifier IC (MAX98357), SMD microphone (SPH0645), and other parts of the MCU boot circuitry.
    - Found example circuit of STM32 MCU
        - Take note of common boot/interrupt interfaces along with programming interface (UART, USBC, etc)
    - Common PCB flow in Kicad
        - Schematic design
        - symbol addition of ICs not on KiCad library (Preferences->Manage Symbol Libraries
        - Hierarchical Pages for larger PCB designs (ctrl+h)
    - Begin adding power components
        - Added symbol for LM317-SOT
- 2/22/2025: Begin Schematic for PCB
    - Calculated resistor values for LDO circuits (followed typical application example of datasheet)

8.2 Typical Application

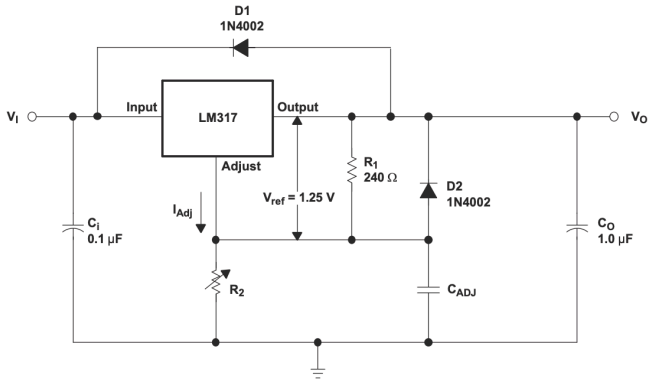
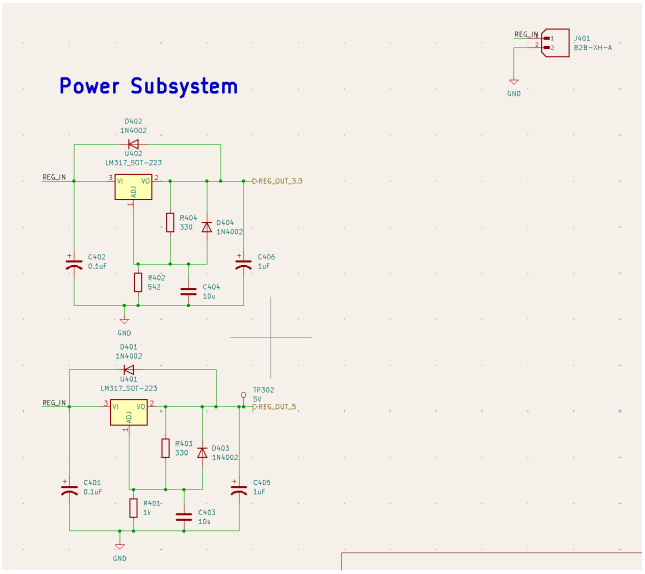


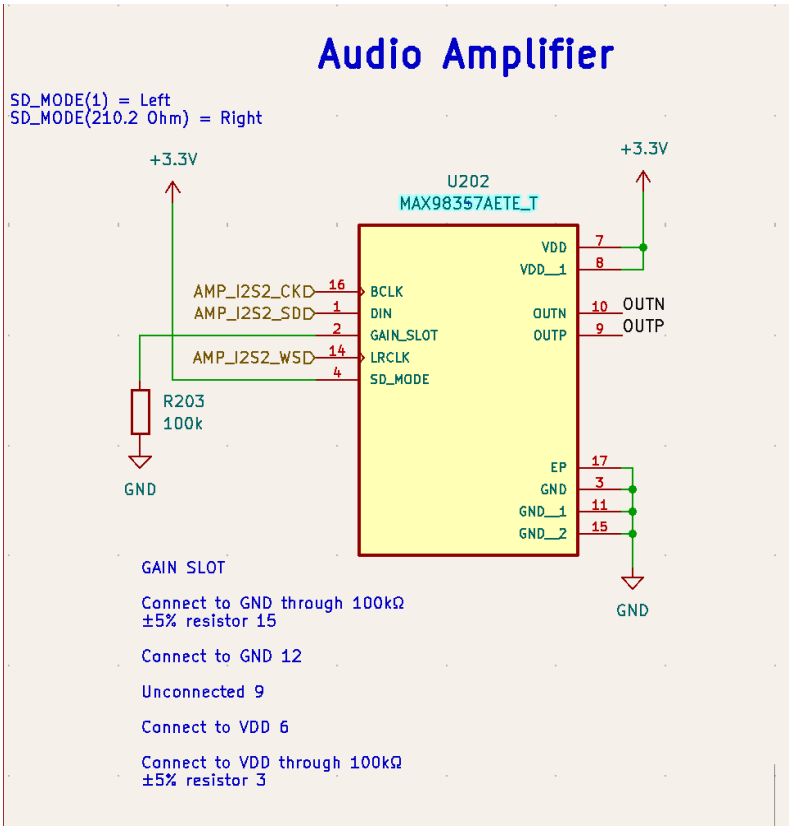
Figure 8-1. Adjustable Voltage Regulator

8.2.1 Design Requirements

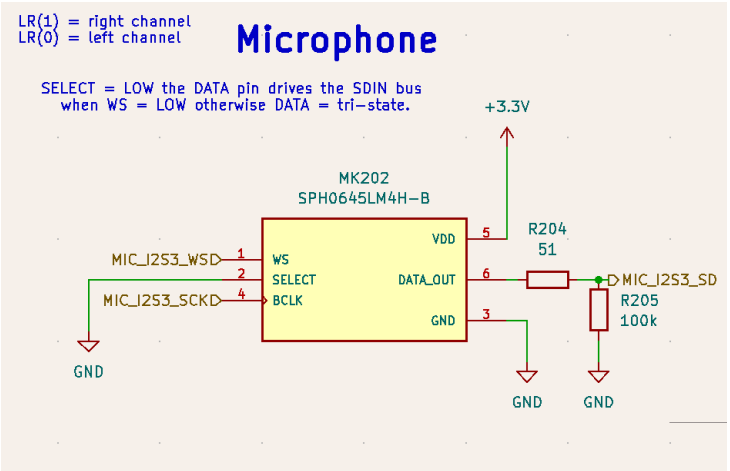
- R1 and R2 are required to set the output voltage.
- Use C_{ADJ} to improve ripple rejection. C_{ADJ} prevents amplification of the ripple when the output voltage is adjusted higher. The impact of C_{ADJ} on the ripple rejection performance is captured in the *Electrical Characteristics* table.
- C_i is recommended, particularly if the regulator is not in close proximity to the power-supply filter capacitors. A 0.1µF or 1µF ceramic or tantalum capacitor provides sufficient bypassing for most applications, especially when adjustment and output capacitors are used.
- C_O improves transient response, but is not needed for stability.
- Protection diode D2 is recommended if C_{ADJ} is used. The diode provides a low-impedance discharge path to prevent the capacitor from discharging into the output of the regulator.
- Protection diode D1 is recommended if C_O is used. The diode provides a low-impedance discharge path to prevent the capacitor from discharging into the output of the regulator.



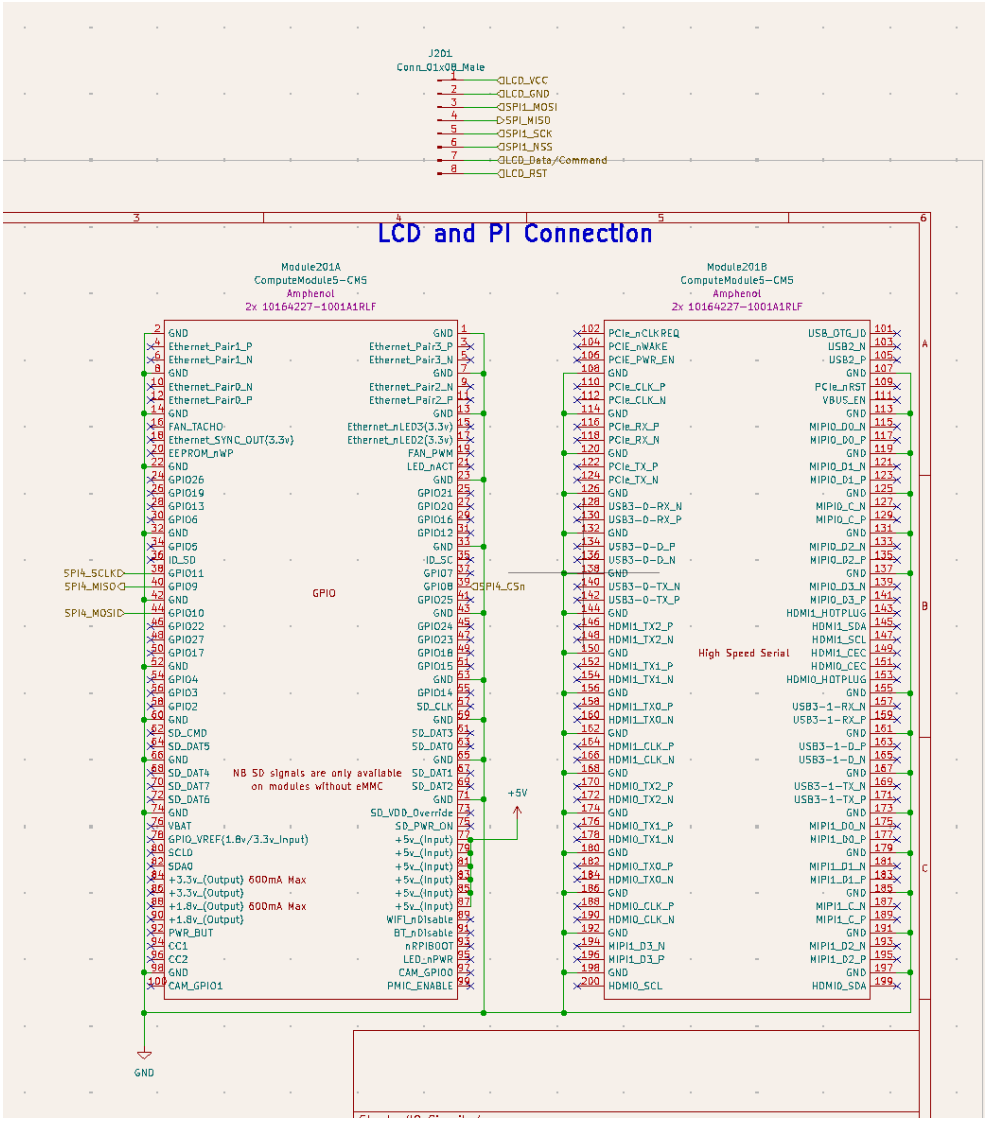
- 2/23/2025: Work on other subsystems of the PCB
    - Worked on I/O portion of the PCB
        - Audio Amplifier
            - Look into different configuration and necessary circuitry



- Microphone:
  - Configured Microphone to operate in mono mode

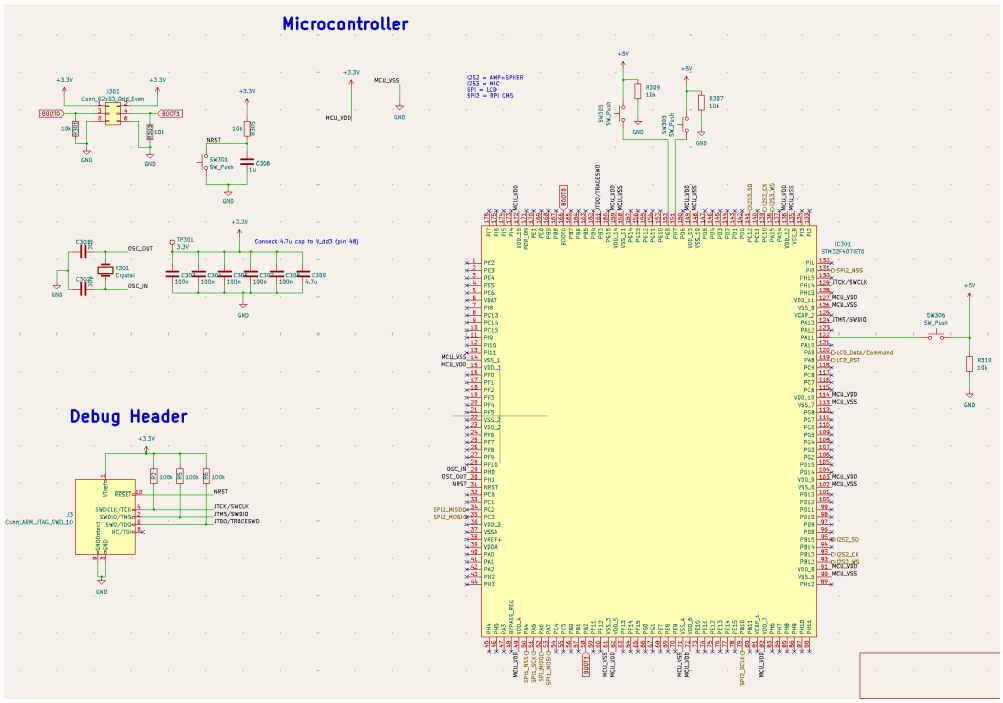


- LCD/PI Connection:
  - Decided to use Header Pins for LCD module; will connect directly on the board and be powered by on-board power supply.
  - Found footprint of CM5 connector
    - Created hierarchical references for inter-subsystem signals (CM5 SPI, LCD SPI, and I2S signals.

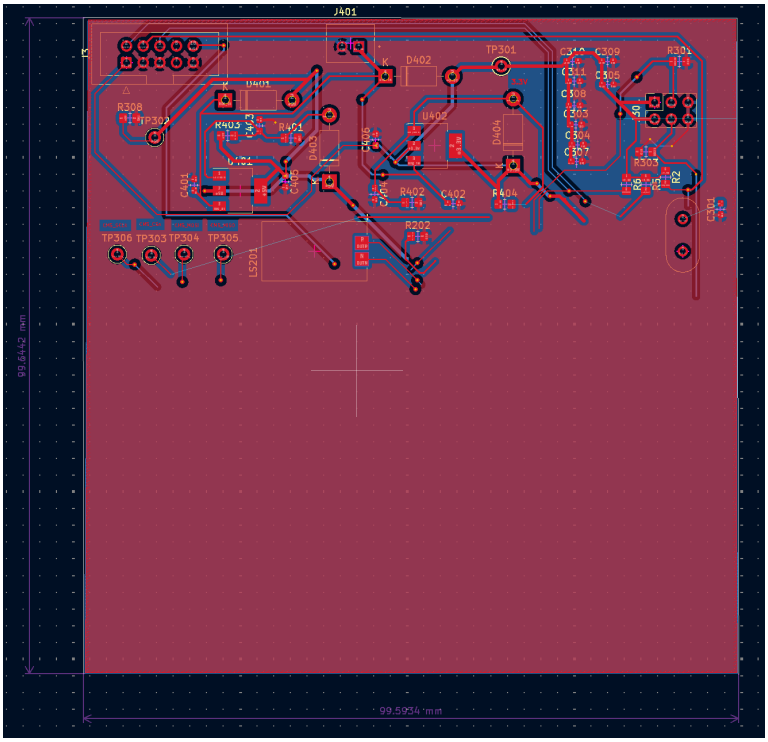


Week 3: Finalize Schematic for PCB review

- 2/24/2025: Finalize Schematic Portion of PCB
  - Worked on MCU subsystem
    - Decided to use USB-C receptacle for programming, debug header, and buttons for boot mode configuration



- 2/26/2025: Begin PCB Portion and Routing
    - 100cm x 100cm constraint for PCB dimensions
    - Looked into common practices such as keeping high-speed components together, power and other high thermal generating components together, and PCB traces never being 90 degrees.



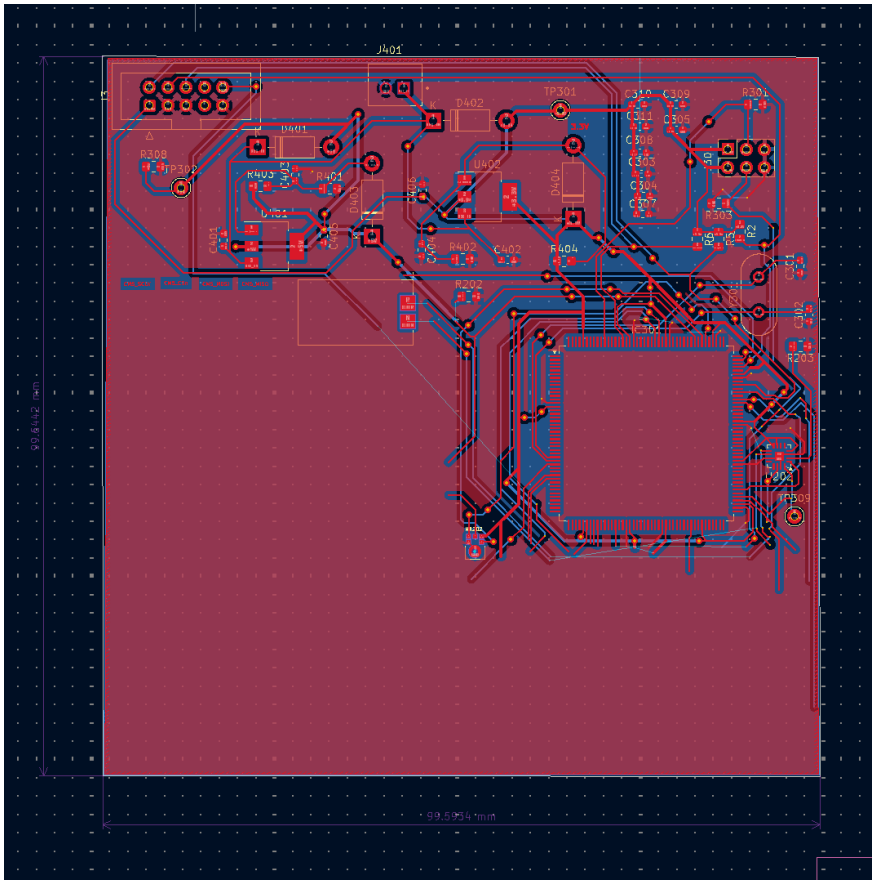
- 2/28/2025: Attend PCB Review
    - Make sure the double check DRC rules, TA instructed to tie power nets to a power signal
    - Looked into optimizing packages that could be easier to solder
        - TA recommended SMT devices which could be easily soldered with a stencil

Week 4: PCB Work and Documents

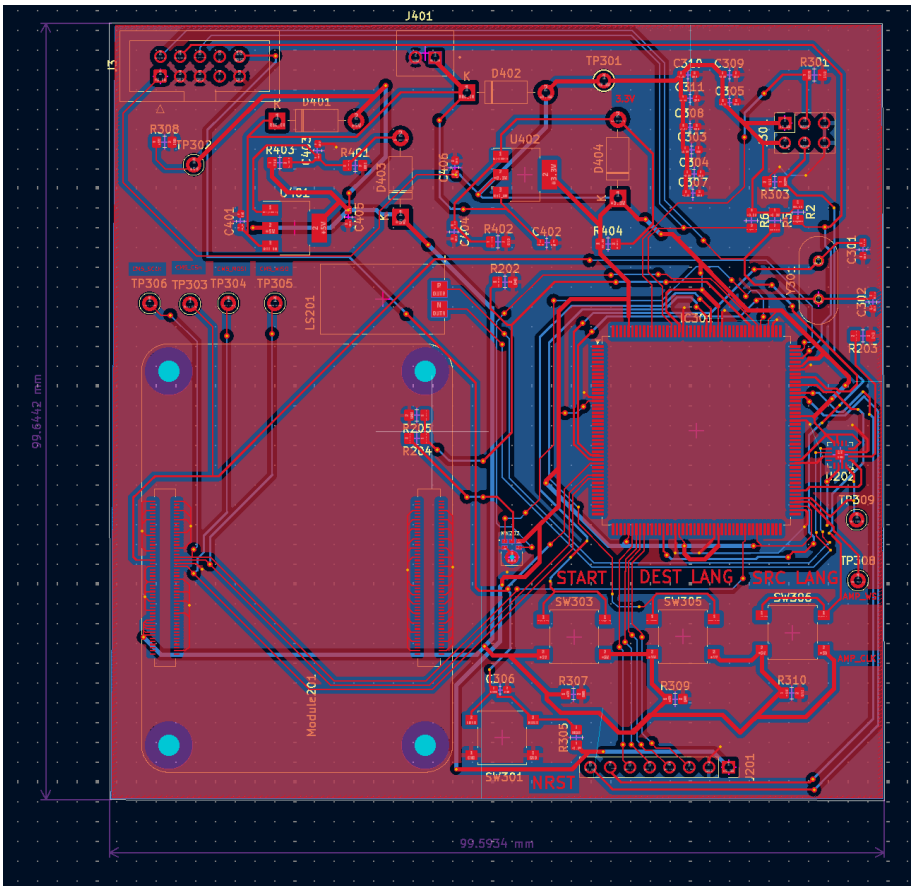
- 3/3/2025: Continue working on PCB for ROUND 2 orders
    - Finalized component selection for first iteration of the PCB
- 3/4/2025: Second TA meeting
    - Instructed to work on Team Evaluation form and Design Document

Week 5: Attend Breadboard Demo and Work on PCB

- 3/11/2025: Breadboard Demo
    - Need to include more interactive menu for LCD
    - Start brainstorming ways to optimize the memory utilization since the BB demo was on MAC SoC and CM5 has much less computing power.
    - PCB work:
        - Continued routing signals around the MCU

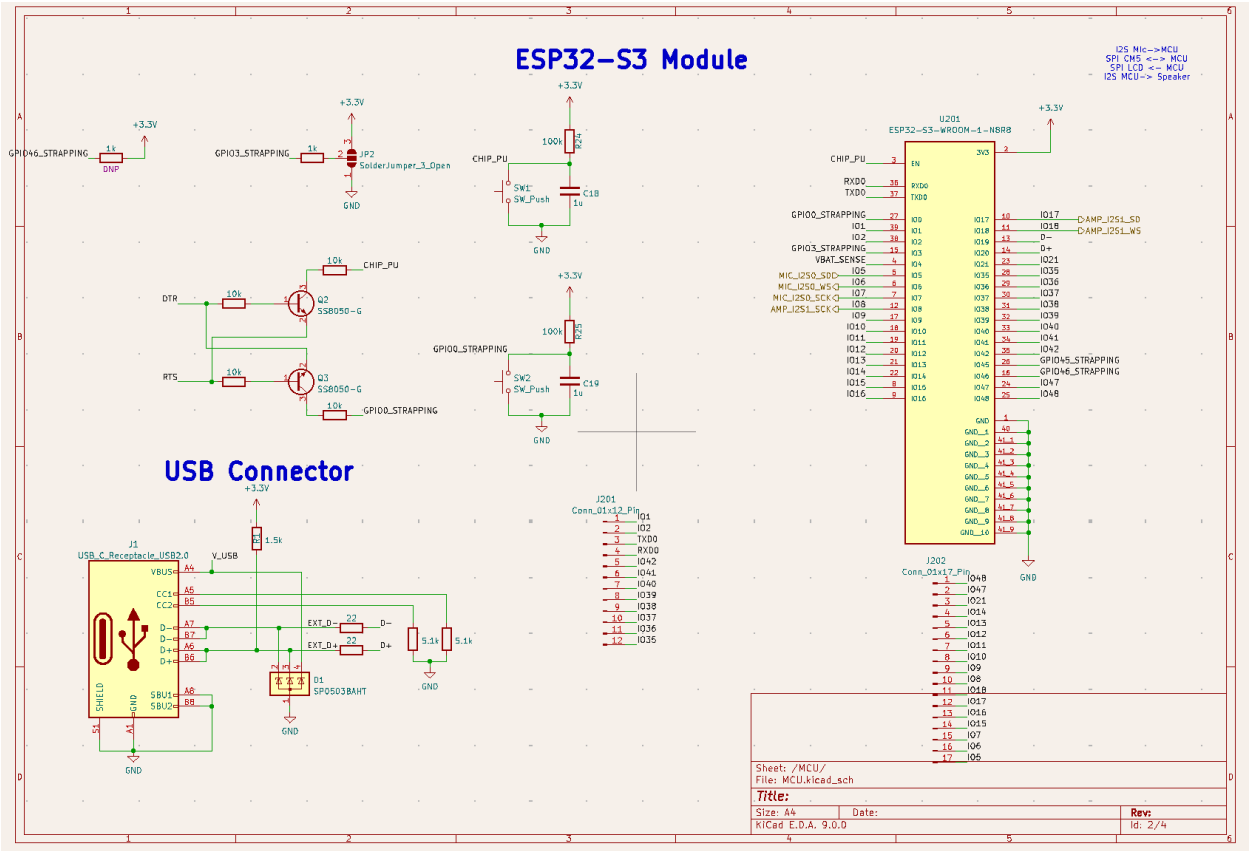


- 3/16/2025: Finalize PCB Design



Week 6: Preparing for PCB round 3

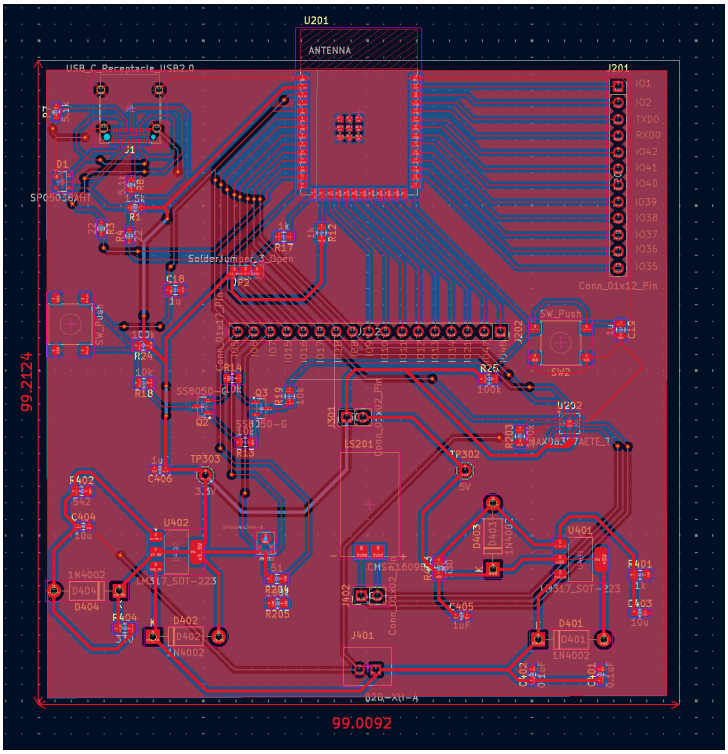
- 3/24/2025: Post Spring Break Meeting
    - Chi instructed us to create another rendition of the project
        - Use ESP32 for less pins on the PCB and try to focus on the bare minimum of the PCB rubric to ensure points
        - Create a PCB with just header-pins for the ESP32 and on board power supply
- 3/25/2025: Being Making New Schematic with ESP32
    - Looked at the ESP32 design example on course wiki



- FInal rendition includes USB connector along with buttons for boot mode configuration

Week 7: Finalize PCB schematic and PCB editor and send for 4th round PCB orders

- New onboard I/O circuitry will only include SMT devices for the audio devices
  - Decided to do so to minimize the room for error and only including the MCU, power subsystem, and devices/receptacles for programming.
- ESP32 will still use a USB-C receptacle for programming, similar to the STM32 rendition of the PCB.
- PCB will no longer mount CM5 on board (to save room) and will use header-pins and jumper wires for interfacing with the CM5



Week 8: Assembling PCB design

- 4/15/2025: Attend Weekly Meeting
    - Got advice for PCB assembly and what needs to be done by the end of the week (Team Contract Assessment, Demonstration, and Presentation)
- 4/16/2025: Begin SMT soldering of components
    - Utilized heat gun and solder paste to solder all SMT devices
    - Outlined the ESP32 using a stencil and soldered with heat gun
- 4/17/2025: Solder through-hole components using soldering iron

Week 9: PCB debugging

- 4/21/2025: Verification of Subsystems
    - Debugged power subsystem and verified with DMM and benchtop power supply
    - Verified USB-C programming by probing test points and analyzing VBAT and other essential signals of the receptacle
    - Further verified current draw and load and line regulation of power subsystem when connected to the breadboard components.

      3.3V Channel:
        - Target Voltage: 3.3V
        - Measured Voltage: 3.24V (±0.01V tolerance)
        - Load Current: Up to 500mA (measured at full load)
        - Ripple Voltage: < 20mV (measured at full load)

5V Channel:

- Target Voltage: 5.0V
- Measured Voltage: 5.13V (±0.02V tolerance)
- Load Current: Up to 1A (measured at full load)
- Ripple Voltage: < 30mV (measured at full load)