

### Summary

Mic500 200k Termination	
Signal Path Setup	🍼 PASSED
Stepped Frequency Sweep MIC 500	▲ FAILED
Mic 2k 200k termination	
Signal Path Setup	PASSED
Stepped Frequency Sweep MIC 2K	▲ FAILED
Mic 2k 15dB PAD 200k termination	
Signal Path Setup	PASSED
Stepped Frequency Sweep 15dB PAD	🛕 FAILED
Line Gain -10 200kTermination	
Signal Path Setup	PASSED
Stepped Frequency Sweep -10	▲ FAILED
Line Gain -10 600 Termination	
Signal Path Setup	PASSED
Level and Gain -10	PASSED
Line Gain +5 200kTermination	
Signal Path Setup	PASSED
Stepped Frequency Sweep +5	▲ FAILED
Line Gain +5 600 Termination	
Signal Path Setup	PASSED
Level and Gain +5	▲ FAILED
Line Gain -5 600 Termination	
Signal Path Setup	PASSED
Level and Gain -5	▲ FAILED
Line Gain 0 600 Termination	
Signal Path Setup	PASSED
Level and Gain 0	▲ FAILED
Line Gain +10 600 Termination	
Signal Path Setup	PASSED
Level and Gain +10	▲ FAILED
Line Gain +10 200k Termination Level Hi	
Signal Path Setup	PASSED
Noise Recorder (RMS) CW	▲ FAILED
Line Gain +10 200k Termination Level Low	
Signal Path Setup	PASSED
Noise Recorder (RMS) CCW	▲ FAILED
Hi Z Gain -10 2.2M 200k Termination	

Signal Path Setup	♥ PASSED
Level and Gain 2.2M	▲ FAILED
Hi Z Gain -10 47k 200k Termination	
Signal Path Setup	PASSED
Level and Gain 47K	🛕 FAILED
Dummy Signal Path For Report	
Signal Path Setup	♥ PASSED
Sequence Result:	
Sequence Result:	

5/8/2023 1:59 PM Page 2 of 54



Mic500 200k Termination : Signal Path Setup

Output Connector: Analog Balanced

Channels: 1

Source Impedance: 100 ohm
AG52 Generator Option: Installed
Output EQ: None

Input Connector: Analog Balanced

Channels: 1

Channel: Ch1

Termination: 200 kohm

Input Bandwidth: AC (<10 Hz) - 90k (192 kHz SR)

Device Delay: 0.000 s
Input EQ: None

References

100.0 mVrms dBr G: dBm (Output Power): 600.0 ohm W(watts) (Output Power): 8.000 ohm Shared Frequency Reference: 1.00000 kHz dBrA: 1.000 Vrms dBrB: 1.000 Vrms dBrA Offset: 0.000 dB dBrB Offset: 0.000 dB dBSPL1: 10.00 mVrms dBSPL2: 10.00 mVrms dBSPL1 Calibrator Level: 94.000 dBSPL dBSPL2 Calibrator Level: 94.000 dBSPL dBm (Input Power): 600.0 ohm

• DCX

W(watts) (Input Power):

DC Output 1: 0.000 V

DC Output 1: Off

DC Output 2: 0.000 V

DC Output 2: Off

Port A (hex): 00

Port B (hex): 00

5/8/2023 1:59 PM Page 3 of 54



Port C (hex): 00
Port D (hex): 00

Clocks

Output Rate: Track Output SR

Sync Out Level: 3.300 V
Sync Out Polarity: Normal
Timebase Reference: Internal
Jitter: Disabled

Triggers

Source: Off
Input Logic Level: 3.300 V
Edge: Rising

Mic500 200k Termination: Verify Connections

Waveform: Sine

Generator Level: -42.300 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/8/2023 1:57:09.349 PM)

Ch1 286.4 mVrms

Gain (5/8/2023 1:57:09.349 PM)

Ch1 33.659 dB

THD+N Ratio (5/8/2023 1:57:09.349 PM)

Ch1 ---- %

Frequency (5/8/2023 1:57:09.349 PM)

Ch1 ---- Hz

5/8/2023 1:59 PM Page 4 of 54



Mic500 200k Termination: Stepped Frequency Sweep MIC 500

Generator Level: -42.300 dBu
DC Offset: 0.000 V
EQ: None

Start Frequency: 20.0000 kHz
Stop Frequency: 20.0000 Hz
Step Type: Logarithmic

Number of Points: 10

Weighting Filter: Signal Path

High-pass Filter: 20 Hz Phase Ref Channel: Ch1

Measured 1 5/8/2023 1:57:14 PM

#### RMS Level (5/8/2023 1:57:14.723 PM)

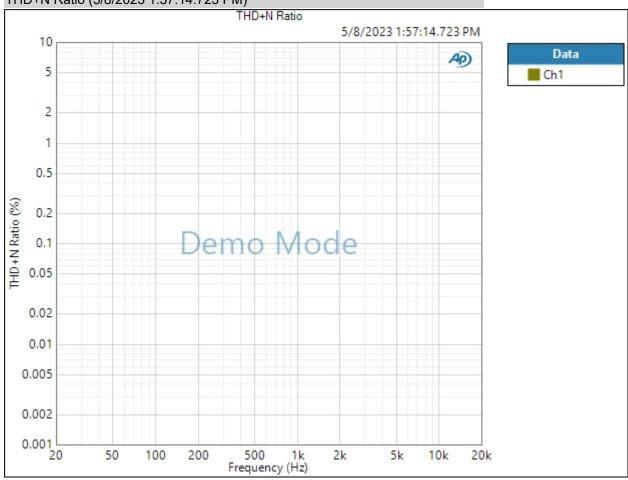


5/8/2023 1:59 PM Page 5 of 54



Result: A FAILED

THD+N Ratio (5/8/2023 1:57:14.723 PM)



Result: V PASSED

THD Ratio (5/8/2023 1:57:14.723 PM)

5/8/2023 1:59 PM Page 6 of 54



Result: 🛕 FAILED

5/8/2023 1:59 PM Page 7 of 54



Mic 2k 200k termination : Signal Path Setup

Output Connector: Analog Balanced

1 Channels:

100 ohm Source Impedance: AG52 Generator Option: Installed Output EQ: None

Input Connector: Analog Balanced

Channels: 1

Channel: Ch1

Termination: 200 kohm

AC (<10 Hz) - 90k (192 kHz SR) Input Bandwidth:

Device Delay: 0.000 sInput EQ: None

References

dBr G: 100.0 mVrms dBm (Output Power): 600.0 ohm W(watts) (Output Power): 8.000 ohm Shared Frequency Reference: 1.00000 kHz dBrA: 1.000 Vrms dBrB: 1.000 Vrms dBrA Offset: 0.000 dB dBrB Offset: 0.000 dB dBSPL1: 10.00 mVrms dBSPL2: 10.00 mVrms dBSPL1 Calibrator Level: 94.000 dBSPL dBSPL2 Calibrator Level: 94.000 dBSPL dBm (Input Power): 600.0 ohm W(watts) (Input Power):

• DCX

DC Output 1: 0.000 V Off DC Output 1: DC Output 2: 0.000 V DC Output 2: Off Port A (hex): 00 00 Port B (hex): 00 Port C (hex):

5/8/2023 1:59 PM Page 8 of 54



Port D (hex): 00

• Clocks

Output Rate: Track Output SR

Sync Out Level: 3.300 V
Sync Out Polarity: Normal
Timebase Reference: Internal
Jitter: Disabled

• Triggers

Source: Off

Input Logic Level: 3.300 V Edge: Rising

Mic 2k 200k termination: Verify Connections

Waveform: Sine

Generator Level: -42.300 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/8/2023 1:57:19.436 PM)

Ch1 288.3 mVrms

Gain (5/8/2023 1:57:19.436 PM)

Ch1 33.717 dB

THD+N Ratio (5/8/2023 1:57:19.436 PM)

Ch1 ---- %

Frequency (5/8/2023 1:57:19.436 PM)

Ch1 ---- Hz

5/8/2023 1:59 PM Page 9 of 54



Mic 2k 200k termination : Stepped Frequency Sweep MIC 2K

Generator Level: -42.300 dBu
DC Offset: 0.000 V
EQ: None

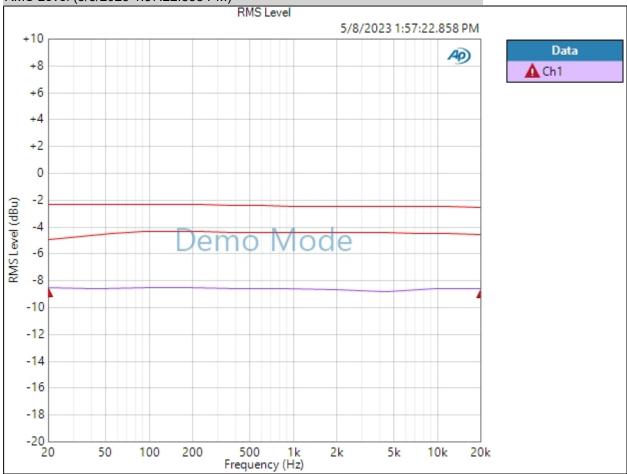
Start Frequency: 20.0000 kHz
Stop Frequency: 20.0000 Hz
Step Type: Logarithmic

Number of Points: 10

Weighting Filter: Signal Path
High-pass Filter: 20 Hz
Phase Ref Channel: Ch1

Measured 1 5/8/2023 1:57:22 PM

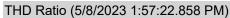
#### RMS Level (5/8/2023 1:57:22.858 PM)

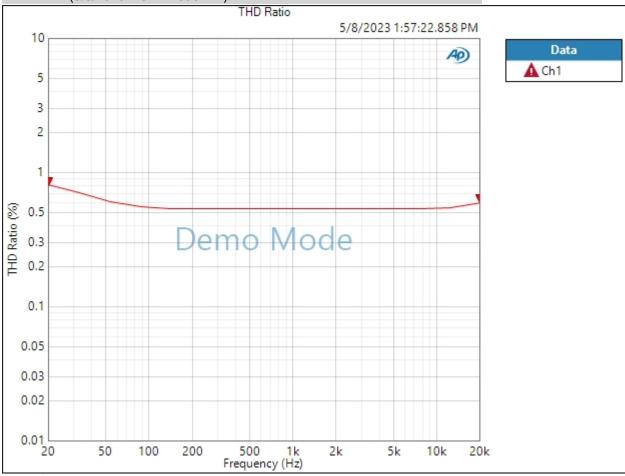


5/8/2023 1:59 PM Page 10 of 54



Result: A FAILED





Ch1 A Failed Upper Limit

Result: A FAILED

5/8/2023 1:59 PM Page 11 of 54



Mic 2k 15dB PAD 200k termination : Signal Path Setup
Output Connector:

Analog Balanced

Channels: 1

Source Impedance: 100 ohm
AG52 Generator Option: Installed
Output EQ: None

Input Connector: Analog Balanced

Channels: 1

Channel: Ch1

Termination: 200 kohm

Input Bandwidth: AC (<10 Hz) - 90k (192 kHz SR)

Device Delay: 0.000 s
Input EQ: None

References

dBr G: 100.0 mVrms dBm (Output Power): 600.0 ohm W(watts) (Output Power): 8.000 ohm Shared Frequency Reference: 1.00000 kHz dBrA: 1.000 Vrms dBrB: 1.000 Vrms dBrA Offset: 0.000 dB dBrB Offset: 0.000 dB dBSPL1: 10.00 mVrms dBSPL2: 10.00 mVrms dBSPL1 Calibrator Level: 94.000 dBSPL dBSPL2 Calibrator Level: 94.000 dBSPL dBm (Input Power): 600.0 ohm W(watts) (Input Power): 8.000 ohm

• DCX

DC Output 1: 0.000 V
DC Output 1: Off

DC Output 2: 0.000 V

DC Output 2: Off

Port A (hex): 00

Port B (hex): 00

Port C (hex): 00

5/8/2023 1:59 PM Page 12 of 54



Port D (hex): 00

• Clocks

Output Rate: Track Output SR

Sync Out Level: 3.300 V
Sync Out Polarity: Normal
Timebase Reference: Internal
Jitter: Disabled

• Triggers

Source: Off

Input Logic Level: 3.300 V Edge: Rising

Mic 2k 15dB PAD 200k termination: Verify Connections

Waveform: Sine

Generator Level: -42.300 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/8/2023 1:57:27.596 PM)

Ch1 293.8 mVrms

Gain (5/8/2023 1:57:27.596 PM)

Ch1 33.880 dB

THD+N Ratio (5/8/2023 1:57:27.596 PM)

Ch1 ---- %

Frequency (5/8/2023 1:57:27.596 PM)

Ch1 ---- Hz

5/8/2023 1:59 PM Page 13 of 54



#### Mic 2k 15dB PAD 200k termination : Stepped Frequency Sweep 15dB PAD

Generator Level: -42.000 dBu
DC Offset: 0.000 V
EQ: None

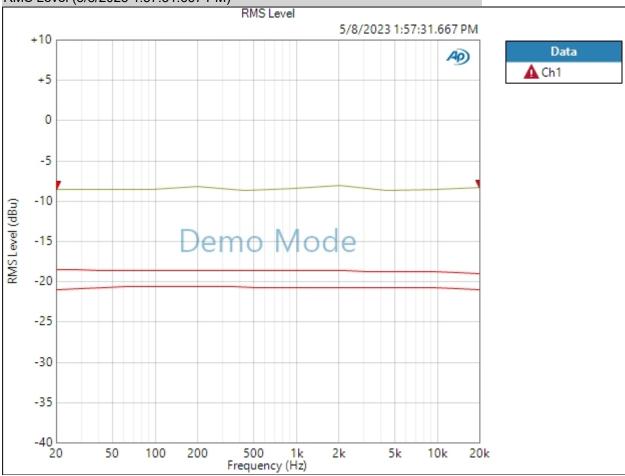
Start Frequency: 20.0000 kHz
Stop Frequency: 20.0000 Hz
Step Type: Logarithmic

Number of Points: 10

Weighting Filter: Signal Path
High-pass Filter: 20 Hz
Phase Ref Channel: Ch1

Measured 1 5/8/2023 1:57:31 PM

#### RMS Level (5/8/2023 1:57:31.667 PM)

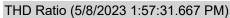


Ch1 A Failed Upper Limit

5/8/2023 1:59 PM Page 14 of 54



Result: A FAILED





Ch1 A Failed Upper Limit

Result: A FAILED

5/8/2023 1:59 PM Page 15 of 54



Line Gain -10 200kTermination : Signal Path Setup

Output Connector: Analog Balanced

Channels: 1

Source Impedance: 100 ohm
AG52 Generator Option: Installed
Output EQ: None

Input Connector: Analog Balanced

Channels: 1

Channel: Ch1

Termination: 200 kohm

Input Bandwidth: AC (<10 Hz) - 90k (192 kHz SR)

Device Delay: 0.000 s
Input EQ: None

References

dBr G: 100.0 mVrms dBm (Output Power): 600.0 ohm W(watts) (Output Power): 8.000 ohm Shared Frequency Reference: 1.00000 kHz dBrA: 1.000 Vrms dBrB: 1.000 Vrms dBrA Offset: 0.000 dB dBrB Offset: 0.000 dB dBSPL1: 10.00 mVrms dBSPL2: 10.00 mVrms dBSPL1 Calibrator Level: 94.000 dBSPL dBSPL2 Calibrator Level: 94.000 dBSPL dBm (Input Power): 600.0 ohm

• DCX

W(watts) (Input Power):

DC Output 1: 0.000 V

DC Output 1: Off

DC Output 2: 0.000 V

DC Output 2: Off

Port A (hex): 00

Port B (hex): 00

Port C (hex): 00

5/8/2023 1:59 PM Page 16 of 54



Port D (hex): 00

• Clocks

Output Rate: Track Output SR

Sync Out Level: 3.300 V
Sync Out Polarity: Normal
Timebase Reference: Internal
Jitter: Disabled

• Triggers

Source: Off

Input Logic Level: 3.300 V Edge: Rising

Line Gain -10 200kTermination: Verify Connections

Waveform: Sine

Generator Level: 0.000 dBu

DC Offset: 0.000 V

Frequency: 1.00000 kHz

RMS Level (5/8/2023 1:57:36.542 PM)

Ch1 282.5 mVrms

Gain (5/8/2023 1:57:36.542 PM)

Ch1 -8.761 dB

THD+N Ratio (5/8/2023 1:57:36.542 PM)

Ch1 ---- %

Frequency (5/8/2023 1:57:36.542 PM)

Ch1 ---- Hz

5/8/2023 1:59 PM Page 17 of 54



#### Line Gain -10 200kTermination: Stepped Frequency Sweep -10

Generator Level: 0.000 dBu
DC Offset: 0.000 V
EQ: None

Start Frequency: 20.0000 kHz
Stop Frequency: 20.0000 Hz
Step Type: Logarithmic

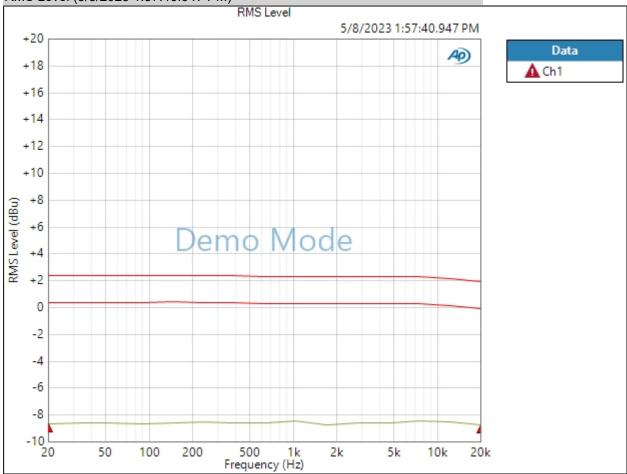
Number of Points: 15

Weighting Filter: Signal Path High-pass Filter: 20 Hz

Phase Ref Channel: Ch1

Measured 1 5/8/2023 1:57:40 PM

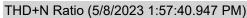
#### RMS Level (5/8/2023 1:57:40.947 PM)

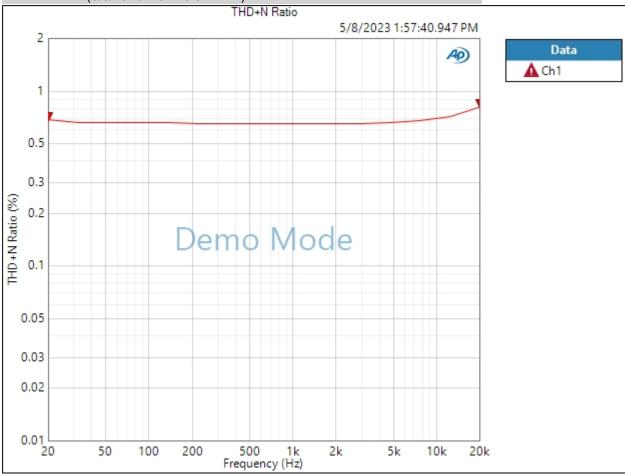


5/8/2023 1:59 PM Page 18 of 54



Result: A FAILED





Ch1 A Failed Upper Limit

Result: A FAILED

5/8/2023 1:59 PM Page 19 of 54



Line Gain -10 600 Termination : Signal Path Setup

Output Connector: Analog Balanced

Channels: 1

Source Impedance: 100 ohm
AG52 Generator Option: Installed
Output EQ: None

Input Connector: Analog Balanced

Channels: 1

Channel: Ch1

Termination: 600 ohm

Input Bandwidth: AC (<10 Hz) - 90k (192 kHz SR)

Device Delay: 0.000 s
Input EQ: None

References

dBr G: 100.0 mVrms dBm (Output Power): 600.0 ohm W(watts) (Output Power): 8.000 ohm Shared Frequency Reference: 1.00000 kHz dBrA: 1.000 Vrms dBrB: 1.000 Vrms dBrA Offset: 0.000 dB dBrB Offset: 0.000 dB dBSPL1: 10.00 mVrms dBSPL2: 10.00 mVrms dBSPL1 Calibrator Level: 94.000 dBSPL dBSPL2 Calibrator Level: 94.000 dBSPL dBm (Input Power): 600.0 ohm

• DCX

W(watts) (Input Power):

DC Output 1: 0.000 V

DC Output 1: Off

DC Output 2: 0.000 V

DC Output 2: Off

Port A (hex): 00

Port B (hex): 00

Port C (hex): 00

5/8/2023 1:59 PM Page 20 of 54



Port D (hex): 00

• Clocks

Output Rate: Track Output SR

Sync Out Level: 3.300 V
Sync Out Polarity: Normal
Timebase Reference: Internal
Jitter: Disabled

• Triggers

Source: Off

Input Logic Level: 3.300 V Edge: Rising

Line Gain -10 600 Termination: Verify Connections

Waveform: Sine

Generator Level: -10.000 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/8/2023 1:57:45.986 PM)

Ch1 283.3 mVrms

Gain (5/8/2023 1:57:45.986 PM)

Ch1 1.263 dB

THD+N Ratio (5/8/2023 1:57:45.986 PM)

Ch1 ---- %

Frequency (5/8/2023 1:57:45.986 PM)

Ch1 ---- Hz

5/8/2023 1:59 PM Page 21 of 54



Line Gain -10 600 Termination: Level and Gain -10

Waveform: Sine

Generator Level: -10.000 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/8/2023 1:57:48.561 PM)

Channel Lower Limit Value Upper Limit
Ch1 -11.500 dBu -8.599 dBu -8.500 dBu

5/8/2023 1:59 PM Page 22 of 54

**9** 



Line Gain +5 200kTermination : Signal Path Setup

Output Connector: Analog Balanced

Channels: 1

Source Impedance: 100 ohm
AG52 Generator Option: Installed
Output EQ: None

Input Connector: Analog Balanced

Channels: 1

Channel: Ch1

Termination: 200 kohm

Input Bandwidth: AC (<10 Hz) - 90k (192 kHz SR)

Device Delay: 0.000 s
Input EQ: None

References

dBr G: 100.0 mVrms dBm (Output Power): 600.0 ohm W(watts) (Output Power): 8.000 ohm Shared Frequency Reference: 1.00000 kHz dBrA: 1.000 Vrms dBrB: 1.000 Vrms dBrA Offset: 0.000 dB dBrB Offset: 0.000 dB dBSPL1: 10.00 mVrms dBSPL2: 10.00 mVrms dBSPL1 Calibrator Level: 94.000 dBSPL dBSPL2 Calibrator Level: 94.000 dBSPL dBm (Input Power): 600.0 ohm W(watts) (Input Power): 8.000 ohm

• DCX

DC Output 1: 0.000 V

DC Output 1: Off

DC Output 2: 0.000 V

DC Output 2: Off

Port A (hex): 00

Port B (hex): 00

Port C (hex): 00

5/8/2023 1:59 PM Page 23 of 54



Port D (hex): 00

• Clocks

Output Rate: Track Output SR

Sync Out Level: 3.300 V
Sync Out Polarity: Normal
Timebase Reference: Internal
Jitter: Disabled

• Triggers

Source: Off

Input Logic Level: 3.300 V Edge: Rising

Line Gain +5 200kTermination : Verify Connections

Waveform: Sine

Generator Level: 0.000 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/8/2023 1:57:53.460 PM)

Ch1 286.2 mVrms

Gain (5/8/2023 1:57:53.460 PM)

Ch1 -8.648 dB

THD+N Ratio (5/8/2023 1:57:53.460 PM)

Ch1 ---- %

Frequency (5/8/2023 1:57:53.460 PM)

Ch1 ---- Hz

5/8/2023 1:59 PM Page 24 of 54



#### Line Gain +5 200kTermination : Stepped Frequency Sweep +5

Generator Level: 0.000 dBu
DC Offset: 0.000 V
EQ: None

Start Frequency: 20.0000 kHz
Stop Frequency: 20.0000 Hz
Step Type: Logarithmic

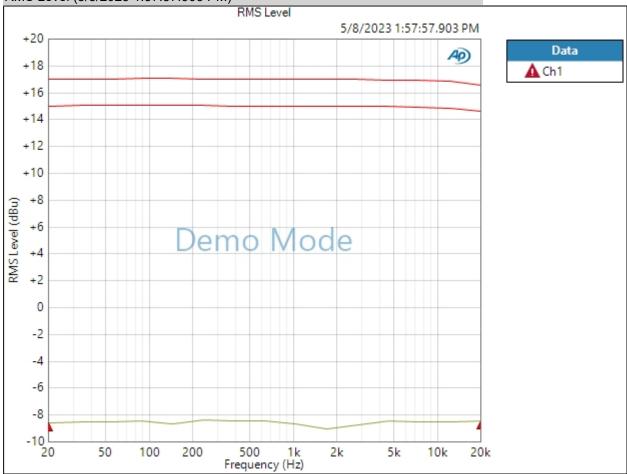
Number of Points: 15

Weighting Filter: Signal Path

High-pass Filter: 20 Hz Phase Ref Channel: Ch1

Measured 1 5/8/2023 1:57:57 PM

#### RMS Level (5/8/2023 1:57:57.903 PM)

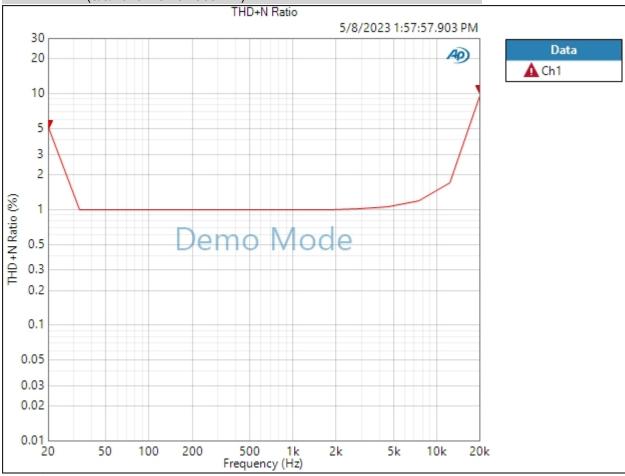


5/8/2023 1:59 PM Page 25 of 54



Result: A FAILED





Ch1 A Failed Upper Limit

Result: A FAILED

5/8/2023 1:59 PM Page 26 of 54



Line Gain +5 600 Termination : Signal Path Setup

Output Connector: Analog Balanced

Channels: 1

Source Impedance: 100 ohm
AG52 Generator Option: Installed
Output EQ: None

Input Connector: Analog Balanced

Channels: 1

Channel: Ch1

Termination: 600 ohm

Input Bandwidth: AC (<10 Hz) - 90k (192 kHz SR)

Device Delay: 0.000 s
Input EQ: None

References

dBr G: 100.0 mVrms dBm (Output Power): 600.0 ohm W(watts) (Output Power): 8.000 ohm Shared Frequency Reference: 1.00000 kHz dBrA: 1.000 Vrms dBrB: 1.000 Vrms dBrA Offset: 0.000 dB dBrB Offset: 0.000 dB dBSPL1: 10.00 mVrms dBSPL2: 10.00 mVrms dBSPL1 Calibrator Level: 94.000 dBSPL dBSPL2 Calibrator Level: 94.000 dBSPL dBm (Input Power): 600.0 ohm

• DCX

W(watts) (Input Power):

DC Output 1: 0.000 V

DC Output 1: Off

DC Output 2: 0.000 V

DC Output 2: Off

Port A (hex): 00

Port B (hex): 00

Port C (hex): 00

5/8/2023 1:59 PM Page 27 of 54



Port D (hex): 00

• Clocks

Output Rate: Track Output SR

Sync Out Level: 3.300 V
Sync Out Polarity: Normal
Timebase Reference: Internal
Jitter: Disabled

• Triggers

Source: Off

Input Logic Level: 3.300 V Edge: Rising

Line Gain +5 600 Termination: Verify Connections

Waveform: Sine

Generator Level: -10.000 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/8/2023 1:58:03.083 PM)

Ch1 282.0 mVrms

Gain (5/8/2023 1:58:03.083 PM)

Ch1 1.224 dB

THD+N Ratio (5/8/2023 1:58:03.083 PM)

Ch1 ---- %

Frequency (5/8/2023 1:58:03.083 PM)

Ch1 ---- Hz

5/8/2023 1:59 PM Page 28 of 54



Line Gain +5 600 Termination: Level and Gain +5

Waveform: Sine

Generator Level: -10.000 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/8/2023 1:58:05.722 PM)

Channel Lower Limit Value Upper Limit
Ch1 +3.500 dBu -8.578 dBu +6.500 dBu

Result: A FAILED

5/8/2023 1:59 PM Page 29 of 54



Line Gain -5 600 Termination : Signal Path Setup

Output Connector: Analog Balanced

Channels: 1

Source Impedance: 100 ohm
AG52 Generator Option: Installed
Output EQ: None

Input Connector: Analog Balanced

Channels: 1

Channel: Ch1

Termination: 600 ohm

Input Bandwidth: AC (<10 Hz) - 90k (192 kHz SR)

Device Delay: 0.000 s
Input EQ: None

References

dBr G: 100.0 mVrms dBm (Output Power): 600.0 ohm W(watts) (Output Power): 8.000 ohm Shared Frequency Reference: 1.00000 kHz dBrA: 1.000 Vrms dBrB: 1.000 Vrms dBrA Offset: 0.000 dB dBrB Offset: 0.000 dB dBSPL1: 10.00 mVrms dBSPL2: 10.00 mVrms dBSPL1 Calibrator Level: 94.000 dBSPL dBSPL2 Calibrator Level: 94.000 dBSPL dBm (Input Power): 600.0 ohm

• DCX

W(watts) (Input Power):

DC Output 1: 0.000 V

DC Output 1: Off

DC Output 2: 0.000 V

DC Output 2: Off

Port A (hex): 00

Port B (hex): 00

Port C (hex): 00

5/8/2023 1:59 PM Page 30 of 54



Port D (hex): 00

• Clocks

Output Rate: Track Output SR

Sync Out Level: 3.300 V
Sync Out Polarity: Normal
Timebase Reference: Internal
Jitter: Disabled

• Triggers

Source: Off

Input Logic Level: 3.300 V Edge: Rising

Line Gain -5 600 Termination: Verify Connections

Waveform: Sine

Generator Level: -10.000 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/8/2023 1:58:10.857 PM)

Ch1 292.6 mVrms

Gain (5/8/2023 1:58:10.857 PM)

Ch1 1.544 dB

THD+N Ratio (5/8/2023 1:58:10.857 PM)

Ch1 ---- %

Frequency (5/8/2023 1:58:10.857 PM)

Ch1 ---- Hz

5/8/2023 1:59 PM Page 31 of 54



Line Gain -5 600 Termination: Level and Gain -5

Waveform: Sine

Generator Level: -10.000 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/8/2023 1:58:13.558 PM)

Channel Lower Limit Value Upper Limit
Ch1 -6.500 dBu -8.455 dBu -3.500 dBu

Result: A FAILED

5/8/2023 1:59 PM Page 32 of 54



Line Gain 0 600 Termination : Signal Path Setup

Output Connector: Analog Balanced

Channels: 1

Source Impedance: 100 ohm
AG52 Generator Option: Installed
Output EQ: None

Input Connector: Analog Balanced

Channels: 1

Channel: Ch1

Termination: 600 ohm

Input Bandwidth: AC (<10 Hz) - 90k (192 kHz SR)

Device Delay: 0.000 s
Input EQ: None

References

dBr G: 100.0 mVrms dBm (Output Power): 600.0 ohm W(watts) (Output Power): 8.000 ohm Shared Frequency Reference: 1.00000 kHz dBrA: 1.000 Vrms dBrB: 1.000 Vrms dBrA Offset: 0.000 dB dBrB Offset: 0.000 dB dBSPL1: 10.00 mVrms dBSPL2: 10.00 mVrms dBSPL1 Calibrator Level: 94.000 dBSPL dBSPL2 Calibrator Level: 94.000 dBSPL dBm (Input Power): 600.0 ohm

• DCX

W(watts) (Input Power):

DC Output 1: 0.000 V

DC Output 1: Off

DC Output 2: 0.000 V

DC Output 2: Off

Port A (hex): 00

Port B (hex): 00

Port C (hex): 00

5/8/2023 1:59 PM Page 33 of 54



Port D (hex): 00

• Clocks

Output Rate: Track Output SR

Sync Out Level: 3.300 V
Sync Out Polarity: Normal
Timebase Reference: Internal
Jitter: Disabled

• Triggers

Source: Off

Input Logic Level: 3.300 V
Edge: Rising

Line Gain 0 600 Termination: Verify Connections

Waveform: Sine

Generator Level: -10.000 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/8/2023 1:58:18.676 PM)

Ch1 293.0 mVrms

Gain (5/8/2023 1:58:18.676 PM)

Ch1 1.554 dB

THD+N Ratio (5/8/2023 1:58:18.676 PM)

Ch1 ---- %

Frequency (5/8/2023 1:58:18.676 PM)

Ch1 ---- Hz

5/8/2023 1:59 PM Page 34 of 54



Line Gain 0 600 Termination: Level and Gain 0

Waveform: Sine

Generator Level: -10.000 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/8/2023 1:58:21.190 PM)

Channel Lower Limit Value Upper Limit
Ch1 -1.500 dBu -8.479 dBu +1.500 dBu

Result: A FAILED

5/8/2023 1:59 PM Page 35 of 54



Line Gain +10 600 Termination : Signal Path Setup

Output Connector: Analog Balanced

Channels: 1

Source Impedance: 100 ohm
AG52 Generator Option: Installed
Output EQ: None

Input Connector: Analog Balanced

Channels: 1

Channel: Ch1

Termination: 600 ohm

Input Bandwidth: AC (<10 Hz) - 90k (192 kHz SR)

Device Delay: 0.000 s
Input EQ: None

References

dBr G: 100.0 mVrms dBm (Output Power): 600.0 ohm W(watts) (Output Power): 8.000 ohm Shared Frequency Reference: 1.00000 kHz dBrA: 1.000 Vrms dBrB: 1.000 Vrms dBrA Offset: 0.000 dB dBrB Offset: 0.000 dB dBSPL1: 10.00 mVrms dBSPL2: 10.00 mVrms dBSPL1 Calibrator Level: 94.000 dBSPL dBSPL2 Calibrator Level: 94.000 dBSPL dBm (Input Power): 600.0 ohm

• DCX

W(watts) (Input Power):

DC Output 1: 0.000 V

DC Output 1: Off

DC Output 2: 0.000 V

DC Output 2: Off

Port A (hex): 00

Port B (hex): 00

Port C (hex): 00

5/8/2023 1:59 PM Page 36 of 54



Port D (hex): 00

• Clocks

Output Rate: Track Output SR

Sync Out Level: 3.300 V
Sync Out Polarity: Normal
Timebase Reference: Internal
Jitter: Disabled

• Triggers

Source: Off

Input Logic Level: 3.300 V
Edge: Rising

Line Gain +10 600 Termination: Verify Connections

Waveform: Sine

Generator Level: -10.000 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/8/2023 1:58:26.404 PM)

Ch1 297.6 mVrms

Gain (5/8/2023 1:58:26.404 PM)

Ch1 1.692 dB

THD+N Ratio (5/8/2023 1:58:26.404 PM)

Ch1 ---- %

Frequency (5/8/2023 1:58:26.404 PM)

Ch1 ---- Hz

5/8/2023 1:59 PM Page 37 of 54



Line Gain +10 600 Termination: Level and Gain +10

Waveform: Sine

Generator Level: -10.000 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/8/2023 1:58:28.999 PM)

Channel Lower Limit Value Upper Limit
Ch1 +8.500 dBu -8.496 dBu +11.500 dBu

Result: A FAILED

5/8/2023 1:59 PM Page 38 of 54



Line Gain +10 200k Termination Level Hi : Signal Path Setup

Output Connector: Analog Balanced

Channels: 1

Source Impedance: 100 ohm
AG52 Generator Option: Installed
Output EQ: None

Input Connector: Analog Balanced

Channels: 1

Channel: Ch1

Termination: 200 kohm

Input Bandwidth: AC (<10 Hz) - 90k (192 kHz SR)

Device Delay: 0.000 s
Input EQ: None

References

dBr G: 100.0 mVrms dBm (Output Power): 600.0 ohm W(watts) (Output Power): 8.000 ohm Shared Frequency Reference: 1.00000 kHz dBrA: 1.000 Vrms dBrB: 1.000 Vrms dBrA Offset: 0.000 dB dBrB Offset: 0.000 dB dBSPL1: 10.00 mVrms dBSPL2: 10.00 mVrms dBSPL1 Calibrator Level: 94.000 dBSPL dBSPL2 Calibrator Level: 94.000 dBSPL dBm (Input Power): 600.0 ohm

• DCX

W(watts) (Input Power):

DC Output 1: 0.000 V

DC Output 1: Off

DC Output 2: 0.000 V

DC Output 2: Off

Port A (hex): 00

Port B (hex): 00

Port C (hex): 00

5/8/2023 1:59 PM Page 39 of 54

8.000 ohm



Port D (hex): 00

• Clocks

Output Rate: Track Output SR

Sync Out Level: 3.300 V
Sync Out Polarity: Normal
Timebase Reference: Internal
Jitter: Disabled

• Triggers

Source: Off

Input Logic Level: 3.300 V
Edge: Rising

Line Gain +10 200k Termination Level Hi: Verify Connections

Waveform: Sine

Generator Level: -20.000 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/8/2023 1:58:34.767 PM)

Ch1 293.8 mVrms

Gain (5/8/2023 1:58:34.767 PM)

Ch1 11.580 dB

THD+N Ratio (5/8/2023 1:58:34.767 PM)

Ch1 ---- %

Frequency (5/8/2023 1:58:34.767 PM)

Ch1 ---- Hz

5/8/2023 1:59 PM Page 40 of 54



#### Line Gain +10 200k Termination Level Hi: Noise Recorder (RMS) CW

Waveform: None
Low-pass Filter: 20 kHz
Weighting Filter: Signal Path

High-pass Filter: 20 Hz

Sweep Time: 0.00:00:03.000

Reading Rate: 10/sec

Input Bandwidth: Use Signal Path

Record Acquisition: False

Measured 1 5/8/2023 1:58:39 PM

## RMS Level (5/8/2023 1:58:39.914 PM)



Result: A FAILED

5/8/2023 1:59 PM Page 41 of 54



5/8/2023 1:59 PM Page 42 of 54



Line Gain +10 200k Termination Level Low: Signal Path Setup

Output Connector: Analog Balanced

Channels: 1

Source Impedance: 100 ohm
AG52 Generator Option: Installed
Output EQ: None

Input Connector: Analog Balanced

Channels: 1

Channel: Ch1

Termination: 200 kohm

Input Bandwidth: AC (<10 Hz) - 90k (192 kHz SR)

Device Delay: 0.000 s
Input EQ: None

References

dBr G: 100.0 mVrms dBm (Output Power): 600.0 ohm W(watts) (Output Power): 8.000 ohm Shared Frequency Reference: 1.00000 kHz dBrA: 1.000 Vrms dBrB: 1.000 Vrms dBrA Offset: 0.000 dB dBrB Offset: 0.000 dB dBSPL1: 10.00 mVrms dBSPL2: 10.00 mVrms dBSPL1 Calibrator Level: 94.000 dBSPL dBSPL2 Calibrator Level: 94.000 dBSPL dBm (Input Power): 600.0 ohm W(watts) (Input Power): 8.000 ohm

• DCX

DC Output 1: 0.000 V
DC Output 1: Off

DC Output 2: 0.000 V

DC Output 2: Off

Port A (hex): 00

Port B (hex): 00

Port C (hex): 00

5/8/2023 1:59 PM Page 43 of 54



Port D (hex): 00

• Clocks

Output Rate: Track Output SR

Sync Out Level: 3.300 V
Sync Out Polarity: Normal
Timebase Reference: Internal
Jitter: Disabled

• Triggers

Source: Off

Input Logic Level: 3.300 V Edge: Rising

Line Gain +10 200k Termination Level Low: Verify Connections

Waveform: Sine

Generator Level: -20.000 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/8/2023 1:58:45.056 PM)

Ch1 280.7 mVrms

Gain (5/8/2023 1:58:45.056 PM)

Ch1 11.184 dB

THD+N Ratio (5/8/2023 1:58:45.056 PM)

Ch1 ---- %

Frequency (5/8/2023 1:58:45.056 PM)

Ch1 ---- Hz

5/8/2023 1:59 PM Page 44 of 54



#### Line Gain +10 200k Termination Level Low: Noise Recorder (RMS) CCW

Waveform: None
Low-pass Filter: 20 kHz
Weighting Filter: Signal Path

High-pass Filter: 20 Hz

Sweep Time: 0.00:00:03.000

Reading Rate: 10/sec

Input Bandwidth: Use Signal Path

Record Acquisition: False

Measured 1 5/8/2023 1:58:50 PM

## RMS Level (5/8/2023 1:58:50.946 PM)



Result: A FAILED

5/8/2023 1:59 PM Page 45 of 54



5/8/2023 1:59 PM Page 46 of 54



Hi Z Gain -10 2.2M 200k Termination : Signal Path Setup

Output Connector: Analog Balanced

2 Channels:

100 ohm Source Impedance: AG52 Generator Option: Installed None Output EQ:

Input Connector: Analog Balanced

Channels: 1

Channel: Ch1

Termination: 200 kohm

AC (<10 Hz) - 90k (192 kHz SR) Input Bandwidth:

Device Delay: 0.000 sInput EQ: None

References

dBr G: 100.0 mVrms dBm (Output Power): 600.0 ohm W(watts) (Output Power): 8.000 ohm Shared Frequency Reference: 1.00000 kHz dBrA: 1.000 Vrms dBrB: 1.000 Vrms dBrA Offset: 0.000 dB dBrB Offset: 0.000 dB dBSPL1: 10.00 mVrms dBSPL2: 10.00 mVrms dBSPL1 Calibrator Level: 94.000 dBSPL dBSPL2 Calibrator Level: 94.000 dBSPL dBm (Input Power): 600.0 ohm W(watts) (Input Power):

• DCX

DC Output 1: 0.000 V Off DC Output 1: DC Output 2: 0.000 V DC Output 2: Off Port A (hex): 00 00 Port B (hex): 00 Port C (hex):

5/8/2023 1:59 PM Page 47 of 54

8.000 ohm



Port D (hex): 00

• Clocks

Output Rate: Track Output SR

Sync Out Level: 3.300 V
Sync Out Polarity: Normal
Timebase Reference: Internal
Jitter: Disabled

• Triggers

Source: Off

Input Logic Level: 3.300 V Edge: Rising

Hi Z Gain -10 2.2M 200k Termination: Verify Connections

Waveform: Sine

Generator Level: -22.300 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/8/2023 1:58:56.341 PM)

Ch1 268.7 mVrms

Gain (5/8/2023 1:58:56.341 PM)

Ch1 13.103 dB

THD+N Ratio (5/8/2023 1:58:56.341 PM)

Ch1 ---- %

Frequency (5/8/2023 1:58:56.341 PM)

Ch1 ---- Hz

5/8/2023 1:59 PM Page 48 of 54



Hi Z Gain -10 2.2M 200k Termination: Level and Gain 2.2M

Waveform: Sine

Generator Level: -22.300 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/8/2023 1:58:59.652 PM)

Channel Lower Limit Value Upper Limit
Ch1 -2.000 dBu -8.445 dBu +2.000 dBu

Result: A FAILED

5/8/2023 1:59 PM Page 49 of 54



Hi Z Gain -10 47k 200k Termination : Signal Path Setup
Output Connector:
Analog Unbalanced

Channels: 2

Source Impedance: 50 ohm
AG52 Generator Option: Installed
Output EQ: None

Input Connector: Analog Balanced

Channels: 1

Channel: Ch1

Termination: 200 kohm

Input Bandwidth: AC (<10 Hz) - 90k (192 kHz SR)

Device Delay: 0.000 s
Input EQ: None

References

dBr G: 100.0 mVrms dBm (Output Power): 600.0 ohm W(watts) (Output Power): 8.000 ohm Shared Frequency Reference: 1.00000 kHz dBrA: 1.000 Vrms dBrB: 1.000 Vrms dBrA Offset: 0.000 dB dBrB Offset: 0.000 dB dBSPL1: 10.00 mVrms dBSPL2: 10.00 mVrms dBSPL1 Calibrator Level: 94.000 dBSPL dBSPL2 Calibrator Level: 94.000 dBSPL dBm (Input Power): 600.0 ohm W(watts) (Input Power): 8.000 ohm

• DCX

DC Output 1: 0.000 V
DC Output 1: Off
DC Output 2: 0.000 V
DC Output 2: Off
Port A (hex): 00
Port B (hex): 00
Port C (hex): 00

5/8/2023 1:59 PM Page 50 of 54



Port D (hex): 00

• Clocks

Output Rate: Track Output SR

Sync Out Level: 3.300 V
Sync Out Polarity: Normal
Timebase Reference: Internal
Jitter: Disabled

• Triggers

Source: Off

Input Logic Level: 3.300 V Edge: Rising

Hi Z Gain -10 47k 200k Termination: Verify Connections

Waveform: Sine

Generator Level: -22.300 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/8/2023 1:59:04.976 PM)

Ch1 296.0 mVrms

Gain (5/8/2023 1:59:04.976 PM)

Ch1 13.944 dB

THD+N Ratio (5/8/2023 1:59:04.976 PM)

Ch1 ---- %

Frequency (5/8/2023 1:59:04.976 PM)

Ch1 ---- Hz

5/8/2023 1:59 PM Page 51 of 54



Hi Z Gain -10 47k 200k Termination: Level and Gain 47K

Waveform: Sine

Generator Level: -22.300 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/8/2023 1:59:07.686 PM)

Channel Lower Limit Value Upper Limit
Ch1 -8.000 dBu -8.656 dBu -4.000 dBu

Result: A FAILED

5/8/2023 1:59 PM Page 52 of 54



Dummy Signal Path For Report : Signal Path Setup

Output Connector: Analog Unbalanced

Channels: 2

Source Impedance: 50 ohm
AG52 Generator Option: Installed
Output EQ: None

Input Connector: Analog Unbalanced

Channels: 2

Termination: 100 kohm

Input Bandwidth: AC (<10 Hz) - 90k (192 kHz SR)

Device Delay: 0.000 s
Input EQ: None

References

dBr G: 100.0 mVrms dBm (Output Power): 600.0 ohm W(watts) (Output Power): 8.000 ohm Shared Frequency Reference: 1.00000 kHz dBrA: 1.000 Vrms dBrB: 1.000 Vrms dBrA Offset: 0.000 dB dBrB Offset: 0.000 dB dBSPL1: 10.00 mVrms dBSPL2: 10.00 mVrms dBSPL1 Calibrator Level: 94.000 dBSPL dBSPL2 Calibrator Level: 94.000 dBSPL 600.0 ohm dBm (Input Power): W(watts) (Input Power): 8.000 ohm

• DCX

DC Output 1: 0.000 V DC Output 1: Off 0.000 V DC Output 2: DC Output 2: Off Port A (hex): 00 Port B (hex): 00 00 Port C (hex): 00 Port D (hex):

5/8/2023 1:59 PM Page 53 of 54



• Clocks

Output Rate: Track Output SR

Sync Out Level: 3.300 V
Sync Out Polarity: Normal
Timebase Reference: Internal
Jitter: Disabled

• Triggers

Source: Off

Input Logic Level: 3.300 V Edge: Rising

Dummy Signal Path For Report : Verify Connections

Waveform: Sine

Generator Level: 100.0 mVrms

DC Offset: 0.000 V

Frequency: 1.00000 kHz

RMS Level (5/8/2023 1:59:12.265 PM)

Ch1 295.5 mVrms Ch2 281.9 mVrms

5/8/2023 1:59 PM Page 54 of 54