

Summary

Mic500 200k Termination	
Signal Path Setup	🍼 PASSED
Stepped Frequency Sweep MIC 500	🛕 FAILED
Mic 2k 200k termination	
Signal Path Setup	PASSED
Stepped Frequency Sweep MIC 2K	▲ FAILED
Mic 2k 15dB PAD 200k termination	
Signal Path Setup	PASSED
Stepped Frequency Sweep 15dB PAD	🛕 FAILED
Line Gain -10 200kTermination	
Signal Path Setup	PASSED
Stepped Frequency Sweep -10	▲ FAILED
Line Gain -10 600 Termination	
Signal Path Setup	PASSED
Level and Gain -10	PASSED
Line Gain +5 200kTermination	
Signal Path Setup	PASSED
Stepped Frequency Sweep +5	▲ FAILED
Line Gain +5 600 Termination	
Signal Path Setup	PASSED
Level and Gain +5	▲ FAILED
Line Gain -5 600 Termination	
Signal Path Setup	PASSED
Level and Gain -5	▲ FAILED
Line Gain 0 600 Termination	
Signal Path Setup	PASSED
Level and Gain 0	▲ FAILED
Line Gain +10 600 Termination	
Signal Path Setup	PASSED
Level and Gain +10	▲ FAILED
Line Gain +10 200k Termination Level Hi	
Signal Path Setup	PASSED
Noise Recorder (RMS) CW	▲ FAILED
Line Gain +10 200k Termination Level Low	
Signal Path Setup	PASSED
Noise Recorder (RMS) CCW	▲ FAILED
Hi Z Gain -10 2.2M 200k Termination	

Signal Path Setup Level and Gain 2.2M	♥ PASSED ♠ FAILED
Hi Z Gain -10 47k 200k Termination	
Signal Path Setup Level and Gain 47K	▼ PASSED ▲ FAILED
Dummy Signal Path For Report	
Signal Path Setup	PASSED
Sequence Result:	
Sequence Result: 🛕 FAILED	

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Mic500 200k Termination : Signal Path Setup

Output Connector: Analog Balanced

Channels: 1

Source Impedance: 100 ohm
AG52 Generator Option: Installed
Output EQ: None

Input Connector: Analog Balanced

Channels: 1

Channel: Ch1

Termination: 200 kohm

Input Bandwidth: AC (<10 Hz) - 90k (192 kHz SR)

Device Delay: 0.000 s
Input EQ: None

References

100.0 mVrms dBr G: dBm (Output Power): 600.0 ohm W(watts) (Output Power): 8.000 ohm Shared Frequency Reference: 1.00000 kHz dBrA: 1.000 Vrms dBrB: 1.000 Vrms dBrA Offset: 0.000 dB dBrB Offset: 0.000 dB dBSPL1: 10.00 mVrms dBSPL2: 10.00 mVrms dBSPL1 Calibrator Level: 94.000 dBSPL dBSPL2 Calibrator Level: 94.000 dBSPL dBm (Input Power): 600.0 ohm W(watts) (Input Power): 8.000 ohm

• DCX

DC Output 1: 0.000 V

DC Output 1: Off

DC Output 2: 0.000 V

DC Output 2: Off

Port A (hex): 00

Port B (hex): 00

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Port C (hex): 00
Port D (hex): 00

Clocks

Output Rate: Track Output SR

Sync Out Level: 3.300 V
Sync Out Polarity: Normal
Timebase Reference: Internal
Jitter: Disabled

• Triggers

Source: Off
Input Logic Level: 3.300 V
Edge: Rising

Mic500 200k Termination: Verify Connections

Waveform: Sine

Generator Level: -42.300 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/2/2023 8:44:13.158 PM)

Ch1 284.1 mVrms

Gain (5/2/2023 8:44:13.158 PM)

Ch1 33.588 dB

THD+N Ratio (5/2/2023 8:44:13.158 PM)

Ch1 ---- %

Frequency (5/2/2023 8:44:13.158 PM)

Ch1 ---- Hz

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Mic500 200k Termination: Stepped Frequency Sweep MIC 500

Generator Level: -42.300 dBu
DC Offset: 0.000 V
EQ: None

Start Frequency: 20.0000 kHz
Stop Frequency: 20.0000 Hz
Step Type: Logarithmic

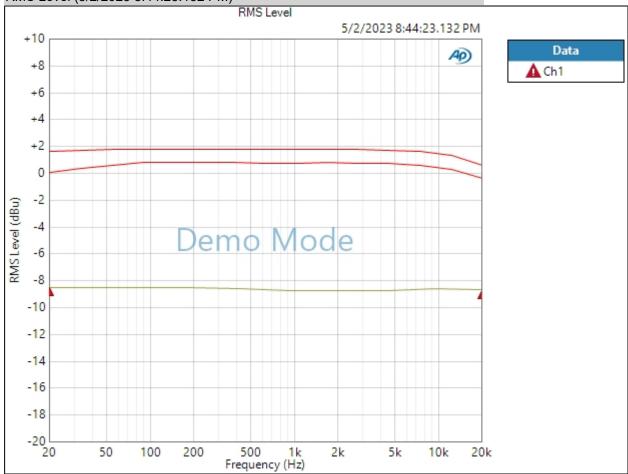
Number of Points: 10

Weighting Filter: Signal Path

High-pass Filter: 20 Hz Phase Ref Channel: Ch1

Measured 1 5/2/2023 8:44:23 PM

RMS Level (5/2/2023 8:44:23.132 PM)

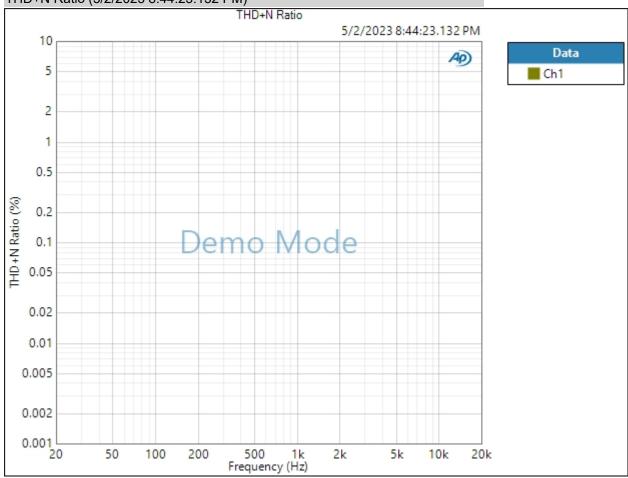


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Result: A FAILED

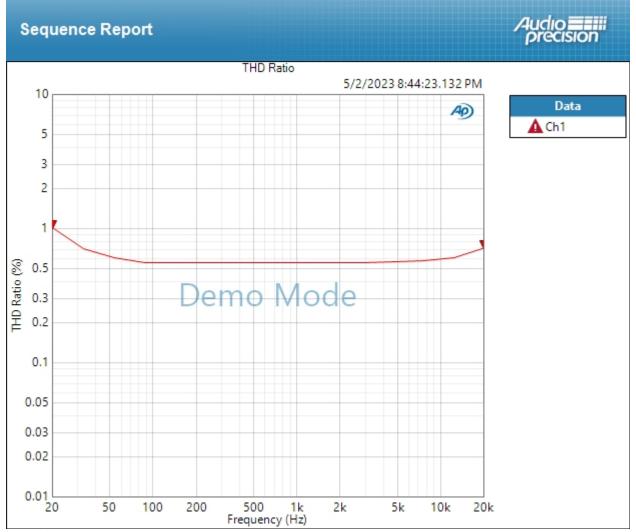
THD+N Ratio (5/2/2023 8:44:23.132 PM)



Result: V PASSED

THD Ratio (5/2/2023 8:44:23.132 PM)

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Result: 🛕 FAILED

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Mic 2k 200k termination : Signal Path Setup

Output Connector: Analog Balanced

Channels: 1

Source Impedance: 100 ohm
AG52 Generator Option: Installed
Output EQ: None

Input Connector: Analog Balanced

Channels: 1

Channel: Ch1

Termination: 200 kohm

Input Bandwidth: AC (<10 Hz) - 90k (192 kHz SR)

Device Delay: 0.000 s
Input EQ: None

References

dBr G: 100.0 mVrms dBm (Output Power): 600.0 ohm W(watts) (Output Power): 8.000 ohm Shared Frequency Reference: 1.00000 kHz dBrA: 1.000 Vrms dBrB: 1.000 Vrms dBrA Offset: 0.000 dB dBrB Offset: 0.000 dB dBSPL1: 10.00 mVrms dBSPL2: 10.00 mVrms dBSPL1 Calibrator Level: 94.000 dBSPL dBSPL2 Calibrator Level: 94.000 dBSPL dBm (Input Power): 600.0 ohm W(watts) (Input Power): 8.000 ohm

• DCX

DC Output 1: 0.000 V

DC Output 1: Off

DC Output 2: 0.000 V

DC Output 2: Off

Port A (hex): 00

Port B (hex): 00

Port C (hex): 00

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Port D (hex): 00

• Clocks

Output Rate: Track Output SR

Sync Out Level: 3.300 V
Sync Out Polarity: Normal
Timebase Reference: Internal
Jitter: Disabled

• Triggers

Source: Off

Input Logic Level: 3.300 V Edge: Rising

Mic 2k 200k termination: Verify Connections

Waveform: Sine

Generator Level: -42.300 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/2/2023 8:44:28.004 PM)

Ch1 296.9 mVrms

Gain (5/2/2023 8:44:28.004 PM)

Ch1 33.972 dB

THD+N Ratio (5/2/2023 8:44:28.004 PM)

Ch1 ---- %

Frequency (5/2/2023 8:44:28.004 PM)

Ch1 ---- Hz

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Mic 2k 200k termination : Stepped Frequency Sweep MIC 2K

Generator Level: -42.300 dBu
DC Offset: 0.000 V
EQ: None

Start Frequency: 20.0000 kHz
Stop Frequency: 20.0000 Hz
Step Type: Logarithmic

Number of Points: 10

Weighting Filter: Signal Path
High-pass Filter: 20 Hz
Phase Ref Channel: Ch1

Measured 1 5/2/2023 8:44:35 PM

RMS Level (5/2/2023 8:44:35.397 PM)



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Result: A FAILED

THD Ratio (5/2/2023 8:44:35.397 PM)



Ch1 A Failed Upper Limit

Result: A FAILED

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Mic 2k 15dB PAD 200k termination : Signal Path Setup
Output Connector:

Analog Balanced

Channels: 1

Source Impedance: 100 ohm
AG52 Generator Option: Installed
Output EQ: None

Input Connector: Analog Balanced

Channels: 1

Channel: Ch1

Termination: 200 kohm

Input Bandwidth: AC (<10 Hz) - 90k (192 kHz SR)

Device Delay: 0.000 s
Input EQ: None

References

dBr G: 100.0 mVrms dBm (Output Power): 600.0 ohm W(watts) (Output Power): 8.000 ohm Shared Frequency Reference: 1.00000 kHz dBrA: 1.000 Vrms dBrB: 1.000 Vrms dBrA Offset: 0.000 dB dBrB Offset: 0.000 dB dBSPL1: 10.00 mVrms dBSPL2: 10.00 mVrms dBSPL1 Calibrator Level: 94.000 dBSPL dBSPL2 Calibrator Level: 94.000 dBSPL dBm (Input Power): 600.0 ohm W(watts) (Input Power): 8.000 ohm

• DCX

DC Output 1: 0.000 V

DC Output 1: Off

DC Output 2: 0.000 V

DC Output 2: Off

Port A (hex): 00

Port B (hex): 00

Port C (hex): 00

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Port D (hex): 00

• Clocks

Output Rate: Track Output SR

Sync Out Level: 3.300 V
Sync Out Polarity: Normal
Timebase Reference: Internal
Jitter: Disabled

• Triggers

Source: Off

Input Logic Level: 3.300 V
Edge: Rising

Mic 2k 15dB PAD 200k termination: Verify Connections

Waveform: Sine

Generator Level: -42.300 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/2/2023 8:44:40.312 PM)

Ch1 288.8 mVrms

Gain (5/2/2023 8:44:40.312 PM)

Ch1 33.729 dB

THD+N Ratio (5/2/2023 8:44:40.312 PM)

Ch1 ---- %

Frequency (5/2/2023 8:44:40.312 PM)

Ch1 ---- Hz

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Mic 2k 15dB PAD 200k termination : Stepped Frequency Sweep 15dB PAD

Generator Level: -42.000 dBu
DC Offset: 0.000 V
EQ: None

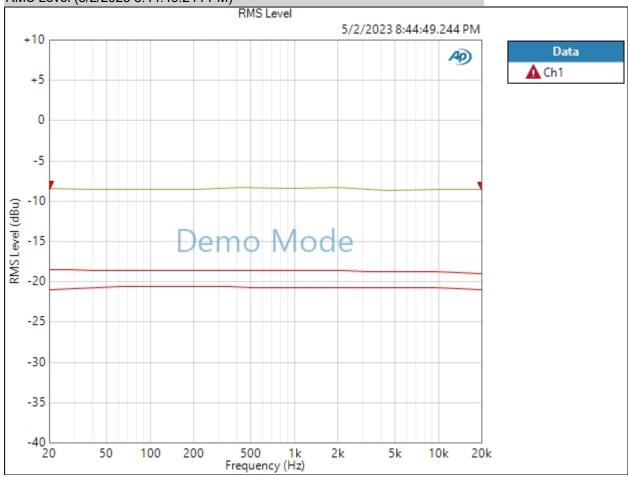
Start Frequency: 20.0000 kHz
Stop Frequency: 20.0000 Hz
Step Type: Logarithmic

Number of Points: 10

Weighting Filter: Signal Path
High-pass Filter: 20 Hz
Phase Ref Channel: Ch1

Measured 1 5/2/2023 8:44:49 PM

RMS Level (5/2/2023 8:44:49.244 PM)



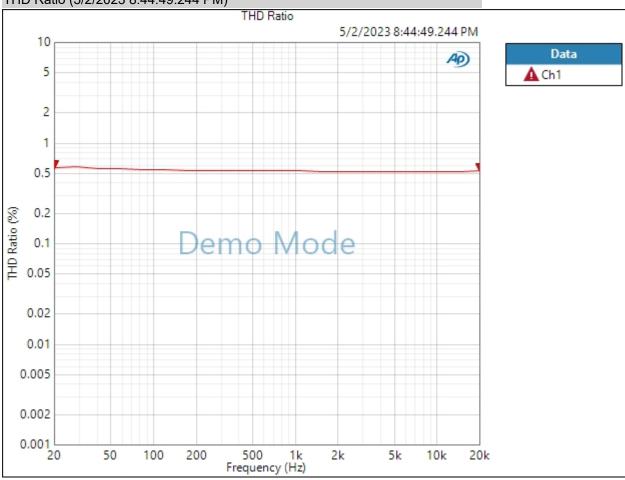
Ch1 A Failed Upper Limit

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Result: A FAILED

THD Ratio (5/2/2023 8:44:49.244 PM)



Ch1 A Failed Upper Limit

Result: A FAILED

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Line Gain -10 200kTermination : Signal Path Setup

Output Connector: Analog Balanced

Channels: 1

Source Impedance: 100 ohm
AG52 Generator Option: Installed
Output EQ: None

Input Connector: Analog Balanced

Channels: 1

Channel: Ch1

Termination: 200 kohm

Input Bandwidth: AC (<10 Hz) - 90k (192 kHz SR)

Device Delay: 0.000 s
Input EQ: None

References

dBr G: 100.0 mVrms dBm (Output Power): 600.0 ohm W(watts) (Output Power): 8.000 ohm Shared Frequency Reference: 1.00000 kHz dBrA: 1.000 Vrms dBrB: 1.000 Vrms dBrA Offset: 0.000 dB dBrB Offset: 0.000 dB dBSPL1: 10.00 mVrms dBSPL2: 10.00 mVrms dBSPL1 Calibrator Level: 94.000 dBSPL dBSPL2 Calibrator Level: 94.000 dBSPL dBm (Input Power): 600.0 ohm

• DCX

W(watts) (Input Power):

DC Output 1: 0.000 V

DC Output 1: Off

DC Output 2: 0.000 V

DC Output 2: Off

Port A (hex): 00

Port B (hex): 00

Port C (hex): 00

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8.000 ohm



Port D (hex): 00

• Clocks

Output Rate: Track Output SR

Sync Out Level: 3.300 V
Sync Out Polarity: Normal
Timebase Reference: Internal
Jitter: Disabled

• Triggers

Source: Off

Input Logic Level: 3.300 V Edge: Rising

Line Gain -10 200kTermination: Verify Connections

Waveform: Sine

Generator Level: 0.000 dBu

DC Offset: 0.000 V

Frequency: 1.00000 kHz

RMS Level (5/2/2023 8:44:54.334 PM)

Ch1 276.8 mVrms

Gain (5/2/2023 8:44:54.334 PM)

Ch1 -8.937 dB

THD+N Ratio (5/2/2023 8:44:54.334 PM)

Ch1 ---- %

Frequency (5/2/2023 8:44:54.334 PM)

Ch1 ---- Hz

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Line Gain -10 200kTermination : Stepped Frequency Sweep -10

Generator Level: 0.000 dBu
DC Offset: 0.000 V
EQ: None

Start Frequency: 20.0000 kHz
Stop Frequency: 20.0000 Hz
Step Type: Logarithmic

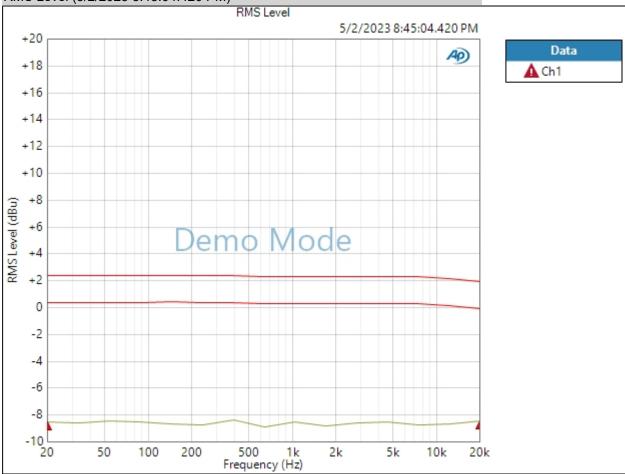
Number of Points: 15

Weighting Filter: Signal Path High-pass Filter: 20 Hz

Phase Ref Channel: Ch1

Measured 1 5/2/2023 8:45:04 PM

RMS Level (5/2/2023 8:45:04.420 PM)

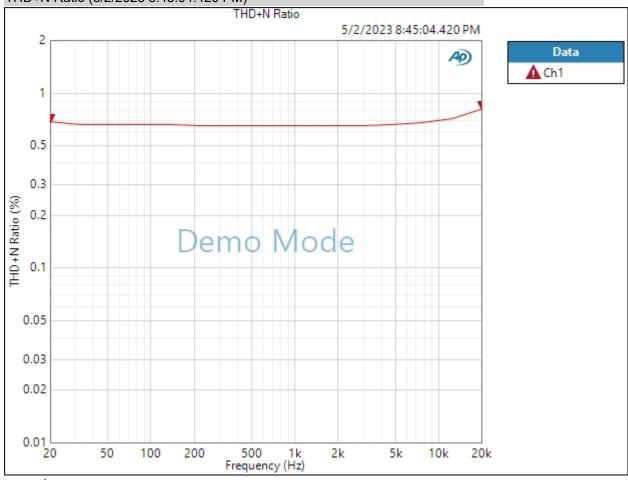


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Result: A FAILED

THD+N Ratio (5/2/2023 8:45:04.420 PM)



Ch1 A Failed Upper Limit

Result: A FAILED

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Line Gain -10 600 Termination : Signal Path Setup

Analog Balanced Output Connector:

1 Channels:

100 ohm Source Impedance: AG52 Generator Option: Installed None Output EQ:

Input Connector: Analog Balanced

Channels: 1

Channel: Ch1

Termination: 600 ohm

AC (<10 Hz) - 90k (192 kHz SR) Input Bandwidth:

Device Delay: 0.000 sInput EQ: None

References

dBr G: 100.0 mVrms dBm (Output Power): 600.0 ohm W(watts) (Output Power): 8.000 ohm Shared Frequency Reference: 1.00000 kHz dBrA: 1.000 Vrms dBrB: 1.000 Vrms dBrA Offset: 0.000 dB dBrB Offset: 0.000 dB dBSPL1: 10.00 mVrms dBSPL2: 10.00 mVrms dBSPL1 Calibrator Level: 94.000 dBSPL dBSPL2 Calibrator Level: 94.000 dBSPL dBm (Input Power): 600.0 ohm W(watts) (Input Power):

• DCX

DC Output 1: 0.000 V Off DC Output 1: DC Output 2: 0.000 V DC Output 2: Off Port A (hex): 00 00 Port B (hex): 00 Port C (hex):

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8.000 ohm



Port D (hex): 00

• Clocks

Output Rate: Track Output SR

Sync Out Level: 3.300 V
Sync Out Polarity: Normal
Timebase Reference: Internal
Jitter: Disabled

• Triggers

Source: Off

Input Logic Level: 3.300 V Edge: Rising

Line Gain -10 600 Termination: Verify Connections

Waveform: Sine

Generator Level: -10.000 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/2/2023 8:45:10.138 PM)

Ch1 288.2 mVrms

Gain (5/2/2023 8:45:10.138 PM)

Ch1 1.411 dB

THD+N Ratio (5/2/2023 8:45:10.138 PM)

Ch1 ---- %

Frequency (5/2/2023 8:45:10.138 PM)

Ch1 ---- Hz

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Line Gain -10 600 Termination: Level and Gain -10

Waveform: Sine

Generator Level: -10.000 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/2/2023 8:45:12.824 PM)

Channel Lower Limit Value Upper Limit
Ch1 -11.500 dBu -8.660 dBu -8.500 dBu

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Line Gain +5 200kTermination : Signal Path Setup

Output Connector: Analog Balanced

Channels: 1

Source Impedance: 100 ohm
AG52 Generator Option: Installed
Output EQ: None

Input Connector: Analog Balanced

Channels: 1

Channel: Ch1

Termination: 200 kohm

Input Bandwidth: AC (<10 Hz) - 90k (192 kHz SR)

Device Delay: 0.000 s
Input EQ: None

References

dBr G: 100.0 mVrms dBm (Output Power): 600.0 ohm W(watts) (Output Power): 8.000 ohm Shared Frequency Reference: 1.00000 kHz dBrA: 1.000 Vrms dBrB: 1.000 Vrms dBrA Offset: 0.000 dB dBrB Offset: 0.000 dB dBSPL1: 10.00 mVrms dBSPL2: 10.00 mVrms dBSPL1 Calibrator Level: 94.000 dBSPL dBSPL2 Calibrator Level: 94.000 dBSPL dBm (Input Power): 600.0 ohm

• DCX

W(watts) (Input Power):

DC Output 1: 0.000 V

DC Output 1: Off

DC Output 2: 0.000 V

DC Output 2: Off

Port A (hex): 00

Port B (hex): 00

Port C (hex): 00

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8.000 ohm



Port D (hex): 00

• Clocks

Output Rate: Track Output SR

Sync Out Level: 3.300 V
Sync Out Polarity: Normal
Timebase Reference: Internal
Jitter: Disabled

• Triggers

Source: Off

Input Logic Level: 3.300 V Edge: Rising

Line Gain +5 200kTermination : Verify Connections

Waveform: Sine

Generator Level: 0.000 dBu

DC Offset: 0.000 V

Frequency: 1.00000 kHz

RMS Level (5/2/2023 8:45:18.134 PM)

Ch1 281.5 mVrms

Gain (5/2/2023 8:45:18.134 PM)

Ch1 -8.792 dB

THD+N Ratio (5/2/2023 8:45:18.134 PM)

Ch1 ---- %

Frequency (5/2/2023 8:45:18.134 PM)

Ch1 ---- Hz

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Line Gain +5 200kTermination : Stepped Frequency Sweep +5

Generator Level: 0.000 dBu
DC Offset: 0.000 V
EQ: None

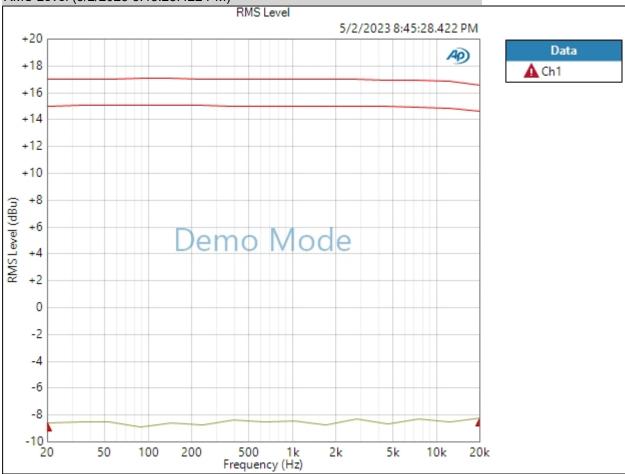
Start Frequency: 20.0000 kHz
Stop Frequency: 20.0000 Hz
Step Type: Logarithmic

Number of Points: 15

Weighting Filter: Signal Path
High-pass Filter: 20 Hz
Phase Ref Channel: Ch1

Measured 1 5/2/2023 8:45:28 PM

RMS Level (5/2/2023 8:45:28.422 PM)

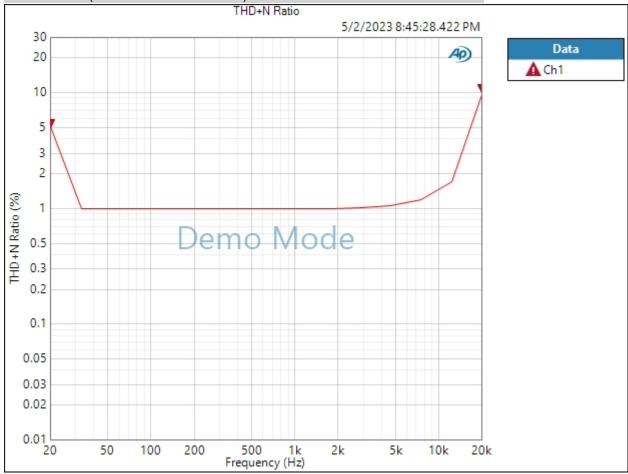


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Result: A FAILED





Ch1 A Failed Upper Limit

Result: A FAILED

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Line Gain +5 600 Termination : Signal Path Setup

Output Connector: Analog Balanced

Channels: 1

Source Impedance: 100 ohm
AG52 Generator Option: Installed
Output EQ: None

Input Connector: Analog Balanced

Channels: 1

Channel: Ch1

Termination: 600 ohm

Input Bandwidth: AC (<10 Hz) - 90k (192 kHz SR)

Device Delay: 0.000 s
Input EQ: None

References

dBr G: 100.0 mVrms dBm (Output Power): 600.0 ohm W(watts) (Output Power): 8.000 ohm Shared Frequency Reference: 1.00000 kHz dBrA: 1.000 Vrms dBrB: 1.000 Vrms dBrA Offset: 0.000 dB dBrB Offset: 0.000 dB dBSPL1: 10.00 mVrms dBSPL2: 10.00 mVrms dBSPL1 Calibrator Level: 94.000 dBSPL dBSPL2 Calibrator Level: 94.000 dBSPL dBm (Input Power): 600.0 ohm

• DCX

W(watts) (Input Power):

DC Output 1: 0.000 V

DC Output 1: Off

DC Output 2: 0.000 V

DC Output 2: Off

Port A (hex): 00

Port B (hex): 00

Port C (hex): 00

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8.000 ohm



Port D (hex): 00

• Clocks

Output Rate: Track Output SR

Sync Out Level: 3.300 V
Sync Out Polarity: Normal
Timebase Reference: Internal
Jitter: Disabled

• Triggers

Source: Off

Input Logic Level: 3.300 V Edge: Rising

Line Gain +5 600 Termination: Verify Connections

Waveform: Sine

Generator Level: -10.000 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/2/2023 8:45:33.678 PM)

Ch1 277.6 mVrms

Gain (5/2/2023 8:45:33.678 PM)

Ch1 1.087 dB

THD+N Ratio (5/2/2023 8:45:33.678 PM)

Ch1 ---- %

Frequency (5/2/2023 8:45:33.678 PM)

Ch1 ---- Hz

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Line Gain +5 600 Termination: Level and Gain +5

Waveform: Sine

Generator Level: -10.000 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/2/2023 8:45:37.533 PM)

Channel Lower Limit Value Upper Limit
Ch1 +3.500 dBu -8.557 dBu +6.500 dBu

Result: A FAILED

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Line Gain -5 600 Termination : Signal Path Setup

Output Connector: Analog Balanced

Channels: 1

Source Impedance: 100 ohm
AG52 Generator Option: Installed
Output EQ: None

Input Connector: Analog Balanced

Channels: 1

Channel: Ch1

Termination: 600 ohm

Input Bandwidth: AC (<10 Hz) - 90k (192 kHz SR)

Device Delay: 0.000 s
Input EQ: None

References

dBr G: 100.0 mVrms dBm (Output Power): 600.0 ohm W(watts) (Output Power): 8.000 ohm Shared Frequency Reference: 1.00000 kHz dBrA: 1.000 Vrms dBrB: 1.000 Vrms dBrA Offset: 0.000 dB dBrB Offset: 0.000 dB dBSPL1: 10.00 mVrms dBSPL2: 10.00 mVrms dBSPL1 Calibrator Level: 94.000 dBSPL dBSPL2 Calibrator Level: 94.000 dBSPL dBm (Input Power): 600.0 ohm

• DCX

W(watts) (Input Power):

DC Output 1: 0.000 V

DC Output 1: Off

DC Output 2: 0.000 V

DC Output 2: Off

Port A (hex): 00

Port B (hex): 00

Port C (hex): 00

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8.000 ohm



Port D (hex): 00

• Clocks

Output Rate: Track Output SR

Sync Out Level: 3.300 V
Sync Out Polarity: Normal
Timebase Reference: Internal
Jitter: Disabled

• Triggers

Source: Off

Input Logic Level: 3.300 V Edge: Rising

Line Gain -5 600 Termination: Verify Connections

Waveform: Sine

Generator Level: -10.000 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/2/2023 8:45:42.756 PM)

Ch1 298.2 mVrms

Gain (5/2/2023 8:45:42.756 PM)

Ch1 1.709 dB

THD+N Ratio (5/2/2023 8:45:42.756 PM)

Ch1 ---- %

Frequency (5/2/2023 8:45:42.756 PM)

Ch1 ---- Hz

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Line Gain -5 600 Termination: Level and Gain -5

Waveform: Sine

Generator Level: -10.000 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/2/2023 8:45:46.501 PM)

Channel Lower Limit Value Upper Limit
Ch1 -6.500 dBu -8.580 dBu -3.500 dBu

Result: A FAILED

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Line Gain 0 600 Termination : Signal Path Setup

Output Connector: Analog Balanced

Channels: 1

Source Impedance: 100 ohm
AG52 Generator Option: Installed
Output EQ: None

Input Connector: Analog Balanced

Channels: 1

Channel: Ch1

Termination: 600 ohm

Input Bandwidth: AC (<10 Hz) - 90k (192 kHz SR)

Device Delay: 0.000 s
Input EQ: None

References

dBr G: 100.0 mVrms dBm (Output Power): 600.0 ohm W(watts) (Output Power): 8.000 ohm Shared Frequency Reference: 1.00000 kHz dBrA: 1.000 Vrms dBrB: 1.000 Vrms dBrA Offset: 0.000 dB dBrB Offset: 0.000 dB dBSPL1: 10.00 mVrms dBSPL2: 10.00 mVrms dBSPL1 Calibrator Level: 94.000 dBSPL dBSPL2 Calibrator Level: 94.000 dBSPL dBm (Input Power): 600.0 ohm

• DCX

W(watts) (Input Power):

DC Output 1: 0.000 V

DC Output 1: Off

DC Output 2: 0.000 V

DC Output 2: Off

Port A (hex): 00

Port B (hex): 00

Port C (hex): 00

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8.000 ohm



Port D (hex): 00

• Clocks

Output Rate: Track Output SR

Sync Out Level: 3.300 V
Sync Out Polarity: Normal
Timebase Reference: Internal
Jitter: Disabled

• Triggers

Source: Off

Input Logic Level: 3.300 V Edge: Rising

Line Gain 0 600 Termination: Verify Connections

Waveform: Sine

Generator Level: -10.000 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/2/2023 8:45:51.736 PM)

Ch1 284.0 mVrms

Gain (5/2/2023 8:45:51.736 PM)

Ch1 1.284 dB

THD+N Ratio (5/2/2023 8:45:51.736 PM)

Ch1 ---- %

Frequency (5/2/2023 8:45:51.736 PM)

Ch1 ---- Hz

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Line Gain 0 600 Termination: Level and Gain 0

Waveform: Sine

Generator Level: -10.000 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/2/2023 8:45:55.455 PM)

Channel Lower Limit Value Upper Limit
Ch1 -1.500 dBu -8.645 dBu +1.500 dBu

Result: A FAILED

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Line Gain +10 600 Termination : Signal Path Setup

Output Connector: Analog Balanced

Channels: 1

Source Impedance: 100 ohm
AG52 Generator Option: Installed
Output EQ: None

Input Connector: Analog Balanced

Channels: 1

Channel: Ch1

Termination: 600 ohm

Input Bandwidth: AC (<10 Hz) - 90k (192 kHz SR)

Device Delay: 0.000 s
Input EQ: None

References

dBr G: 100.0 mVrms dBm (Output Power): 600.0 ohm W(watts) (Output Power): 8.000 ohm Shared Frequency Reference: 1.00000 kHz dBrA: 1.000 Vrms dBrB: 1.000 Vrms dBrA Offset: 0.000 dB dBrB Offset: 0.000 dB dBSPL1: 10.00 mVrms dBSPL2: 10.00 mVrms dBSPL1 Calibrator Level: 94.000 dBSPL dBSPL2 Calibrator Level: 94.000 dBSPL dBm (Input Power): 600.0 ohm

• DCX

W(watts) (Input Power):

DC Output 1: 0.000 V

DC Output 1: Off

DC Output 2: 0.000 V

DC Output 2: Off

Port A (hex): 00

Port B (hex): 00

Port C (hex): 00

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8.000 ohm



Port D (hex):

• Clocks

Output Rate: Track Output SR

Sync Out Level: 3.300 V
Sync Out Polarity: Normal
Timebase Reference: Internal
Jitter: Disabled

• Triggers

Source: Off

Input Logic Level: 3.300 V Edge: Rising

Line Gain +10 600 Termination: Verify Connections

Waveform: Sine

Generator Level: -10.000 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/2/2023 8:46:00.706 PM)

Ch1 292.6 mVrms

Gain (5/2/2023 8:46:00.706 PM)

Ch1 1.545 dB

THD+N Ratio (5/2/2023 8:46:00.706 PM)

Ch1 ---- %

Frequency (5/2/2023 8:46:00.706 PM)

Ch1 ---- Hz

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Line Gain +10 600 Termination: Level and Gain +10

Waveform: Sine

Generator Level: -10.000 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/2/2023 8:46:04.599 PM)

Channel Lower Limit Value Upper Limit
Ch1 +8.500 dBu -8.555 dBu +11.500 dBu

Result: A FAILED

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Line Gain +10 200k Termination Level Hi : Signal Path Setup

Output Connector: Analog Balanced

Channels: 1

Source Impedance: 100 ohm
AG52 Generator Option: Installed
Output EQ: None

Input Connector: Analog Balanced

Channels: 1

Channel: Ch1

Termination: 200 kohm

Input Bandwidth: AC (<10 Hz) - 90k (192 kHz SR)

Device Delay: 0.000 s
Input EQ: None

References

100.0 mVrms dBr G: dBm (Output Power): 600.0 ohm W(watts) (Output Power): 8.000 ohm Shared Frequency Reference: 1.00000 kHz dBrA: 1.000 Vrms dBrB: 1.000 Vrms dBrA Offset: 0.000 dB dBrB Offset: 0.000 dB dBSPL1: 10.00 mVrms dBSPL2: 10.00 mVrms dBSPL1 Calibrator Level: 94.000 dBSPL dBSPL2 Calibrator Level: 94.000 dBSPL dBm (Input Power): 600.0 ohm

• DCX

W(watts) (Input Power):

DC Output 1: 0.000 V

DC Output 1: Off

DC Output 2: 0.000 V

DC Output 2: Off

Port A (hex): 00

Port B (hex): 00

Port C (hex): 00

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8.000 ohm



Port D (hex):

• Clocks

Output Rate: Track Output SR

Sync Out Level: 3.300 V
Sync Out Polarity: Normal
Timebase Reference: Internal
Jitter: Disabled

• Triggers

Source: Off

Input Logic Level: 3.300 V Edge: Rising

Line Gain +10 200k Termination Level Hi: Verify Connections

Waveform: Sine

Generator Level: -20.000 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/2/2023 8:46:09.891 PM)

Ch1 303.1 mVrms

Gain (5/2/2023 8:46:09.891 PM)

Ch1 11.849 dB

THD+N Ratio (5/2/2023 8:46:09.891 PM)

Ch1 ---- %

Frequency (5/2/2023 8:46:09.891 PM)

Ch1 ---- Hz

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Line Gain +10 200k Termination Level Hi: Noise Recorder (RMS) CW

Waveform: None
Low-pass Filter: 20 kHz
Weighting Filter: Signal Path

High-pass Filter: 20 Hz

Sweep Time: 0.00:00:03.000

Reading Rate: 10/sec

Input Bandwidth: Use Signal Path

Record Acquisition: False

Measured 1 5/2/2023 8:46:22 PM

RMS Level (5/2/2023 8:46:22.380 PM)



Result: A FAILED

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Line Gain +10 200k Termination Level Low: Signal Path Setup

Output Connector: Analog Balanced

Channels: 1

Source Impedance: 100 ohm
AG52 Generator Option: Installed
Output EQ: None

Input Connector: Analog Balanced

Channels: 1

Channel: Ch1

Termination: 200 kohm

Input Bandwidth: AC (<10 Hz) - 90k (192 kHz SR)

Device Delay: 0.000 s
Input EQ: None

References

100.0 mVrms dBr G: dBm (Output Power): 600.0 ohm W(watts) (Output Power): 8.000 ohm Shared Frequency Reference: 1.00000 kHz dBrA: 1.000 Vrms dBrB: 1.000 Vrms dBrA Offset: 0.000 dB dBrB Offset: 0.000 dB dBSPL1: 10.00 mVrms dBSPL2: 10.00 mVrms dBSPL1 Calibrator Level: 94.000 dBSPL dBSPL2 Calibrator Level: 94.000 dBSPL dBm (Input Power): 600.0 ohm W(watts) (Input Power): 8.000 ohm

• DCX

DC Output 1: 0.000 V
DC Output 1: Off

DC Output 2: 0.000 V

DC Output 2: Off

Port A (hex): 00

Port B (hex): 00

Port C (hex): 00

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Port D (hex): 00

• Clocks

Output Rate: Track Output SR

Sync Out Level: 3.300 V
Sync Out Polarity: Normal
Timebase Reference: Internal
Jitter: Disabled

• Triggers

Source: Off

Input Logic Level: 3.300 V Edge: Rising

Line Gain +10 200k Termination Level Low: Verify Connections

Waveform: Sine

Generator Level: -20.000 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/2/2023 8:46:27.782 PM)

Ch1 287.2 mVrms

Gain (5/2/2023 8:46:27.782 PM)

Ch1 11.382 dB

THD+N Ratio (5/2/2023 8:46:27.782 PM)

Ch1 ---- %

Frequency (5/2/2023 8:46:27.782 PM)

Ch1 ---- Hz

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Line Gain +10 200k Termination Level Low: Noise Recorder (RMS) CCW

Waveform: None
Low-pass Filter: 20 kHz
Weighting Filter: Signal Path

High-pass Filter: 20 Hz

Sweep Time: 0.00:00:03.000

Reading Rate: 10/sec

Input Bandwidth: Use Signal Path

Record Acquisition: False

Measured 1 5/2/2023 8:46:42 PM

RMS Level (5/2/2023 8:46:42.036 PM)



Result: A FAILED

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Hi Z Gain -10 2.2M 200k Termination : Signal Path Setup

Output Connector: Analog Balanced

Channels: 2

Source Impedance: 100 ohm
AG52 Generator Option: Installed
Output EQ: None

Input Connector: Analog Balanced

Channels: 1

Channel: Ch1

Termination: 200 kohm

Input Bandwidth: AC (<10 Hz) - 90k (192 kHz SR)

Device Delay: 0.000 s
Input EQ: None

References

dBr G: 100.0 mVrms dBm (Output Power): 600.0 ohm W(watts) (Output Power): 8.000 ohm Shared Frequency Reference: 1.00000 kHz dBrA: 1.000 Vrms dBrB: 1.000 Vrms dBrA Offset: 0.000 dB dBrB Offset: 0.000 dB dBSPL1: 10.00 mVrms dBSPL2: 10.00 mVrms dBSPL1 Calibrator Level: 94.000 dBSPL dBSPL2 Calibrator Level: 94.000 dBSPL dBm (Input Power): 600.0 ohm W(watts) (Input Power): 8.000 ohm

• DCX

DC Output 1: 0.000 V
DC Output 1: Off

DC Output 2: 0.000 V

DC Output 2: Off

Port A (hex): 00

Port B (hex): 00

Port C (hex): 00

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Port D (hex): 00

• Clocks

Output Rate: Track Output SR

Sync Out Level: 3.300 V
Sync Out Polarity: Normal
Timebase Reference: Internal
Jitter: Disabled

• Triggers

Source: Off

Input Logic Level: 3.300 V Edge: Rising

Hi Z Gain -10 2.2M 200k Termination: Verify Connections

Waveform: Sine

Generator Level: -22.300 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/2/2023 8:46:47.167 PM)

Ch1 294.2 mVrms

Gain (5/2/2023 8:46:47.167 PM)

Ch1 13.892 dB

THD+N Ratio (5/2/2023 8:46:47.167 PM)

Ch1 ---- %

Frequency (5/2/2023 8:46:47.167 PM)

Ch1 ---- Hz

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Hi Z Gain -10 2.2M 200k Termination: Level and Gain 2.2M

Waveform: Sine

Generator Level: -22.300 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/2/2023 8:46:52.786 PM)

Channel Lower Limit Value Upper Limit
Ch1 -2.000 dBu -8.561 dBu +2.000 dBu

Result: A FAILED

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Hi Z Gain -10 47k 200k Termination : Signal Path Setup
Output Connector:
Analog Unbalanced

Channels: 2

Source Impedance: 50 ohm
AG52 Generator Option: Installed
Output EQ: None

Input Connector: Analog Balanced

Channels: 1

Channel: Ch1

Termination: 200 kohm

Input Bandwidth: AC (<10 Hz) - 90k (192 kHz SR)

Device Delay: 0.000 s
Input EQ: None

References

dBr G: 100.0 mVrms dBm (Output Power): 600.0 ohm W(watts) (Output Power): 8.000 ohm Shared Frequency Reference: 1.00000 kHz dBrA: 1.000 Vrms dBrB: 1.000 Vrms dBrA Offset: 0.000 dB dBrB Offset: 0.000 dB dBSPL1: 10.00 mVrms dBSPL2: 10.00 mVrms dBSPL1 Calibrator Level: 94.000 dBSPL dBSPL2 Calibrator Level: 94.000 dBSPL dBm (Input Power): 600.0 ohm W(watts) (Input Power): 8.000 ohm

• DCX

DC Output 1: 0.000 V
DC Output 1: Off
DC Output 2: 0.000 V
DC Output 2: Off
Port A (hex): 00
Port B (hex): 00
Port C (hex): 00

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Port D (hex): 00

• Clocks

Output Rate: Track Output SR

Sync Out Level: 3.300 V
Sync Out Polarity: Normal
Timebase Reference: Internal
Jitter: Disabled

• Triggers

Source: Off

Input Logic Level: 3.300 V Edge: Rising

Hi Z Gain -10 47k 200k Termination: Verify Connections

Waveform: Sine

Generator Level: -22.300 dBu
DC Offset: 0.000 V
Frequency: 1.00000 kHz

RMS Level (5/2/2023 8:46:58.138 PM)

Ch1 285.2 mVrms

Gain (5/2/2023 8:46:58.138 PM)

Ch1 13.623 dB

THD+N Ratio (5/2/2023 8:46:58.138 PM)

Ch1 ---- %

Frequency (5/2/2023 8:46:58.138 PM)

Ch1 ---- Hz

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Hi Z Gain -10 47k 200k Termination: Level and Gain 47K

1.00000 kHz

Waveform: Sine

Generator Level: -22.300 dBu DC Offset: 0.000 V Frequency:

RMS Level (5/2/2023 8:47:02.014 PM)

Channel Lower Limit Value **Upper Limit** -8.000 dBu -4.000 dBu Ch1 -8.672 dBu

Result: A FAILED

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Dummy Signal Path For Report : Signal Path Setup

Output Connector: Analog Unbalanced

Channels: 2

Source Impedance: 50 ohm
AG52 Generator Option: Installed
Output EQ: None

Input Connector: Analog Unbalanced

Channels: 2

Termination: 100 kohm

Input Bandwidth: AC (<10 Hz) - 90k (192 kHz SR)

Device Delay: 0.000 s
Input EQ: None

References

dBr G: 100.0 mVrms dBm (Output Power): 600.0 ohm W(watts) (Output Power): 8.000 ohm Shared Frequency Reference: 1.00000 kHz dBrA: 1.000 Vrms dBrB: 1.000 Vrms dBrA Offset: 0.000 dB dBrB Offset: 0.000 dB dBSPL1: 10.00 mVrms dBSPL2: 10.00 mVrms dBSPL1 Calibrator Level: 94.000 dBSPL dBSPL2 Calibrator Level: 94.000 dBSPL 600.0 ohm dBm (Input Power): W(watts) (Input Power): 8.000 ohm

• DCX

DC Output 1: 0.000 V DC Output 1: Off 0.000 V DC Output 2: DC Output 2: Off Port A (hex): 00 Port B (hex): 00 00 Port C (hex): 00 Port D (hex):

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• Clocks

Output Rate: Track Output SR

Sync Out Level: 3.300 V
Sync Out Polarity: Normal
Timebase Reference: Internal
Jitter: Disabled

• Triggers

Source: Off

Input Logic Level: 3.300 V Edge: Rising

Dummy Signal Path For Report : Verify Connections

Waveform: Sine

Generator Level: 100.0 mVrms

DC Offset: 0.000 V

Frequency: 1.00000 kHz

RMS Level (5/2/2023 8:47:05.618 PM)

Ch1 285.9 mVrms Ch2 287.7 mVrms

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