Modern LNA Design for Wireless Applications

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***Abstract*—This paper is the final project for EENG429 (Active RF & Microwaves). It will discuss the design process of a low noise amplifier (LNA). The team chose an operating frequency of 2.5 GHz, a 1.6 dB or less noise figure, and a gain of 16 dB for the LNA. The project will explore low noise amplifier concepts from a theoretical standpoint then discuss schematic design, simulation results, tuning and optimization, Smith charts, and a final land pattern layout. This project will encompass a wide variety of concepts to ensure that a proper LNA is designed from start to finish. The design process will be replicated through utilizing the software ADS by Keysight.**

***Index Terms*— LNA, ATF-52189, SOT-89, Noise Figure, Gain, Optimization, Schematic, Land Pattern**

I. Introduction

THE use of LNAs is prevalent in wireless communications. Typically, modern wireless communications have a frequency range of 1 to 100 GHz, with wireless local area networks (WLANs) of 2.5 to 5 GHz, and telephone operations from 1.9 to 2.2 GHz. LNAs are mostly integrated within receivers and its main purpose is to amplify a received signal above a noise floor. LNA operation allows a small signal to be received and boosted for demodulation purposes as well.

Therefore, LNAs can be designed and used for a variety of applications. They can be modified for specific frequencies, high gain, and to a specific degree of noise. In this paper, the team decided to go with the ATF-52189 low noise E-pHEMT FET running at a 2.5 GHz frequency point, and looked at the behavior in a frequency sweep of 2 to 3 GHz. A gain of about 16 dB was chosen and a noise figure less than 1.6 dB was desired as well, but to accomplish this, the team needed to analyze S11 and S21's behavior. These S-parameters will need to be optimized to be both at or less than -10 dB to achieve these design goals. The team will go through extensive analysis, design, and tuning and optimization to create a schematic that checks off the specifications. The team will also accommodate DC bias to ensure the transistor works properly and show how the SOT-89 package is used for the layout of this LNA to ultimately see what it would look like in land pattern form.

II. Methods

A. *Specifications*

Choosing the ATF-52189 low noise E-pHEMT FET in combination with the SOT-89 package was sought out after reading over the documentation in the data sheet [1]. Using these two components together would allow an ideal medium power, high linearity amplifier, with a frequency range from 50 MHz to 6 GHz. The team shifted through the data to find an acceptable bias and decided to go with 3 V at 200 mA. This ATF-52189 data sheet also had the acceptable S2P file to go with the bias, so the team attached that to the s2p component for the ADS schematic. Additionally, the SOT-89 datasheet was found for the layout of the land pattern [2]. This is beneficial for the layout part of the project that will occur after the schematics, tuning and optimization, and DC biasing. Altogether, the team had all the documentation and materials necessary to start the project.

B. *Initial Schematic and Simulations*

The team began the first initial schematic design which consisted of two terms, attached to the s2p file for the AFT-52189 in the center. S-parameters were analyzed at and around the 2.5 GHz frequency point and additional figures were simulated to show the behavior. The additional components ran were Gain, Noise Circles, Gs Circles, and Gl circles.

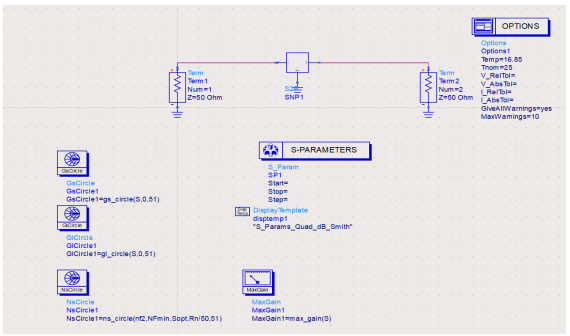

Fig 1. Initial Schematic

To get a better understanding of the initial schematic, it was necessary to run the simulations to see what the load and source gain circles were compared to the noise circles. In addition, the load stability circles and source stability circles were generated to make sure that we had unconditionally stable behavior for the transistor. As seen in Figure 2 below, there are no conditionally stable portions as it fell outside of the Smith chart, therefore the team did not have to work about

having certain unstable portions. In addition, other variables were calculated in the simulation. These were the additional noise parameters that were also included in the s2p file from the datasheet. However, to prove that the schematic worked properly it was calculated directly through ADS from multiple frequencies. ADS was able to take the data and interpolate values itself, and therefore was able to calculate variables like Rn, NFmin, and Sopt. Figure 2 also shows the Smith chart with markers for these designated variables.

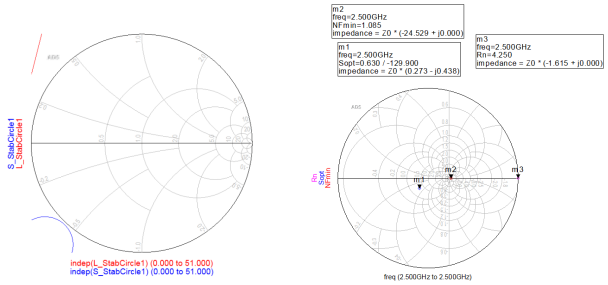

Fig 2. Stability Circles and Variables

The noise parameters were cross checked with the datasheet and approved to keep moving on. Therefore, the additional circles were simulated and can be found in Figure 4. As one can see the Gl circle goes through the center which means there is no additional need for any inductive loading to be added to the schematic as well. Then markers were placed for the Gl smith chart and then for the Gs versus Noise Smith Chart for the impedance matching network.

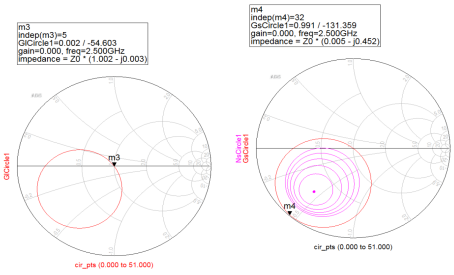

Fig 3. Noise Circles vs. Gl and Gs Circles

C. Second Schematic and Simulations

Once those smith charts were generated, the team continued with the Gl and Gs markers with respect to noise. These values were utilized to come up with a matching design network through using hand calculations with a calculator for the impedance matching portion. The process required Lecture 9's Impedance Transformers and Matching Networks, so the team used those methods to calculate the values for the capacitors and inductors [3]. Also, the markers from Figure 3 were used for its impedance values with respect to the source and load and the team came up with a new matching schematic shown in Figure 4.

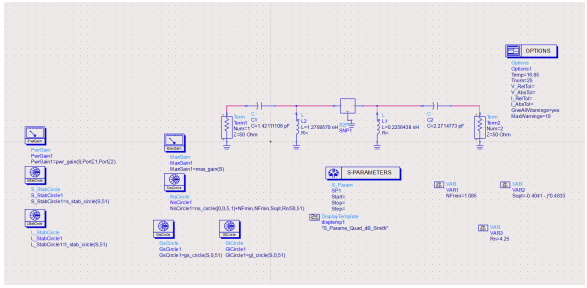

Fig 4. Second Design Schematic

This draft schematic has the added inductors and capacitor values necessary for a simulation run. A simulation was conducted and a list was generated to see the behavior at 2.5 GHz. This would give great insight about the gain value and noise figure for this schematic and if additional tuning and optimization needed to be done. Once the list was generated, there was a gain value of 16.252 dB which was good as it was close to the 16 dB value from the datasheet. However, the noise figure that should be around 1.6 dB was reading 5.241 dB which is too high for a low noise amplifier. The team needed to do further work to get the noise figure to be lower.

D. Tuning and Optimization

The team decided to simplify the schematic and add optimization goals and tuning capabilities to the schematic to ensure that the specifications were reached. The team added four goals which included a power gain of around 16 dB, a noise figure of less than 1.6 dB, a S11 value lower than -10 dB, and a S22 value lower than -10 dB. The S-parameter goals were added to ensure proper behavior within the transistor and allow a compromise between the gain, noise, and properties of the transistor. The team then added tuning to the inductors and capacitors in case the optimization goals could not be met, however after running the optimization a couple of times, the team was able to get really good results that passed the goals and tuning was not necessary. The results of the optimization was a value of -11.9 dB for S11, -11.56 dB for S22, a power gain of 15.039 dB, and a noise figure of 1.183 dB. The team was satisfied with those numbers and moved on to the next step.

Fig 5. Optimization Goals

E. DC Bias Network

Another important part of the design process for the LNA is creating a DC biasing network for the 3V at 200 mA specified biasing. This is due to the fact that a resistor of the right value needs to be added to the network as well. It also

needs to have additional capacitors and inductors due to the RF choke and DC blocks available. For the RF choke a baseline of X_L = 500 Ω and for the DC block X_C = 2 Ω is used. Now starting off with the calculations for the inductor and capacitor values the team arrived at equations 1 and 2.

$$L_{2.5} = \frac{x_L}{2\pi f} = \frac{500}{2\pi(2.5\ GHz)} = 31.83\ \text{nH} \quad (1)$$

$$C_{2.5} = \frac{1}{2\pi x_c} = \frac{1}{2\pi(2\ \Omega)} = 31.83\ \text{pF} \quad (2)$$

With these values used for the RF choke and DC block, the schematic was elaborated on from Figure 5. In addition, the DC bias was created from this schematic to get the resistor value which is attached to the DC voltage source. Figure 6 shows the circuit for it.

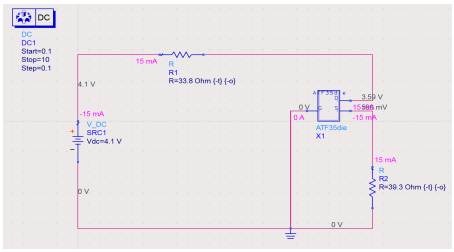

Fig 6. DC Biasing Circuit

Unfortunately, the team was unable to find the ATF-52189 P-spice model for the transistor, so for designing purposes the team used the zap file from the ATF-35143 model and tuned it to get as close to 3 V as possible, due to the fact that this transistor did not have as high of a capacity to do 200 mA. However, the team was able to proceed and create a schematic to follow for the layout modeling as seen in Figure 7.

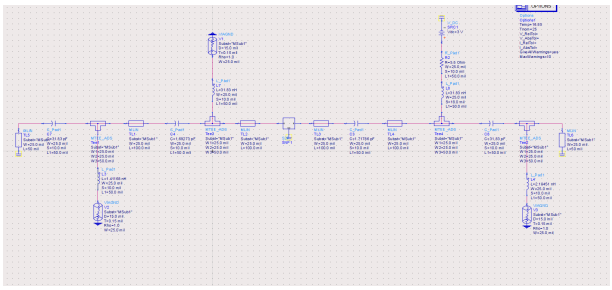

Fig 7. Final ADS Schematic with Pads

F. Layout Modeling

Utilizing the SOT-89 with the schematic was necessary to show the land pattern of the LNA. Once the layout was generated, the team was able to create the small outline transistor and place the schematic components accordingly to the connector pads. The components were tapered and the pads were adjusted in width to ensure that each component was properly connected. The team was able to create Figure 8, which is the LNA with all of the components using the R18 package size and is now ready for possible fabrication.

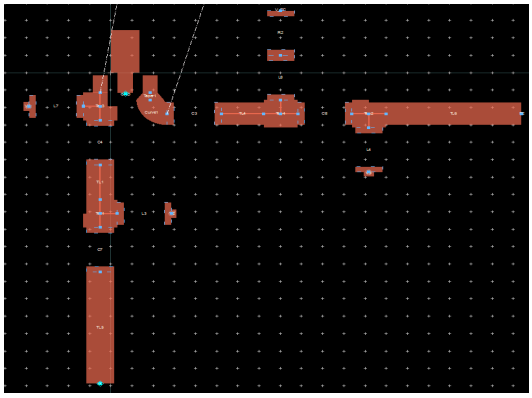

Fig 8. Land Pattern of LNA

III. Results

Altogether, the team was able to design a low noise amplifier that reached its specifications at 2.5 GHz. The team was able to take a transistor and small outline transistor package and design it from its S2P file to a complete schematic. The team went through an extensive design process of multiple schematics and simulations to be able to create a unique LNA from start to finish. The only note of the project was not being able to find the P-spice model for the transistor, so the ATF-35143 was used. The team used concepts from EENG 429 to understand how DC biasing, Smith charts, optimization strategies, S-parameters, and many components come together in a design process. The team was successful in meeting the defined goals and learned many lessons in the process.

ACKNOWLEDGEMENTS

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References

[1]"ATF-52189-BLK," DigiKey. [Online]. Available: https://www.digikey.com/en/products/detail/broadcom-limited/ATF-52189-BLK/1233284?utm_adgroup=Semiconductor+Modules&utm_source=google&utm_medium=cpc&utm_campaign=Dynamic+Search_EN_Product&utm_term=&utm_content=Semiconductor+Modules&gclid=Cj0KCQjwvYSEBhDjARIsAJMn0lgGj_H0-Tl2mBudVIwnl8BffAPNVTF2M1afKhIl_51Y4JVlEbLLHr0aArksEALw_wcB. [Accessed: 22-Apr-2021].

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