**EDA HW1**

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**(1) Record different configurations of the core utilization, clock period, DRC violations, slack, chip area, and wire length. Furthermore, explain the observation of the experiment. (Try more than 5 different configurations to get full points in this question.)**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Core Utilization | Clock Period | DRC violations | Slack | Chip Area (um^2) | Wire length (um) |
| 0.4 | 600 | 0 | 5.169 | 62888.35 | 187609.9 |
| 0.4 | 400 | 16 | -81.9 | 62888.35 | 221149.8 |
| 0.5 | 600 | 1 | -47.4 | 50917 | 188329.2 |
| 0.5 | 400 | 6 | -81.1 | 50917 | 215984 |
| 0.6 | 600 | 1 | 2.2 | 42877.8 | 186532.9 |
| 0.6 | 400 | 16 | -81.9 | 42877.8 | 221149.752 |
| 0.7 | 600 | 4 | 8.6 | 37121.98 | 175988.9 |
| 0.7 | 400 | 3 | -68.6 | 37121.98 | 199177.2 |
| 0.8 | 600 | 11 | -21.3 | 32789.09 | 164378.552 |
| 0.8 | 400 | 24 | -67.8 | 32789.09 | 181556.24 |

Table 1: Experiment results

I’ve conducted around 100 different settings of core utilization and clock period. The above table (Table 1) shows 10 of the results from the settings.

As the table shows, we can observe that chip area is associated with core utilization. As the core utilization becomes larger, the value for chip area decreases. But the decrease isn’t linear. The decrease is around 12000 when increase core utilization from 0.4 to 0.5 but decrease only 5000 when increase from 0.7 to 0.8.

On top of that, we can also see that clock period is associated with wire length. The value of wire length doesn’t have large difference between different settings of core utilization but have similar values when having the same clock period. I also notice that the value of wire length drops when increasing the clock period. But core utilization still affects wire length in a way since when increasing the core utilization, the value of wire length decreases a little bit but not as much compared to the clock period.

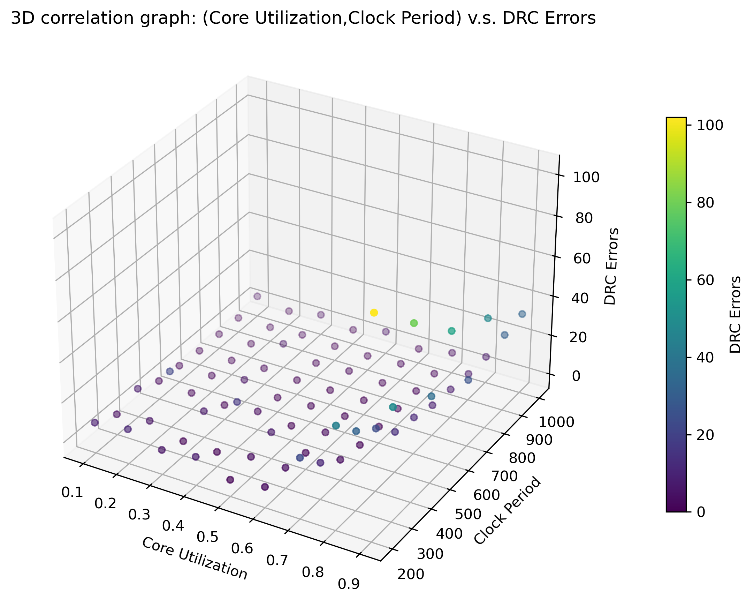
As for the slack time and DRC violations, I’ve noticed that when increasing the core utilization, I need to also increase the clock period to not get any DRC violations or a negative slack time. And there seems to be a limitation of the amount of clock period for a specific setting of core utilization so that there would be no DRC violation or negative slack time.

**(2)Explain how the adjustments of the clock period and the core utilization affect the metrics (DRC violations, slack, chip area, and wire length).**

***The following graphs are the correlation graphs between core utilization, clock period and the four metrics to better visualize how the adjustments of core utilization and clock period affect the metrics. Arrows represent the effectiveness of the two adjustments have on the matrix when increasing. (ex.* *clock period↓: when increasing clock period the matrix will go down)***

**DRC violation: (core utilization↑↑ clock period↓)**

Fig. (Left) & Fig. 2(Right)

一張含有 文字, 圖表, 螢幕擷取畫面, 行 的圖片

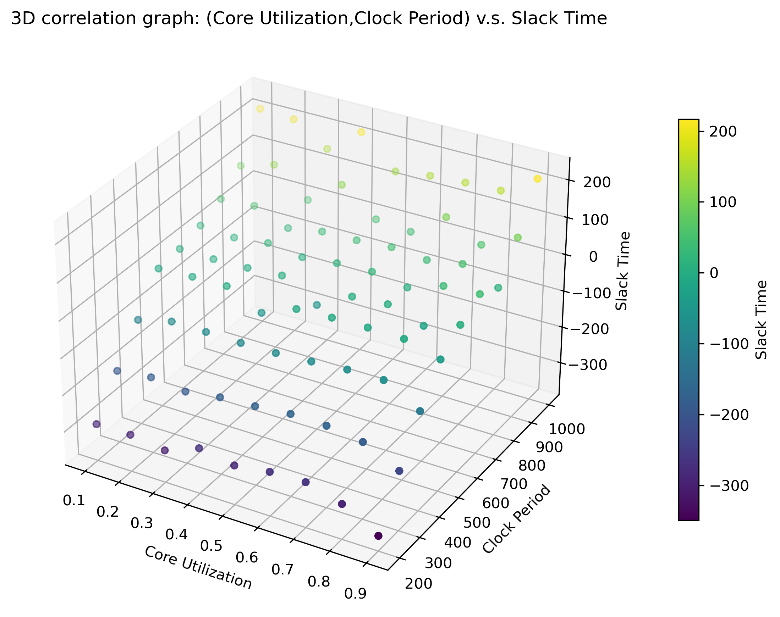
AI 產生的內容可能不正確。

The graph (Fig.1) shows the changes in DRC errors when adjusting. The graph on the right (Fig. 2) have the points that the DRC errors are above 0 which are marked red and the others points green.

As the graphs show, we can see that there is an upward trend when the values of core utilization increase and a downward trend when the values of clock period increase. But the effectiveness of the core utilization is more powerful than clock period since there are none of the points that have 0 DRC violation when the core utilization is up to 0.9 even when the clock period is also up to 1000.

**Slack time: (core utilization≈ clock period↑↑)**

Fig. 3(Left) & Fig. 4(Right)

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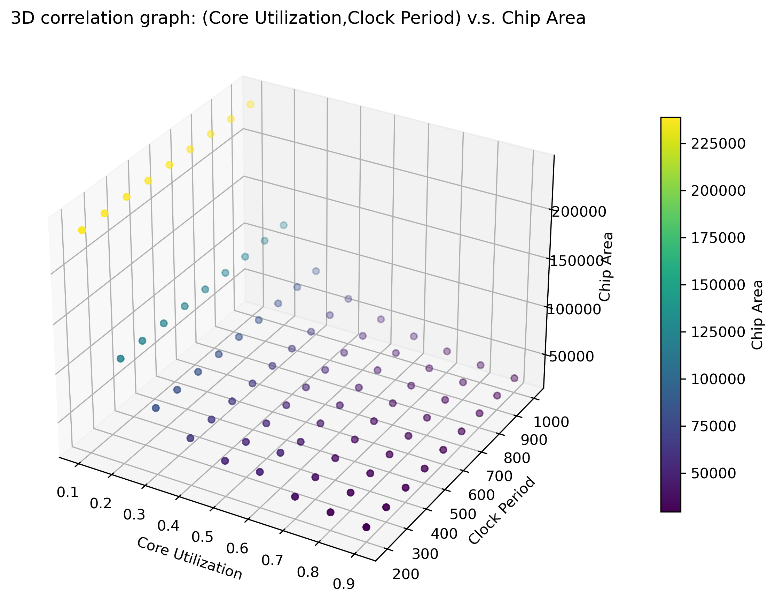
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The graph (Fig.3) shows the changes in Slack time when adjusting. The graph on the right (Fig. 4) has the points that the Slack time are below 0 which are marked red, and the others points green (Slack time >= 0).

As the graph (Fig. 4) shows, we can see that slack time is strongly affected by the values of clock period but not core utilization. The value of slack time is affected by both core utilization and clock period. But if we only look at the graph on the left which only marks the points green if its slack time is above 0, we can see that the points where the clock period above 600~700 are all green. Different core utilizations have their own minimum clock period that their slack time is not negative but nonetheless the clock periods are all between 600-700 which is quite interesting.

**Chip area: (core utilization↓↓↓ clock period X )**

Fig. 5



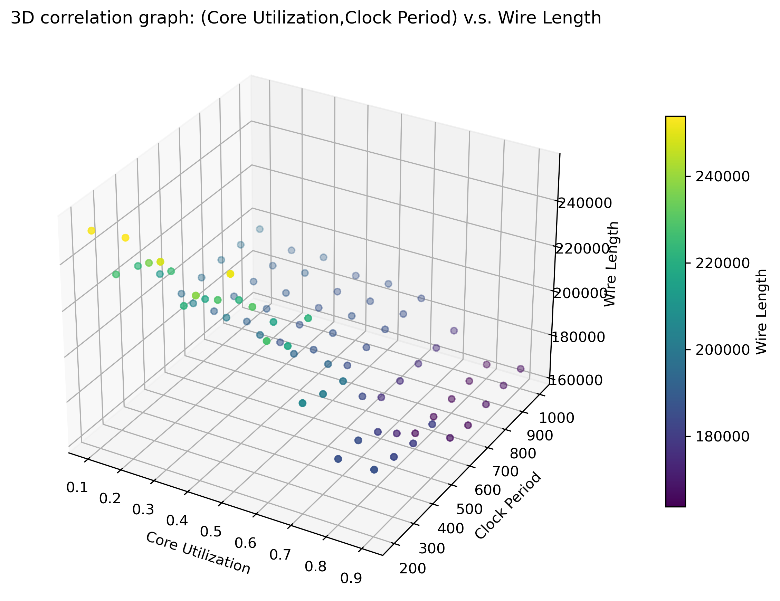
As the above graph and the table from Q1 show, chip area is directly affected by the values of core utilization, it’s a fixed values with the same core utilization. But we can see that as the core utilization goes up, the amount of decrease that has on the chip area become smaller.

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Core  utilization | 0.1 | 0.2 | 0.3 | 0.4 | 0.5 | 0.6 | 0.7 | 0.8 | 0.9 |
| Chip area | 238932 | 122090 | 82695 | 62888 | 50916 | 42877 | 37121 | 32789 | 29387 |
| Difference | - | 116842 | 39395 | 19807 | 11972 | 8039 | 5756 | 4332 | 3402 |

Table 2: Difference represents the difference from the previous columns.

Wire length: **(core utilization↓↓↓ clock period↓)**

Fig.6



There are some interesting findings when the result been plot. As the above graph (Fig.6) shows, we can see that there is a down trend when the core utilization increases. But there is a catch, the values of wire length changes dramatically when the clock period is low but are relatively mellow when clock period is above 500-600. Both core utilization and clock period can affect the wire length but at different levels. The main force for the wire length to be small is to make core utilization smaller but the clock period can affect the values that can be decrease in wire length.

**(3)Explain the purpose of inserting well tap cell.**

To prevent latch-up (a short circuit between VDD and GND) issues which can cause high power consumption or circuit failure. And ensure the circuit functions correctly by providing low-resistance path for well biasing (N-well to VDD, P-well to GND).

* 1. **(4)Show the configuration from your best result. The information to be included in the configuration is listed below. Please try to maintain non-negative slack and zero DRC violations.**
  2. i. Clock period (in file *sha256.sdc*)
  3. Clock period : 575

1. 
   1. ii. Slack time (in generated file *timing.rpt*)
   2. Slack time: 1.8
2. 一張含有 文字, 螢幕擷取畫面, 字型 的圖片

   AI 產生的內容可能不正確。
   1. iii. Total area of chip (in generated file *summary.rpt*)
3. Total area of chip: 42877.797 um^2
4. 一張含有 文字, 字型, 螢幕擷取畫面, 數字 的圖片

   AI 產生的內容可能不正確。
   1. iv. Total wire length (in generated file *summary.rpt*)
   2. Total wire length: 187365.0720 um
5. 一張含有 文字, 字型, 螢幕擷取畫面, 數字 的圖片

   AI 產生的內容可能不正確。
   1. v. DRC violations (in generated file *drc.rpt*).
   2. DRC violations: 0
6. 一張含有 文字, 螢幕擷取畫面, 字型 的圖片

   AI 產生的內容可能不正確。
   1. **(5) Show the final chip layout of your best result generated by Innovus (use print-screen to save the final layout and paste on the report)**
7. 一張含有 文字, 螢幕擷取畫面, 鮮豔, 多媒體軟體 的圖片

   AI 產生的內容可能不正確。
8. 一張含有 文字, 螢幕擷取畫面, 軟體, 電子產品 的圖片

   AI 產生的內容可能不正確。