University of Karachi

Second Semester Examination **MCQ 30 Marks**

Time 30 Min **Date =**

Subject : Industrial Electronics SST 670

1 The word demultiplex means _____
a) One into many
b) Many into one
c) Distributor
d) One into many as well as Distributor

2 In 1-to-4 demultiplexer, how many select lines are required?
a) 2
b) 3
c) 4
d) 5

3 How many select lines are required for a 1-to-8 demultiplexer?
a) 2
b) 3
c) 4
d) 5

4 1. 4 to 1 MUX would have _____
a) 2 inputs
b) 3 inputs
c) 4 inputs
d) 5 inputs

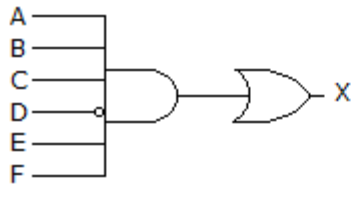
5 Which of the following circuit can be used as parallel to serial converter?
a) Multiplexer
b) Demultiplexer
c) Decoder
d) Digital counter

6 A combinational circuit is one in which the output depends on the _____
a) Input combination at the time
b) Input combination and the previous output
c) Input combination at that time and the previous input combination
d) Present output and the previous output

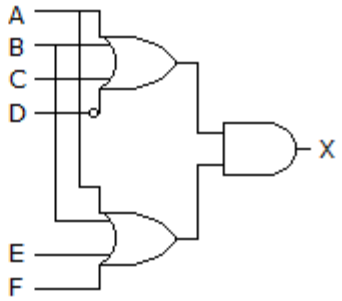
7 A basic multiplexer principle can be demonstrated through the use of a _____
a) Single-pole relay
b) DPDT switch
c) Rotary switch
d) Linear stepper

8 What is the function of an enable input on a multiplexer chip?
a) To apply Vcc
b) To connect ground
c) To active the entire chip
d) To active one half of the chip

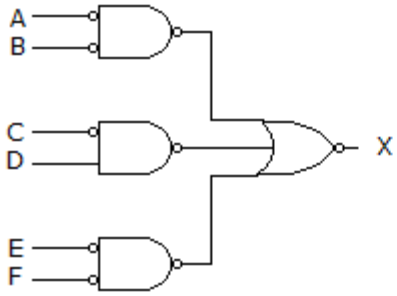
9 Which of the circuits in figure (a to d) is the sum-of-products implementation of figure (e)?



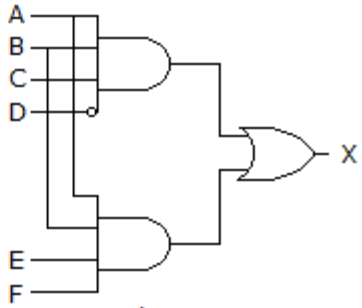
a.



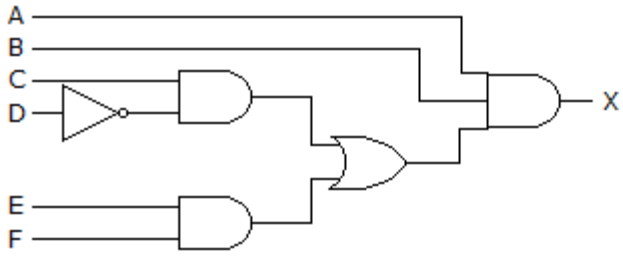
b.



c.



d.

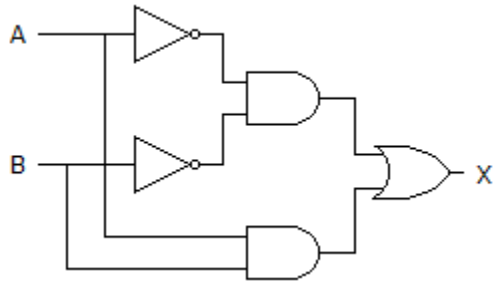


e.

a) a
b) b

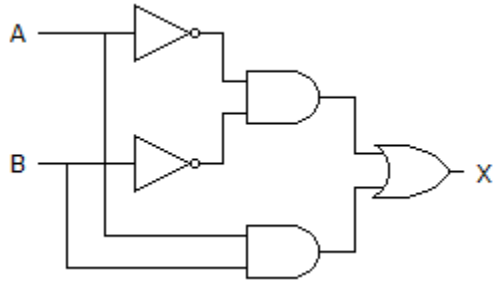
c) c
d) d

10 Which of the following logic expressions represents the logic diagram shown?



a) X=AB'+A'B
b) X=(AB)'+AB
c) X=(AB)'+A'B'
d) X=A'B'+AB

11 What type of logic circuit is represented by the figure shown below?



a) XOR
b) XNOR
c) AND
d) XAND

12 The decimal number system represents the decimal number in the form of _____
a) Hexadecimal
b) Binary coded
c) Octal
d) Decimal

13 2^9 input circuit will have total of _____
a) 32 entries
b) 128 entries
c) 256 entries
d) 512 entries

14 The output sum of two decimal digits can be represented in _____
a) Gray Code
b) Excess-3

c) BCD
d) Hexadecimal

15 The addition of two decimal digits in BCD can be done through _____
a) BCD adder
b) Full adder
c) Ripple carry adder
d) Carry look ahead

16 3 bits full adder contains _____
a) 3 combinational inputs
b) 4 combinational inputs
c) 6 combinational inputs
d) 8 combinational inputs

17 The simplified expression of full adder carry is _____
a) c = xy+xz+yz
b) c = xy+xz
c) c = xy+yz
d) c = x+y+z

18 Decimal digit in BCD can be represented by _____
a) 1 input line
b) 2 input lines
c) 3 input lines
d) 4 input lines

19 A serial subtractor can be obtained by converting the serial adder by using the _____
a) 1's complement system
b) 2's complement system
c) 10's complement
d) 9's complement

20 What is the frequency of a clock waveform if the period of that waveform is 1.25sec?
a) 8 kHz
b) 0.8 kHz
c) 0.8 MHz
d) 8 MHz

21 Why is parallel data transmission preferred over serial data transmission for most applications?
a) It is much slower
b) It is cheaper
c) More people use it
d) It is much faster

22 What can a relay provide between the triggering source and the output that semiconductor switching devices cannot?
a) Total isolation
b) Faster
c) Higher current rating
d) Total isolation and higher current rating

23 The serial format for transmitting binary information uses _____
a) A single conductor
b) Multiple conductors
c) Infrared technology
d) Fiber-optic

24 Serial communication can be sped up by _____
a) Using silver or gold conductors instead of copper
b) Using high-speed clock signals
c) Adjusting the duty cycle of the binary information
d) Using silver or gold conductors instead of copper and high-speed clock signals

25 The inverter can be produced with how many NAND gates?
a) 2
b) 1
c) 3
d) 4

26 How many NOT gates are required to implement the Boolean expression: X = AB'C + A'BC?
a) 2
b) 3
c) 4
d) 5

27 In serial addition, the addition is carried out _____
a) 3 bit per second
b) Byte by byte
c) Bit by bit
d) All bits at the same time

28 How many shift registers are used in a 4 bit serial adder?
a) 4
b) 3
c) 2
d) 5

29 The summing outputs of a half or full-adder are designated by which Greek symbol?
a) Omega
b) Theta
c) Lambda
d) Sigma

30 Why XOR gate is called an inverter?
a) Because of the same input
b) Because of the same output
c) It behaves like a NOT gate
d) It behaves like a AND gate

31 A logic circuit that provides a HIGH output for both inputs HIGH or both inputs LOW is _____
a) Ex-NOR gate
b) OR gate
c) Ex-OR gate
d) NAND gate

32 What is the major difference between half-adders and full-adders?
a) Full-adders are made up of two half-adders
b) Full adders can handle double-digit numbers
c) Full adders have a carry input capability
d) Half adders can handle only single-digit numbers

33 The binary subtraction of 0 – 0 =?
a) Difference = 0, borrow = 0
b) Difference = 1, borrow = 0
c) Difference = 1, borrow = 1
d) Difference = 0, borrow = 1

34 How many basic binary subtraction operations are possible?
a) 1
b) 4
c) 3
d) 2

35 Which of the examples below expresses the commutative law of multiplication?
a) A + B = B + A
b) A • B = B + A
c) A • (B • C) = (A • B) • C
d) A • B = B • A

36 The Boolean expression Y = (AB)’ is logically equivalent to what single gate?
a) NAND
b) NOR

c) AND
d) OR

37 The observation that a bubbled input OR gate is interchangeable with a bubbled output AND gate is referred to as _____
a) A Karnaugh map
b) DeMorgan's second theorem
c) The commutative law of addition
d) The associative law of multiplication

38 Which of the following is an important feature of the sum-of-products form of expressions?
a) All logic circuits are reduced to nothing more than simple AND and OR operations
b) The delay times are greatly reduced over other forms
c) No signal must pass through more than two gates, not including inverters
d) The maximum number of gates that any signal must pass through is reduced by a factor of two

39 Which of the following expressions is in the product-of-sums form?
a) (A + B)(C + D)
b) (AB)(CD)
c) AB(CD)
d) AB + CD

40 The basic building blocks of the arithmetic unit in a digital computers are _____
a) Subtractors
b) Adders
c) Multiplexer
d) Comparator

41 A digital system consists of _____ types of circuits.
a) 2
b) 3
c) 4
d) 5

42 In a combinational circuit, the output at any time depends only on the _____ at that time.
a) Voltage
b) Intermediate values
c) Input values
d) Clock pulses
43 In a sequential circuit, the output at any time depends only on the input values at that time.
a) Past output values
b) Intermediate values
c) Both past output and present input
d) Present input values

44 All logic operations can be obtained by means of _____
a) AND and NAND operations
b) OR and NOR operations
c) OR and NOT operations
d) NAND and NOR operations

45 The design of an ALU is based on _____
a) Sequential logic
b) Combinational logic
c) Multiplexing
d) De-Multiplexing

46 Let the input of a subtractor is A and B then what the output will be if A = B?
a) 0
b) 1
c) A
d) B

47 The full subtractor can be implemented using _____
a) Two XOR and an OR gates
b) Two half subtractors and an OR gate
c) Two multiplexers and an AND gate
d) Two comparators and an AND gate

48 The output of a subtractor is given by (if A, B and X are the inputs).
a) A AND B XOR X
b) A XOR B XOR X
c) A OR B NOR X
d) A NOR B XOR X

49 The difference between half adder and full adder is _____
a) Half adder has two inputs while full adder has four inputs
b) Half adder has one output while full adder has two outputs
c) Half adder has two inputs while full adder has three inputs
d) All of the Mentioned

50 The method of connecting a driving device to a loading device is known as _____
a) Compatibility
b) Interface
c) Sourcing
d) Sinking

51 All input of NOR as low produces result as _____
a) Low
b) Mid

c) High
d) High Impedance

52 The full form of CMOS is _____
a) Capacitive metal oxide semiconductor
b) Capacitive metallic oxide semiconductor
c) Complementary metal oxide semiconductor
d) Complemented metal oxide semiconductor

53 Two important characteristics of CMOS devices are _____
a) High noise immunity
b) Low static power consumption
c) High resistivity
d) Both high noise immunity and low static power consumption

54 CMOS logic dissipates _____ power than NMOS logic circuits.
a) More
b) Less
c) Equal
d) Very High

55 Which logic is the fastest of all the logic families?
a) TTL
b) ECL
c) HTL
d) DTL

56 Transistor–transistor logic (TTL) is a class of digital circuits built from _____
a) JFET only
b) Bipolar junction transistors (BJT)
c) Resistors
d) Bipolar junction transistors (BJT) and resistors

57 TTL is called transistor–transistor logic because both the logic gating function and the amplifying function are performed by _____
a) Resistors
b) Bipolar junction transistors
c) One transistor
d) Resistors and transistors respectively
58 TTL was invented in 1961 by _____
a) Baker clamp
b) James L. Buie
c) Chris Brown
d) Frank Wanlass

59 Standard TTL circuits operate with a __ volt power supply.
a) 2
b) 4
c) 5
d) 3

60 TTL devices consume substantially _____ power than equivalent CMOS devices at rest.
a) Less
b) More
c) Equal
d) Very High

61 The speed of _____ circuits is limited by the tendency of common emitter circuits to go into saturation.
a) TTL
b) ECL
c) RTL
d) DTL

62 Propagation delay is defined as _____
a) the time taken for the output of a gate to change after the inputs have changed
b) the time taken for the input of a gate to change after the outputs have changed
c) the time taken for the input of a gate to change after the intermediates have changed
d) the time taken for the output of a gate to change after the intermediates have changed

63 Fan-in is defined as _____
a) the number of outputs connected to gate without any degradation in the voltage levels
b) the number of inputs connected to gate without any degradation in the voltage levels
c) the number of outputs connected to gate with degradation in the voltage levels
d) the number of inputs connected to gate with degradation in the voltage levels

64 Fan-in and Fan-out are the characteristics of _____
a) Registers
b) Logic families
c) Sequential Circuits
d) Combinational Circuits

65 Integrated circuits are classified as _____
a) Large, Small and Medium
b) Very Large, Small and Linear
c) Linear and Digital
d) Non-Linear and Digital

66 What must be done to interface TTL to CMOS?
a) A dropping resistor must be used on the CMOS of 12 V supply to reduce it to 5 V for the TTL
b) As long as the CMOS supply voltage is 5 V they can be interfaced (however, the fan-out of

the TTL is limited to five CMOS gates)
c) A 5 V zener diode must be placed across the inputs of the TTL gates in order to protect them from the higher output voltages of the CMOS gates
d) A pull-up resistor must be used between the TTL output-CMOS input node and Vcc; the value of RP will depend on the number of CMOS gates connected to the node

67 Latches constructed with NOR and NAND gates tend to remain in the latched condition due to which configuration feature?
a) Low input voltages
b) Synchronous operation
c) Gate impedance
d) Cross coupling

68 The truth table for an S-R flip-flop has how many VALID entries?
a) 1
b) 2
c) 3
d) 4

69 A basic S-R flip-flop can be constructed by cross-coupling of which basic logic gates?
a) AND or OR gates
b) XOR or XNOR gates
c) NOR or NAND gates
d) AND or NOR gates

70 Whose operations are more faster among the following?
a) Combinational circuits
b) Sequential circuits
c) Latches
d) Flip-flops

71 How many types of sequential circuits are?
a) 2
b) 3
c) 4
d) 5

72 In S-R flip-flop, if Q = 0 the output is said to be _____
a) Set
b) Reset
c) Previous state
d) Current state

73 How many types of flip-flops are?
a) 2
b) 3

c) 4
d) 5

74 On a positive edge-triggered S-R flip-flop, the outputs reflect the input condition when _____
a) The clock pulse is LOW
b) The clock pulse is HIGH
c) The clock pulse transitions from LOW to HIGH
d) The clock pulse transitions from HIGH to LOW

75 If an active-HIGH S-R latch has a 0 on the S input and a 1 on the R input and then the R input goes to 0, the latch will be _____
a) SET
b) RESET
c) Clear
d) Invalid

76 The circuit that is primarily responsible for certain flip-flops to be designated as edge-triggered is the _____
a) Edge-detection circuit
b) NOR latch
c) NAND latch
d) Pulse-steering circuit

77 How is a J-K flip-flop made to toggle?
a) J = 0, K = 0
b) J = 1, K = 0
c) J = 0, K = 1
d) J = 1, K = 1

78 1's complement of 1011101 is _____
a) 0101110
b) 1001101
c) 0100010
d) 1100101

79 1's complement can be easily obtained by using _____
a) Comparator
b) Inverter
c) Adder
d) Subtractor

80 Binary coded decimal is a combination of _____
a) Two binary digits
b) Three binary digits

c) Four binary digits
d) Five binary digits

81 A decimal counter has _____ states.
a) 5
b) 10
c) 15
d) 20

82 BCD counter is also known as _____
a) Parallel counter
b) Decade counter
c) Synchronous counter
d) VLSI counter

83 The parallel outputs of a counter circuit represent the _____
a) Parallel data word
b) Clock frequency
c) Counter modulus
d) Clock count

84 How many natural states will there be in a 4-bit ripple counter?
a) 4
b) 8
c) 16
d) 32

85 One of the major drawbacks to the use of asynchronous counters is that _____
a) Low-frequency applications are limited because of internal propagation delays
b) High-frequency applications are limited because of internal propagation delays
c) Asynchronous counters do not have major drawbacks and are suitable for use in high- and low-frequency counting applications
d) Asynchronous counters do not have propagation delays, which limits their use in high-frequency applications

86 How many different states does a 3-bit asynchronous counter have?
a) 2
b) 4
c) 8
d) 16

87 A 4-bit ripple counter consists of flip-flops, which each have a propagation delay from clock to Q output of 15 ns. For the counter to recycle from 1111 to 0000, it takes a total of _____
a) 15 ns
b) 30 ns

c) 45 ns
d) 60 ns

88 Three cascaded decade counters will divide the input frequency by _____
a) 10
b) 20
c) 100
d) 1000

89 How many clock pulses will be required to completely load serially a 5-bit shift register?
a) 2
b) 3
c) 4
d) 5

90 The instruction used in a program for executing them is stored in the _____
a) CPU
b) Control Unit
c) Memory
d) Microprocessor

91 A flip flop stores _____
a) 10 bit of information
b) 1 bit of information
c) 2 bit of information
d) 3-bit information

92 A minute magnetic toroid is also called as _____
a) Large memory
b) Small memory
c) Core memory
d) Both small and large memory

93 The full form of EPROM is _____
a) Easy Programmable Read Only Memory
b) Erasable Programmable Read Only Memory
c) Eradicate Programmable Read Only Memory
d) Easy Programmable Read Out Memory

94 Which of the following is a reprogrammable gate array?
a) EPROM
b) FPGA
c) Both EPROM and FPGA
d) ROM

95 Exclusive-OR (XOR) logic gates can be constructed from what other logic gates?
a) OR gates only
b) AND gates and NOT gates
c) AND gates, OR gates, and NOT gates
d) OR gates and NOT gates

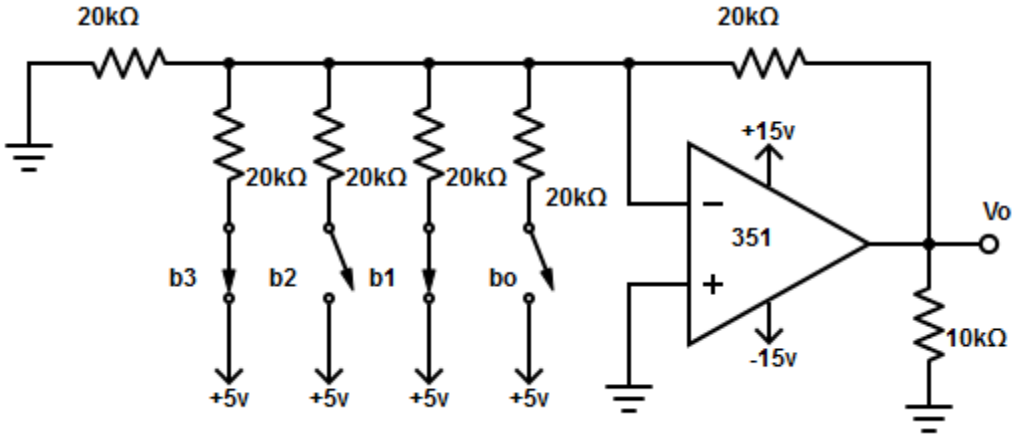
96 Which among the following has long conversion time?
a) Servo converter
b) Dual ramp converter
c) Flash converter
d) None of the mentioned

97 Find out the resolution of 8 bit DAC/ADC?
a) 562
b) 625
c) 256
d) 265

98 The flash type A/D converters are called as
a) Parallel non-inverting A/D converter
b) Parallel counter A/D converter
c) Parallel inverting A/D converter
d) Parallel comparator A/D converter

99 How many clock pulses do a successive approximation converter requires for obtaining a digital output.
a) Twelve
b) Six
c) Eight
d) None of the mentioned

100 For the given circuit find the output voltage?



a) -5.625v
b) -3.50v

c) -4.375v

d) -3.125v

Solution V_o = -20kΩ[(5/2×20kΩ)+0+(5/8×20kΩ)+0]= -3.125v.