GEORGIA INSTITUTE OF TECHNOLOGY

SCHOOL of ELECTRICAL AND COMPUTER ENGINEERING

Lab 4: Feedforward Processor Pipeline

Due Date : Thursday September 28 (11:55 pm)

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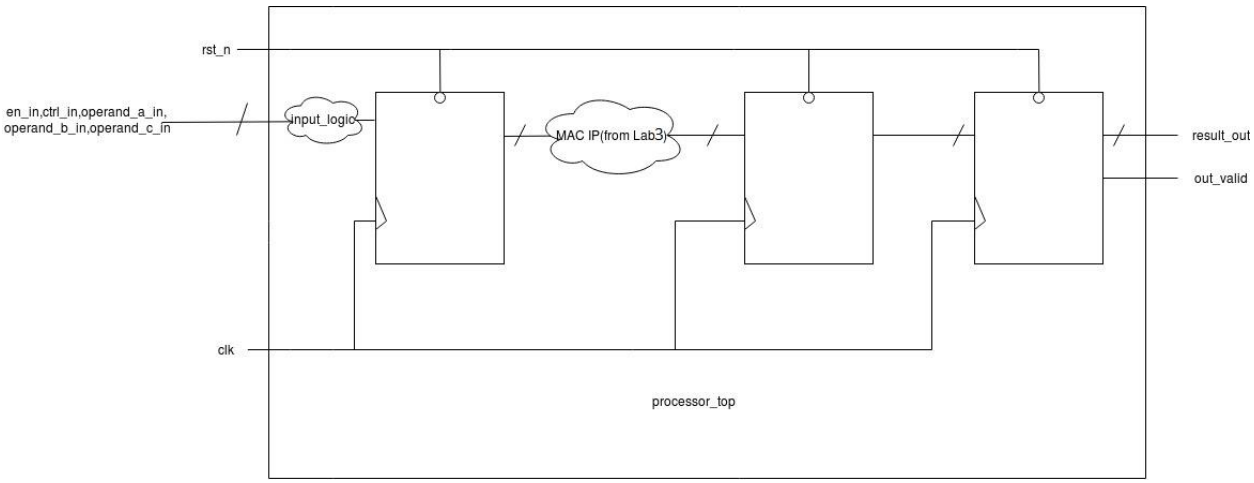
1. Introduction

This lab is serves as an introduction to sequential circuits. In this Lab, we will explore a simple 3 stage processor architecture. The first stage emulates the instruction fetch. The second stage emulates the decode and execute. The third stage emulates the memory access and writeback. For this lab, we ignore things like dependencies, data forwarding, branch predicting and other processor concepts. Also, note that we are also not going to worry about memory access, address and operand decoding. We will have the instruction and operand provided by the test bench, your task is to compute the answer and output it from the design at the end of the third stage (i.e. in the appropriate clock cycle). The template for the processor is provided in the file "processor_top.vhd" in /src directory.

The explanations of the input and output ports are given below.

i. clk => Clock signal
ii. rst_n => Reset signal. Note that the sequential elements that are used in your design should have **asynchronous active low reset**. i.e. if the reset is pulled low, the flops should reset regardless of the state of the clock
iii. en_in => Input enable signal. It qualifies all the inputs. If en_in ='1', you should capture all the inputs (i.e. ctrl and operands)
iv. ctrl_in=> The control signal indicates what operation is to be performed. Use the same table given in Lab_3 for decoding the operations.
v. operand_a_in,operand_b_in,operand_c_in => These are the data inputs
vi. out_valid => Ctrl signal for the output. When ctrl ='1', the output(result_out) is valid
vii. result_out=> the output of the arithmetic operations.



There is a sample input file from which the data is read into the testbench . The testbench dumps out an output file. The block diagram describes the design of the system. Compare this output with the reference output file provided with the assignment. The grading will take into consideration the functional correctness, utilization (area), timing and the power of the design. A good modular design will be helpful to you for debugging. Note that you must create a clock for the Vivado Process Flow. This can be done by adding “lab4_constraints.xdc”to the constraints while creating the project. In this lab, we use a clock of period 25ns. The constraints file contains the name and period of the clock which is created. 3 re-submissions are allowed for this lab. The resources information is obtained from “processor_top_utilization_placed.rpt”. The timing information is obtained from “processor_top_timing_summary_routed.rpt”. The power information is obtained from “processor_top_power_routed.rpt”.

2. **Instructions**
    i. Write the design in vhdl(processor_top.vhd) per the block diagram. The template for the design has been provided processor_top.vhd in /src folder. Verify the design by comparing it with the reference output. (70% of grade)
    ii. Perform Synthesis and Implementation for the design. List the area (#Slice LUTs, #Bonded IO Buffers), power (Dynamic and Static Power) and Timing (Worst Negative slack) (15 % of grade).
    iii. Answer the following question – "There are 3 stages of sequential elements in the design for the signals which are to be propagated from the input to the output. Is it needed that the flops corresponding to all the signals in all the three stages have resettable capability? Explain your answer in not more than 2-3 sentences." (15% of grade)
3. **Deliverables**
    i. Create a PDF which lists the power (Dynamic and Static), #resources (Slice Logic Distribution, IO Information, #Primitives) and Worst Negative Slack of "processor_top.vhd". The title of the document should be of the form "lab4_firstname. lastname.pdf".
    ii. The PDF should also have the answer to the question
    iii. The design top file "processor_top.vhd"
    iv. Other design files needed for running the system (if applicable)
    v. Output file for the design.
    vi. The implemented area(utilization)report, implemented power report and timing report of the mac unit design namely "processor_top_utilization_placed.rpt" ,"processor_top_power_routed.rpt" and "processor_top_timing_summary_routed.rpt"

Move all of these files into a folder "lab4_lastname.firstname".Zip the folder and upload on t-square.

Note : Late submissions are not accepted. In case of extraordinary circumstances, written permission must be obtained from Dr.Madisetti.