ECE 6276
DSP Hardware System Design
Fall 2017

Lab 3

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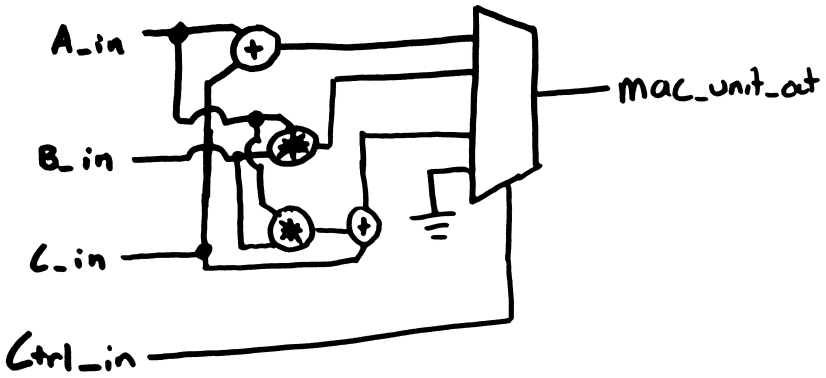
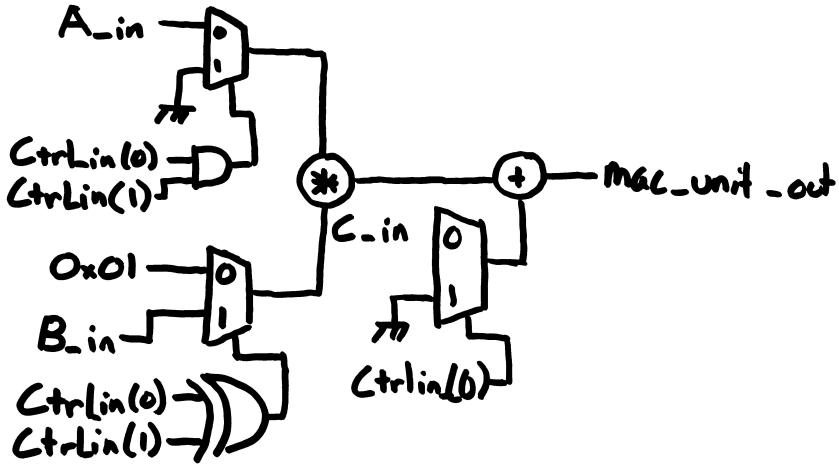
Block Diagrams

Block diagram from lab handout



Updated Block Diagram



Mac not-optimized Slice LUTs

Site Type	Used	Fixed	Available	Util%
CLB LUTs	94	0	663360	0.01
LUT as Logic	94	0	663360	0.01
LUT as Memory	0	0	293760	0.00
CLB Registers	0	0	1326720	0.00
Register as Flip Flop	0	0	1326720	0.00
Register as Latch	0	0	1326720	0.00
CARRY8	11	0	82920	0.01
F7 Muxes	0	0	331680	0.00
F8 Muxes	0	0	165840	0.00
F9 Muxes	0	0	82920	0.00

Mac optimized Slice LUTs

Site Type	Used	Fixed	Available	Util%
CLB LUTs	25	0	663360	<0.01
LUT as Logic	25	0	663360	<0.01
LUT as Memory	0	0	293760	0.00
CLB Registers	0	0	1326720	0.00
Register as Flip Flop	0	0	1326720	0.00
Register as Latch	0	0	1326720	0.00
CARRY8	3	0	82920	<0.01
F7 Muxes	0	0	331680	0.00
F8 Muxes	0	0	165840	0.00
F9 Muxes	0	0	82920	0.00

Mac not-optimized Bonded Buffers

Site Type	Used	Fixed	Available	Util%
Bonded IOB	43	0	832	5.17
HPIOB	43	0	676	6.36
INPUT	26			
OUTPUT	17			
BIDIR	0			
HRIO	0	0	156	0.00
HPIOBDIFFINBUF	0	0	480	0.00
HPIOBDIFFOUTBUF	0	0	480	0.00
HRIODIFFINBUF	0	0	96	0.00
HRIODIFFOUTBUF	0	0	96	0.00
BITSLICE_CONTROL	0	0	192	0.00
BITSLICE_RX_TX	0	0	1248	0.00
BITSLICE_TX	0	0	192	0.00
RIU_OR	0	0	96	0.00

Mac optimized Bonded Buffers

Site Type	Used	Fixed	Available	Util%
Bonded IOB	43	0	832	5.17
HPIOB	43	0	676	6.36
INPUT	26			
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BIDIR	0			
HRIO	0	0	156	0.00
HPIOBDIFFINBUF	0	0	480	0.00
HPIOBDIFFOUTBUF	0	0	480	0.00
HRIODIFFINBUF	0	0	96	0.00
HRIODIFFOUTBUF	0	0	96	0.00
BITSLICE_CONTROL	0	0	192	0.00
BITSLICE_RX_TX	0	0	1248	0.00
BITSLICE_TX	0	0	192	0.00
RIU_OR	0	0	96	0.00

Mac not-optimized Primitives

Ref Name	Used	Functional Category
LUT4	50	CLB
LUT6	26	CLB
INBUF	26	I/O
IBUFCTRL	26	Others
LUT2	24	CLB
LUT3	23	CLB
OBUF	17	I/O
CARRY8	11	CLB
LUT5	6	CLB

Mac optimized Primitives

Ref Name	Used	Functional Category
LUT3	33	CLB
INBUF	26	I/O
IBUFCTRL	26	Others
OBUF	17	I/O
CARRY8	3	CLB
DSP48E2	1	Arithmetic

Mac not-optimized power

Total On–Chip Power (W)	16.770
Dynamic (W)	15.157
Device Static (W)	1.613
Effective TJA (C/W)	0.8
Max Ambient (C)	86.5
Junction Temperature (C)	38.5
Confidence Level	Low
Setting File	–––
Simulation Activity File	–––
Design Nets Matched	NA

Mac optimized power

Total On–Chip Power (W)	20.515
Dynamic (W)	18.814
Device Static (W)	1.701
Effective TJA (C/W)	0.8
Max Ambient (C)	83.4
Junction Temperature (C)	41.6
Confidence Level	Low
Setting File	–––
Simulation Activity File	–––
Design Nets Matched	NA

Comparison of un-optimized and optimized designs

	STD	Updated
Adders	2	1
Multipliers	2	1
Muxes	1	3