ECE 6276
DSP Hardware System Design
Fall 2017

Lab 6

William Sutton

October 12, 2017

Slice LUTs

Site Type	Used	Fixed	Available	Util%
CLB LUTs	954	0	203128	0.47
LUT as Logic	954	0	203128	0.47
LUT as Memory	0	0	112800	0.00
CLB Registers	322	0	406256	0.08
Register as Flip Flop	322	0	406256	0.08
Register as Latch	0	0	406256	0.00
CARRY8	154	0	30300	0.51
F7 Muxes	0	0	121200	0.00
F8 Muxes	0	0	60600	0.00
F9 Muxes	0	0	30300	0.00

IO

Site Type	Used	Fixed	Available	Util%
Bonded IOB	324	0	520	62.31
HPIOB	228	0	416	54.81
INPUT	67			
OUTPUT	161			
BIDIR	0			
HRIO	96	0	104	92.31
INPUT	0			
OUTPUT	96			
BIDIR	0			
HPIOBDIFFINBUF	0	0	192	0.00
HPIOBDIFFOUTBUF	0	0	192	0.00
HRIODIFFINBUF	0	0	48	0.00
HRIODIFFOUTBUF	0	0	48	0.00
BITSLICE_CONTROL	0	0	80	0.00
BITSLICE_RX_TX	0	0	520	0.00
BITSLICE_TX	0	0	80	0.00
RIU_OR	0	0	40	0.00

Primitives

Ref Name	Used	Functional Category
LUT2	715	CLB
FDRE	321	Register
OBUF	257	I/O
LUT3	208	CLB
CARRY8	154	CLB
LUT1	113	CLB
LUT4	94	CLB
INBUF	67	I/O
IBUFCTRL	67	Others
LUT5	22	CLB
DSP48E2	16	Arithmetic
LUT6	12	CLB
FDCE	1	Register
BUFGCE	1	Clock

Mac not-optimized power

Total On-Chip Power (W)	0.603
Dynamic (W)	0.098
Device Static (W)	0.505
Effective TJA (C/W)	1.4
Max Ambient (C)	99.1
Junction Temperature (C)	25.9
Confidence Level	Low
Setting File	---
Simulation Activity File	---
Design Nets Matched	NA

Worst Negative Slack (WNS)

Answer: 43.007ns

| Design Timing Summary
| ---

WNS(ns)	TNS(ns)	TNS Failing Endpoints	TNS Total Endpoints
38.933	0.000	0	257

WHS(ns)	THS(ns)	THS Failing Endpoints	THS Total Endpoints
0.161	0.000	0	257

WPWS(ns)	TPWS(ns)	TPWS Failing Endpoints	TPWS Total Endpoints
24.725	0.000	0	323

Answer to question:

The values of the twiddle factors are chosen because they are a certain angular distance away from each other on the unit circle. Since they are all ROOTS of unity, they all reside on the unit circle itself (therefore making them useful for a DFT). The angle by which they are separated is what actually gets us our 1.8 resolution for the signed numbers.