GEORGIA INSTITUTE OF TECHNOLOGY

SCHOOL of ELECTRICAL AND COMPUTER ENGINEERING

Lab 6: FFT using the Butterfly Technique using Decimation in Time

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Due Date : Thursday October 12 (11:55 pm)

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1. Introduction

FFT is a method of performing Discrete Fourier Transform which basically represents a time domain signal in terms of its components at different discretized frequency levels (frequency bins). In this lab, we will design an FFT Transform system for n=8. The twiddle factors are 9 bits wide and will be provided. Also, note that the multiplication and addition are **signed operations**. The template for fft is provided in "fft_top.vhd" in /src directory. Also, note that some useful data structures have been provided in "fft_pkg.vhd" in /src directory. http://vhdlguru.blogspot.com/2011/06/non-synthesisable-vhdl-code-for-8-point.html is a good reference source for the design. Although the code given in the link is non-synthesizable, you can base your final code on this. The explanations of the input and output ports are given below.

i. clk => Clock signal

ii. rst_n => Reset signal. Note that the sequential elements that are used in your design should have **asynchronous active low reset**. i.e. if the reset is pulled low, the flops should reset regardless of the state of the clock

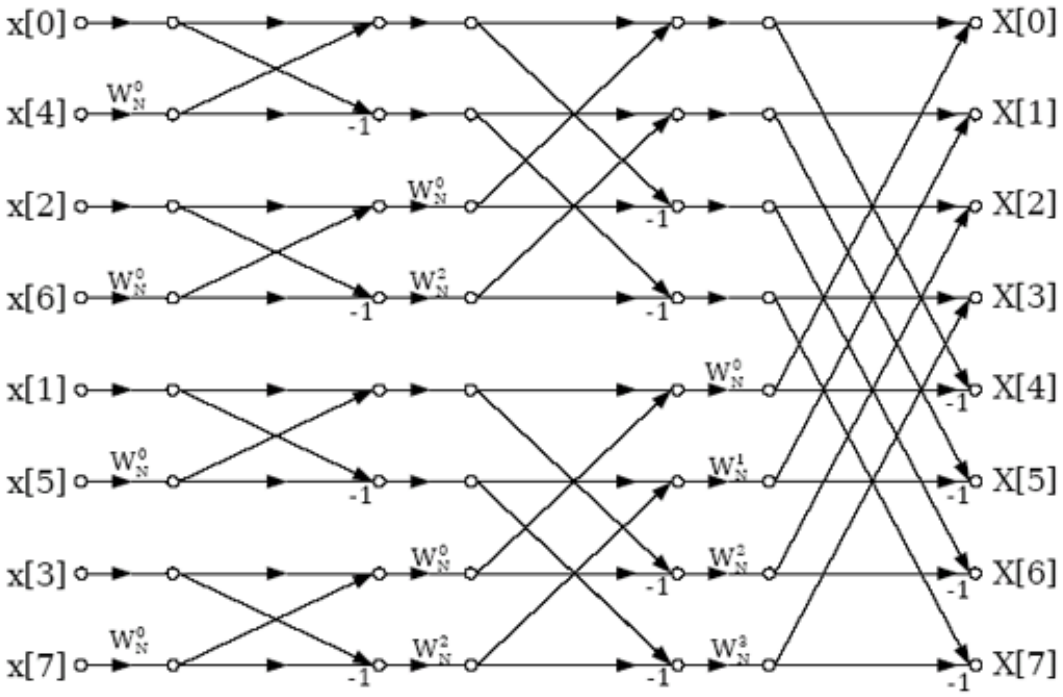
iii. en_in => en_in is the qualifier for the data. When en_in ='1', data which is passed from testbench is valid and is to be captured in the design.

iv. data_input => The input data port from which data is passed to the design. **Note that real data is passed from the design.** Also, data_input is a variable of type input_data_array which is a user defined data-type in "fft_top.pkg". It is an array of 8 elements each element being 8 bits wide. Basically, when en_in ='1', all the 8 data inputs are to be captured in the design.

v. data_valid_out => control signal for the output. When ctrl = '1', the outputs data_output_real and data_output_imag are valid. This

information is useful to the testbench which captures the data only when output is valid.

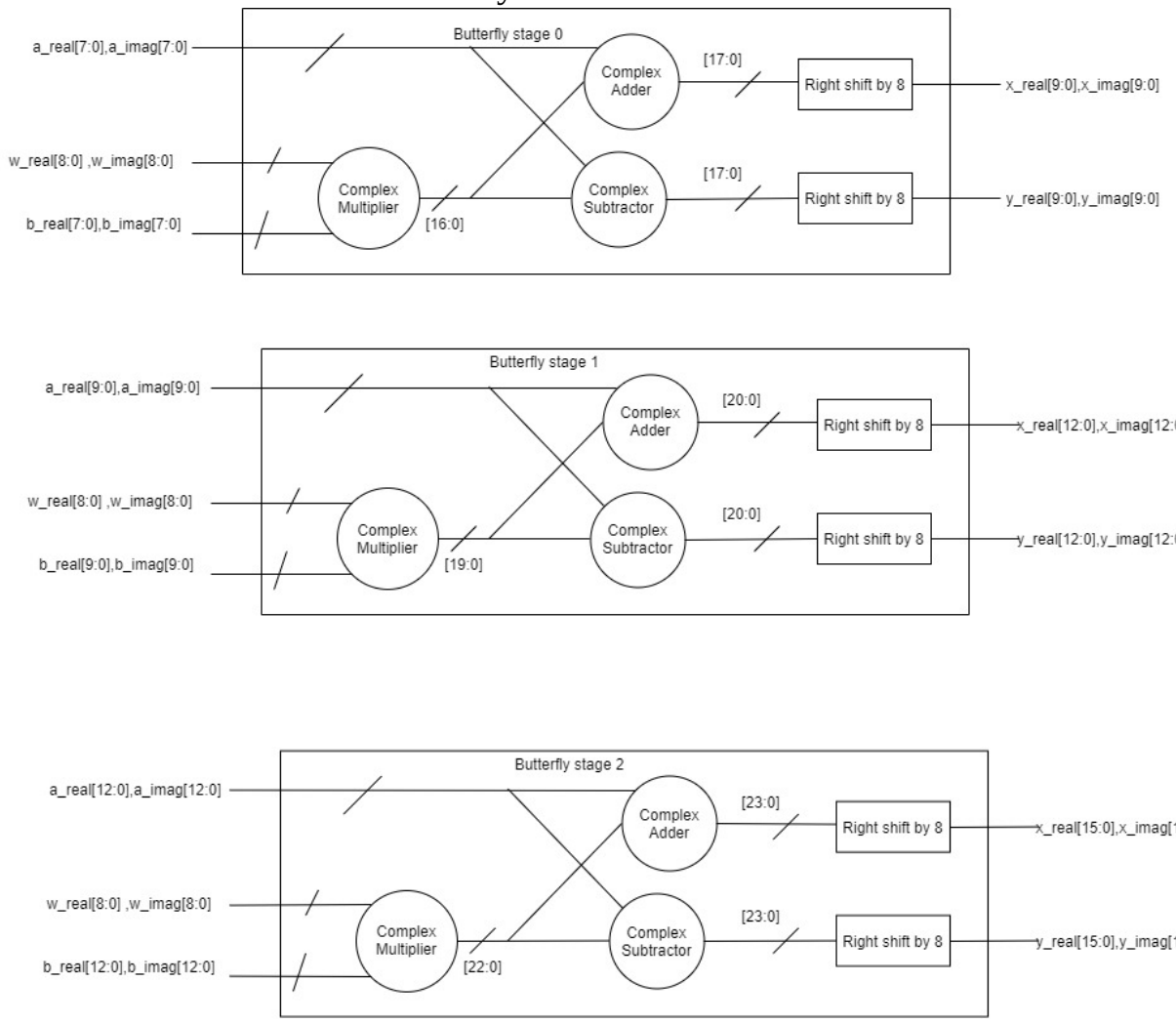
vi. data_output_real and data_output_imag => Outputs from the design. After the complex operations, the real data which is passed into the input is transformed into real and imaginary components. Note that data_output_real and data_output_imag are variables of type output_data_array which is a user defined data-type in “fft_top.pkg”. They are arrays of 8 elements with each element being 16 bits wide. When data_valid_out = ‘1’, all the 16 output values (8 real and 8 imaginary) will be captured by the testbench.



FFT Butterfly Structure [Describes the FFT procedure using Decimation in Time]. (n.d.). Retrieved September 15, 2017, from https://qph.ec.quoracdn.net/main-qimg-657717c02db3efbef5dd37729d676ba1

	Real	Imaginary
w_8^0	011111111	000000000
w_8^1	010110100	101001100
w_8^2	000000000	100000001
w_8^3	101001100	101001100

The table lists the twiddle factors which should be used in the design. The other twiddle factors are not listed as they will not be used in the calculation of FFT.



Taking care of the bit-growth will be among the biggest challenges in this lab. The above block diagram helps you keep track of the bit-growth. Note that there is no imaginary part at the input of the first stage.

Useful Hints: The datatypes declared in the fft_pkg.vhd will be helpful in creating intermediate signals**. Please note that the very first file that you compile should be fft_pkg.vhd because the tb_fft.vhd uses some datatypes declared in the package.**

This system can be implemented in numerous ways with different latencies,area and power. You can use any architecture as long as you can clearly draw the block diagram of your architecture in the report.
There is a sample input file from which the data is read into the testbench . The testbench dumps out an output file. Compare this output with the reference output file provided with the assignment. The output will be the same for any architecture. The grading will take into consideration the functional correctness, utilization (area), and timing of the design. Note that you must create a clock for the Vivado Process Flow. This can be done by adding "constraints_lab6.xdc"to the constraints while creating the project. The constraints file contains the name and period of the clock which is created. 3 re-submissions are allowed for this lab. The resources information is obtained from "fft_top_utilization_placed.rpt". The timing information is obtained from "fft_top_timing_summary_routed.rpt". The power information is obtained from "fft_top_power_routed.rpt".
Note that our design is extremely bad for area but is quick. So the testbench gives a data sample every cycle. In your design, you can choose to use a memory/buffer which stores all these samples and will parse it to main logic at a speed which is decided by the latency of your architecture. This additional memory overhead will not be considered for grading.

2. **Instructions**
    i. Draw the block diagram of the architecture you will be using.
    ii. Write the design in vhdl(fft_top.vhd) per the block diagram. The template for the design has been provided fft_top.vhd in /src folder. Verify the design by comparing it with the reference output. (70% of grade for the first two deliverables). (**Note that if the design is not verified, the block diagram and implementation will not be considered**).
    iii. Perform Synthesis and Implementation for the design. List the area (#Slice LUTs, #Bonded IO Buffers) and timing (Worst Negative slack) (10 % of grade).
    iv. Answer the following question – "What is the rationale behind choosing the values of the twiddle factor as given in the table? Note that the twiddle factors are **signed numbers of resolution 1.8**" (20% of grade) Hint: Think of how you do fractional multiplication for fixed point numbers. We do a right shift of 8 after each stage of the butterfly
3. **Deliverables**
    i. Create a PDF which lists the power (Dynamic and Static), #resources (Slice Logic Distribution, IO Information, #Primitives) and Worst Negative Slack of "fft_top.vhd". The title of the document should be of the form "lab6_firstname. lastname.pdf"
    ii. The PDF should also have the answer to the question
    iii. The design top file "fft_top.vhd"
    iv. Other modules (if applicable)
    v. Output files "sample_output_fft.txt" and "sample_output_fft_cycle.txt"

I have been facing grading issues because students are not following the naming convention of the files and folders. **Please do not move these files into a folder. Upload all the attachments directly on t-square. Also, note that not following the naming conventions or any of the instructions might lead to a penalty.**

Note : Late submissions are not accepted. In case of extraordinary circumstances, written permission must be obtained from Dr.Madisetti.