Instructions for using Xilinx Vivado

The following instructions will help you work with Vivado in the ece linux environment. If you already have Vivado installed on your system, you can used that as well

(The text in green font are comments, and the text in red font are the commands to be executed)

%To enable tcsh,

- tcsh

%Go to the run folder of lab_1, if you have created the lab_1 hierarchy in the home directory, then the command is

- cd ~/lab_1/run

%Create a folder called vivado_run,

- mkdir vivado_run

%Move into vivado_run

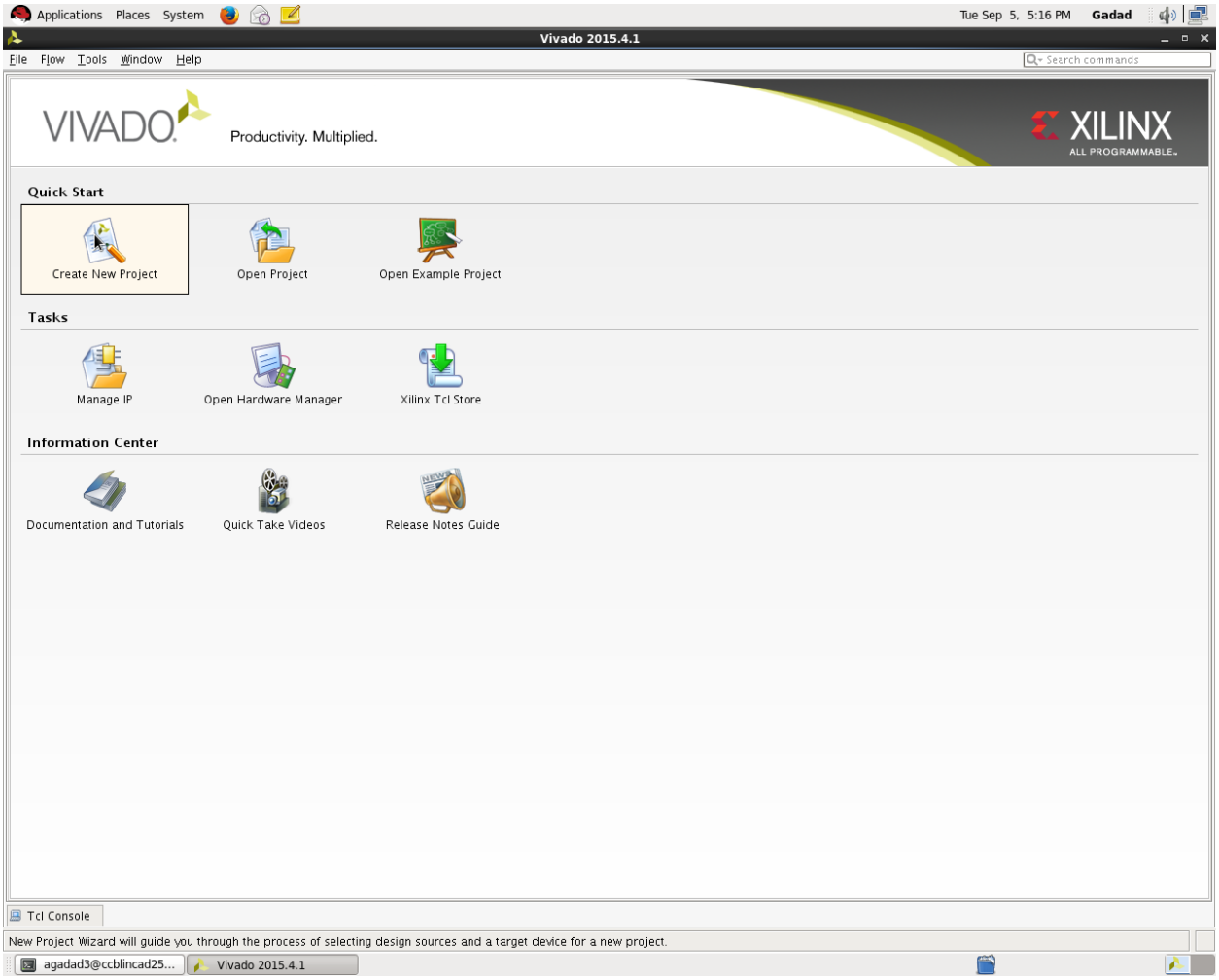
- cd vivado_run

%Source the script

- source /tools/xilinx/vivado201504/Vivado/2015.4/settings64.csh

%Launch Vivado (note that this is a heavy application, close other windows and don't panic if it takes a lot of time to open)

- vivado &


Applications
Places
System
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Gadad
Vivado 2015.4.1
File
Flow
Tools
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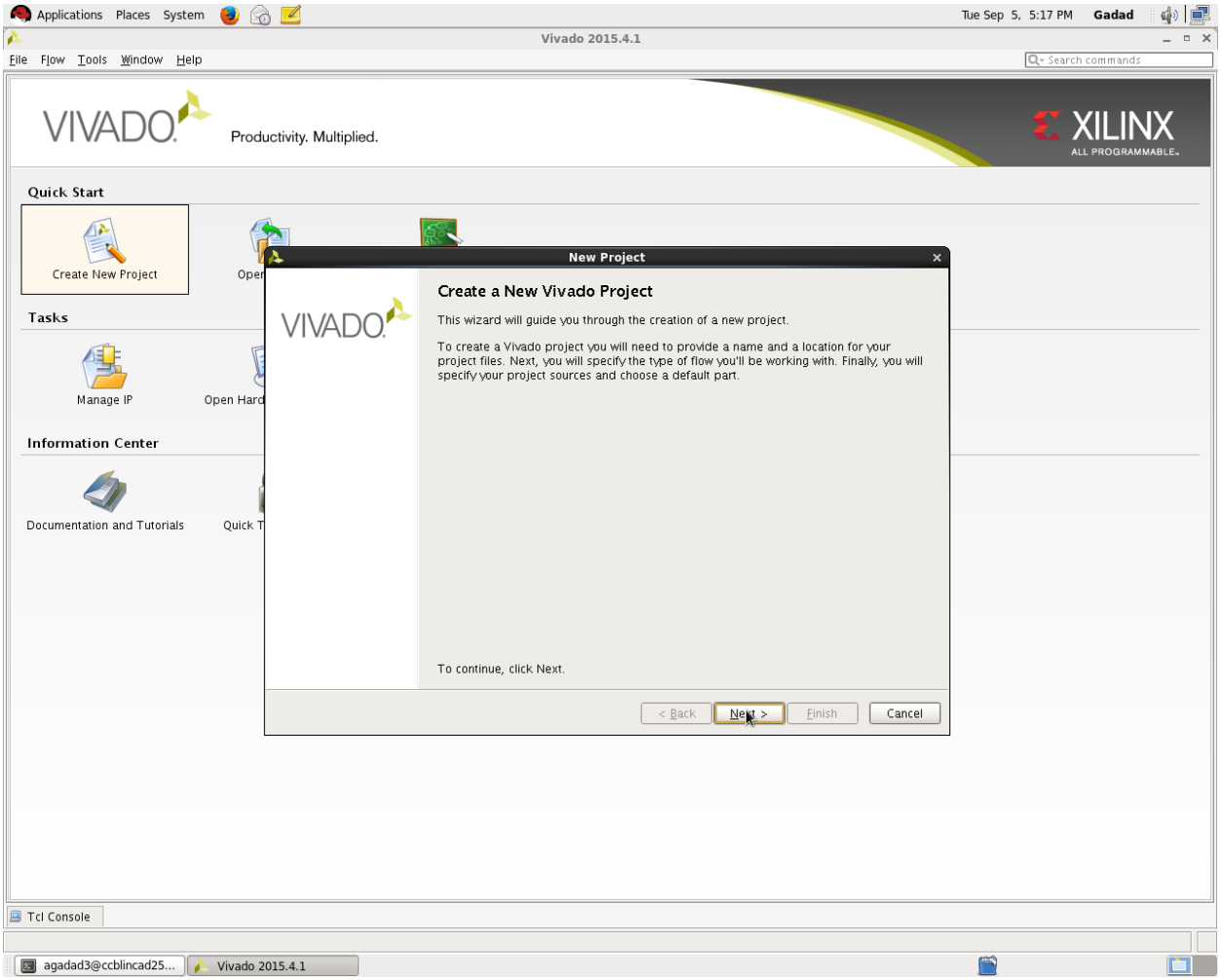
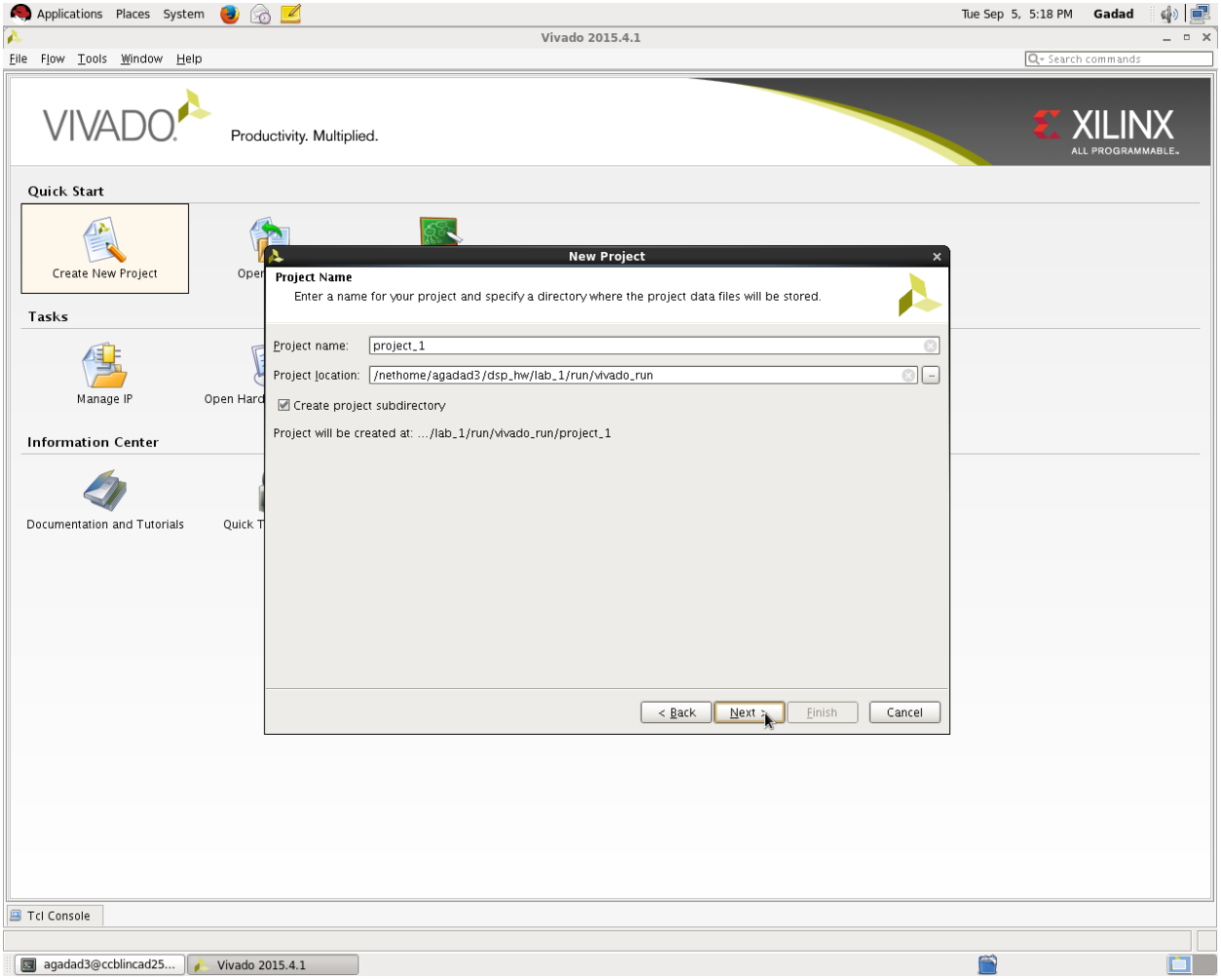
Search commands
VIVADO
Productivity. Multiplied.
XILINX
ALL PROGRAMMABLE.
Quick Start
Create New Project
Open Project
Open Example Project
Tasks
Manage IP
Open Hardware Manager
Xilinx Tcl Store
Information Center
Documentation and Tutorials
Quick Take Videos
Release Notes Guide
Tcl Console
New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.
agadad3@ccblincad25...
Vivado 2015.4.1

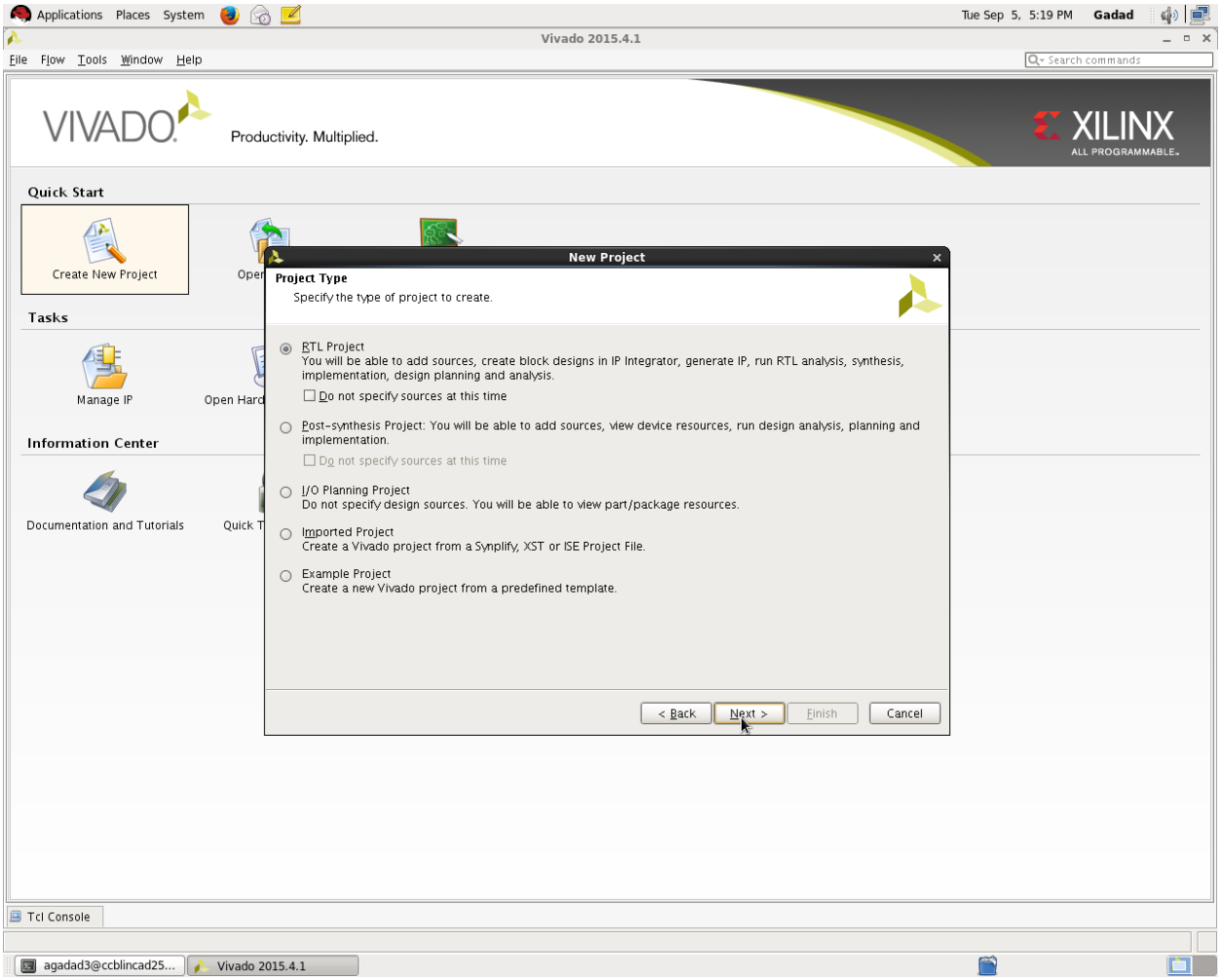
Create new project and click next



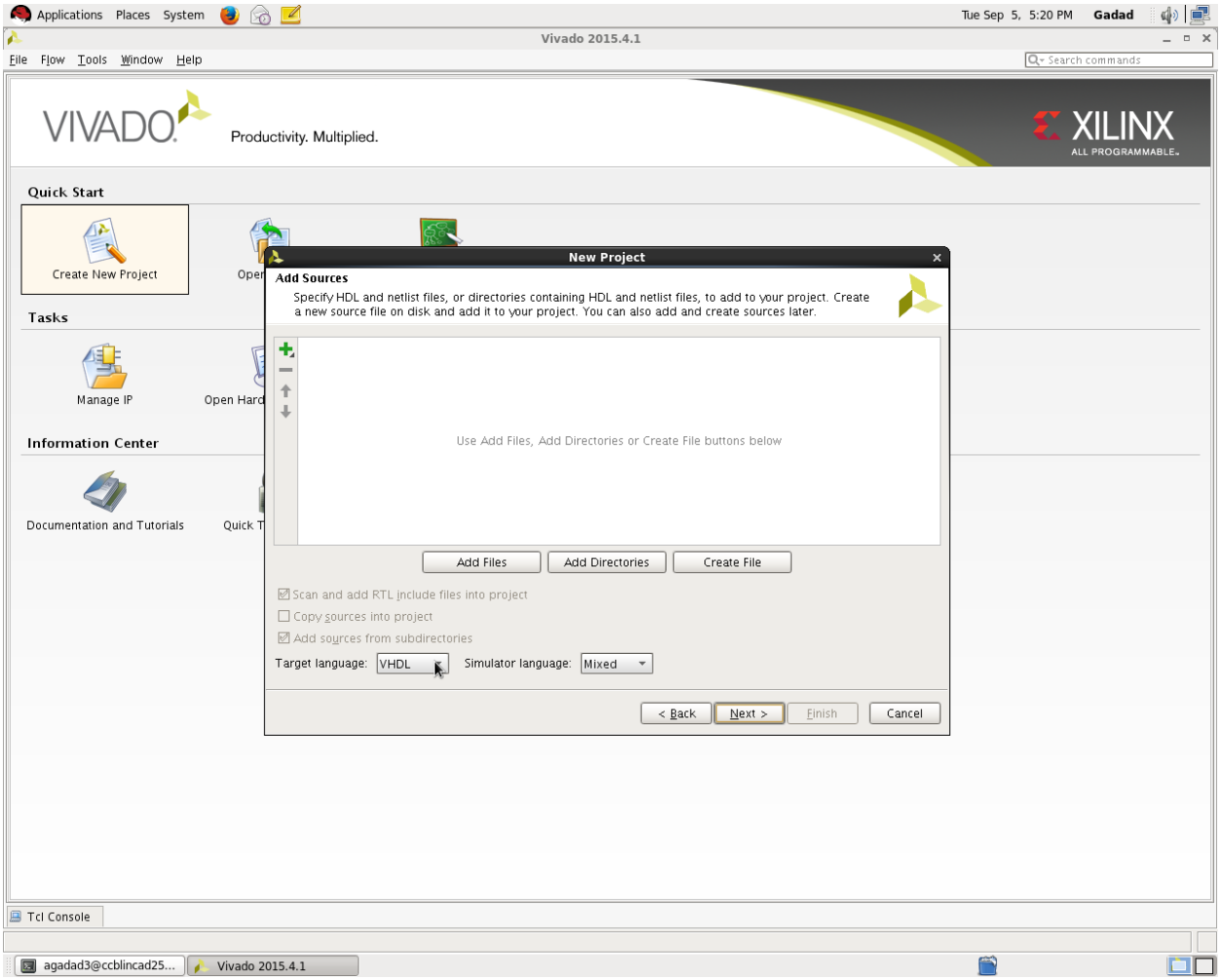
By default, the project will be saved as ‘project_1’ in the folder ‘vivado_run’ and click next



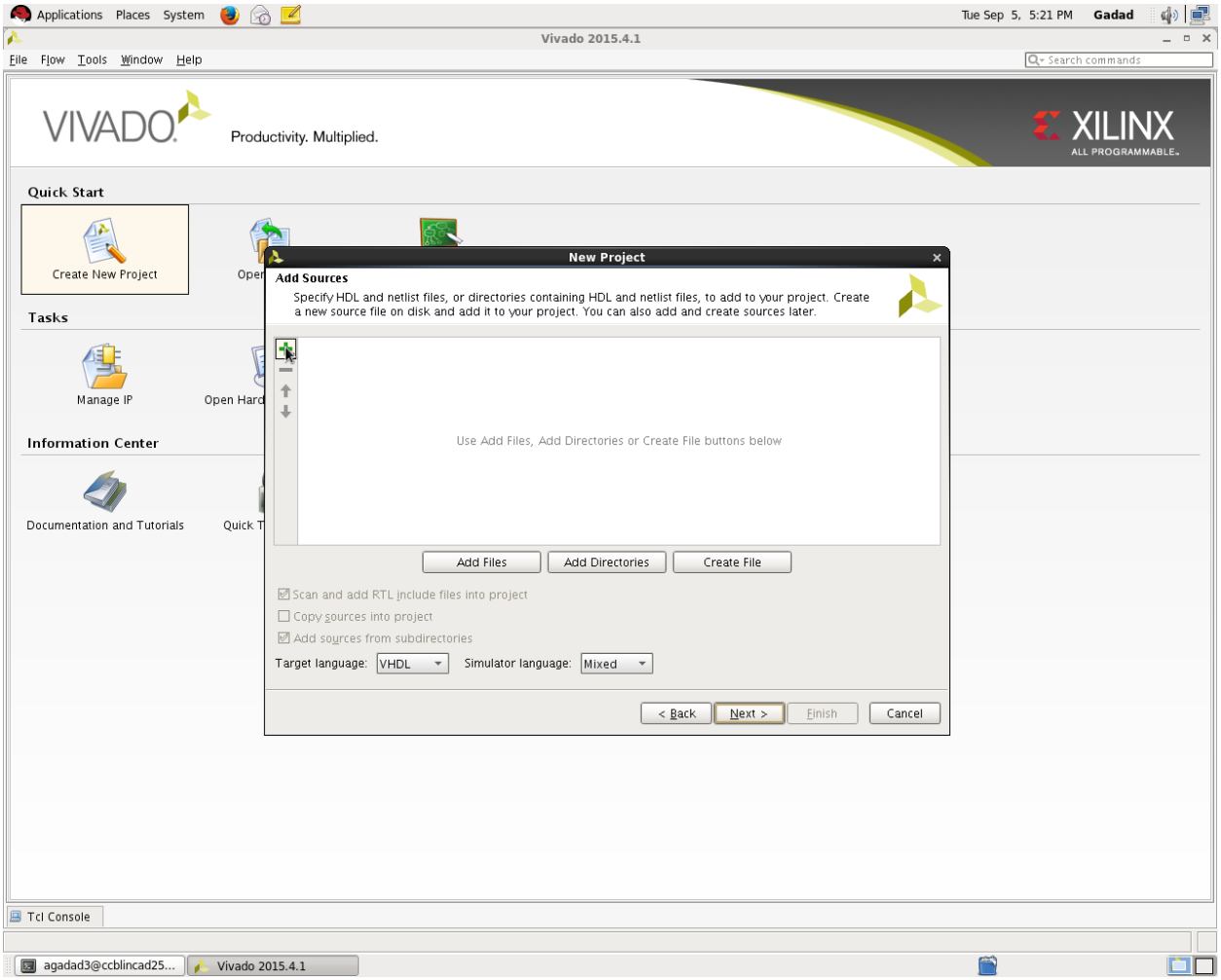
Create a RTL Project and click next



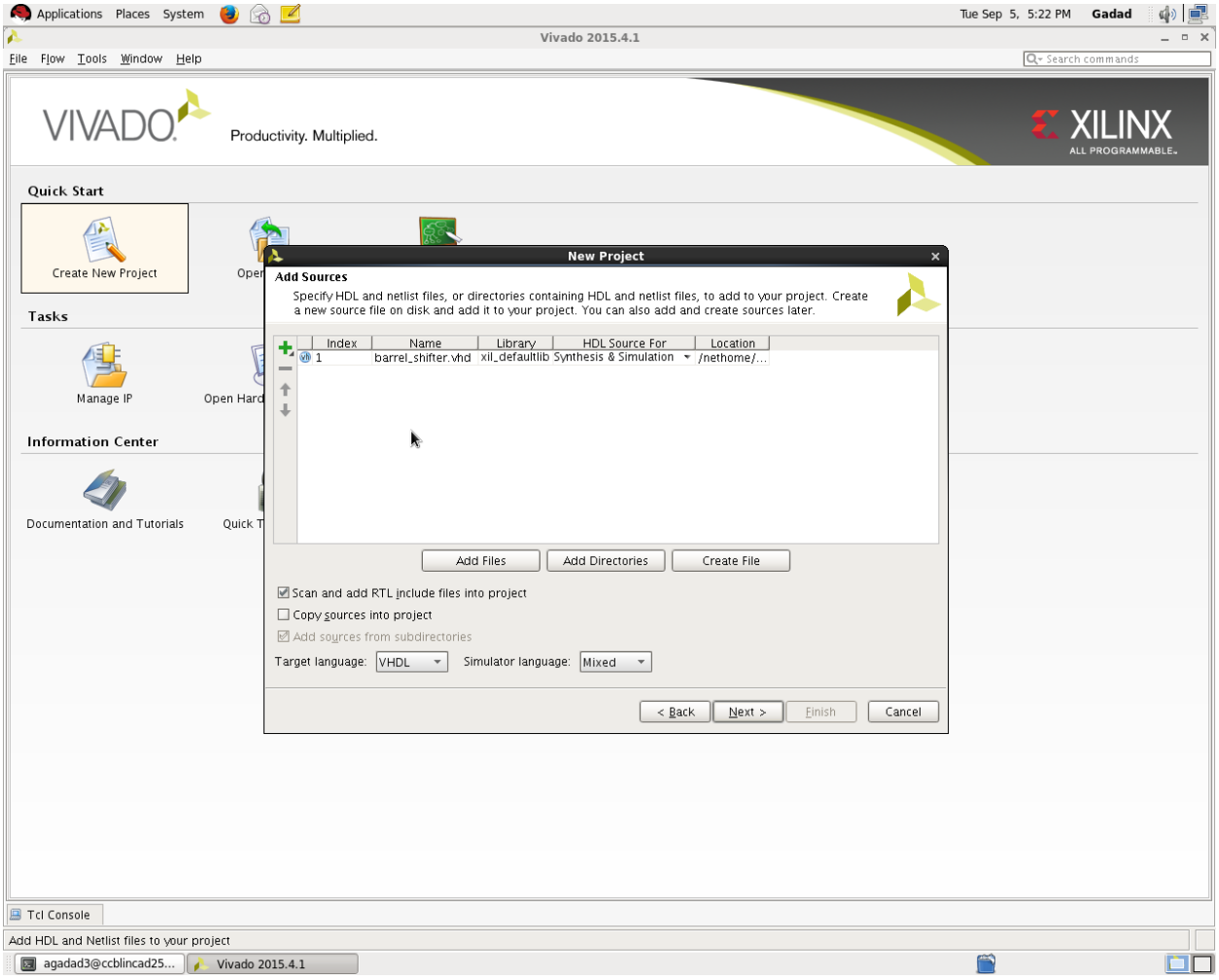
Change the Target language to VHDL and simulator language to mixed



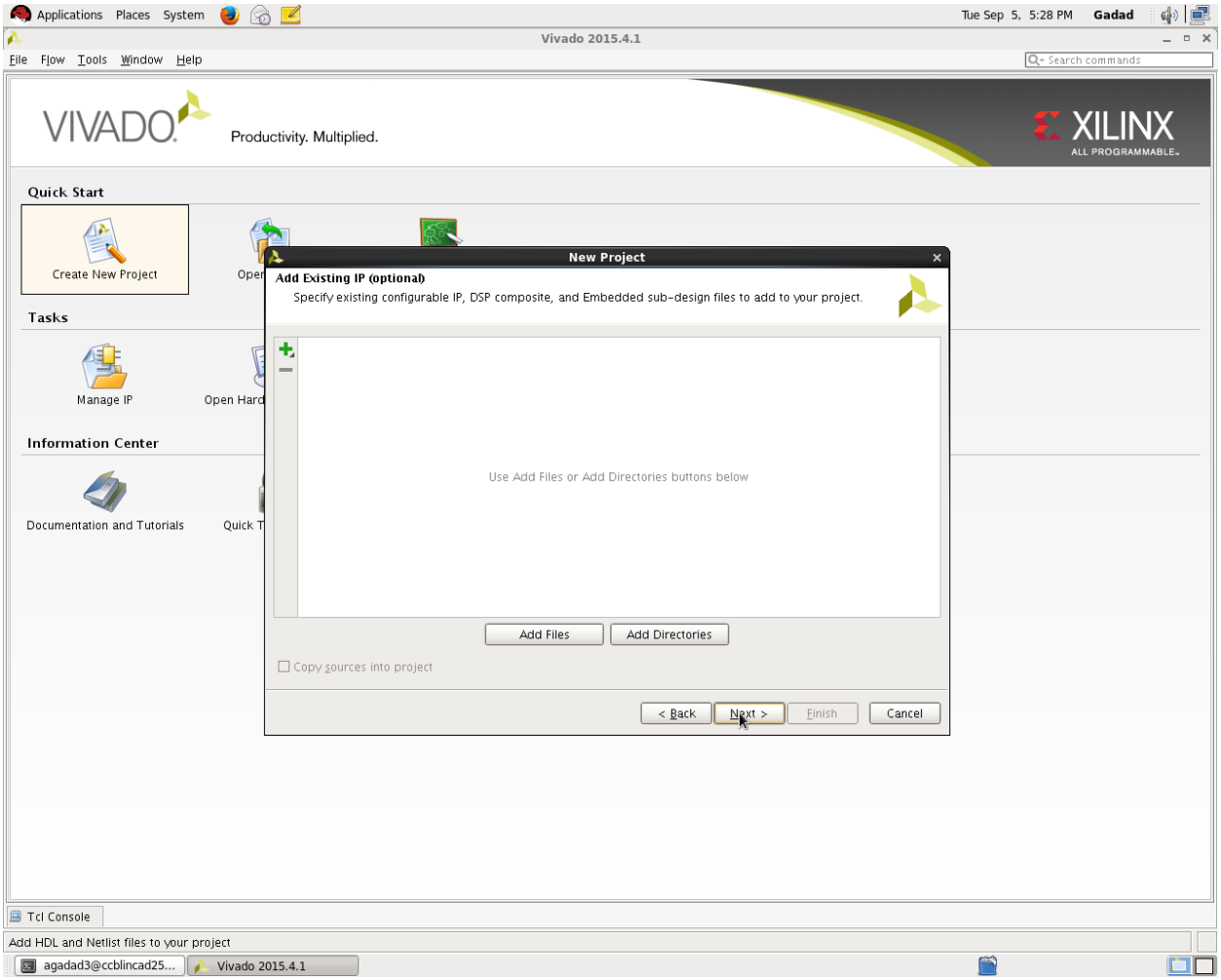
Add Files by clicking on +



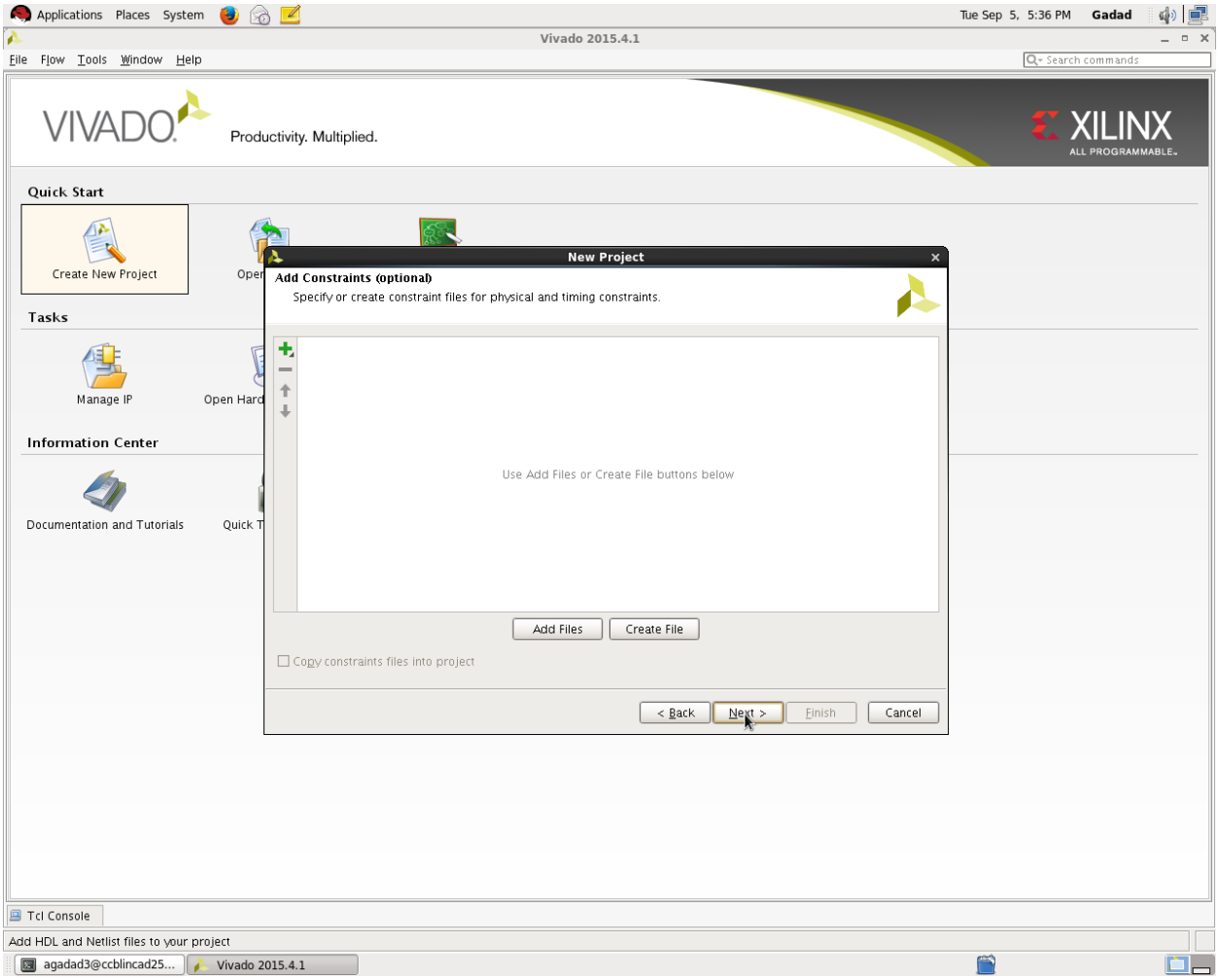
Add “barrel_shifter.vhd”; select ‘Scan and add rtl include files into project’; deselect ‘Copy sources into project’ (The reason we deselect is that during the synthesis and implementation process, if we edit the source files in gvim/emacs/gedit outside Vivado, the changes should be reflected into the Vivado environment)



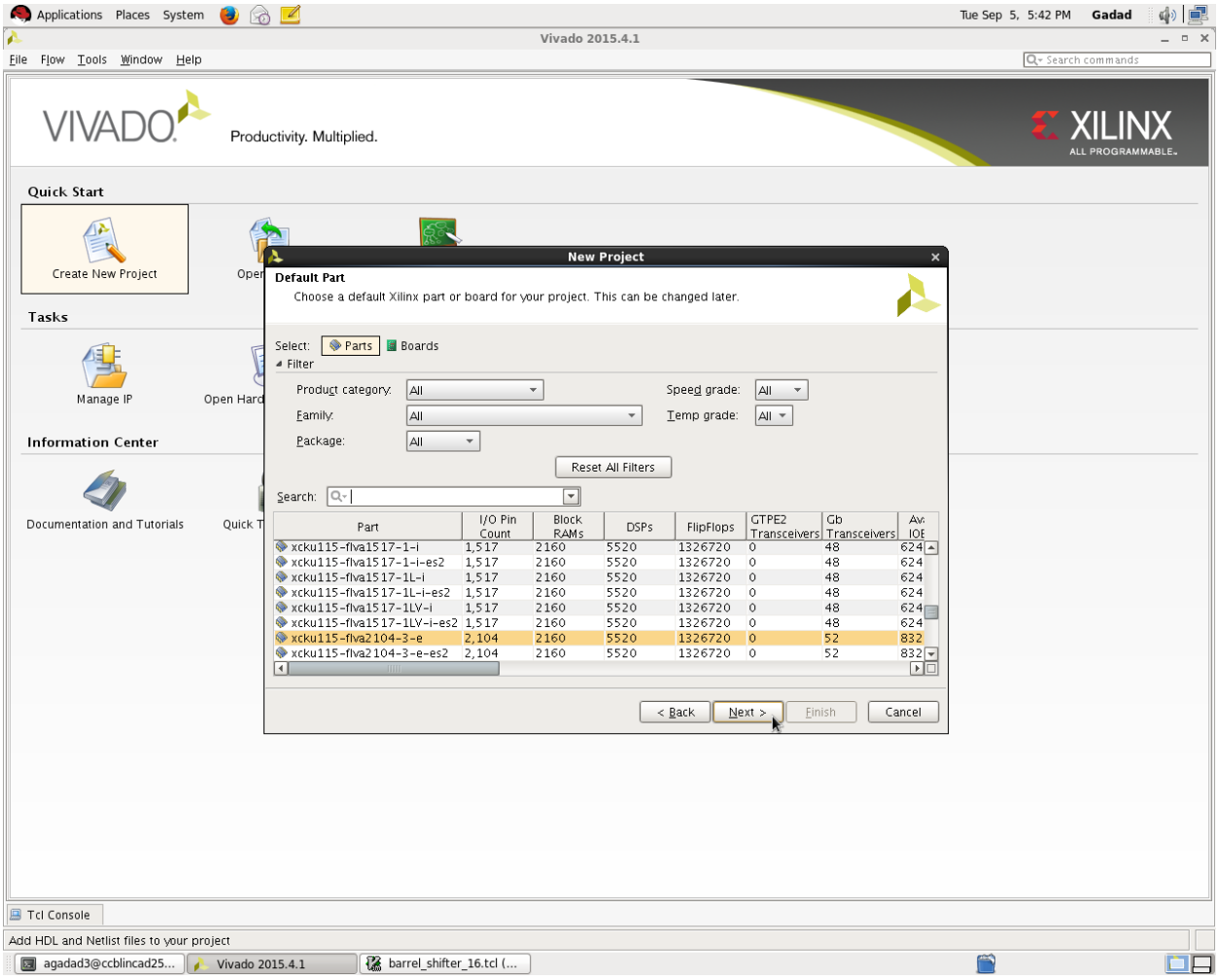
We are not using any inbuilt IP, so click next



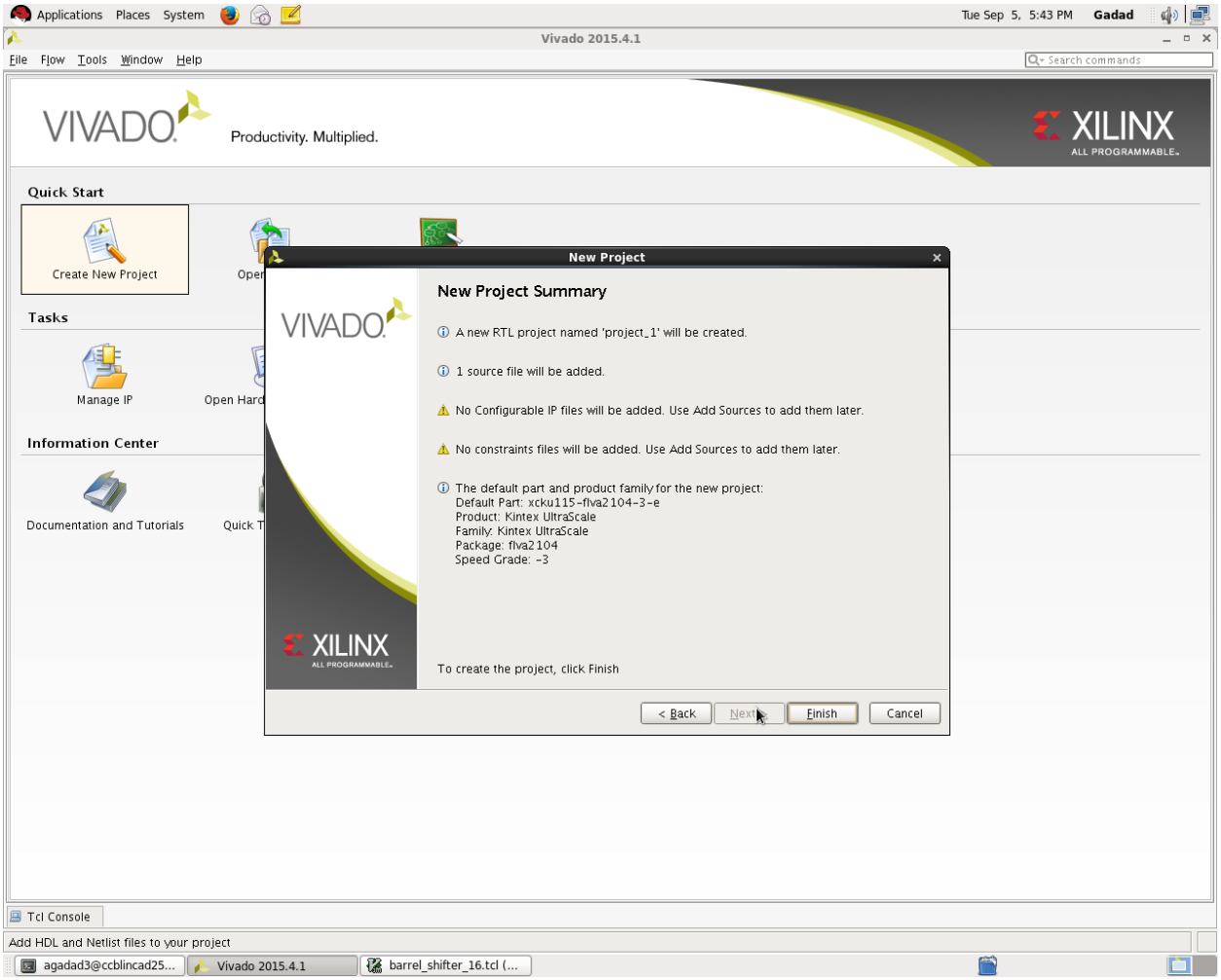
We need constraints for porting the Logic onto the FPGA, but we are not doing that in this Lab. Also, for this lab we do not have a clock (combinational design), so constraints will not be needed. Basically, constraints are directives to Vivado. Click next.



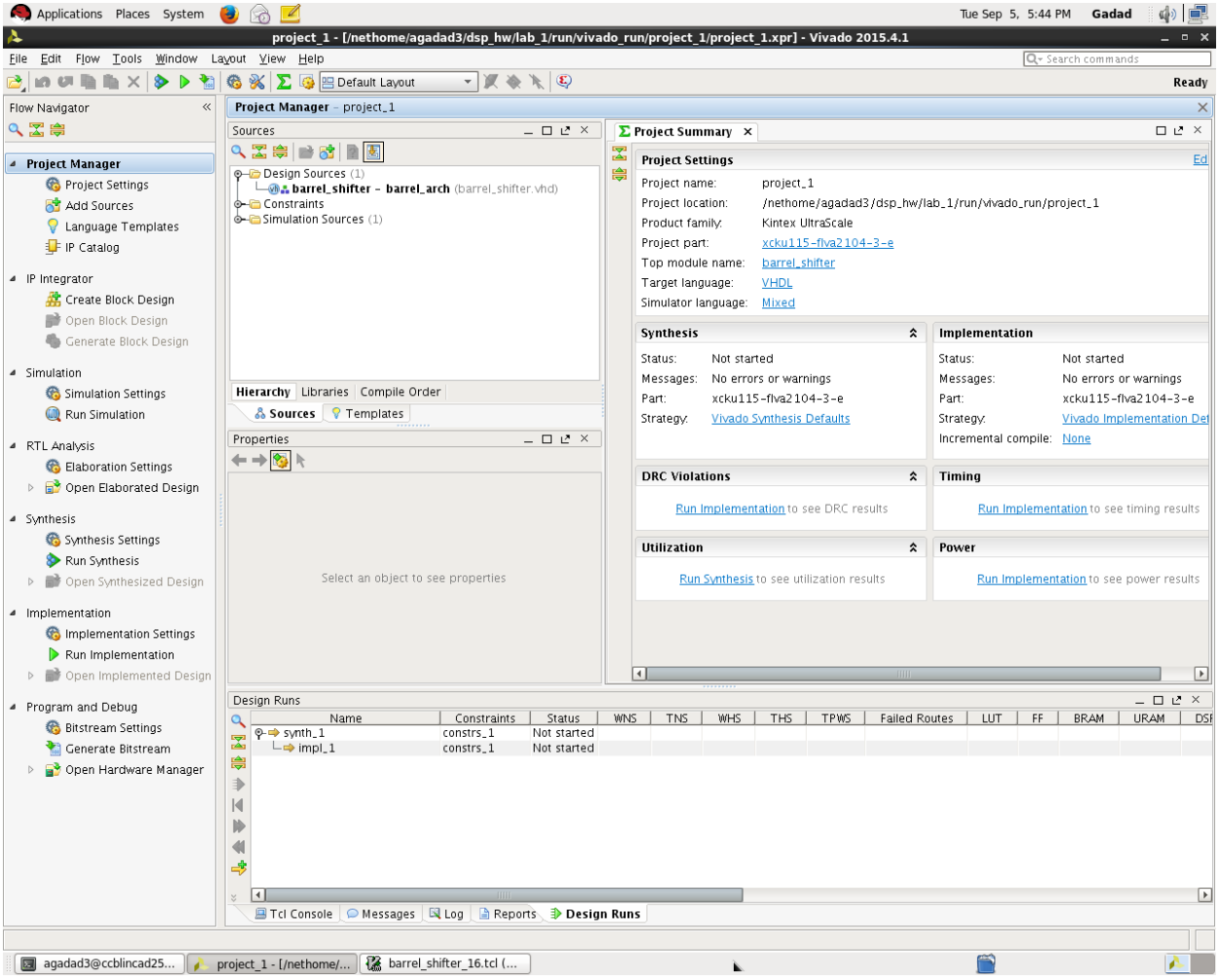
The part number is xcku115-flva2104-3-e. This does not correspond to the Basys board. The rationale for using this is it has a lot of resources and the chances of running out of resources is relatively low for this board. Feel free to use any other part that you like. The lab for which design will be ported to Basys and for your project, the part corresponding to Basys should be used. (More on this later.) Click next



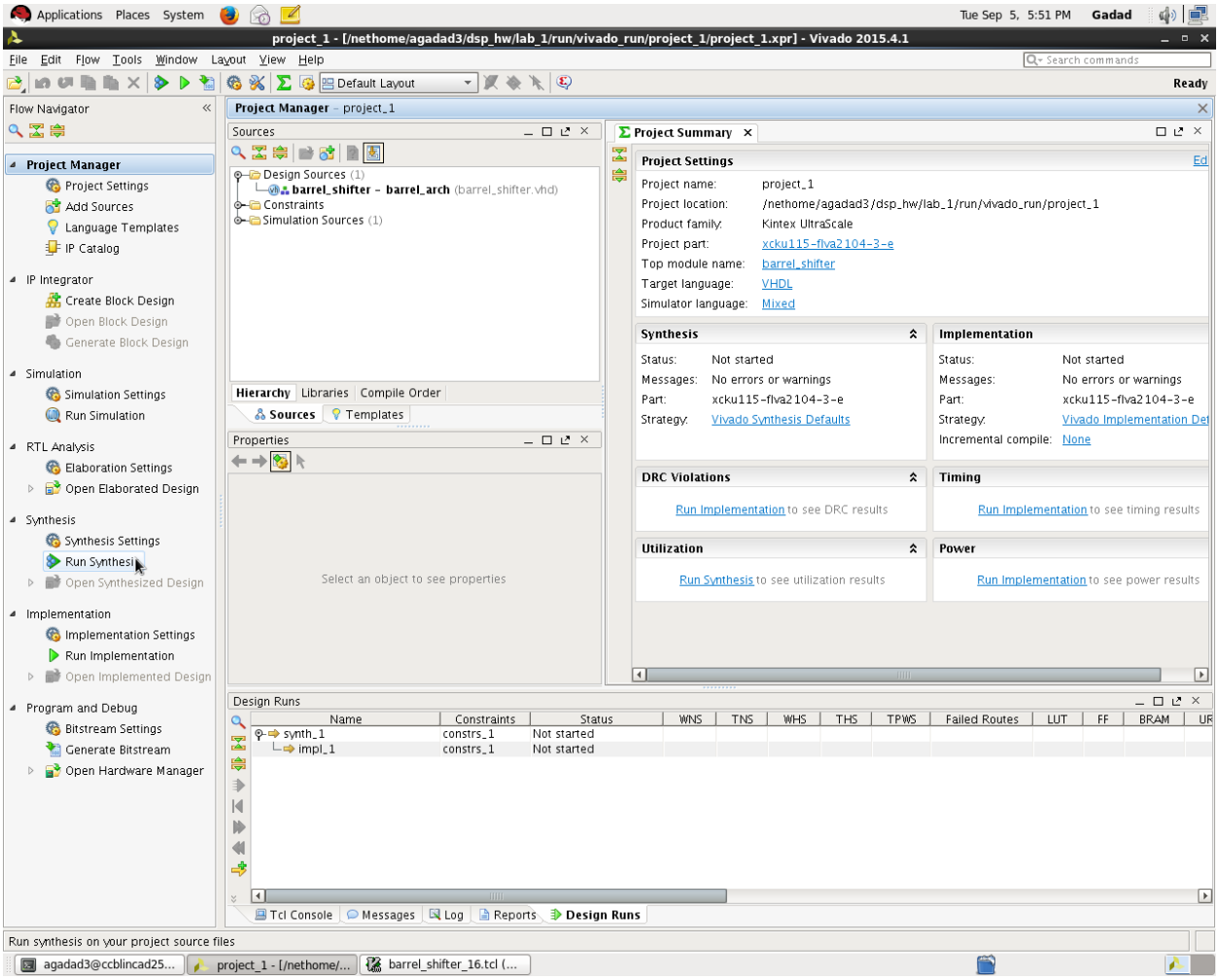
Click on Finish



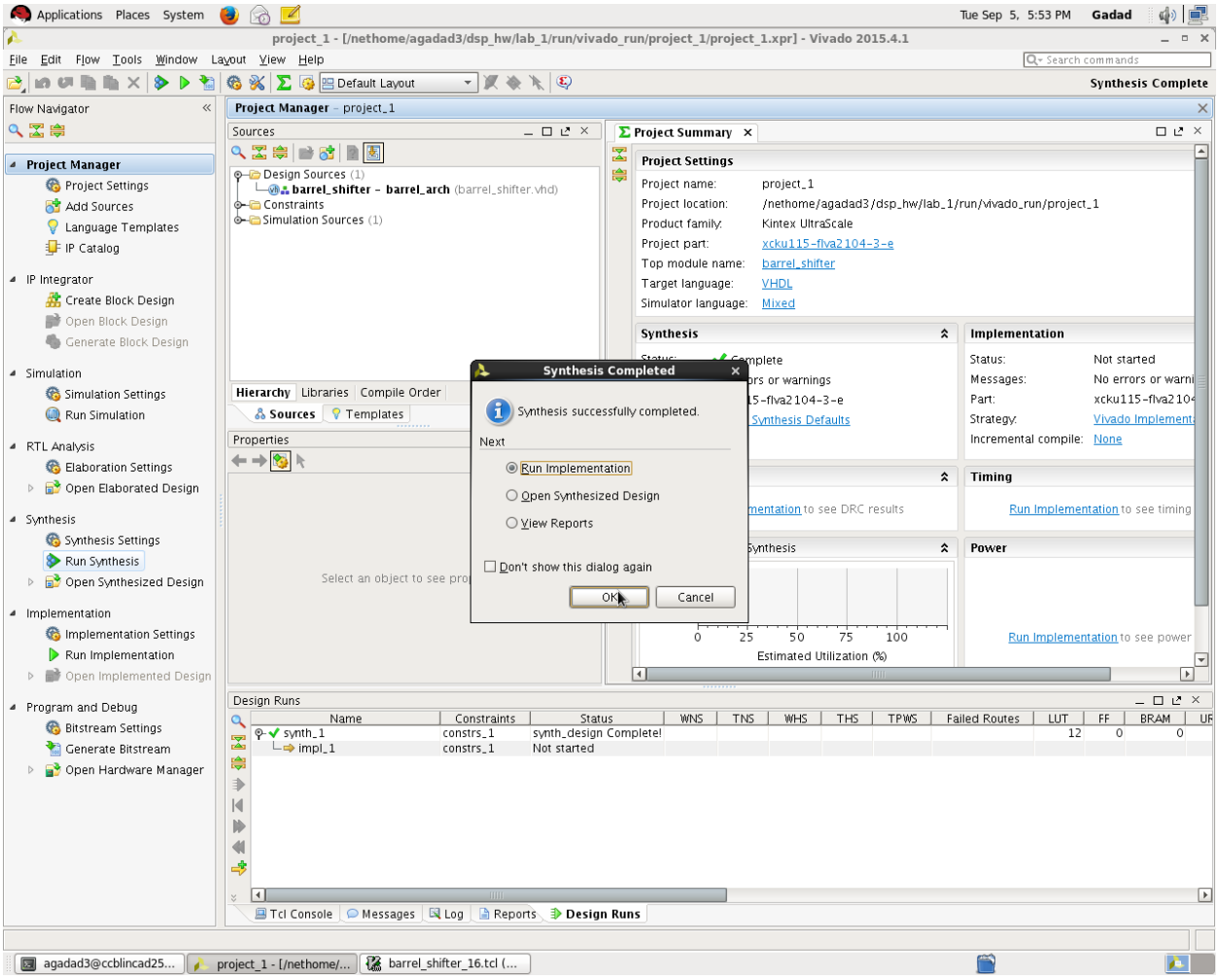
We want you to get familiar with the environment. http://ece-research.unm.edu/jimp/codesign/Vivado/VivadoHelloWorldTutorial.pdf is a good link. The Design sources are in the hierarchy window of the project manager



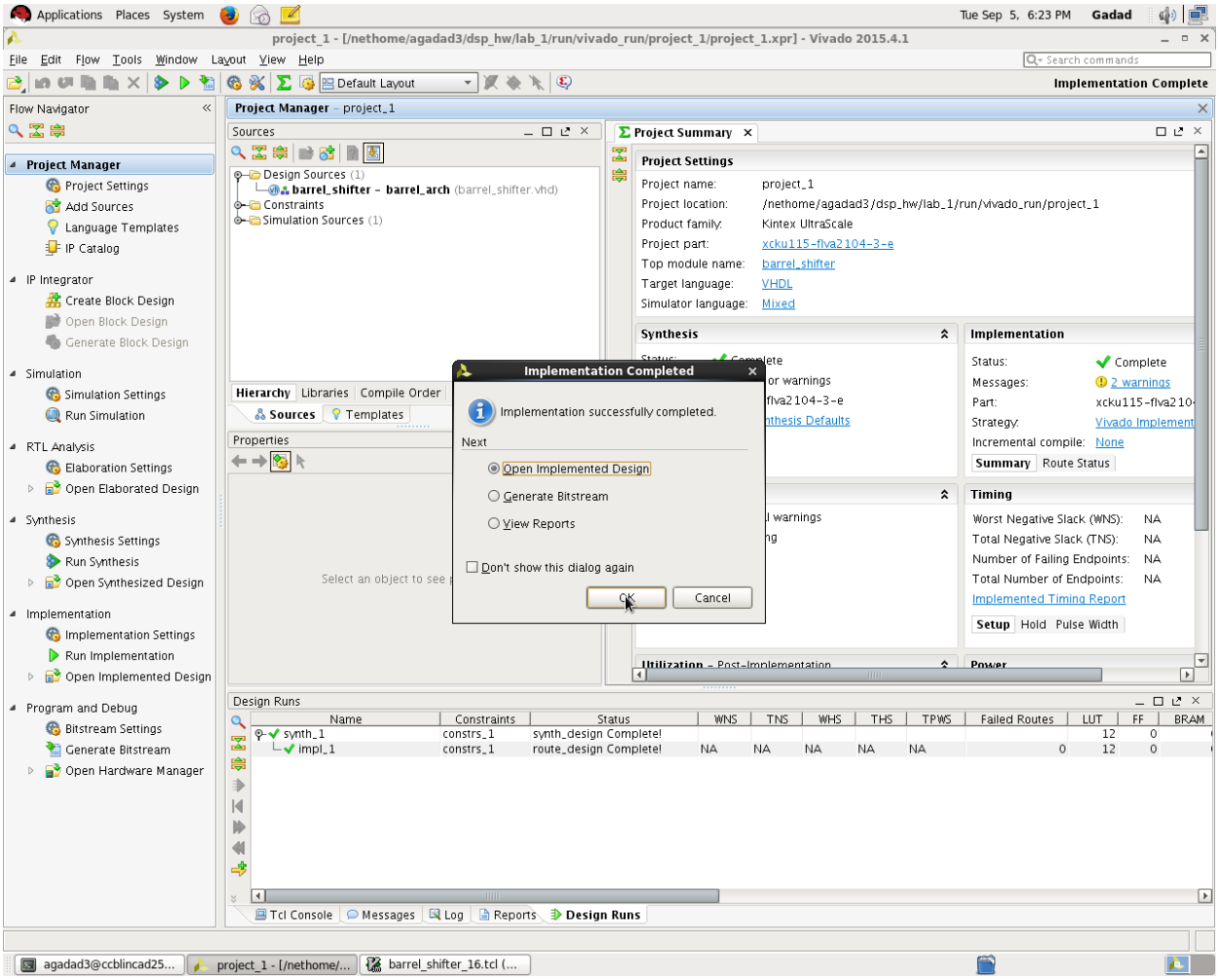
Click on Run Synthesis on the left side of the screen.



After the synthesis, the following window will appear, Select Run Implementation and Click OK (Run Implementation option is also available in the left side below run synthesis)



Click on Open Implemented Design and you are done.



Now the relevant files are in the sub-directory vivado_run/project_1/project_1.runs

You will notice that there are 2 folders here; synth_1 for the synthesis results and impl_1 for the implementation results. We expect you to have a look at the files generated in these folders. The file ‘barrel_shifter_utilization_synth.rpt’ is in synth_1 folder and the file ‘barrel_shifter_power_routed.rpt’ is in impl_1 folder.

For the new design (16 bit barrel shifter), create a new folder lab_2 parallel to lab_1. Create the folders tb,src,run and scripts(scripts is optional). Create the design ‘barrel_shifter_16.vhd’ in src. Write the testbench in tb. Go to run folder and run the modelsim simulations. Verify your designs.

After this create the vivado_run folder,descend into that. Repeat the same steps as barrel_shifter for Synthesis and implementation. The file ‘barrel_shifter_16_utilization_synth.rpt’ will be in synth_1 and ‘barrel_shifter_16_power_routed.rpt’ will be in impl_1.