GEORGIA INSTITUTE OF TECHNOLOGY

SCHOOL of ELECTRICAL AND COMPUTER ENGINEERING

Lab 2: Introduction to Synthesis and Implementation using Xilinx Vivado

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Due Date : Thursday September 14 (11:55 pm)

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1. Introduction

The purpose of this lab is to get acquainted with synthesis and implementation using Xilinx Vivado. Synthesis is the process of converting an RTL into its gate(component)level representation. For e.g.: A Multiplexer written in VHDL with case statements is converted to its gate level logic (using gates). The gate-level logic is also called netlist. The Programmable Logic of an FPGA has a basic element called Logic Cell(Slice). Each Logic Cell has a Look-up Table, Flip-Flops and multiplexer. Since a mux can be used to map any digital logic, it is possible to map any netlist to these resources on FPGA. This is called Implementation. In addition to Logic Cells, FPGA also has Block RAMs (for memories), DSP elements (optimized adders and multipliers) and IO ports. In this lab, we will be performing the synthesis and implementation of the barrel_shifter implemented in Lab1. In addition, we will extend the design to support an input of 16 bits and control of 4 bits.

2. Instructions

i. Perform Synthesis and Implementation for the design in lab 1(Instructions are provided in the document "lab_2_instructions.docx")

ii. Create a new source file "barrel_shifter_16.vhd" for the new design with input and output data being 16 bits wide and the control word being 4 bits wide (the direction of the shift being the same as in lab-1) and the port names being the same as barrel_shifter(only the entity and architectures names will change).

iii. Simulate barrel_shifter_16 (update the testbench with random testcases, then simulate). Note that you don't have to submit simulation results for the new design. This step just serves as a "sanity check".
iv. Perform Synthesis and Implementation for "barrel_shifter_16.vhd"
v. Compare the area (#Slice LUTs,#Bonded IO Buffers,# Primitives) and power(Dynamic and Static Power) of the two designs.

3. Deliverables

i. Create a PDF document which compares the area and power of the two designs. There is no need for any explanation for the difference in the area and power, just provide the values of the #resources and power. The title of the document should be of the form "lab2_firstname.lastname".pdf
ii. The new design file "barrel_shifter_16.vhd"
iii. The synthesized area(utilization)report and implemented power report of the barrel_shifter design namely "barrel_shifter_utilization_synth.rpt" and "barrel_shifter_power_routed.rpt"
iv. The synthesized area(utilization)report and implemented power report of the barrel_shifter_16 design namely "barrel_shifter_16_utilization_synth.rpt" and "barrel_shifter_16_power_routed.rpt"

Move all of these files into a folder "lab2_lastname.firstname".Zip the folder and upload on t-square.

Note : Late submissions are not accepted. In case of extraordinary circumstances, written permission must be obtained from Dr.Madisetti.