# GEORGIA INSTITUTE OF TECHNOLOGY

# SCHOOL of ELECTRICAL AND COMPUTER ENGINEERING

## Lab 3: Programmable MAC Unit

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**Due Date : Thursday September 21 (11:55 pm)**

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### 1. Introduction

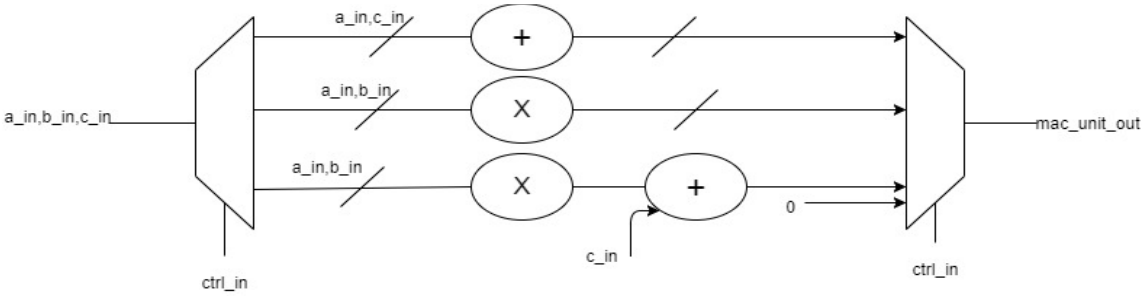
In DSPs and in a significant number of other IPs, multiplication and addition happen in the same cycle. In Lab 3 we will design a MAC IP (**for signed operations**) for which the functionality is described in the following table.

| ctrl_in | Operation for mac_unit_out |
|---|---|
| 0 | a_in + c_in |
| 1 | a_in*b_in |
| 2 | (a_in*b_in) + c_in |
| 3 | 0 |

The template for the design file is provided. There is a sample input file from which the data is read into the testbench . The testbench dumps out an output file. Compare this output with the reference output file provided with the assignment. We will also implement the design in an optimized way. The grading will take into consideration the functional correctness, utilization (area) and the power of the design. Also, note that it is important that you get this IP right because we will be using this as a component for Lab 4. Note that all the operations described in the table are signed operations. 3 re-submissions are allowed for this lab.

## 2. Instructions

i. Write the design in vhdl (mac.vhd) for the specifications given in the table by implementing the following block diagram. The template for the design has been provided (mac.vhd in /src folder). Verify the design by comparing it with the reference output. (40% of grade)




ii. Perform Synthesis and Implementation for the design. List the area (#Slice LUTs, #Bonded IO Buffers) and power (Dynamic and Static Power) (10 % of grade)

iii. Update the block diagram to have a more optimized implementation in terms of area. Write the updated design in vhdl(mac_updated.vhd). Verify the design by comparing it with the same reference output. The DUT instantiation in the testbench will have a different name as the name of the design has changed. So, update this in the testbench (40% of grade)

iv. Perform Synthesis and Implementation for the updated design. (10 % of grade).

## 3. Deliverables

i. Create a PDF with the updated block diagram. Also, list the # multipliers and adders used in both the designs. In the same PDF, compare the power (Dynamic and Static) and #resources (Slice Logic Distribution, IO Information, #Primitives) of “mac.vhd” and “mac_updated.vhd”. Note that for the resources report, use “mac_utilization_placed.rpt” and “mac_updated_utilization_placed.rpt” i.e. use the post-implementation reports and not the post-synthesis reports (we used post-synthesis in lab2 for resources). You can just copy and paste the required tables of the two designs into the document. The title of the document should be of the form “lab3_firstname. lastname”.pdf

ii. The design file “mac.vhd”

iii. The design file “mac_updated.vhd”

iv. Sample output files for the two designs. Name them as "sample_output.txt" and "sample_output_updated.txt" for the mac.vhd and mac_updated.vhd designs respectively.
v. The synthesized area(utilization)report and implemented power report of the mac unit design namely "mac_utilization_placed.rpt" and "mac_power_routed.rpt"
vi. The synthesized area(utilization)report and implemented power report of the updated mac unit design namely "mac_updated_utilization_placed.rpt" and "mac_updated_power_routed.rpt"

Move all of these files into a folder "lab3_lastname.firstname".Zip the folder and upload on t-square.

Note : Late submissions are not accepted. In case of extraordinary circumstances, written permission must be obtained from Dr.Madisetti.