A PVT-Independent Constant-G_m Bias Technique Based on Analog Computation

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***Abstract*—This brief presents a new process, voltage, and temperature (PVT)-independent constant-G_m bias technique for any $I_{\rm out}(V_{\rm in})$-monotonic convex (or concave) transconductors. In this brief, the conventional constant-g_m biasing is formulated into an analog computation process that calculates the constant-G_m bias voltage V_0 from an input current. An analog computer measures the effective G_m from two matched transconductors and converges it to the inverse of a precision resistance by adjusting V_0. Through this, a well-defined large-signal constant-G_m bias voltage can be found. The proposed technique eliminates the power-law or exponential-law assumptions on the $I_{\rm out}(V_{\rm in})$ characteristics in a conventional design. An interpolation calculation follows to find the optimal small-signal constant-g_m bias voltage $V_{\rm out}$. The fundamental limitations of the proposed technique are the required monotonicity and convexity (or concavity) of the transconductor's $I_{\rm out}(V_{\rm in})$. Error sources include mismatches of paired devices and the input offset voltage and open-loop gain of the operation amplifier (OpAmp). These errors are analyzed in detail in this brief. Biasing circuits based on different transistor types are designed using the Taiwan Semiconductor Manufacturing Company (TSMC) 65-nm CMOS process. Computer simulations show that the proposed biasing circuitry can achieve $\pm 0.22\%$ g_m variations from -60 °C to 130 °C.**

***Index Terms*—Constant G_m, process, voltage, temperature (PVT) variation.**

I. Introduction

In ANALOG-INTEGRATED circuits such as radiofrequency (RF) amplifiers [1], analog front end [2], or g_m-C filters [3], [4], constant-transconductance biasing [5] is important in keeping their gain and bandwidth stable against process, voltage, and temperature (PVT) variations. Errors of conventional constant-g_m biasing come from the following: 1) The transconductor $I_{\rm out}(V_{\rm in})$ does not follow a simple power law, particularly in short-channel MOSFETs; 2) the precision of g_m is affected by transistors' secondary effects, including input current $I_{\rm in}$ (base current or gate leakage current), body effects, and output impedance $R_{\rm out}$ (early effect or channel-length modulation); and 3) an insufficient phase margin in the feedback loop can cause transient bias errors or even bias oscillation [6]. In addition to errors, circuits like power amplifiers need large-signal constant-G_m biasing that cannot be readily derived using conventional biasing techniques.

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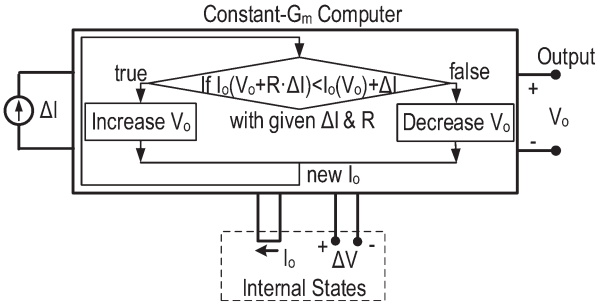

Fig. 1. Block diagram of the constant-G_m analog computer for a monotonic and convex $I_{\rm out}(V_{\rm in})$ without any output interpolator.

This brief presents a constant-G_m bias technique for any $I_{\rm out}(V_{\rm in})$ *monotonic* and *convex (or concave)* transconductors. The organization of this brief is as follows. Section II formulates the conventional constant-g_m-biasing problem into an *analog computation* problem and uses it to examine the underlying fundamentals of conventional constant-g_m biasing circuitry. Based on this, *a constant-G_m computer* is derived from the definition of G_m with discussions on error models. The small-signal constant-g_m bias voltage can be generated based on optimal interpolation. Section III discusses several design tradeoffs, including temperature, device sizing, etc., and the optimal interpolation to provide the optimal constant-g_m bias voltage using computer simulations. A conclusion is drawn in the final section.

II. Architecture

A. Formulation of the Constant-G_m Biasing Problem

For any transconductor, output current $I_{\rm out}$ is a function of its input voltage $V_{\rm in}$. The general G_m is defined in a difference sense by relating the output currents $I_{\rm out}(V_0) \equiv I_0$ and $I_{\rm out}(V_0+\Delta V) \equiv I_0+\Delta I$ between two input voltages V_0 and $V_0+\Delta V$ with $G_m \equiv \Delta I/\Delta V$. To design a constant-$G_m$ biasing circuit is equivalent to designing an analog computer that continuously calculates the bias voltage V_0 that keeps the ratio of $\Delta I/\Delta V$ constant regardless of PVT drifts based on the input current ΔI shown in Fig. 1. Therefore, ΔI and V_0 are the input and output to the analog computer, and I_0 and $\Delta V = \Delta I/G_m$ are the internal states.

The algorithm of this computation is as follows: 1) $I_{\rm out}(V_0)+\Delta I$ and $I_{\rm out}(V_0+\Delta V)$ are constructed using two matched transconductors as shown in Fig. 2(a). Note that a monotonic and convex $I_{\rm out}(V_{\rm in})$ is assumed in this figure; 2) these two currents are compared; and 3) when $I_{\rm out}(V_0+\Delta I/G_m) < I_{\rm out}(V_0)+\Delta I$, the V_0 should be increased until

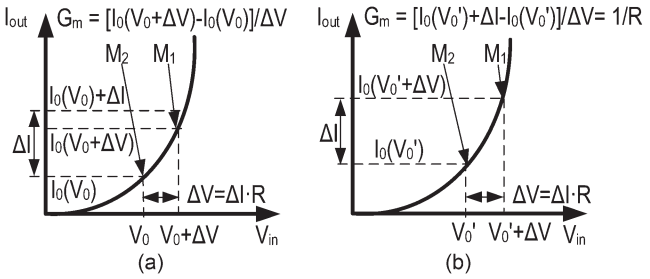

Fig. 2. Operating principles of the constant-G_m analog computer. Instantaneous state (a) where $I_{\rm out}(V_0 + \Delta I/G_m) < I_{\rm out}(V_0) + \Delta I$ for a monotonic and convex $I_{\rm out}(V_{\rm in})$ and (b) when it is biased properly with $G_m = 1/R$. Note that $I_0(V_0)$ and $I_0(V_0 + \Delta V)$ are the output currents of matched transistors M_1 and M_2, respectively.

they are equal as in Fig. 2(b). If $I_{\rm out}(V_{\rm in})$ is concave, V_0 should be decreased in the same scenario. This process can also be realized in digital with more complexity.

B. Conventional Design as an Analog Computer

With the idea of analog computation in mind, how should the conventional constant-g_m biasing circuit in Fig. 3(a) [7] be interpreted? In this circuit, M_1 and M_2 have a sizing ratio of $1 : N$. We can scale them to a $1 : 1$ ratio without changing voltages in all nets using the circuit of Fig. 3(b). Note that the upper current sources M_3 and M_4 are scaled to an $N : 1$ ratio, and the resistor is scaled to $N \cdot R$ to maintain its voltage drop. An equivalent way to represent this circuit is to transform it into an equivalent circuit as shown in Fig. 3(c). Now, M_3 and M_4 are back to the same size with an input current ΔI provided. It can be identified that the difference current ΔI between the matched M_1 and M_2 is $N - 1$ times the internal state I_0 through feedback as shown in Fig. 3(d). In addition, the difference voltage ΔV between the matched M_1 and M_2 is $N \cdot R \cdot I_0$.

Note that ΔI and ΔV in a conventional design are not related by $\Delta V = \Delta I \cdot R$ as in Fig. 2. In Fig. 3(c), the gate-to-source voltage of M_2 is equal to V_0, and its drain current is I_0. The gate-to-source voltage of M_1 is equal to $V_0 + \Delta V$, and its drain current is $I_0 + \Delta I$. Since M_1 and M_2 are matched, the equivalent G_m at V_0 can be derived by dividing ΔI by ΔV as described in Fig. 2. From Fig. 3(c), $\Delta V = I_0 \cdot N \cdot R$. Hence

$$G_m \equiv \left.\frac{\Delta I}{\Delta V}\right|_{\Delta I=(N-1)I_0} = \frac{\Delta I}{N \cdot R \cdot I_0} = \left(\frac{N-1}{N}\right)\frac{1}{R}. \quad (1)$$

This is to say that the conventional circuit in Fig. 3(a) is a constant-G_m computer that calculates the bias voltage V_0 based on input $\Delta I = (N - 1) \cdot I_0$. Note that ΔI is iteratively defined based on I_0. This suggests that, when V_0 is used to bias another transistor, its output ac current swing differs for different PVT conditions when the biased transistor is driven by an input ac voltage swing equal to ΔV.

C. Proposed Constant-G_m Computer

The performance of the constant-G_m computer in Fig. 3(a) can be improved by directly providing a constant input ΔI without any internal-state feedback. The schematics of the proposed constant-G_m computer is shown in Fig. 4. The input ΔI provides various design options. For small-signal or fixed input-swing application, ΔI can be generated from a constant current reference. However, for applications that need high-dynamic-range output swings, ΔI can be made proportional to the magnitude of the input signal.

The major difference between the circuits in Figs. 3(c) and 4 is how ΔV is generated. In Fig. 3(c), $\Delta V \propto I_0$. However, in the proposed circuit, $\Delta V \propto \Delta I$, which is mirrored directly from the input. Under the scheme of analog computation, OpAmp A_1 does not have any internal-state feedback to the input. In addition, when the device $I_{\rm out}(V_{\rm in})$ changes due to PVT drifts, OpAmp A_1 forces $I_{\rm out}(V_0 + \Delta I \cdot R)$ to be equal to $I_{\rm out}(V_0) + \Delta I$. Hence

$$G_m \equiv \left.\frac{\Delta I}{\Delta V}\right|_{\Delta I} = \frac{\Delta I}{R \cdot \Delta I} = \frac{1}{R}. \quad (2)$$

No assumption is made for the device $I_{\rm out}(V_{\rm in})$, except for it being monotonically increasing and convex. If $I_{\rm out}(V_{\rm in})$ of M_1 and M_2 in Fig. 4 is monotonically increasing but concave, the input terminals of A_1 in Fig. 4 will need to be swapped.

D. Small-Signal g_m Bias Voltage

The circuit of Fig. 4 has a well-defined constant-G_m bias voltage V_0. However, biasing the transistor using V_0 will not result in constant-g_m biasing. Since the $I_{\rm out}(V_{\rm in})$ of M_1 and M_2 is convex, $g_m(V_0) < G_m < g_m(V_0 + \Delta V)$. An optimal small-signal constant-g_m voltage $V_{\rm out}$ can be found by using an interpolated $V_{\rm out} \equiv V_0 + \xi\Delta V$ to bias M_0. This interpolation is accomplished through a resistive voltage divider shown in Fig. 4. The optimization of interpolation factor ξ will be discussed in Section III.

E. Error Models and Analysis

The proposed circuit shown in Fig. 4 relies on the matching between the $M_1 - M_2$ pair and the mirrored currents I_0 and ΔI. Mismatches between each pair will contribute to errors in the output voltage V_0. Assume that the currents of M_1 and M_2 are $I_{\rm out}(V_1) + ((\delta I_{\rm out})/2)$ and $I_{\rm out}(V_2) - ((\delta I_{\rm out})/2)$, respectively. $(\delta I_{\rm out})/2$ is the mismatch current in the transconductor's average $I_{\rm out}(V_{\rm in})$ characteristic. The drain currents of M_3 and M_4 are $I_0 + \Delta I + ((\delta I_0)/2)$ and $I_0 + \Delta I - ((\delta I_0)/2)$, respectively, with $(\delta I_0)/2$ mismatches.

Moreover, voltage V_1 can be expressed as $V_2 - V_{os} + \Delta I \cdot R$. V_{os} is the residual voltage difference across the positive and negative terminals of OpAmp A_1 as $V_{os} = (V_{SG,3}/A_1) + V'_{os}$. Here, V'_{os} is the input offset voltage of A_1, and $V_{SG,3}$ is the source-to-gate voltage of M_3. For a 1-mV V'_{os}, a more than 60-dB A_1 is sufficient to make the term $(V_{SG,3}/A_1)$ insignificant.

Define the large-signal G_m as $(I_{\rm out}(V_2 + \Delta I \cdot R) - I_{\rm out}(V_2))/\Delta IR$ and the reference G_{m0} as $(1/R)$, respectively. The error of G_m from G_{m0} can be calculated by

$$\frac{\Delta G_m}{G_{m0}} \equiv \frac{G_m - G_{m0}}{G_{m0}} \approx \left(-\frac{\delta I_{\rm out}}{\Delta I} + \frac{\delta I_0}{\Delta I} + \frac{V_{os}}{\Delta I \cdot R}\right). \quad (3)$$

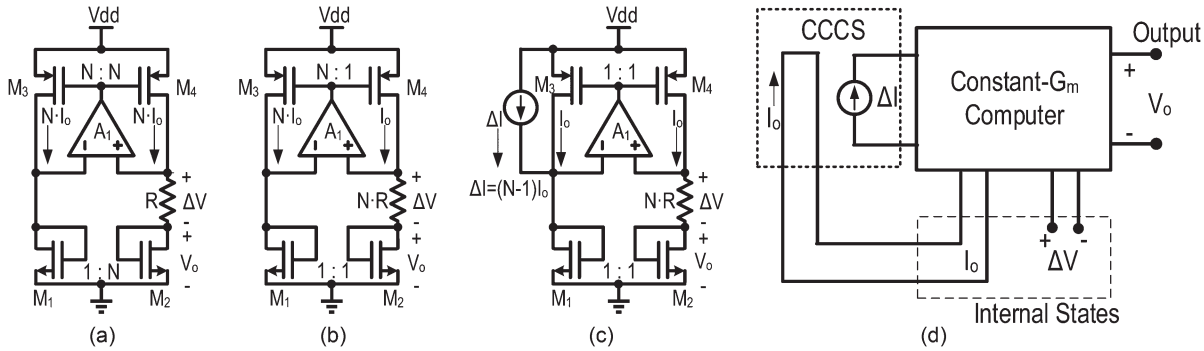

Fig. 3. Conversion of a conventional constant-g_m biasing circuit into a conceptual analog computer: (a) Original circuit, (b) circuit after the right branch is scaled down, (c) circuit with the difference current ΔI separated, and (d) block diagram of the analog computer.

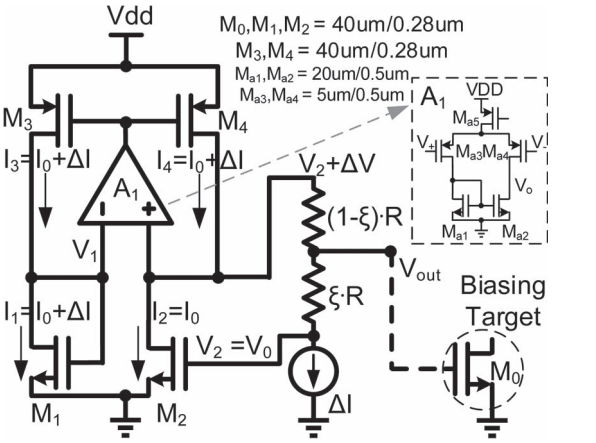

Fig. 4. Proposed architecture for a monotonically increasing and convex device $I_{\text{out}}(V_{\text{in}})$. A voltage interpolator is used to provide optimal constant-g_m bias voltage for M_0. ΔI is the only overhead current consumption.

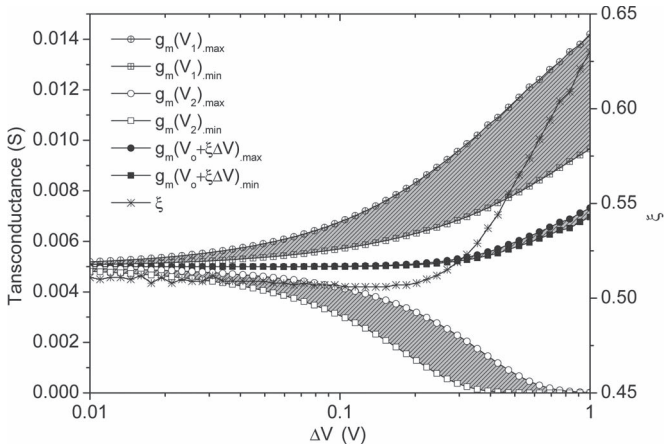

Fig. 5. Optimal ξ, $g_m(V_1)$, $g_m(V_2)$, and $g_m(V_0+\xi\Delta V)$ for ΔV from 10 mV to 1 V with temperature from -60 °C to 130 °C. The W/L values of M_1 and M_2 are kept at 40 μm/0.28 μm.

Mismatches cause systematic error in G_m. Input current ΔI should be made sufficiently large compared to all mismatch currents.

III. Simulation Results

Computer simulations of the circuit in Fig. 4 are presented in this section. All the simulations are based on the TSMC 65-nm CMOS process. The resistor R used in the simulation has *zero* temperature coefficient (TC) as the reference for G_m. In practice, an external low-TC precision resistor should be used. From Figs. 5–8, behavioral OpAmps with 120-dB open-loop gain and *zero* input offset voltage are used in the simulations and the optimizations of ξ. Both the gain and input offset voltage of the OpAmp have *zero* TC. Device sizes other than those of M_1 and M_2 are listed in Fig. 4. Since there is no channel-length modulation issue in this circuit, all devices have a minimum length.

DC and ac simulations are used to find operating points and to calculate the *effective* small-signal g_m for M_1, M_2, and the V_{out}-biased equally sized transistor M_0. The effective g_m is not equal to the intrinsic g_{mi} in the transistor model due to parasitic resistors in all transistor terminals. In MOSFET, $g_m \approx g_{mi} \cdot (1 - g_m r_s)(1 - g_{ds} r_d)$, where r_s and r_d are the source and drain parasitic resistors, respectively.

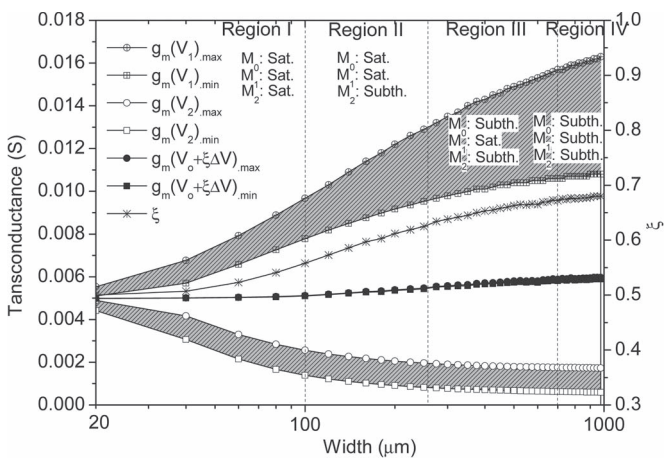

Fig. 6. Optimal ξ for W of M_1 and M_2 from 20 to 1000 μm with temperature from -60 °C to 130 °C, along with corresponding $g_m(V_1)$, $g_m(V_2)$, and $g_m(V_{\text{out}})$. For all simulations, the lengths of M_1 and M_2 are chosen as 0.28 μm, and ΔV is kept at 100 mV.

In all simulations, the *effective* small-signal transconductances of M_1, M_2, and the V_{out}-biased transistor M_0 are plotted and compared. The large-signal effective G_m's are calculated based on $G_m \equiv (I_{D1} - I_{D2})/(V_{GS1} - V_{GS2})$, where I_{D1} and I_{D2} and V_{GS1} and V_{GS2} are the drain currents and

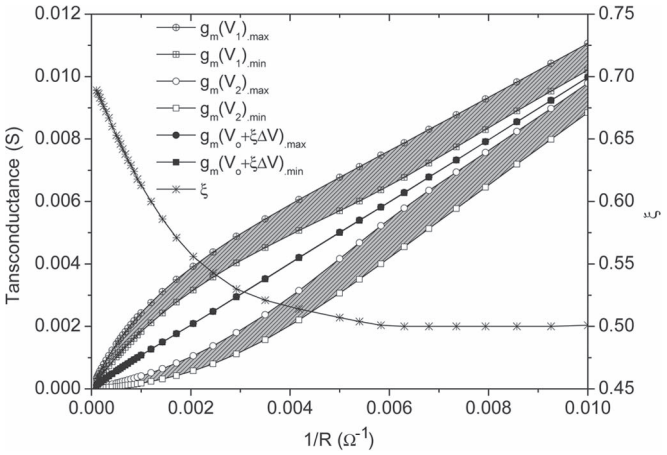

Fig. 7. Optimal ξ, $g_m(V_1)$, $g_m(V_2)$, and $g_m(V_0+\xi\Delta V)$ for a varying $1/R$ with temperature from -60 °C to 130 °C. For all simulations, W/L values of M_1 and M_2 are chosen as 40 μm/0.28 μm, and ΔV is kept at 100 mV.

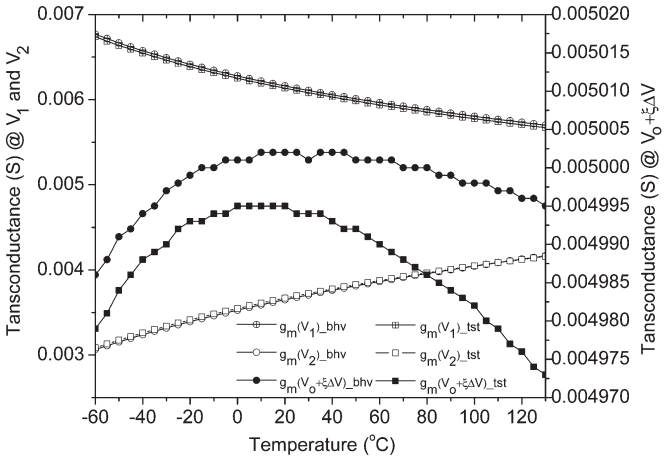

Fig. 8. $g_m(V_1)$, $g_m(V_2)$, and $g_m(V_0+\xi\Delta V)$ from -60 °C to 130 °C for a behavioral and a 25-dB transistor-level OpAmp. For all simulations, W/L values of M_1 and M_2 are chosen as 40 μm/0.28 μm, and ξ is kept at 0.503.

gate-to-source voltages of M_1 and M_2, respectively. From Figs. 5–8, M_1 and M_2 use thick-gate-oxide MOSFETs.

The effects of ΔV on the proposed circuit are first studied. In these simulations, the W/L values of M_1 and M_2 are kept at 40 μm/0.28 μm, and the $1/R$ is kept at 5 mS. The gate voltage difference ΔV between M_1 and M_2 is swept by increasing the input current ΔI. For each simulated ΔV, its optimal ξ that presents the minimum g_m variations from -60 °C to 130 °C, is found. From Fig. 5, as ΔV increases, the optimal ξ slightly increases. Also, the g_m variation at optimal ξ increases as ΔV increases. This is due to the fact that $g_m(V_2)$ is clipped to zero for some temperatures from $\Delta V > 0.3$ V.

Then, the effects of transistors' operating regions are studied. In these simulations, ΔV is kept at 100 mV for various widths of M_1 and M_2, and the $1/R$ is kept at 5 mS. As the device size increases, the operating region of the $M_1 - M_2$ pair will move from the saturation region to the subthreshold region. For each simulated W/L, the optimal ξ to achieve minimum g_m variations from -60 °C to 130 °C is found and presented in Fig. 6. The operation regions for M_1 and M_2 will shift from Region I, where both transistors are in saturation, to Region IV, where both transistors are in the subthreshold region. From this figure, as the operation region moves from the saturation region to the subthreshold region, ξ increase from 0.50 to 0.67. This is due to the $I_{\text{out}}(V_{\text{in}})$ of the devices shifting from the power-law to exponential function, as analyzed in Appendix A. Also, the g_m in the temperature range with optimal ξ increases slightly as W/L increases since g_m variations instead of g_m itself are minimized during ξ optimization.

Next, the effects of $1/R$ on ξ are studied. In this simulation, $\Delta V = 100$ mV, and the W/L of M_1 and M_2 is 40 μm/0.28 μm. However, the reference resistance R is swept. For each simulated R, ΔI is adjusted to maintain a constant ΔV. In addition, its optimal ξ to achieve minimum g_m variations from -60 °C to 130 °C is found and presented. From the simulation results shown in Fig. 7, as the $1/R$ increases, ξ decreases to 0.50. Also, the g_m in the temperature range with optimal ξ increases as $1/R$ increases.

Finally, an optimal and constant $\xi = 0.503$ to provide minimum g_m variation in saturation mode is chosen. Transconductance simulation results for -60° C to 130° C are presented in Fig. 8. g_{m1} and g_{m2} converge toward $1/R$ as the temperature increases due to the fact that the $I_{\text{out}}(V_{\text{in}})$ curve of M_1 and M_2 becomes more linear at higher temperatures. For the g_m of the biased transistor, $\pm 0.16\%$ variations are found over the temperature range.

To verify that the proposed technique is independent of transconductor $I_{\text{out}}(V_{\text{in}})$ characteristics, three other optimal and constant ξ's to provide minimum g_m variation for different operating regions and devices are similarly found. The simulation results for all cases, including process variations, are summarized in Table I.

The performance of the 2.5-V NMOSFET in the saturation region case is chosen to compare with the performance of other reported works. The direct replacement of the behavioral OpAmp to a minimally implemented single-stage 25-dB OpAmp only slightly degrades its g_m variations from $\pm 0.16\%$ to $\pm 0.22\%$ as shown in Fig. 8 and Table II. From this table, this work achieves a promising performance in the simulation level covering a wider temperature range.

TABLE I
SIMULATION RESULTS OF CONSTANT-G_m ANALOG COMPUTER

Device	Optimal ξ	Temp.	G_m*	$g_m(V_0)$*
2.5V NMOSFET in sat. region $W/L = 40um/0.28um$	0.503	$-60°C$	4.986	5.004±0.361
		$27°C$	5.002	5.017±0.311
		$130°C$	4.995	5.009±0.283
2.5V NMOSFET in subth. region $W/L = 800um/0.28um$	0.675	$-60°C$	5.834	5.847±0.301
		$27°C$	5.912	5.922±0.234
		$130°C$	5.841	5.848±0.182
1.0V NMOSFET in sat. region $W/L = 5um/60nm$	0.562	$-60°C$	5.437	5.446±0.383
		$27°C$	5.401	5.417±0.322
		$130°C$	5.428	5.443±0.295
1.0V NMOSFET in subth. region $W/L = 100um/60nm$	0.665	$-60°C$	6.196	6.218±0.327
		$27°C$	6.175	6.193±0.251
		$130°C$	6.201	6.220±0.199

* Units are in mS.

** ΔV is kept at $100mV$ and $1/R$ is equal to $5mS$.

*** Mismatches of all transistors pairs and M_0 are considered.

TABLE II
PERFORMANCE SUMMARY OF THE CONSTANT-G_m CIRCUITS

	this work*	**[8]**	**[7]**	**[9]**
Implementation Level	simulation	simulation	simulation	simulation
G_m standard deviations	$\pm 0.22\%$	$\pm 0.76\%$	$\pm 1\%$	$\pm 1.5\%$
Temperature range	-60 to $130°C$	-30 to $110°C$	-25 to $125°C$	20 to $80°C$
Current consumption	2mA**	1.1mA(subth. region)	1.5mA(sat. region)	1.5mA(sat. region)

* 2.5V NMOSFET in saturation region with a ΔI as 500uA

** OpAmp draws $100\mu A$.

IV. CONCLUSION

Formulating the classical constant-g_m biasing problem into an analog computation problem allows us to study it from a different angle. From this perspective, it is found that the conventional constant-g_m biasing technique relies on iterative computation that obscures the definition of both G_m and g_m. This also makes biasing depend on device characteristics.

By removing the iterative path in analog computation, G_m in conventional biasing can be better defined. This results in a design independent of device characteristics. In addition, an optimal constant-g_m bias voltage can be generated using optimal interpolation ξ as analyzed in Appendix A. From simulation results, high-precision G_m and g_m can be achieved from -60 °C to 130 °C as summarized in Table II.

APPENDIX A
RELATIONSHIPS BETWEEN SMALL-SIGNAL g_m AND ξ

Consider the exponential and power-law $I_{\rm out}(V_{\rm in})$ for MOSFETs in the subthreshold region and saturation region, respectively.

For the exponential case, $I_{\rm out}(V_0)$ and $I_{\rm out}(V_0+\Delta V)$ can be obtained based on

$$I_{\rm out}(V_{\rm in}) = I_s \cdot \left(e^{\frac{V_{\rm in}-V_{\rm th}}{\phi_t}} - 1\right) \tag{A.1}$$

where $V_{\rm th}$ is the threshold voltage and ϕ_t is the effective thermal voltage. The tranconductance that is biased at $V_0+\xi\Delta V$ can be expressed as

$$\frac{\partial I_{\rm out}(V_0+\xi\Delta V)}{\partial V_{\rm in}} = \frac{I_s \cdot e^{\frac{V_0-V_{\rm th}+\xi\Delta V}{\phi_t}}}{\phi_t}. \tag{A.2}$$

ξ can be found through solving

$$\frac{I_{\rm out}(V_0+\Delta V)-I_{\rm out}(V_0)}{\Delta V} = \frac{\partial I_{\rm out}(V_0+\xi\Delta V)}{\partial V_{\rm in}}. \tag{A.3}$$

After some rearrangements, ξ can be derived as

$$\xi = \frac{1}{X_e}\cdot \ln\left(\frac{e^{X_e}-1}{X_e}\right) \tag{A.4}$$

where $X_e \equiv (\Delta V)/\phi_t$ to simplify the equation.

For a $I_{\rm out}(V_{\rm in}) = C_0\cdot(V_{\rm in}-V_{\rm th})^n$ nth-order power-law device, ξ can be calculated similarly to

$$\xi = \left(\frac{(1+X_p)^n-1}{n\cdot(X_p)^n}\right)^{\frac{1}{n-1}} - \frac{1}{X_p} \tag{A.5}$$

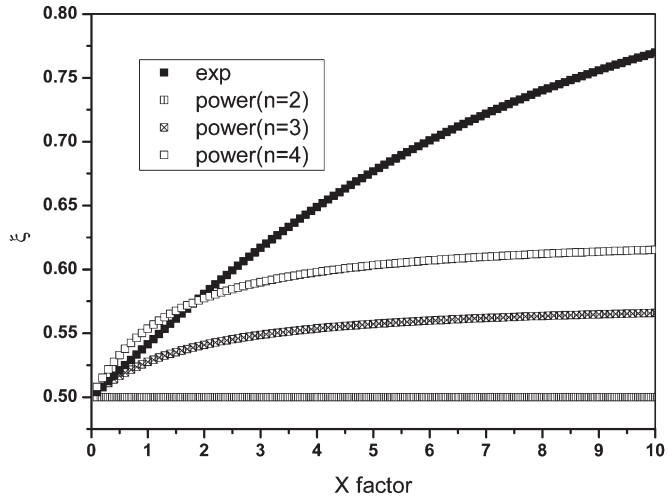

Fig. 9. Relationships between ξ versus X_e and X_p for exponential and power-law (order $= 2, 3, 4$) devices, respectively.

where $X_p \equiv \Delta V/(V_0 - V_{\rm th})$. The relationships between ξ versus X_e and X_p are plotted in Fig. 9. In the proposed design, the X_e is approximately 4.93 for MOSFETs in the subthreshold region, and thus, the corresponding ξ is 0.65.

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