

NCTU IEE 5046

高頻電路設計與實驗

PCB design with  
Pad Designer

Lecturer: Professor Yu-Jiu Wang

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Document coauthor: Jon-Jin Chen

# Related EDA tools

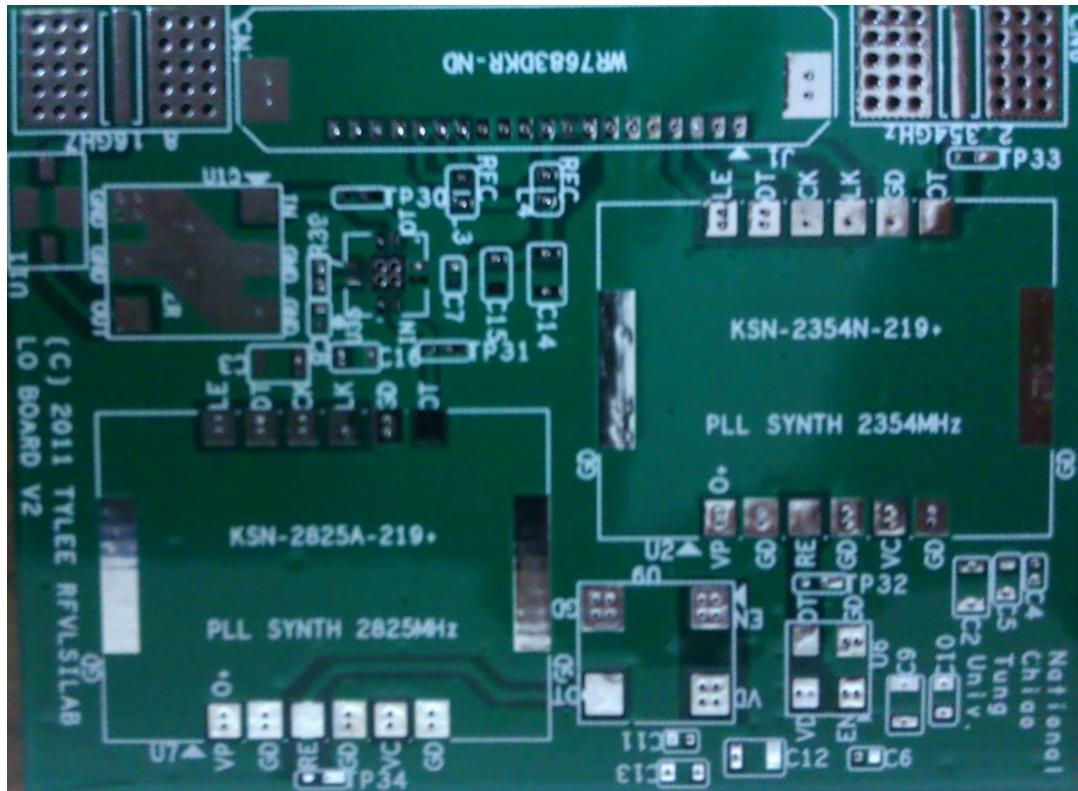
- Pad Designer



Pad Designer

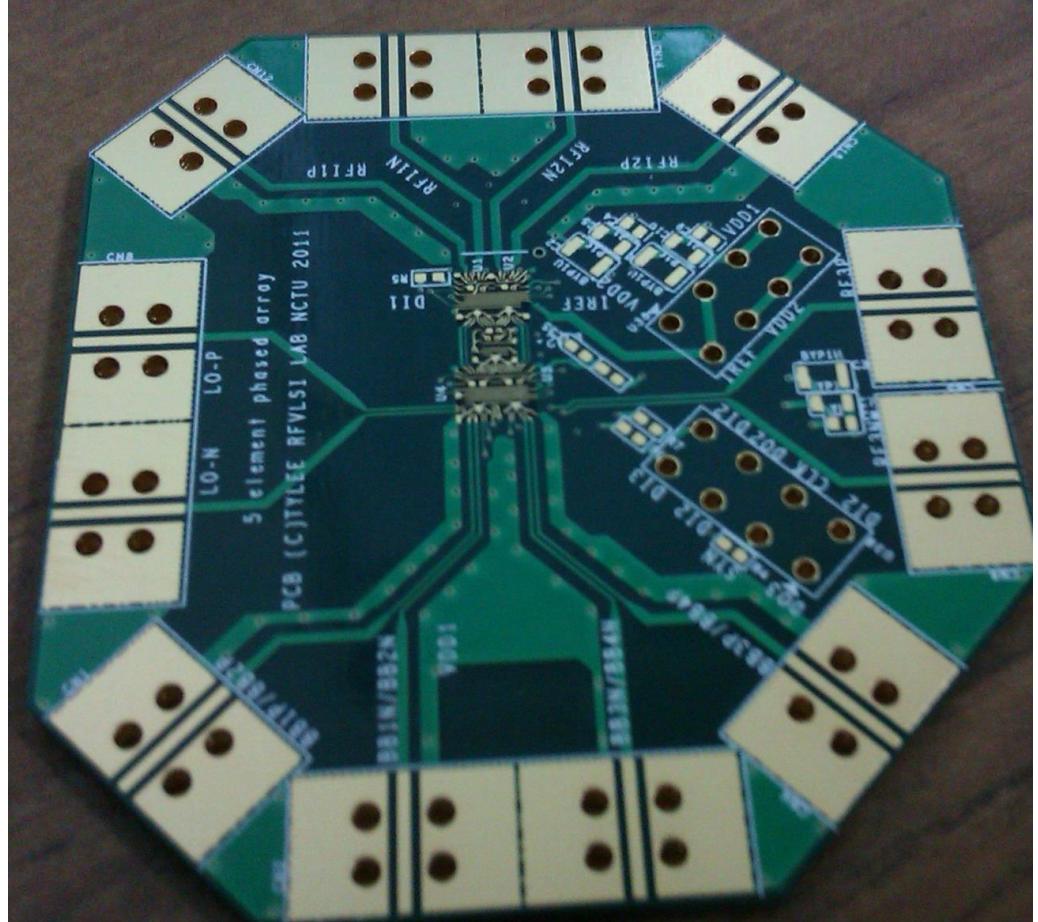
# PCB basics

- Solder mask
  - Dark Green
- Etch layer
  - i.e. Conductors
- Drill holes
  - Look closer to the pads
- Silk Screen
  - White characters and lines



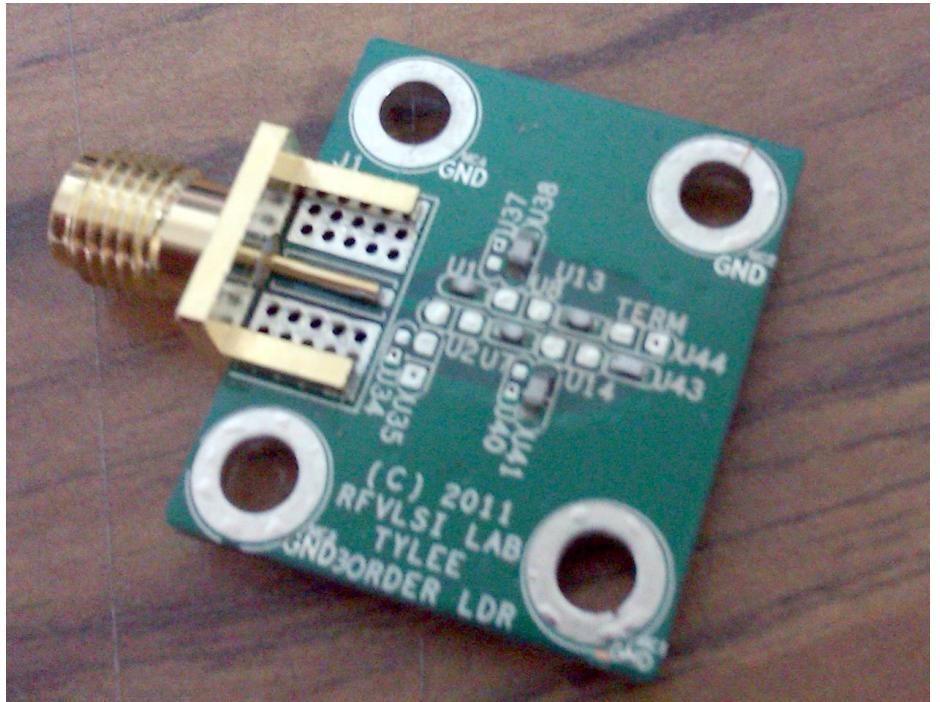
# High Frequency PCB

- Impedance control
- GND plane
- Cable to board transition
- EMI/EMC

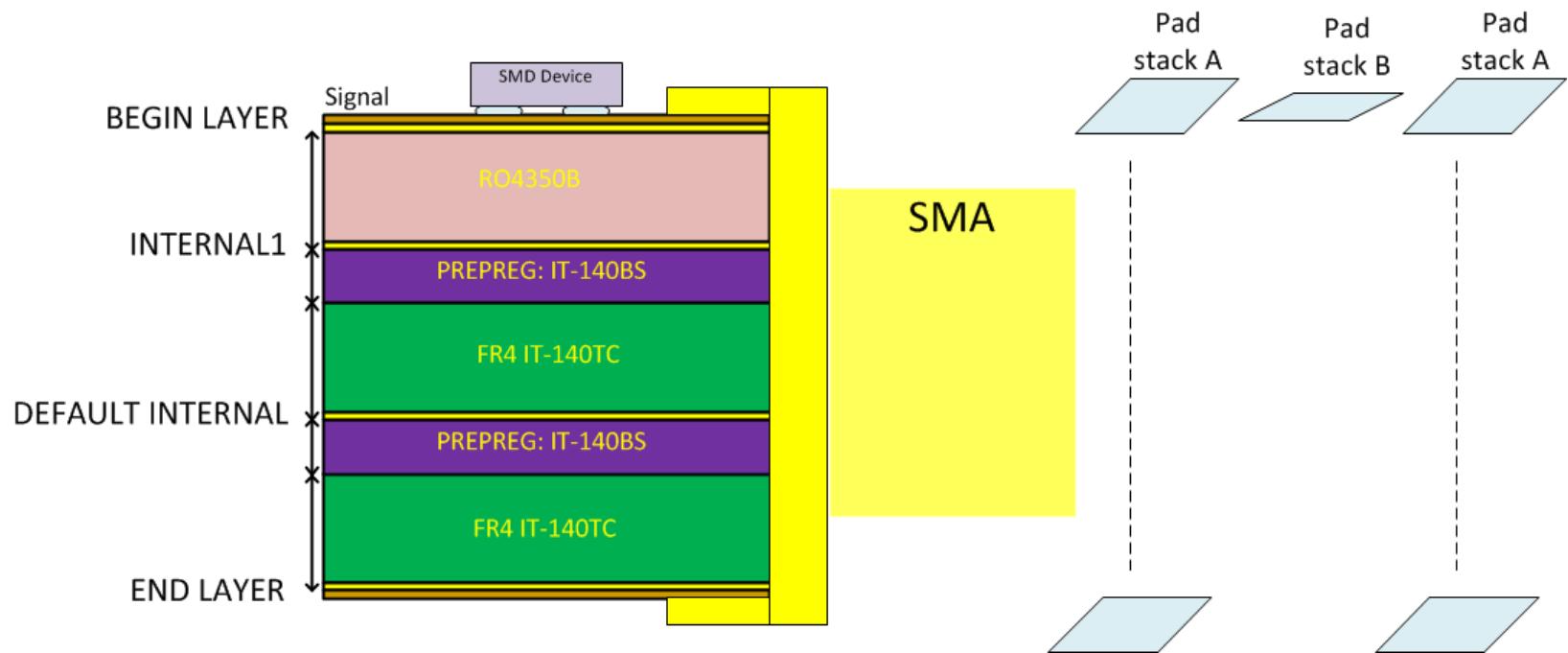


# SMT Soldering

- Solder
- Solder paste
- Solder iron

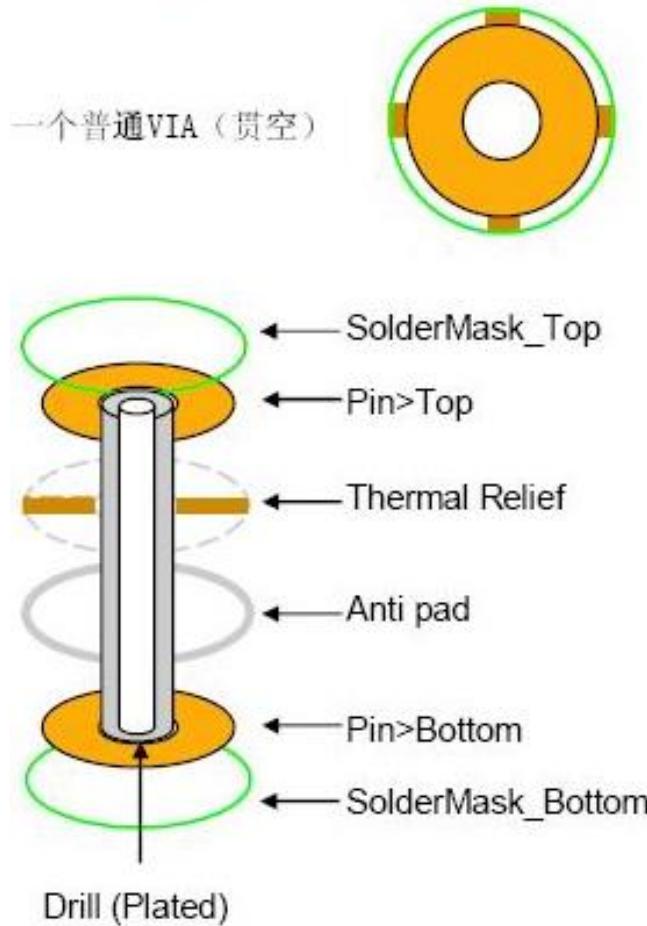


# Pad-Stack (4 Layer Stack Up)



# Definitions

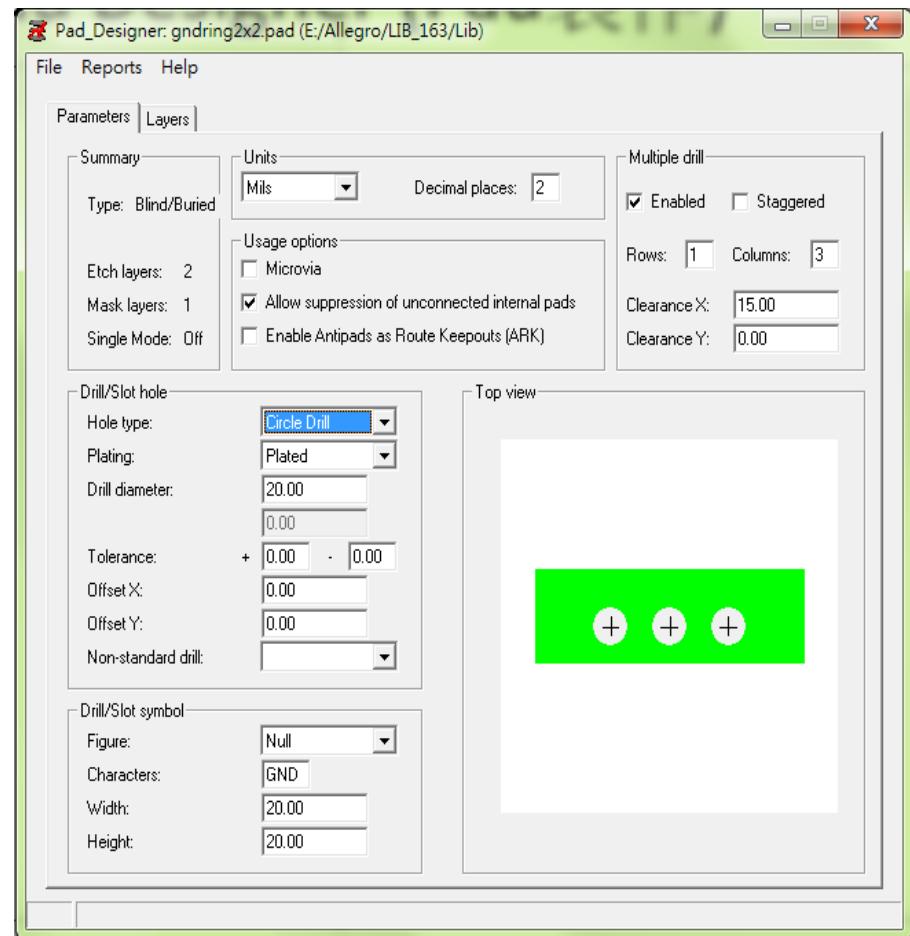
- Copper pad
- *Antipad*
- Thermal Relief
- Soldermask
- Drill
  - Plated: Conductive
  - Non-Plated: Isolated



# Create a Pad in *Pad Designer*

## “Parameters” Tab

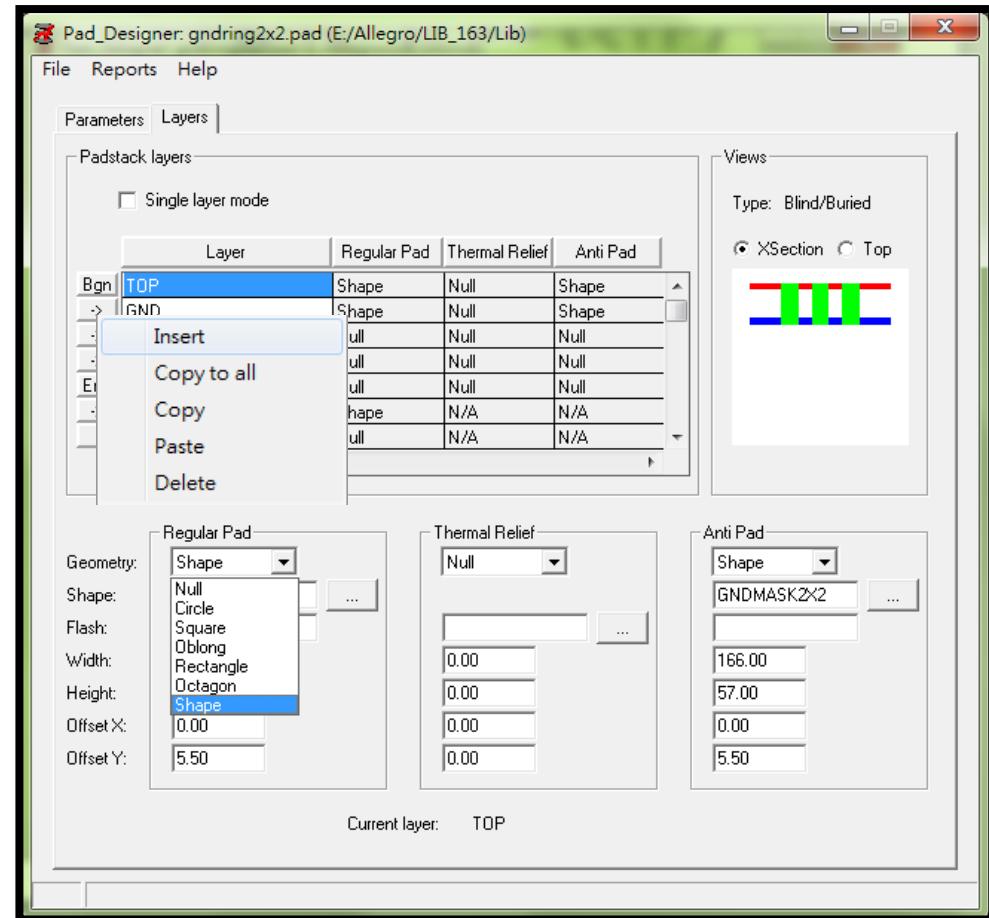
- Start Pad Designer
- Switch to “Parameters” tab
- Set units to “mils” with decimal places 2
- Decide whether to place drill holes on pad, if no drills needed, set drill diameter to 0.
- Do not use rectangle shaped drill holes in your project
- Drill/Slot symbol: optional
- Define multiple drill on the upper right pane, check “enabled” to enable; Specify clearances if needed.



# Create a Pad in Pad Designer

## “Layers” Tab

- For SMD: Check “Single layer mode”
- Right click on “Bgn” to insert layers
- Select regular pad shape and specify size
- **Antipads**
  - for PCB with internal conducting layers, define antipads
  - should be larger than regular pad , 6 mils around
- **Solder-masks** should also be larger than regular pad
- Save your \*.pad to the specified “PADPATH” in Allegro



# Create *antipad / soldermask* for a padstack

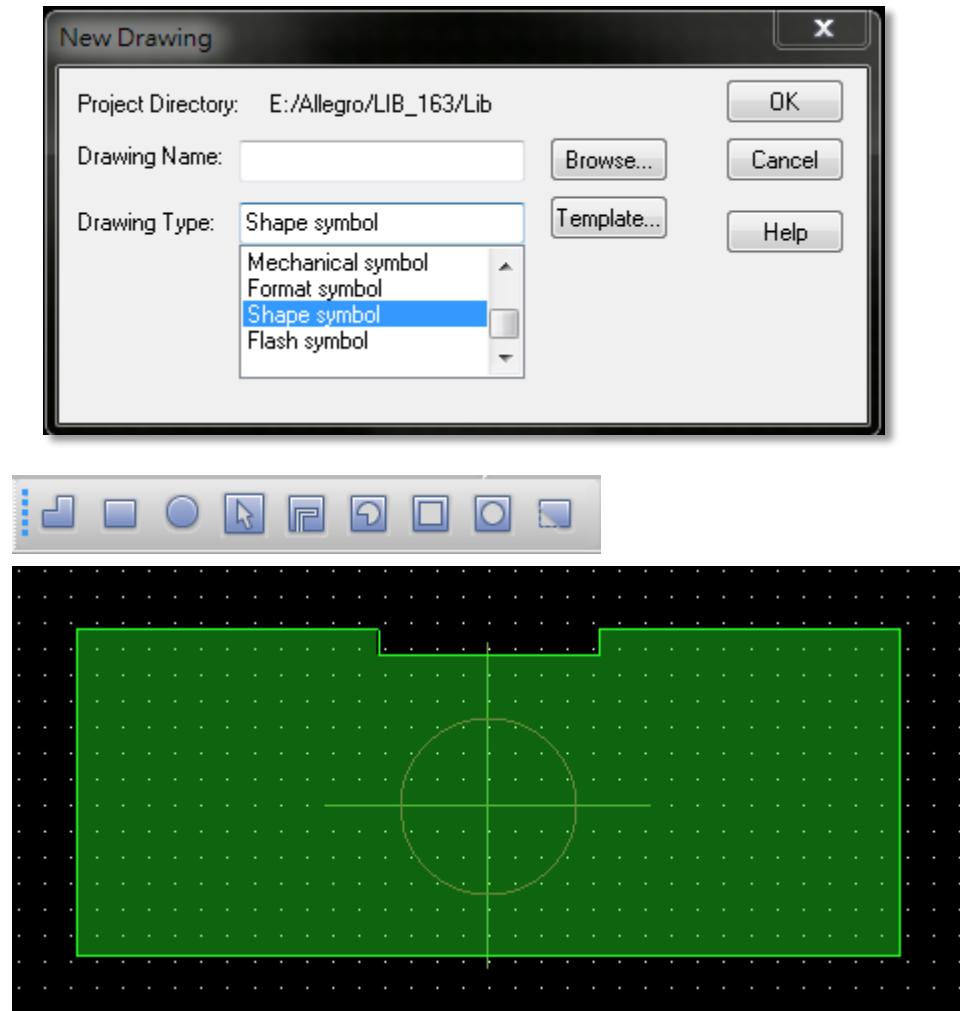
- Generally, antipad and soldermask encloses regular pad by 3 mil (Depends on the min. etching gap of PCB process)

	Circle	Rectangle	Shape
Regular Pad	R mil	W mil × L mil	Manually assign
Antipad	R+6 mil	W+6mil × L+6 mil	Manually assign (Align Origin)
Solder Mask Top	R+6 mil	W+6mil × L+6 mil	Manually assign (Align Origin)
Thermal Relief	R+6 mil	W+6mil × L+6 mil	Manually assign (Align Origin)

# Special Shaped Pads

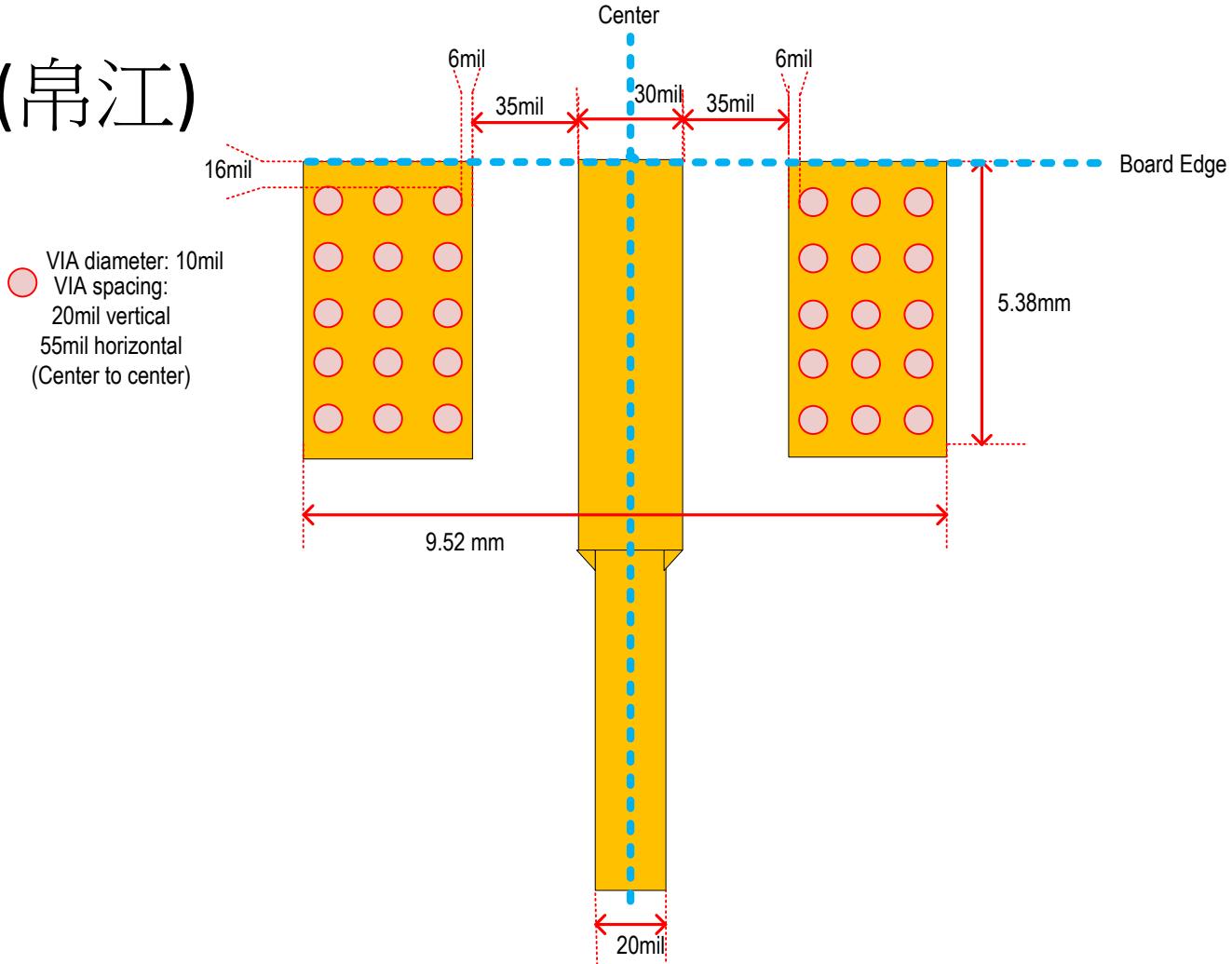
## New “Shape symbol” in PCB Editor

- File -> New
  - Create a *shape symbol*
- 此時只有Etch可以用
- 用上列工具列畫出想要的圖形後
- Shape -> Merge Shapes可以把圖合再一起，才不會有DRC Error
- 畫完後直接在外面加一層3mil的框用來做Pad的Soldermask (要另存)這樣他們就會對齊
- Default drill hole location is the origin

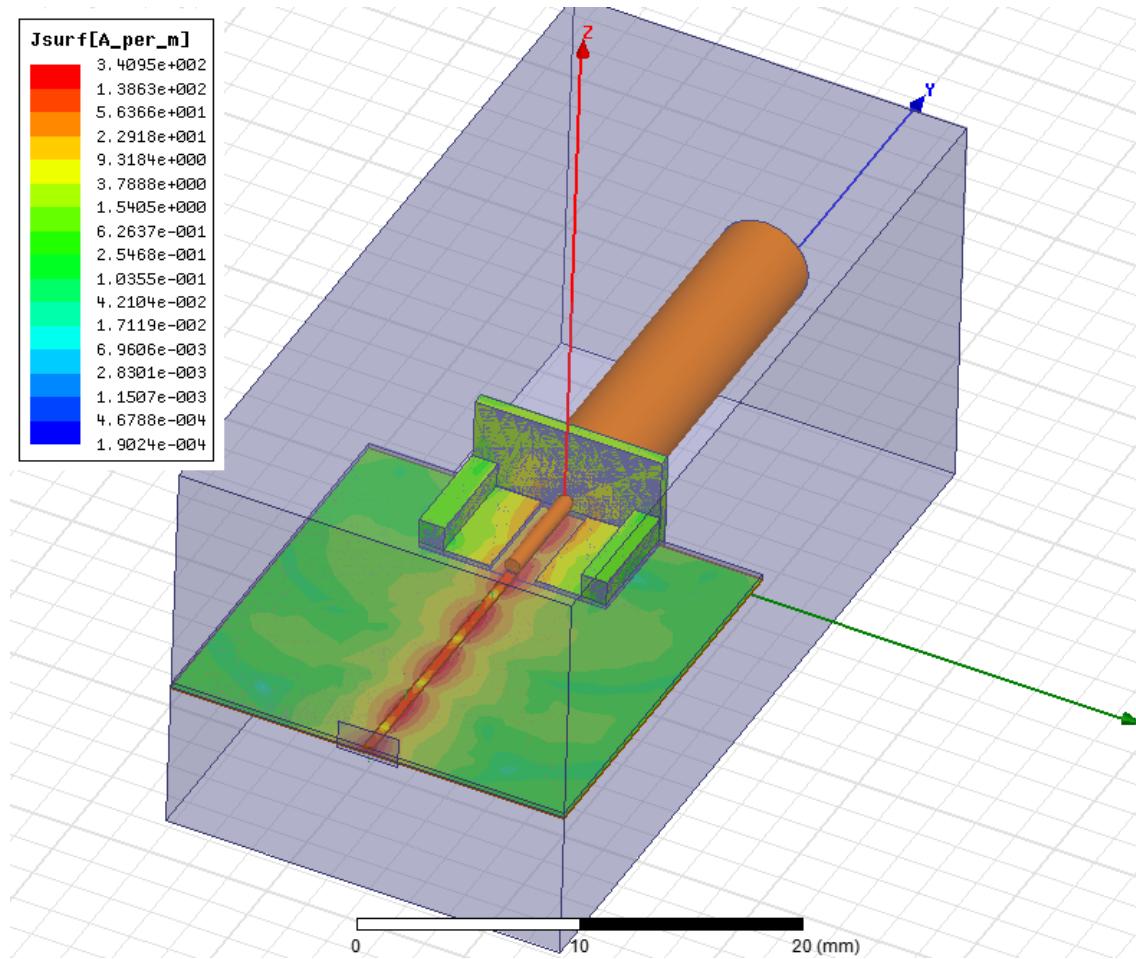


# SMA Connector Padstack

- Bo-Jiang(帛江)
- 7867LS



# Surface Current Density Plot @ Radio Frequency



# NCTU IEE 5046

# 高頻電路設計與實驗

## Allegro PCB Editor -

## Create Package Symbol

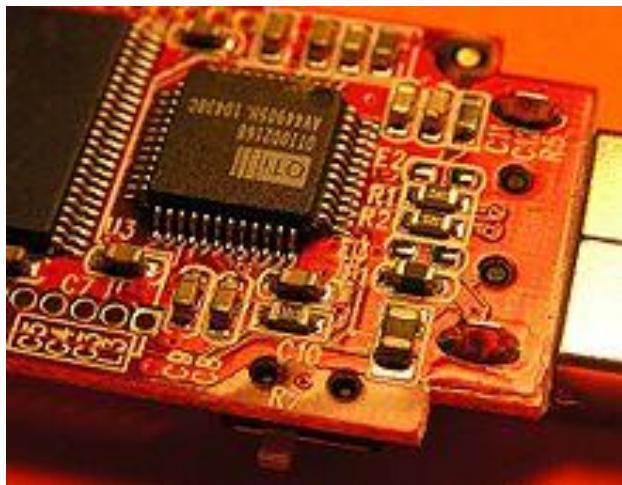
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Document coauthor: Jon-Jin Chen

# Package Symbol

- Two category of footprints:
  - SMT – Surface Mount Technology
  - TH – Through Hole



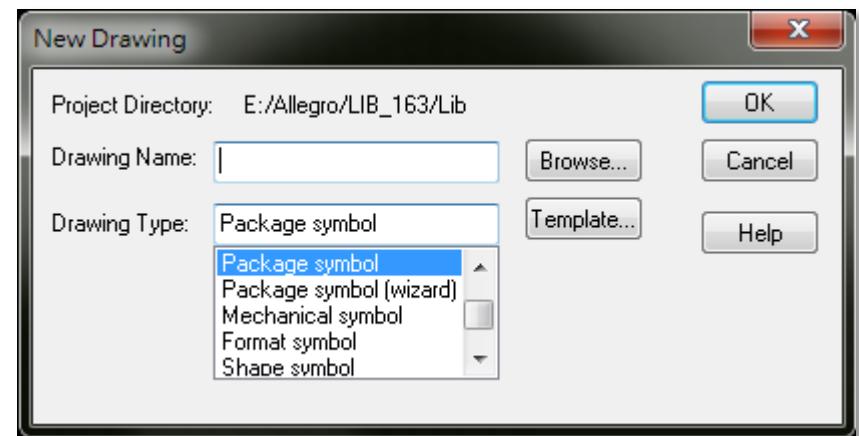
Surface Mount Technology



Through Hole

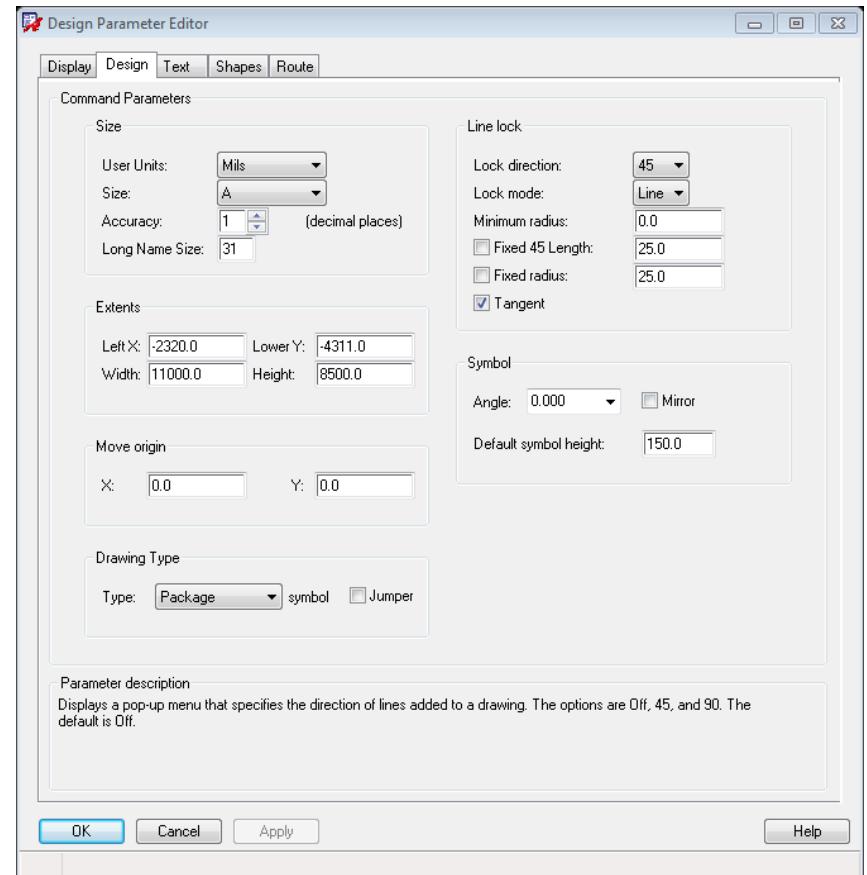
# New Package Symbol

- Menu -> File -> New
- Remember to save package symbol at \$psmpath



# Basic Environment Setup

- Menu-> Setup -> Design Parameters
- Grid
  - Turn on 
  - 1 mil
- Units
  - Use English units (mil) to avoid conversion errors

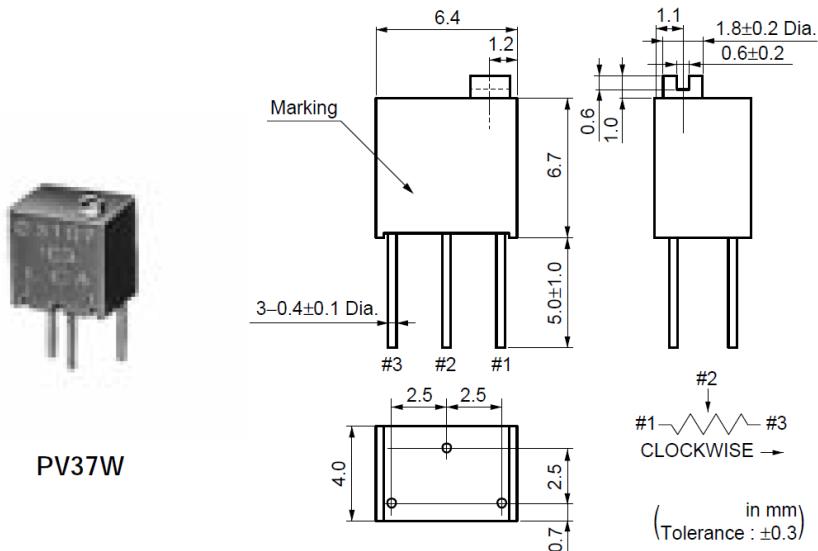


# Look For Datasheet

- Digikey
  - <http://www.digikey.com>
- Mouser
  - <http://www.mouser.com>
- Extract Dimensions
  - Use professional version of Adobe Acrobat
  - Use Autocad
  - By hand

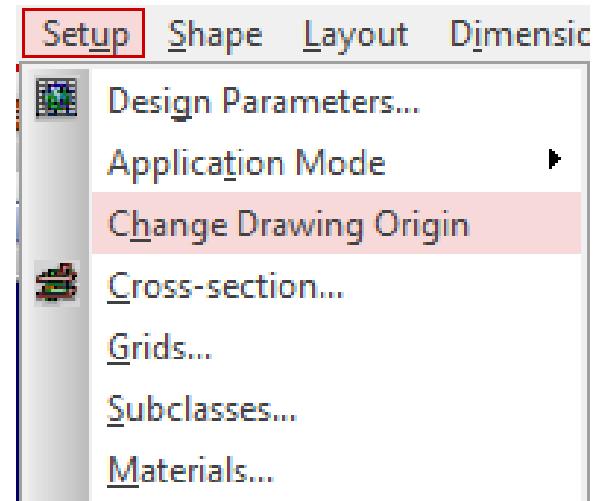
# Through Hole Example

- Using: Murata PV 37 Series
- Be careful of the units
- Define pin numbers as datasheet suggests



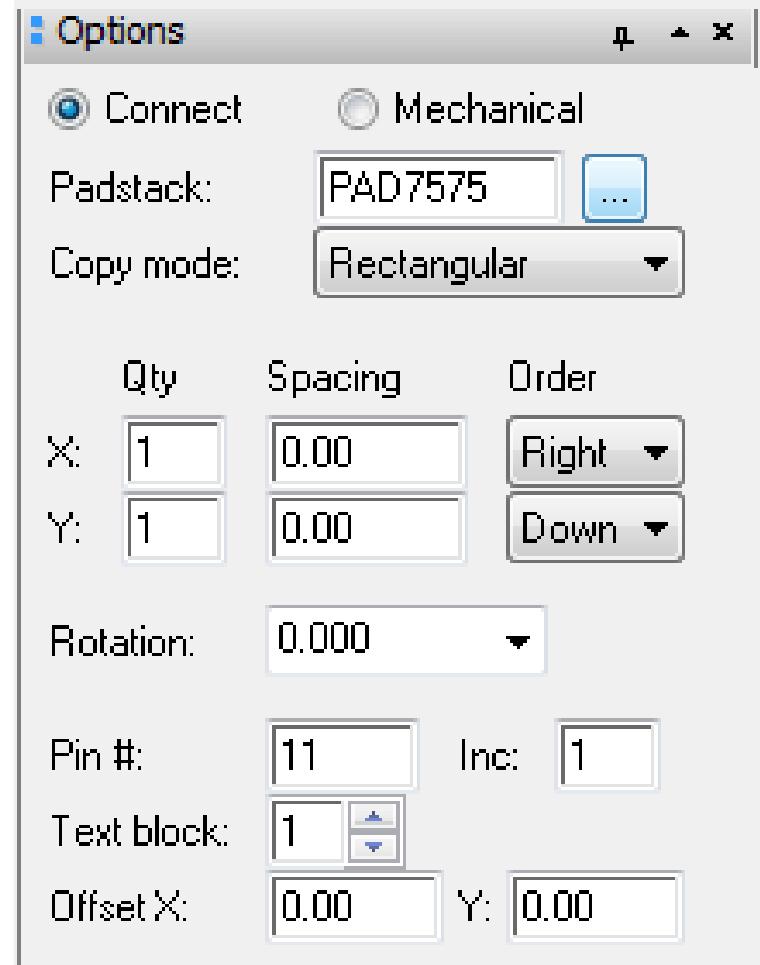
# Through Hole Example

- Steps:
  - Define Origin
    - Center of n-th pin
    - Package Edge
    - Change origin dynamically for convenience
  - Write down dimensions on a draft paper first
  - Prepare pad-stack with pad designer
    - Configure drill holes on pad-stack
  - Place Pads



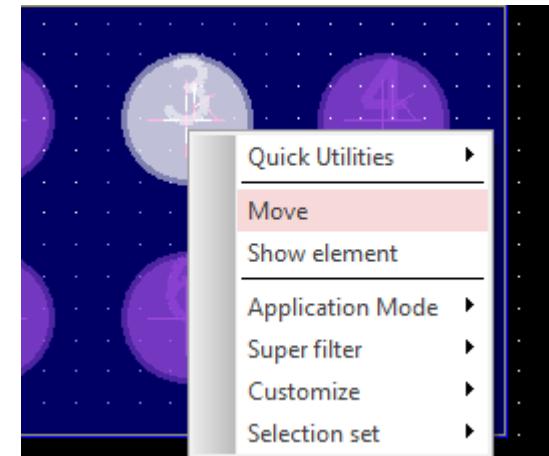
# Place Pins for a Symbol

- 把Pin放到Package上
- Layout -> Pins 
- 從右邊的option選擇要用的Padstack
- Manually assign coordinate for accuracy
  - P : Pick Point  
  - A : Toggle Absolute /Relative Mode



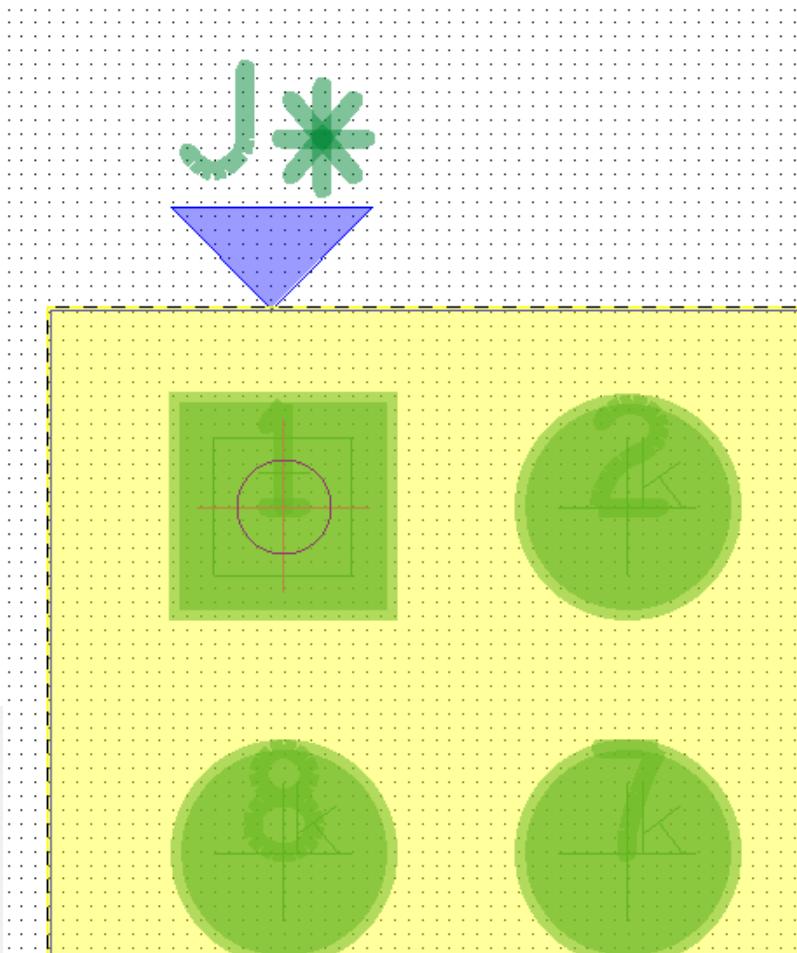
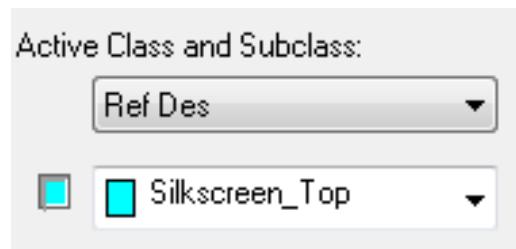
# Modify Pins After Placement

- 還有Rotation的角度(選完後再按一次 Layout -> Pins)
  - Use context menu to move, than use context menu again to rotate
- 還有最重要的Pin #
  - 要和capture上的腳位一模一樣
  - Use Edit text to change Pin #



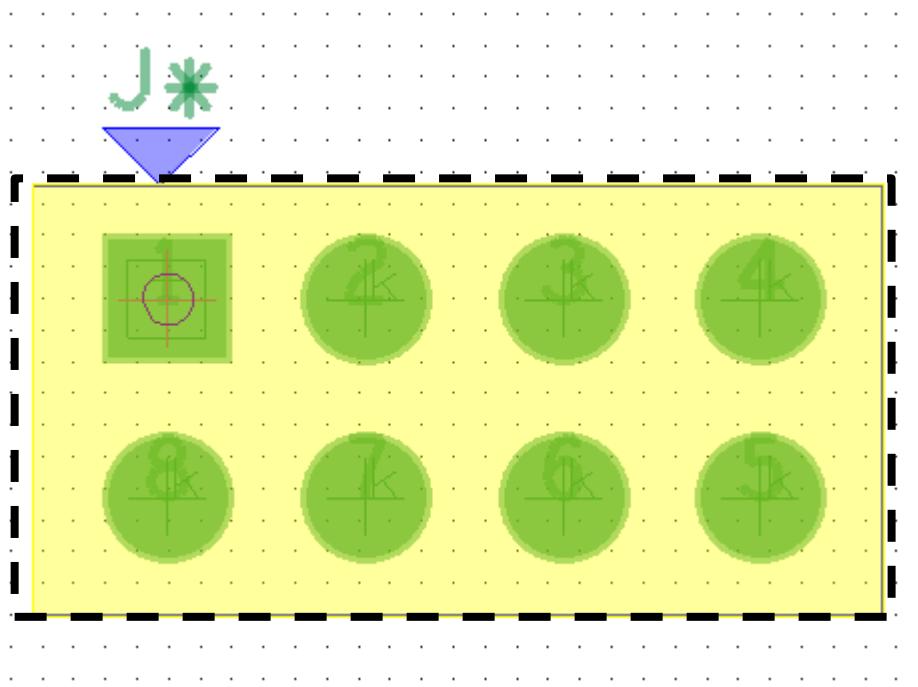
# Assign Reference Designator (RefDes)

- 設定Device Type和Ref Des
- Add -> Text (任意字串 e.g. J\*)
- 在右邊Option選擇 Device Type/ Silkscreen\_Top放在第一個pin



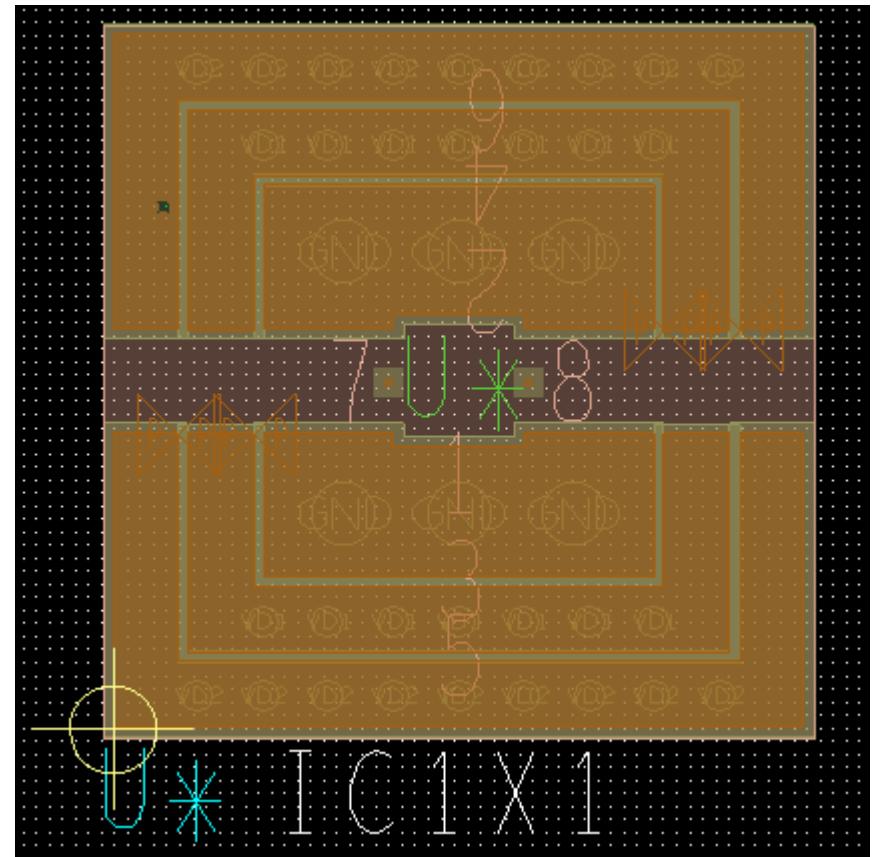
# Assign Package Boundaries

- 選擇Setup -> Areas -> Package Boundarys 後, 選矩形  把整個元件包起來(Pin的部分)



# Create Device File and Symbol (\*.psm)

- 存檔: File -> Save
- 製作元件: File -> Create Device



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OrCAD Capture

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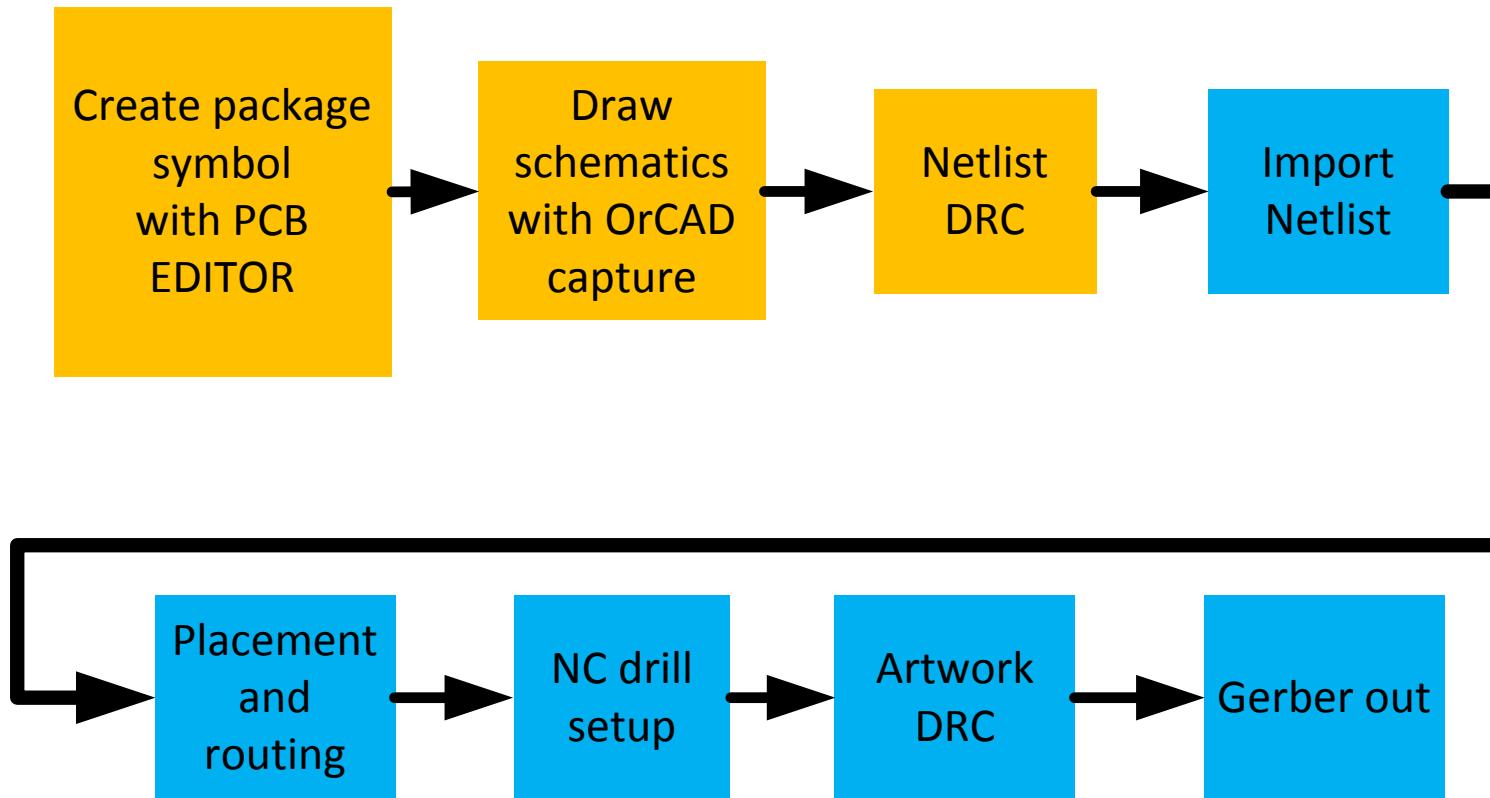
TA: 李道一 [michael@rfvlsi.ee.nctu.edu.tw](mailto:michael@rfvlsi.ee.nctu.edu.tw)

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# Related EDA tools

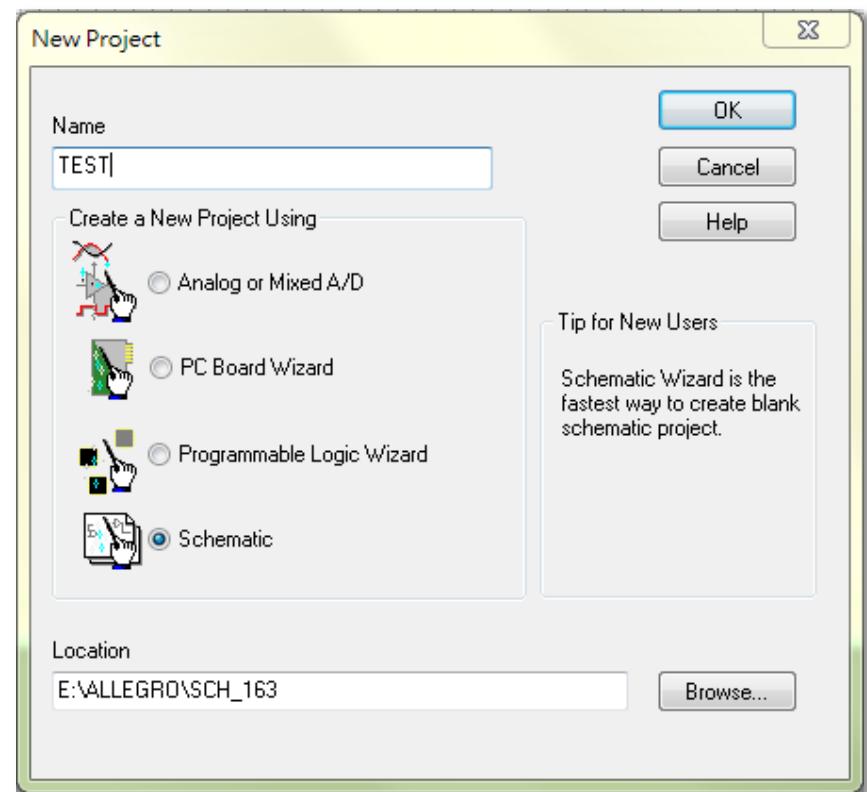
- OrCAD Capture  OrCAD Capture
- PCB Editor  PCB Editor
- Pad Designer  Pad Designer

# Design Flow



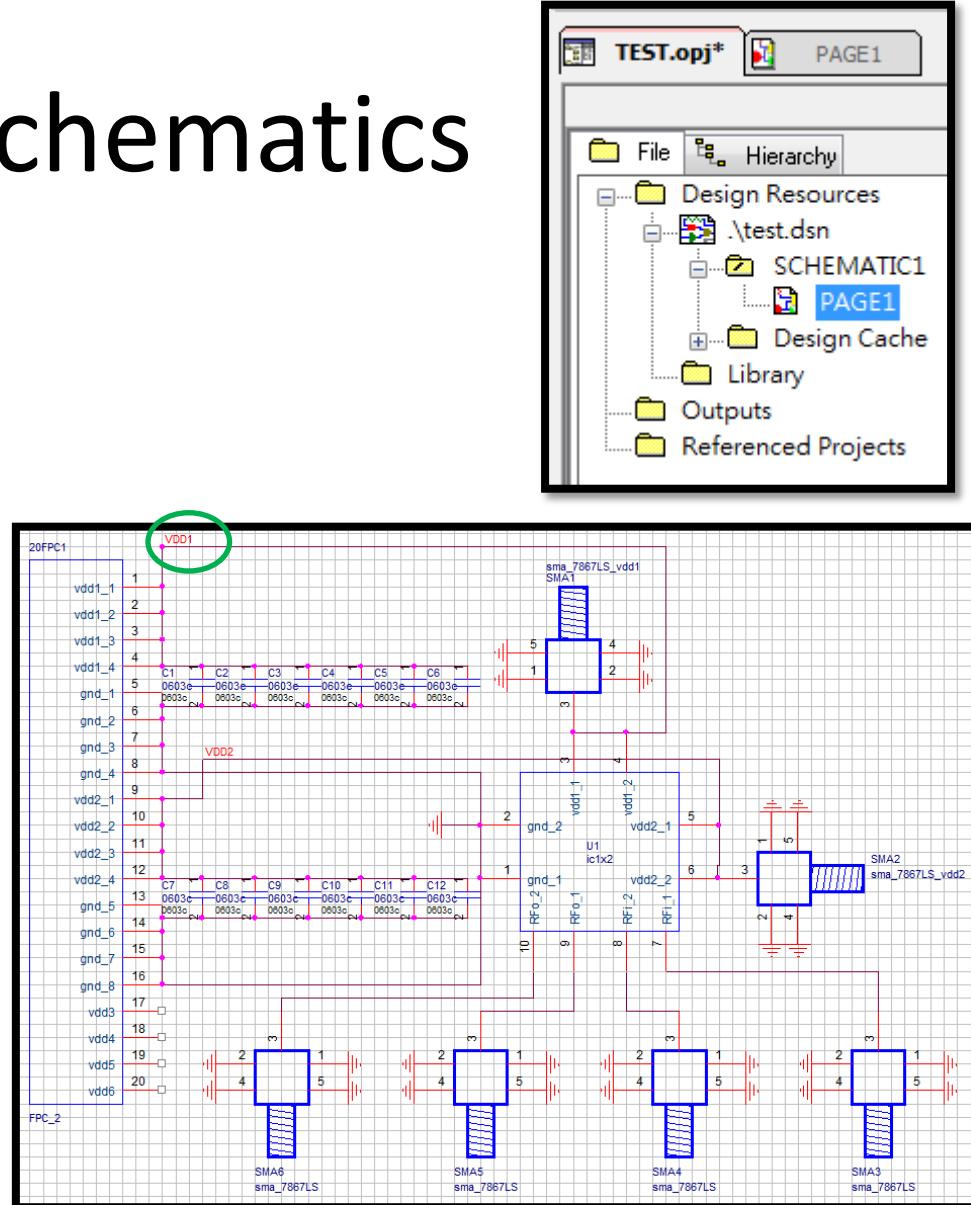
# OrCAD Capture

- 第一次打開OrCAD Capture選擇選單中的第一個OrCAD Capture,並在use as default打勾
- File -> new -> Project
- 選擇Schematic以及儲存的位置
- 按ok



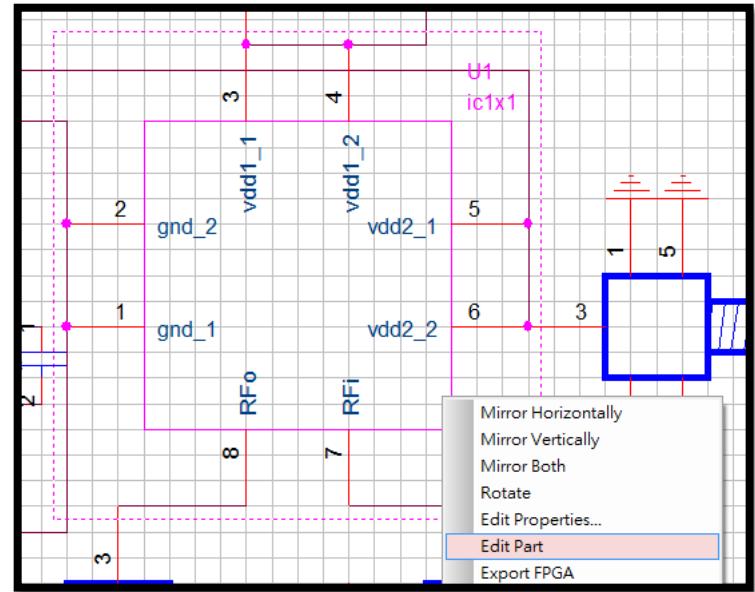
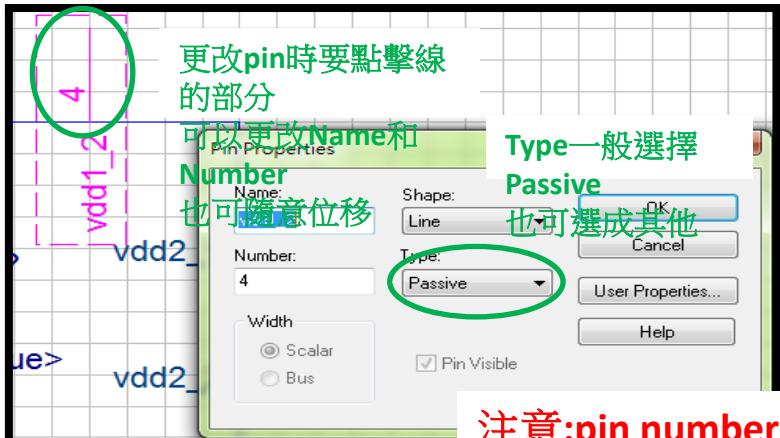
# Create Schematics

- 在XXX.opj的子頁面中
- 點開XXX.dsn之後再點開SCHMATIC1, 點開PAGE1
- 接出自己想要用的電路
- 電路上的元件可從做好的電路複製
- 如果板子不夠大, 可從Options->Schematic Page Properties改變板子大小(optional)
- 如果想要幫某條net取名字可從Place->Net Alias, ok後放到想取名的net上(optional)



# Create Schematics

- 如果要更改元件
- 先點一下讓元件變成粉紅色
- 再按右鍵選擇Edit Part



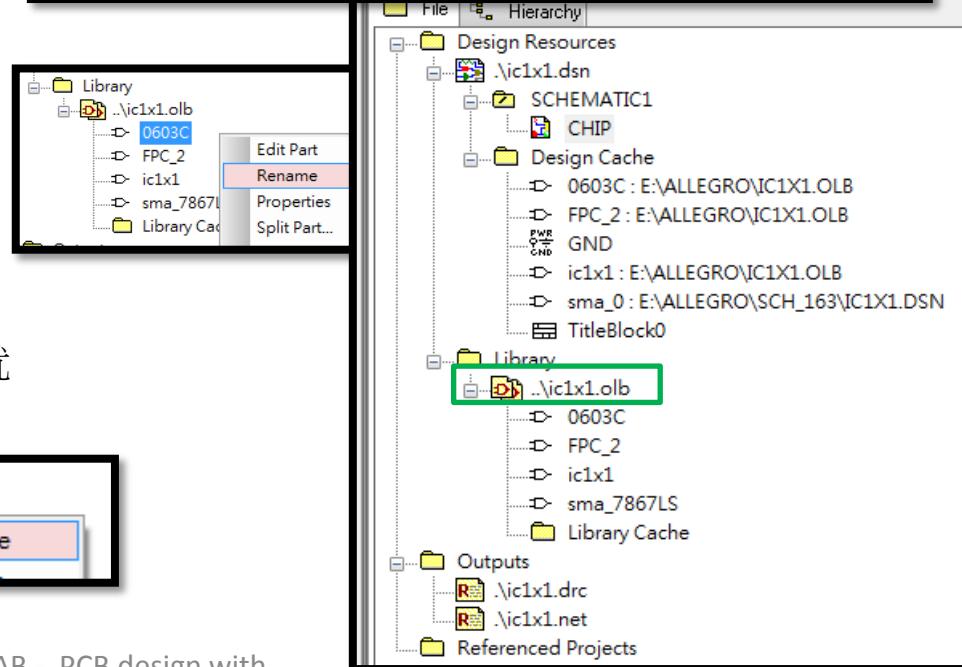
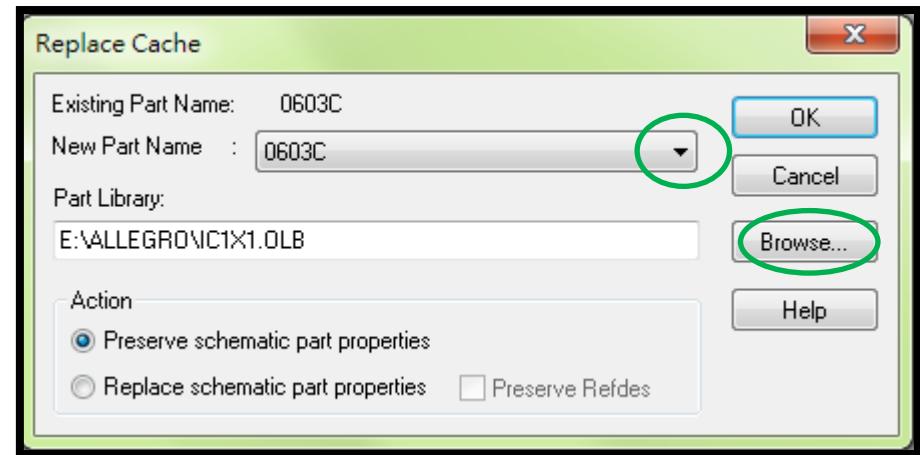
若要新增pin可從place->pin  
或直接點右邊直列的圖式



若要刪除則直接按delete

# Create Library

- 電路完成後,回到XXX.obj的頁面,並建立library:
- File -> New -> Library
- 就會看到Library底下的XXX.olb (可改成自己喜歡的名字)
- 接著把Design Cache底下的元件拖曳到XXX.olb上
- 並且把加入Library的元件名稱改為和在PCB Editor裡面的dra檔名相同
- 接著回到Design Cache 對剛剛加入的元件按右鍵
  - 選擇Replace Cache
  - 先從Browse選擇剛剛建立的XXX.olb
  - 接著在New Part Name的下拉式選單中選擇想要換成的元件名稱,並按ok就完成了



# Assign PCB Footprint

- 輸出電路前確認電路元件
- 在SCHEMATIC1上按右鍵選擇Edit Object Properties
- 紅色框內的欄皆要和對應的PCB Package Symbol的Device Type相同
- 綠色框內的欄則要和對應的PCB Package Symbol的Ref Des相同
- 藍色框內的欄則要和對應的PCB Package Symbol的dra檔名相同

The screenshot shows a parts list table and a context menu for a component in the schematic editor.

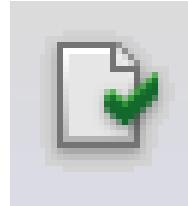
**Parts List Table:**

Graphic	Source Package	Source Part	PCB Footprint	Value	Part Reference	Reference
FPC_2.Normal	FPC_2	FPC_2.Normal	FPC_2	FPC_2	20FPCT	20FPCT
0603C.Normal	0603C	0603C.Normal	0603c	0603c	C1	C1
0603C.Normal	0603C	0603C.Normal	0603c	0603c	C2	C2
0603C.Normal	0603C	0603C.Normal	0603c	0603c	C3	
0603C.Normal	0603C	0603C.Normal	0603c	0603c	C4	
0603C.Normal	0603C	0603C.Normal	0603c	0603c	C5	
0603C.Normal	0603C	0603C.Normal	0603c	0603c	C6	
0603C.Normal	0603C	0603C.Normal	0603c	0603c	C7	
0603C.Normal	0603C	0603C.Normal	0603c	0603c	C8	
0603C.Normal	0603C	0603C.Normal	0603c	0603c	C9	
0603C.Normal	0603C	0603C.Normal	0603c	0603c	C10	
0603C.Normal	0603C	0603C.Normal	0603c	0603c	C11	C11
0603C.Normal	0603C	0603C.Normal	0603c	0603c	C12	C12
sma_0.Normal	sma_0	sma_0.Normal	sma_7867LS_vdd1	sma_7867LS_vdd1	SMA1	SMA1
sma_0.Normal	sma_0	sma_0.Normal	sma_7867LS_vdd2	sma_7867LS_vdd2	SMA2	SMA2
sma_0.Normal	sma_0	sma_0.Normal	sma_7867LS	sma_7867LS	SMA3	SMA3
sma_0.Normal	sma_0	sma_0.Normal	sma_7867LS	sma_7867LS	SMA4	SMA4
ic1x1.Normal	ic1x1	ic1x1.Normal	ic1x1	ic1x1	U1	U1

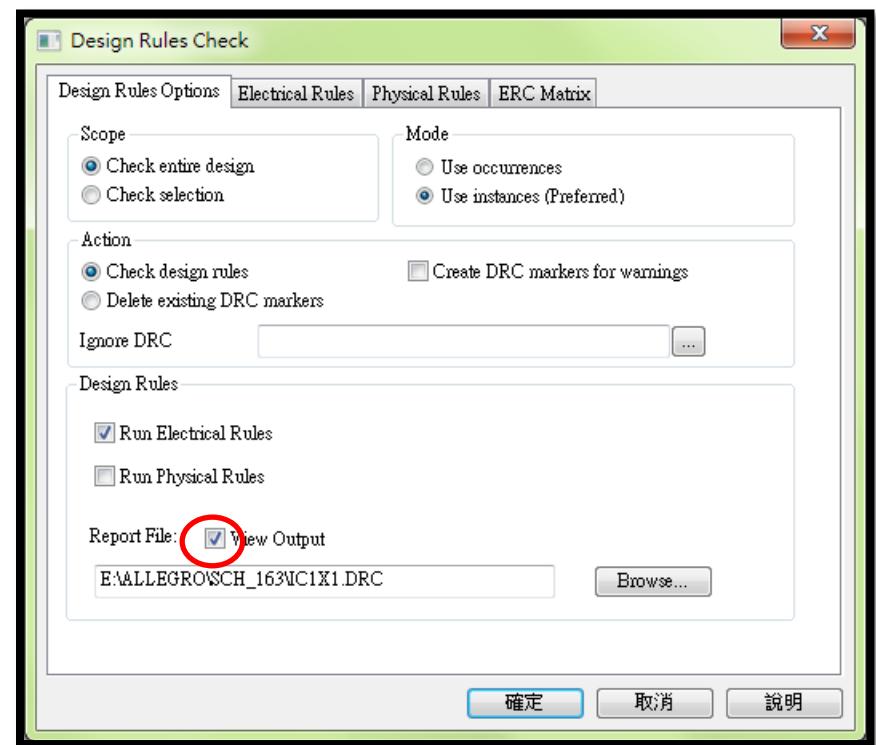
**Context Menu (Right-clicked on a component in the schematic):**

- New Page
- Make Root
- Rename
- Properties
- Edit Object Properties (highlighted)

# Schematics DRC check

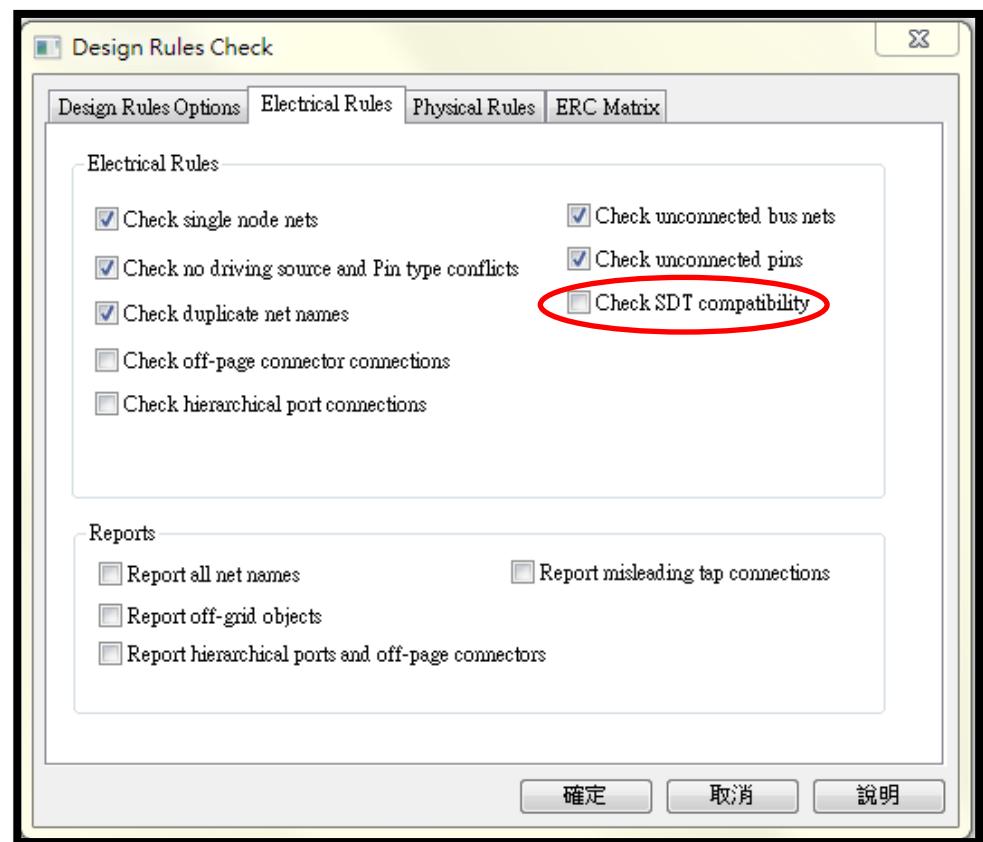


- 輸出電路前先做DRC Check
- Tools->Design Rule Check
- 設定完後按確定
- 並將錯誤更正



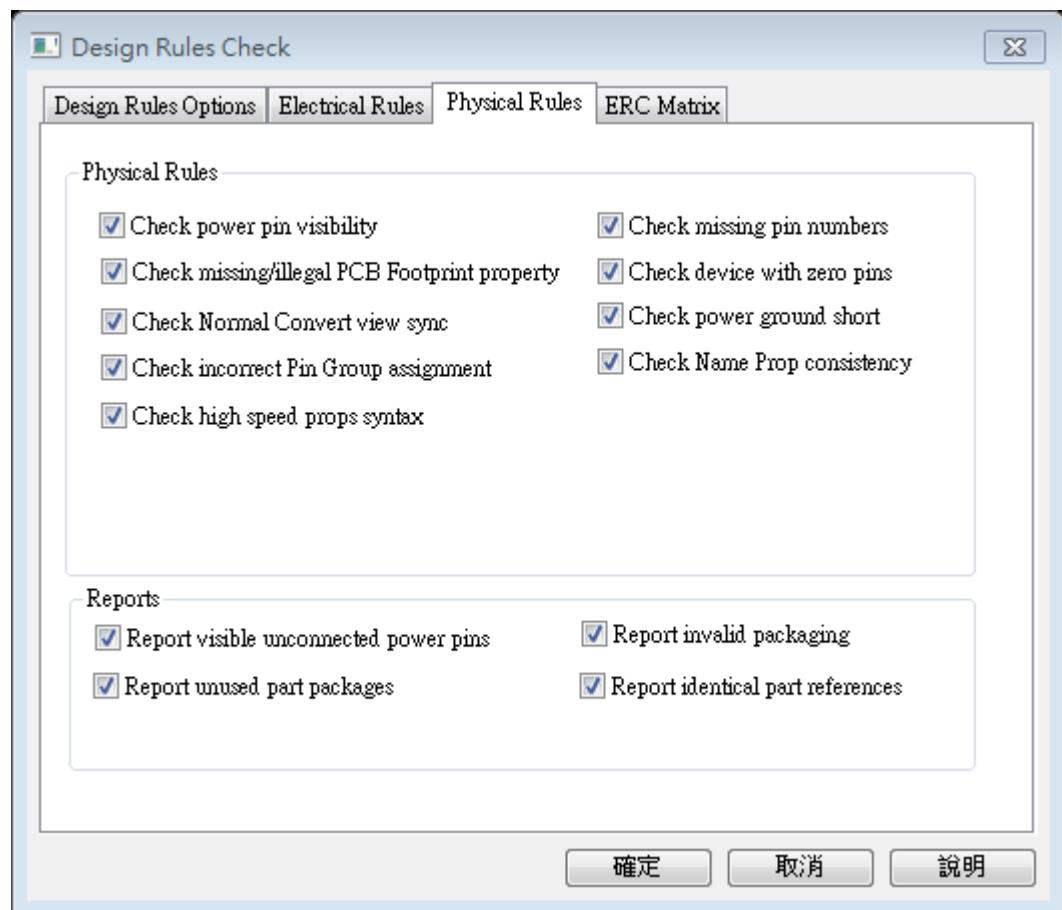
# Schematics DRC check (cont'd)

- Second tab of DR checker



# Schematics DRC check (cont'd)

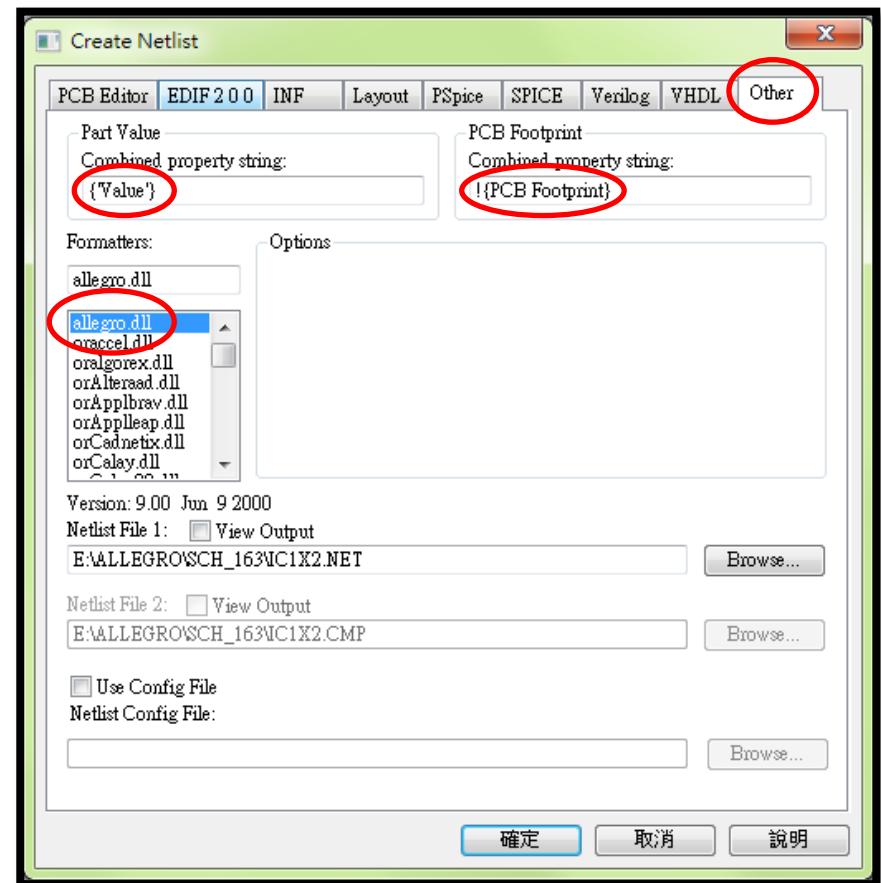
- Third tab of DR checker



# Generate Netlist



- 輸出電路
- Tools->Create Netlist
- 直接跳到Other的子頁面
- 注意allegro.dll檔要放在
- C:\Cadence\SPB\_16.3\tools  
  \capture\netforms\
- **{'Value'}**和**!{PCB Footprint}**  
要打對
- 按確定後電路就會輸出  
XXX.NET



# NCTU IEE 5046

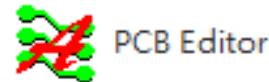
## 高頻電路設計與實驗

## Allegro PCB Editor

Lecturer: Professor Yu-Jiu Wang  
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# Related EDA tools

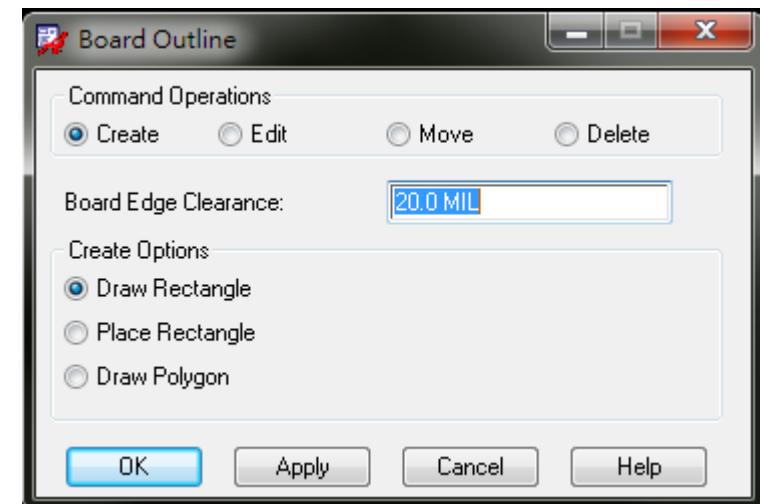
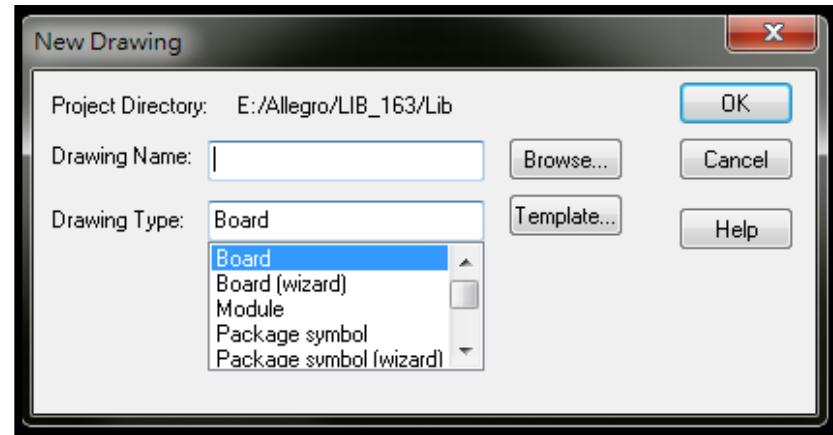
- PCB Editor



PCB Editor

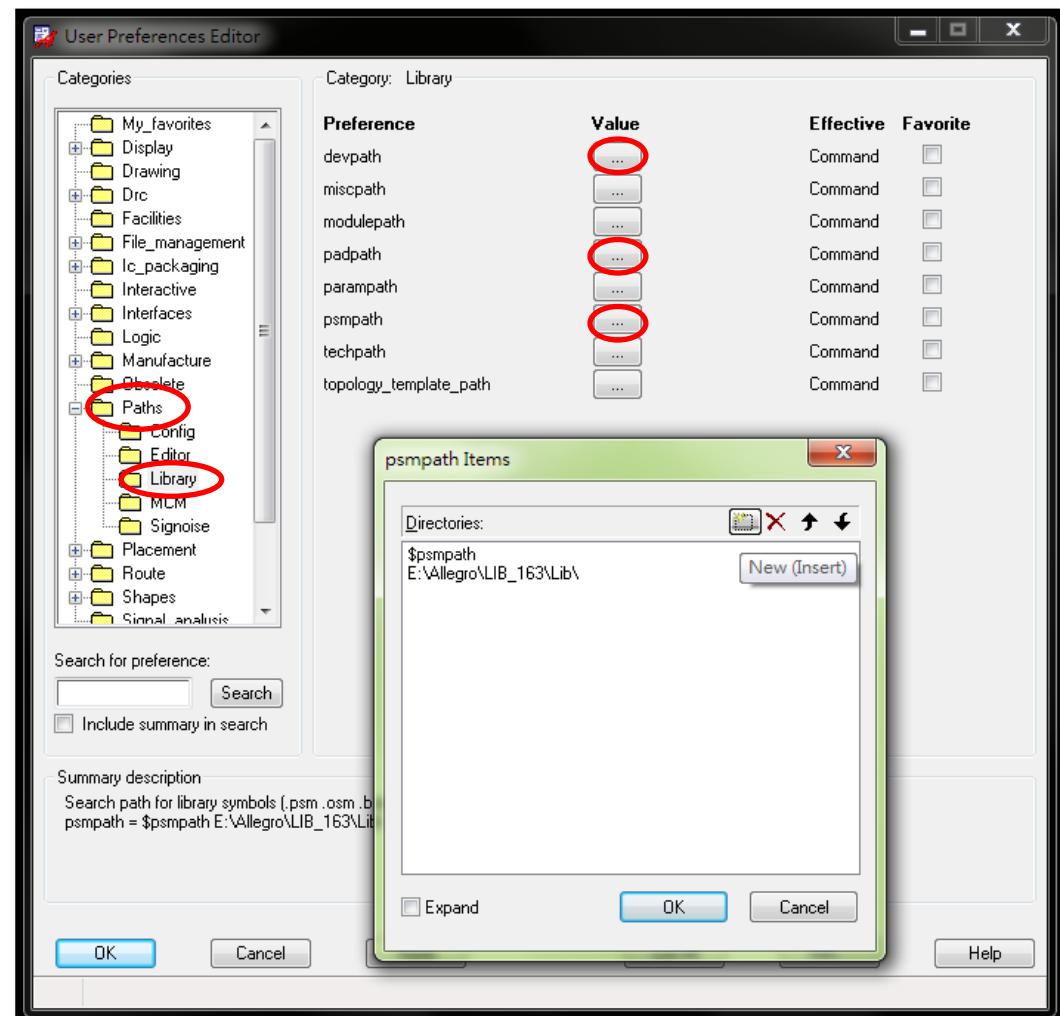
# New PCB design in PCB Editor

- 打開PCB Editor
- File ->New
- 選擇Board並打上檔名按OK
- 一開始會看到一片黑和一個小小的綠色十字(就是原點)
- 想要把什麼地方放大縮小用滑鼠先指到那個位置
- 再用滾輪放大縮小畫面
- 接下來畫一塊板子
- Setup -> Outlines -> Board Outline
- 先隨便畫一個框
- 畫好了以後再點ok
- 如果之後要改變大小/位置可以按Edit/Move



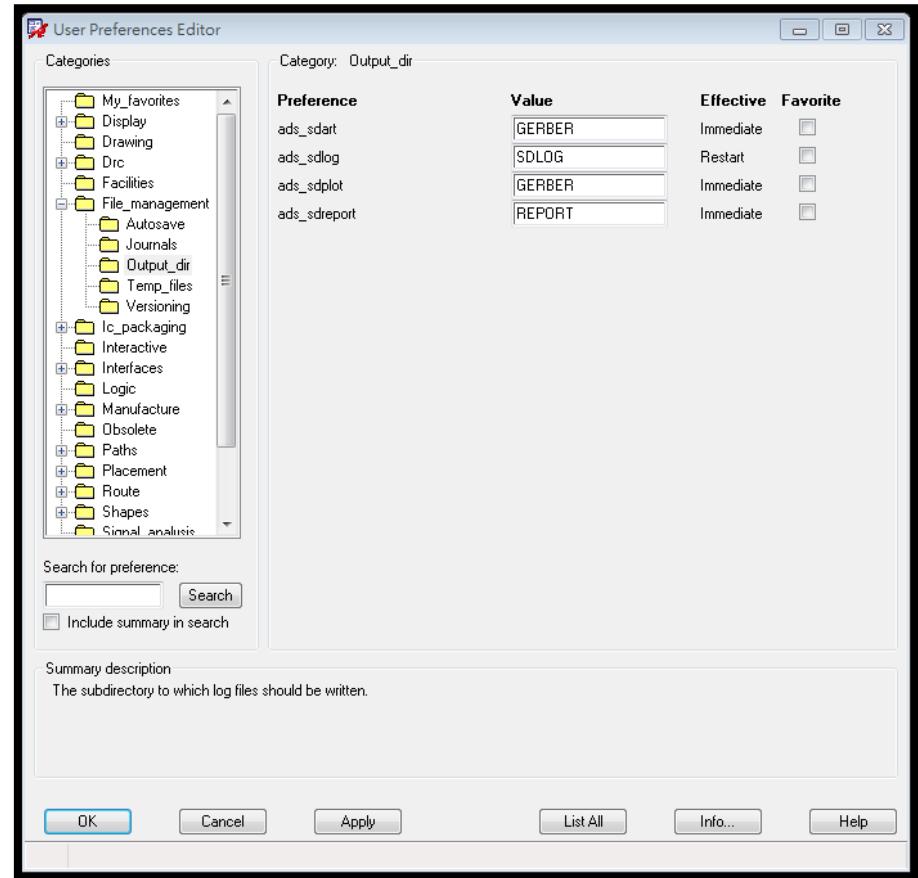
# Setup Search Paths

- Setup -> User Preferences
- 點選Paths底下的Library
- devpath
- padpath
- psmpath都增加放.dra檔和放.pad檔的位置



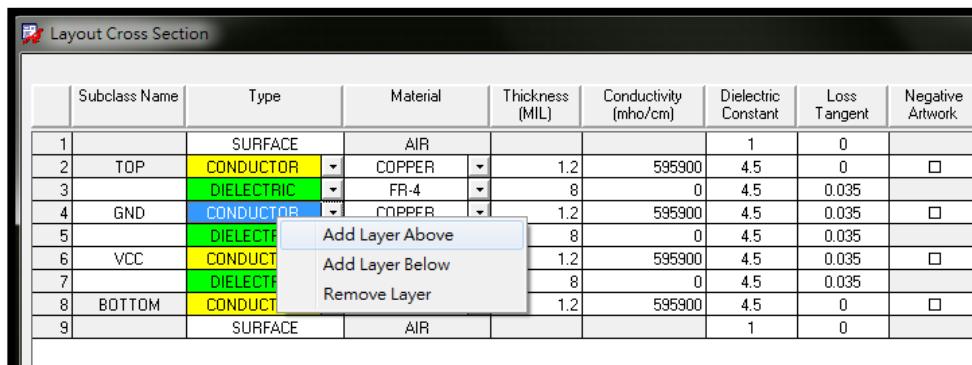
# Setup Output Directories

- 設定Gerber和log檔輸出目錄，會讓你的工作目錄變整齊



# Setup Layout Cross Sections

- Setup -> Cross-section 
- TOP和BOTTOM不可更改
- 如果要增加或減少層數可按右鍵選Add Layer Above/Below
- 並將名字改成和使用的Package Symbol的層數相同
- 也可以選擇Negative Artwork
- 如果要更改顏色
- Display -> Color/Visibility 
- 先在下面的調色盤選好顏色後
- 再點上面想要改變的顏色

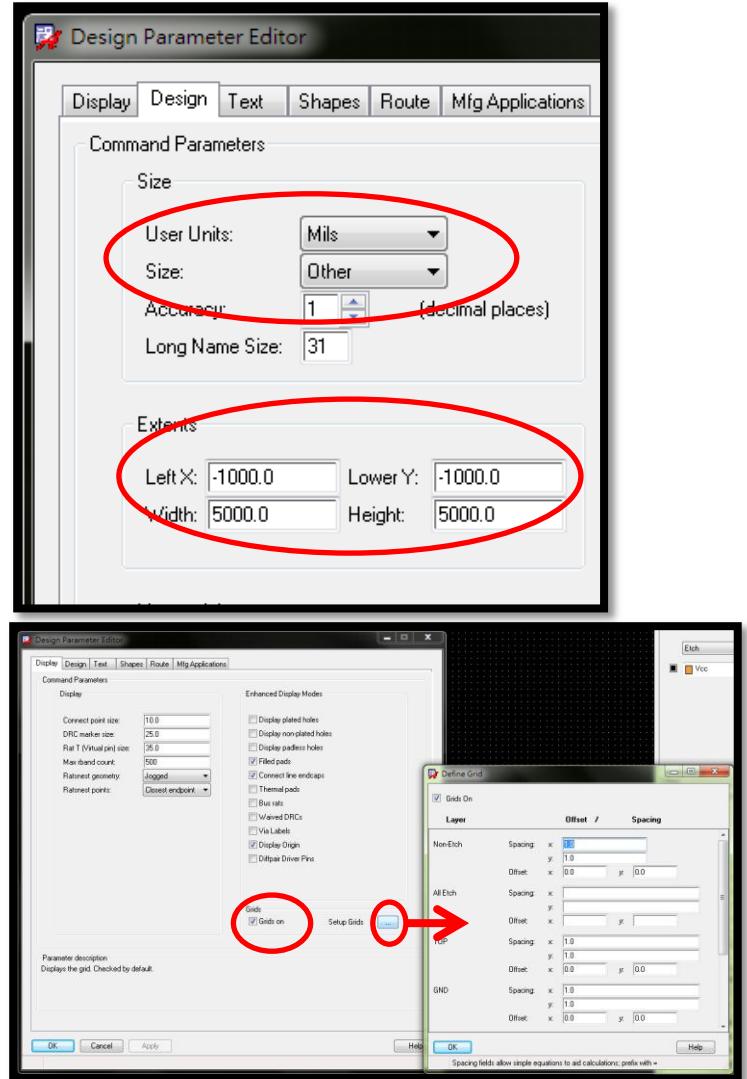


# Three Edit Modes

- General Edit
  - 適合作placement
  - 適合作routing微調
- Etch Edit
  - 適合作routing
- Placement Edit
  - 適合作placement

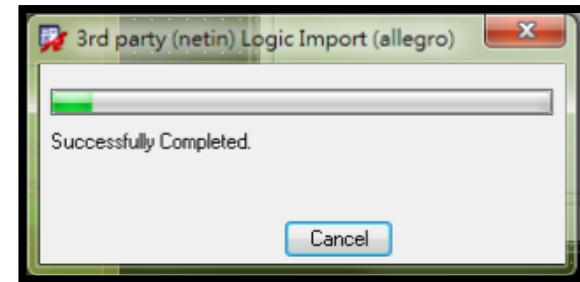
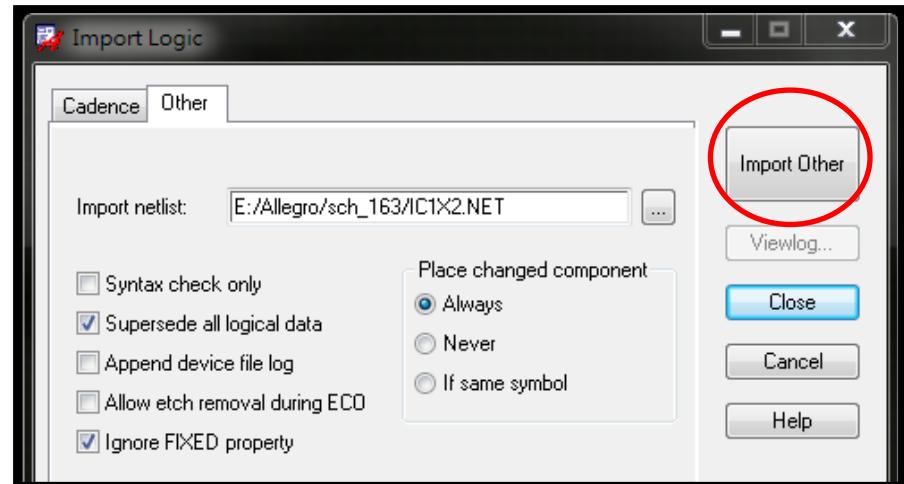
# Setup Design Parameters

- 設定格子點,單位和板子大小
- Setup -> Design Parameters
- 單位固定用Mils, Accuracy 1
- Size : 可選ABCD(D最大)
- Extents為繼續向外伸展
- Grids記得要勾選Grids on, 並設定格子點大小(可隨需要調整)



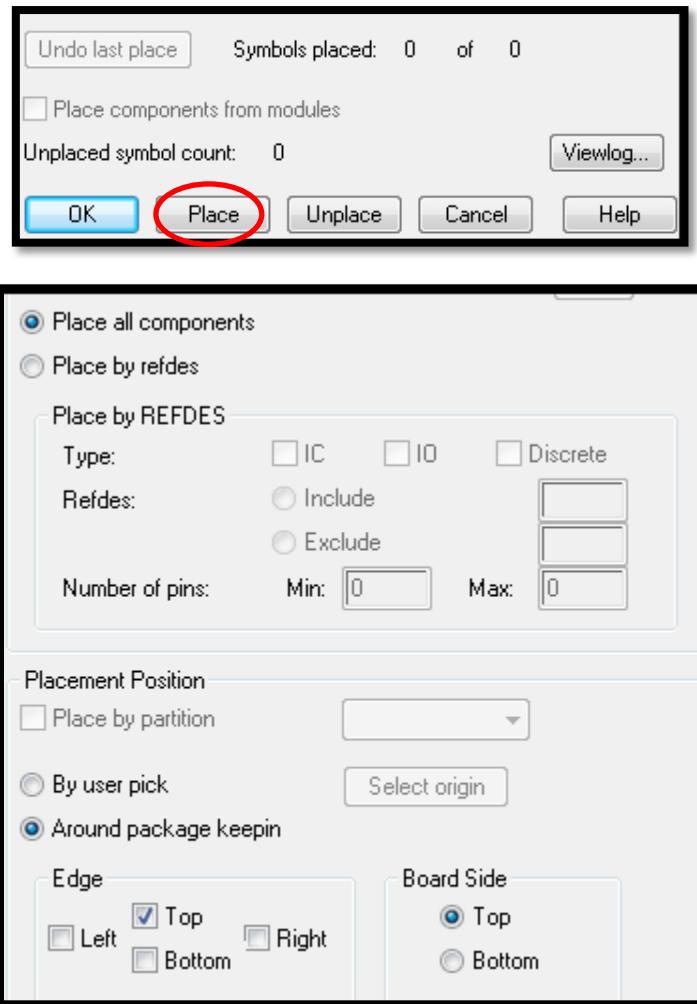
# Import Netlist

- 接著Import做好的.net檔
- File -> Import -> Logic
- 直接打開Other的子頁面
- 照圖上設定
- 檔案選擇你要import的.net
- 最後按Import Other
- 成功會出現上圖的視窗，失敗則會跳出失敗的原因
- 更正後重新Import直到成功
- Import成功後，畫面上還是沒有任何元件 → 正常，不要驚慌



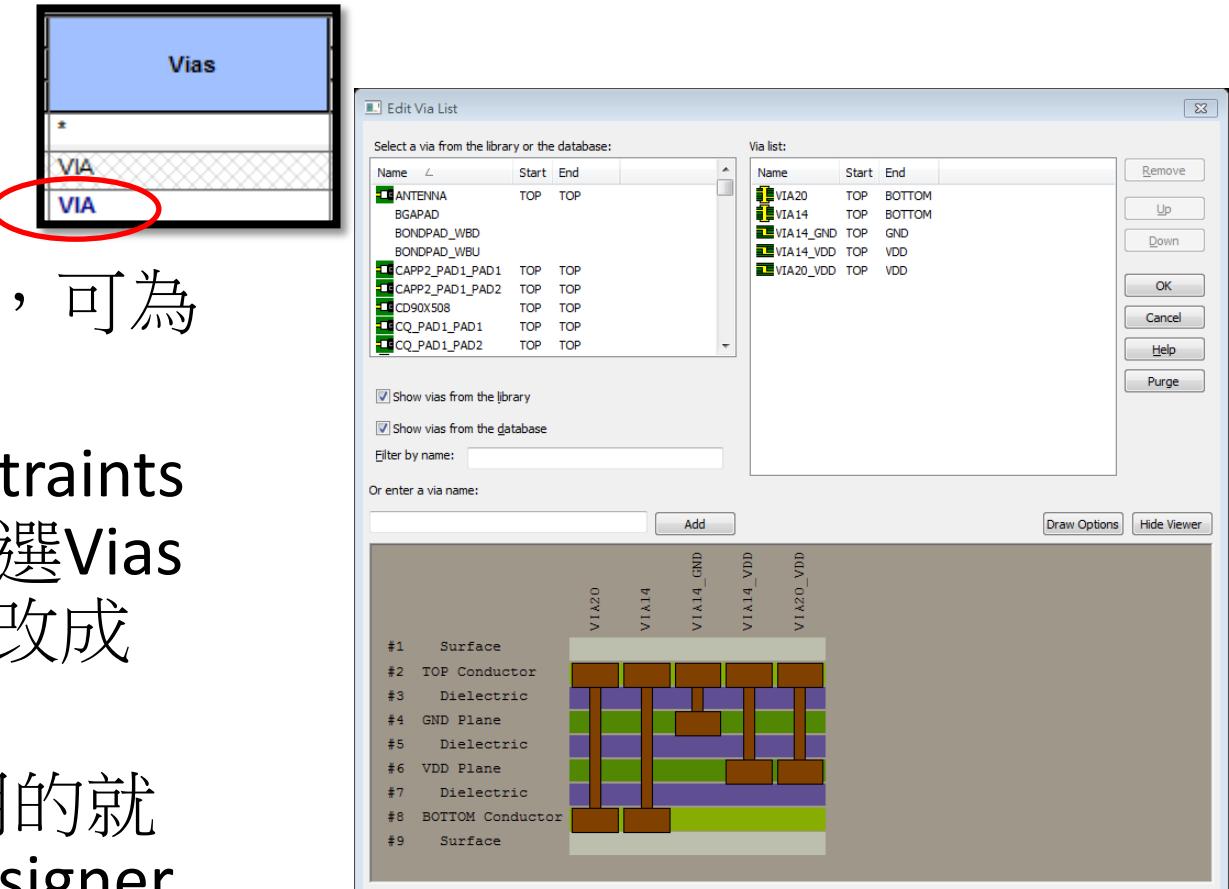
# Quick Place Components

- 接下來要把元件擺到板子上: Place -> Quick Place
- 選擇Place的方式(一開始選Place all components)
- 放在上下左右皆可,並按Place
- 如果有沒放到的元件可能是板子不夠大或定義層沒設好
- 最後按OK



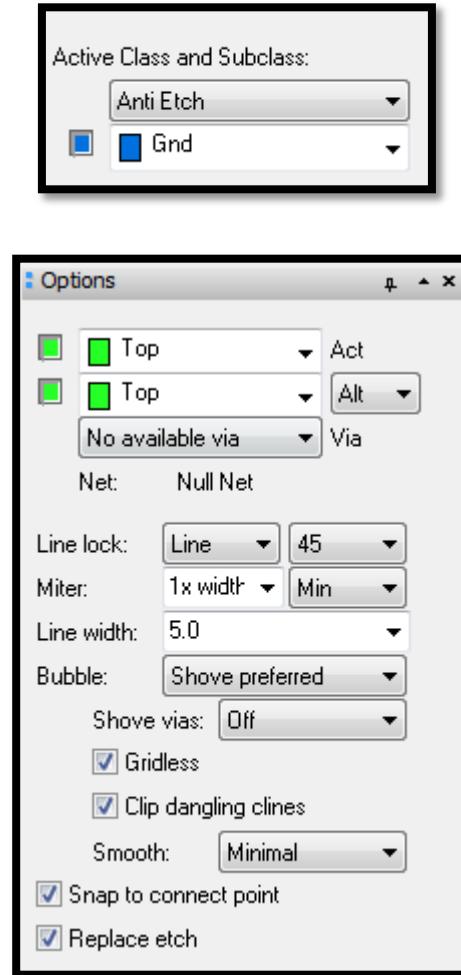
# Specify Via Padstacks

- 從 Constraint Manager 開
- 選取 padstack，可為貫孔或埋孔
- Setup -> Constraints -> Physical 點選 Vias 欄的 via 兩下，改成可用的 via
- 如果沒有可用的就自己從 pad designer 新增



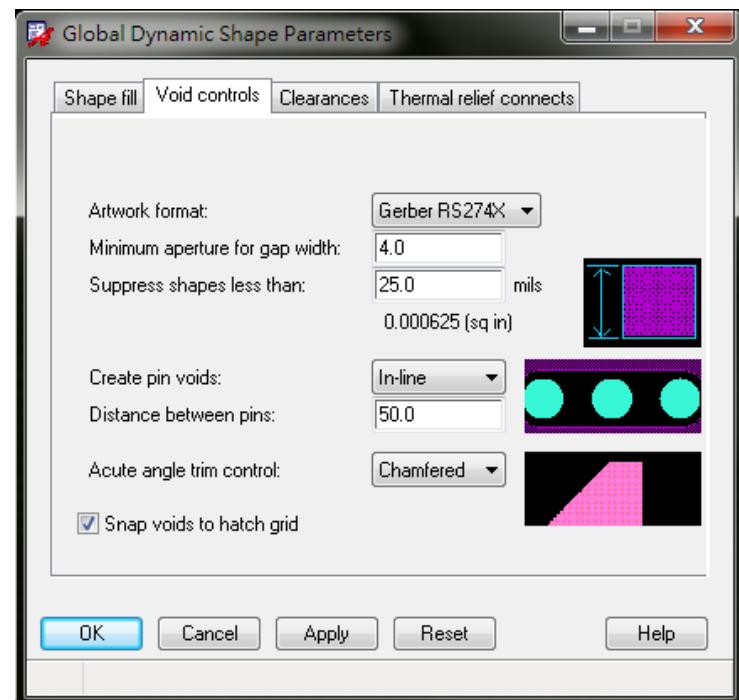
# VIA placement

- 將元件擺放到板子上你想要的位置後
- 開始走線 Route -> Connect 
- 在右邊的Option可以直接釘選起來
- 會根據使用不同的功能做選擇
- 選擇想要走的層以及繞線方法 
- 還有線寬後, 就可以開始拉線了
- Act表示現在要走的layer
- Alt表示等等可能會換到的layer
- 要換層的時候可以按右鍵Add Via



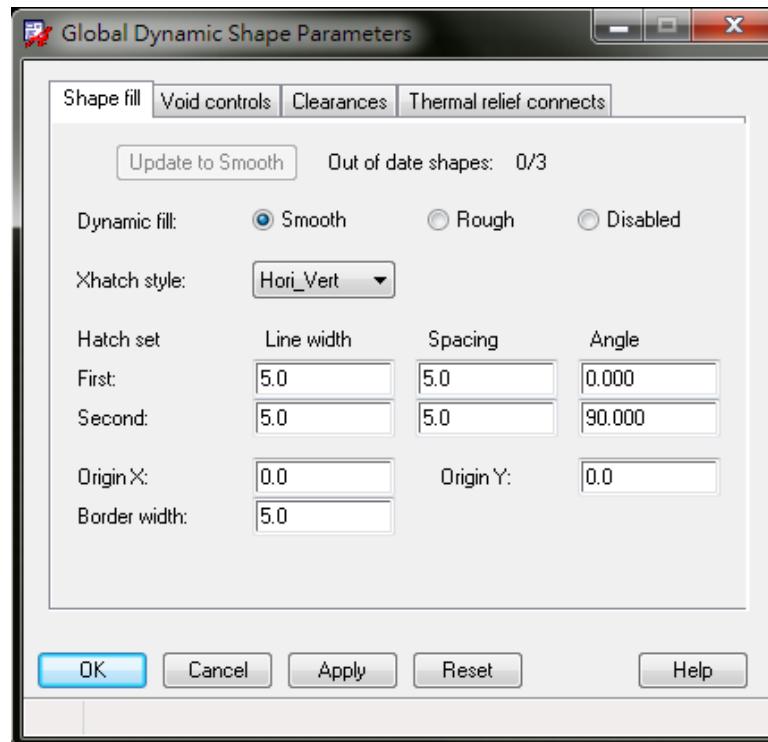
# Dynamic shape 參數

- 新版的Shape有兩種
  - Dynamic copper : 隨著netlist連接的不同，動態調正void位置
  - Static solid : 靜態多邊形
- 注意:並不是對應的層會和net有相同名字
- Net的名字是Capture決定的
- 如果想改名前面有教



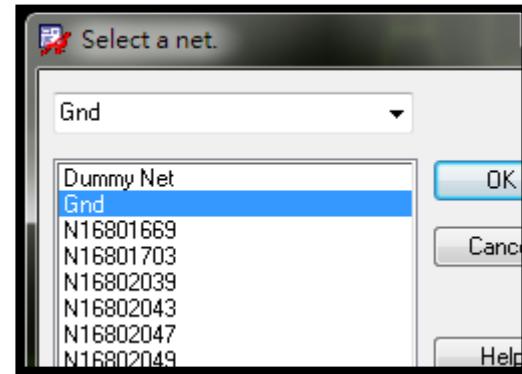
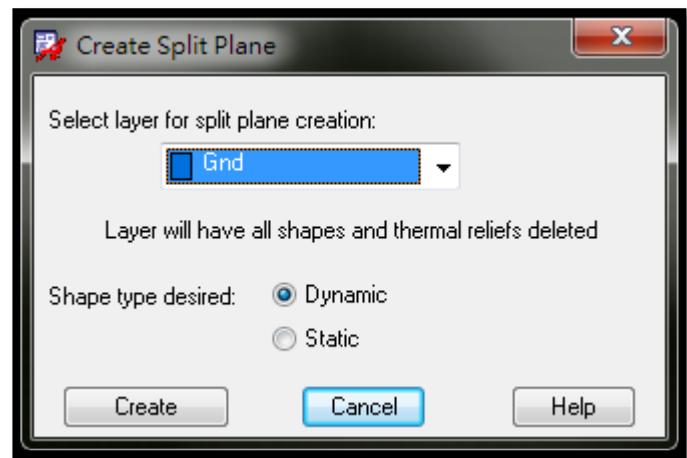
# Dynamic shape

- When DRC rules (constraints) are updated, click “Update to Smooth”



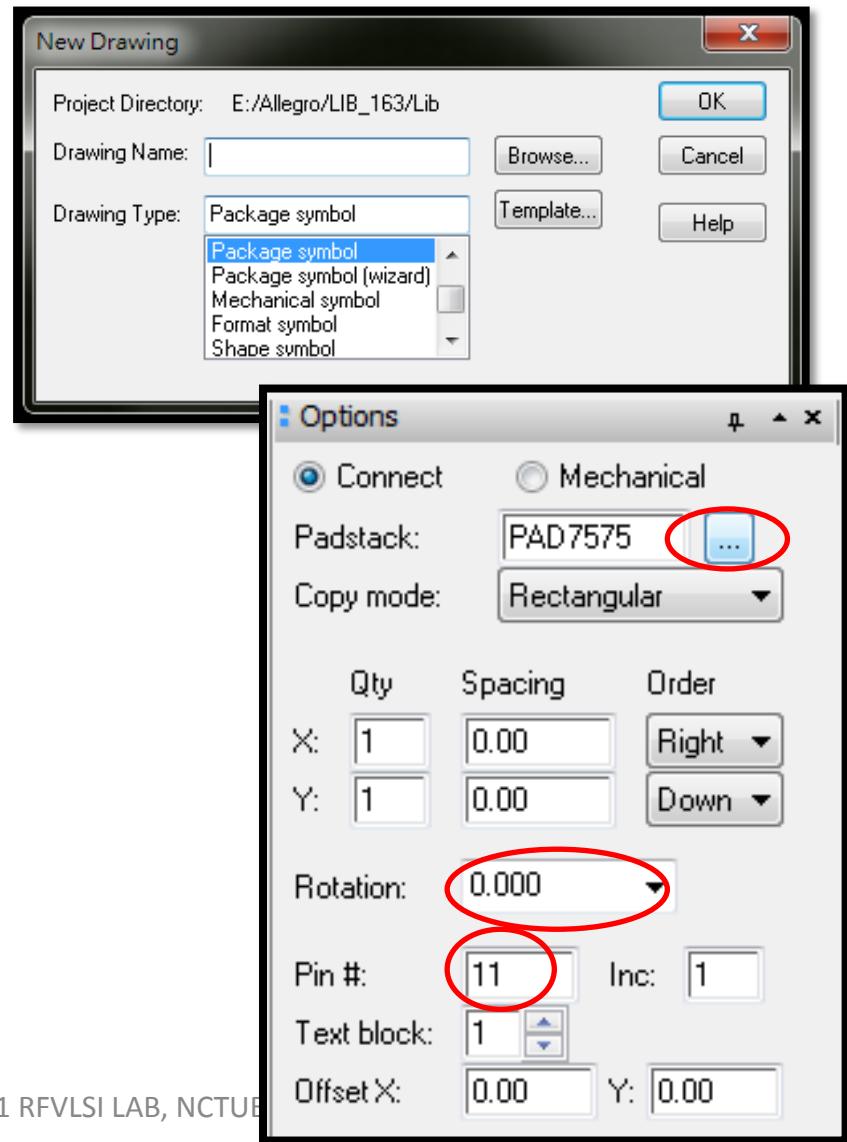
# Split Plane

- 走完線之後，接下來要鋪地平面和VDD平面
- Shape->Global Dynamic Param
- 照上面兩圖設定後按OK
- 接著按Edit -> Split plane -> Create
- 選擇要鋪的layer並選擇Dynamic後按Create
- 接著在Select a net中選擇相對應的net



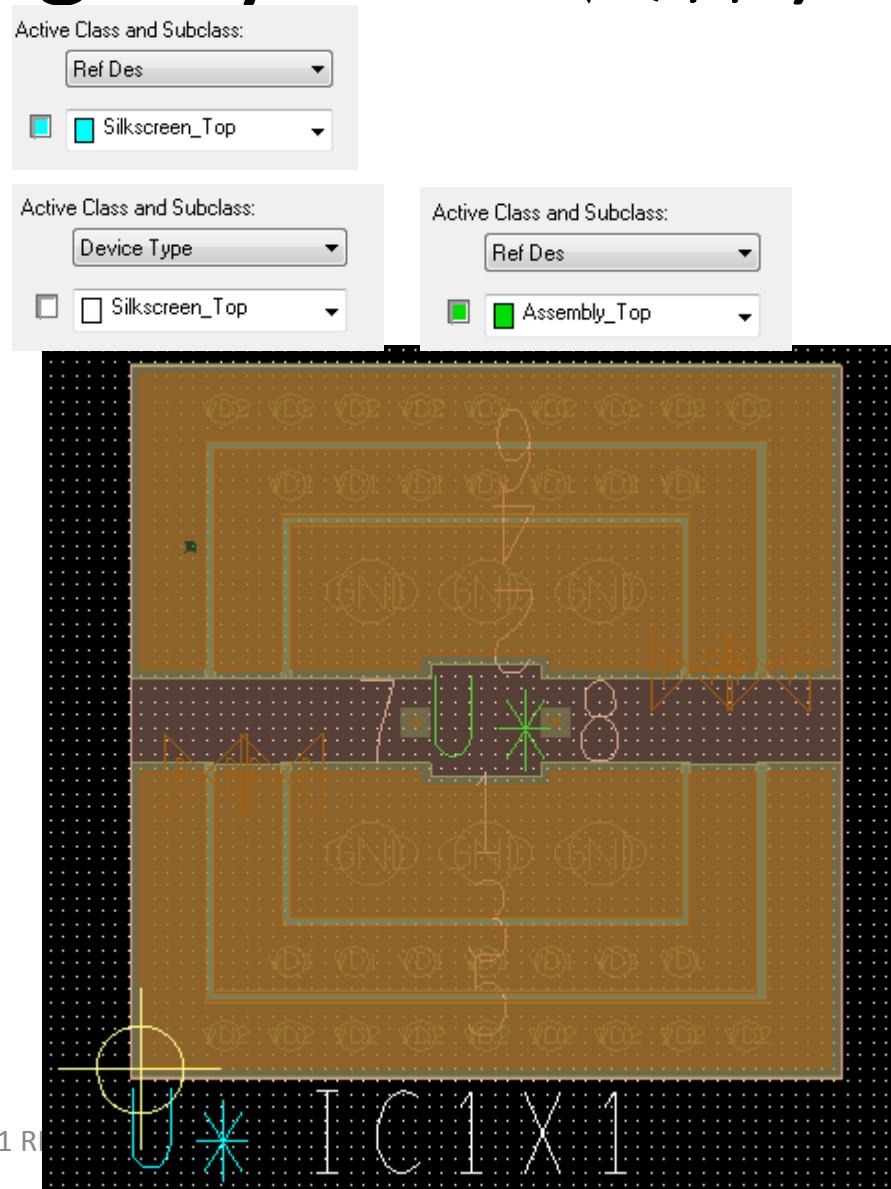
# PCB Editor (Package Symbol 製作)

- File -> New
- 選擇 Package symbol 並輸入檔名
- 按照之前的步驟設定板子層數跟grid
- 接著要把Pin放到Package上
- Layout -> Pins
- 從右邊的option選擇要用的Padstack
- 還有Rotation的角度(選完後再按一次 Layout -> Pins)
- 還有最重要的Pin # (要和capture上的腳位一模一樣)



# PCB Editor (Package Symbol 製作)

- Pin都放好了以後
- 要設定Device Type和Ref Des
- Add -> Text
- 在右邊Option選擇
- Device Type/ Silkscreen\_Top放在整個的下面
- Ref Des/ Assembly\_Top放在中間
- Ref Des/ Silkscreen\_Top放在旁邊
- 選擇Setup -> Areas -> Package Boudarys 後,選矩形 把整個元件包起來(Pin的部分)
- 存檔: File -> Save
- 製作元件: File -> Create Device



# Constraint Manager

- 按按鈕
- 改設定
  - 最小最大線寬
  - 各種間距
  - VIA



Allegro Constraint Manager (connected to Allegro PCB Design GXL 16.3) - [Spacing Constraint Sets: All Layers [DUALBAND\_TX\_v3]]

Type	Objects	Line	Thru Pin	SMD Pin	Test Pin	Thru Via	BB Via	Test Via	Microvia	Shape	Bond Finger	Hole
*	*	*	*	*	*	*	*	*	*	*	*	*
Dsn	DUALBAND_TX_v3	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0
SCS	DEFAULT	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0

Allegro Constraint Manager (connected to Allegro PCB Design GXL 16.3) - [Physical Constraint Sets: All Layers [DUALBAND\_TX\_v3]]

Type	Objects	Line Width		Neck		Differential Pair				Vias
		Min	Max	Min Width	Max Length	Min Line Spac	Primary Gap	Neck Gap	(+)Tolerance	
*	*	*	*	*	*	*	*	*	*	*
Dsn	DUALBAND_TX_v3	3.0	20.0	5.0	0.0	0.0	0.0	0.0	0.0	VIA20:VIA14:VIA14_GND...
PCS	DEFAULT	3.0	20.0	5.0	0.0	0.0	0.0	0.0	0.0	VIA20:VIA14:VIA14_G...

# NCTU IEE 5046

# 高頻電路設計與實驗

## Placement in

## Allegro PCB Editor

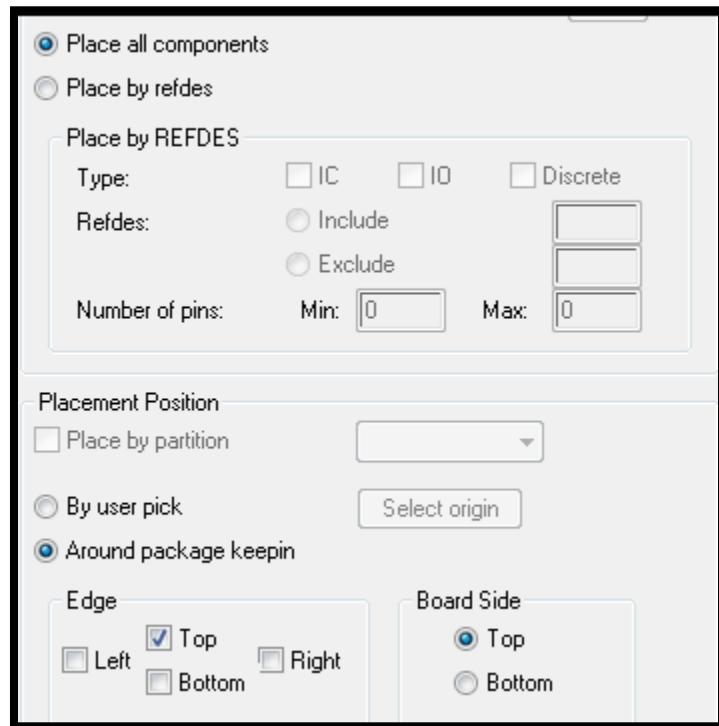
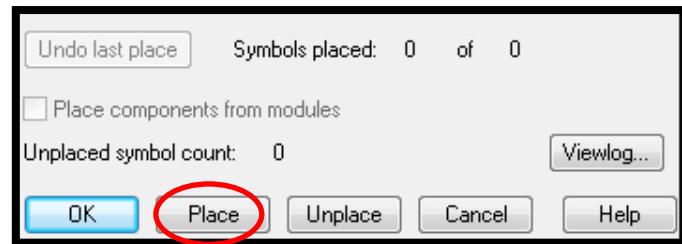
Lecturer: Professor Yu-Jiu Wang

TA: 李道一 [michael@rfvlsi.ee.nctu.edu.tw](mailto:michael@rfvlsi.ee.nctu.edu.tw)

Document coauthor: Jon-Jin Chen

# Quick Place Components

- 接下來要把元件擺到板子上: Place -> Quick Place
- 選擇Place的方式(一開始選Place all components)
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- 最後按OK



# NCTU IEE 5046

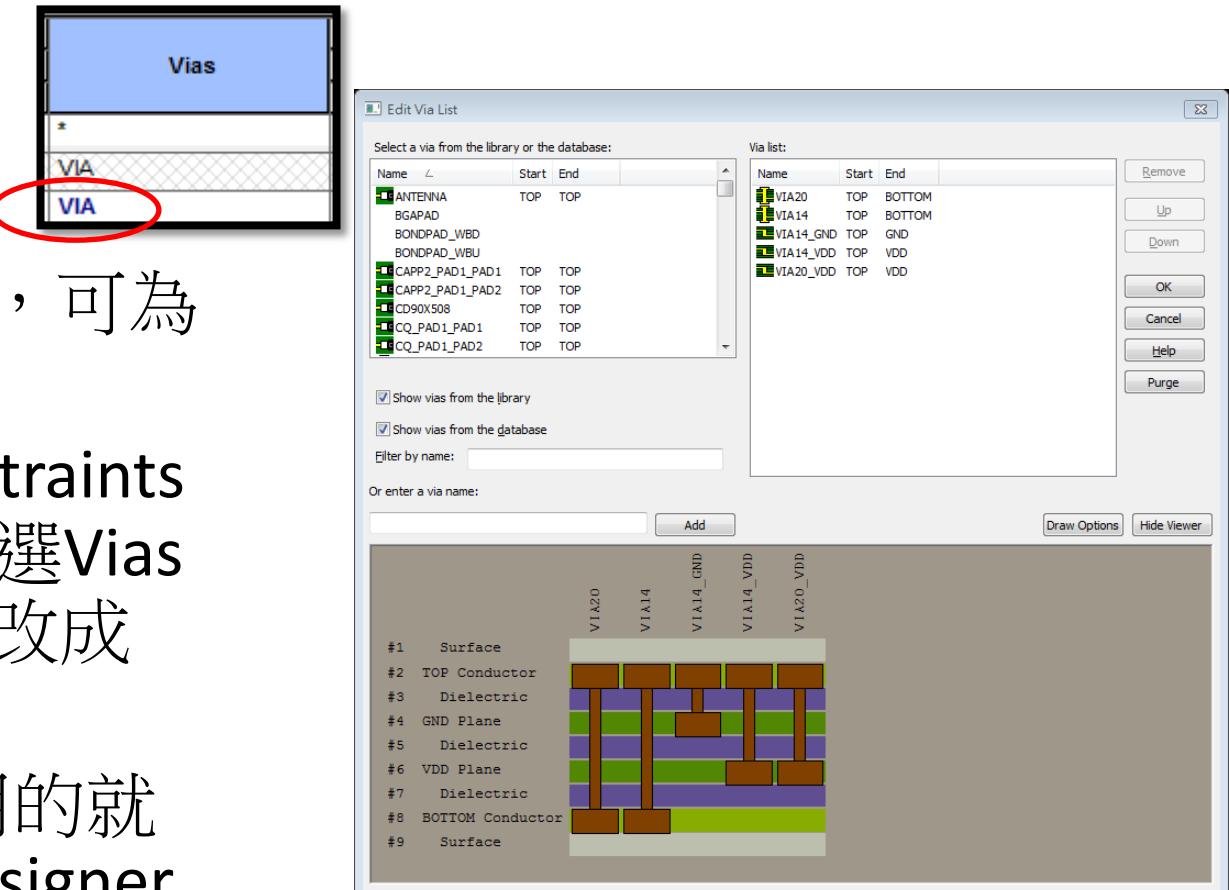
## 高頻電路設計與實驗

### Routing in Allegro PCB Editor

Lecturer: Professor Yu-Jiu Wang  
TA: 李道一 [michael@rfvlsi.ee.nctu.edu.tw](mailto:michael@rfvlsi.ee.nctu.edu.tw)  
Document coauthor: Jon-Jin Chen

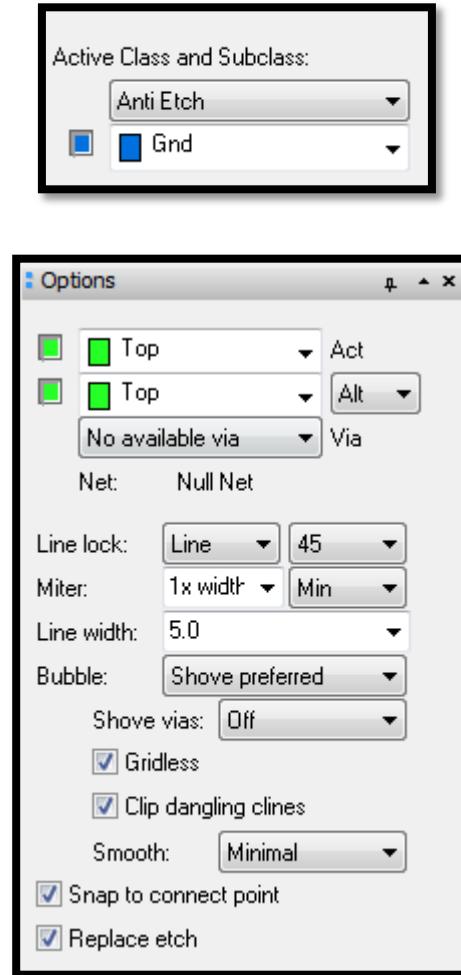
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- 如果沒有可用的就自己從 pad designer 新增



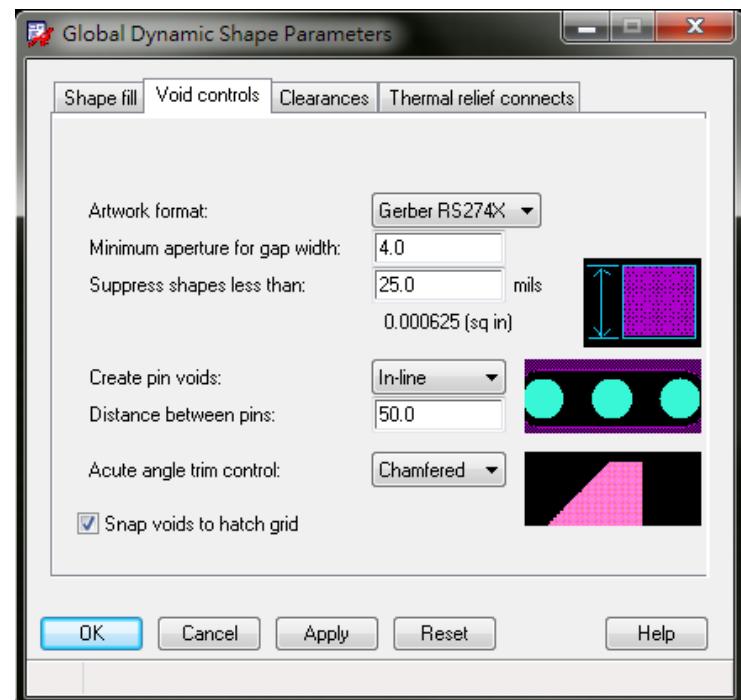
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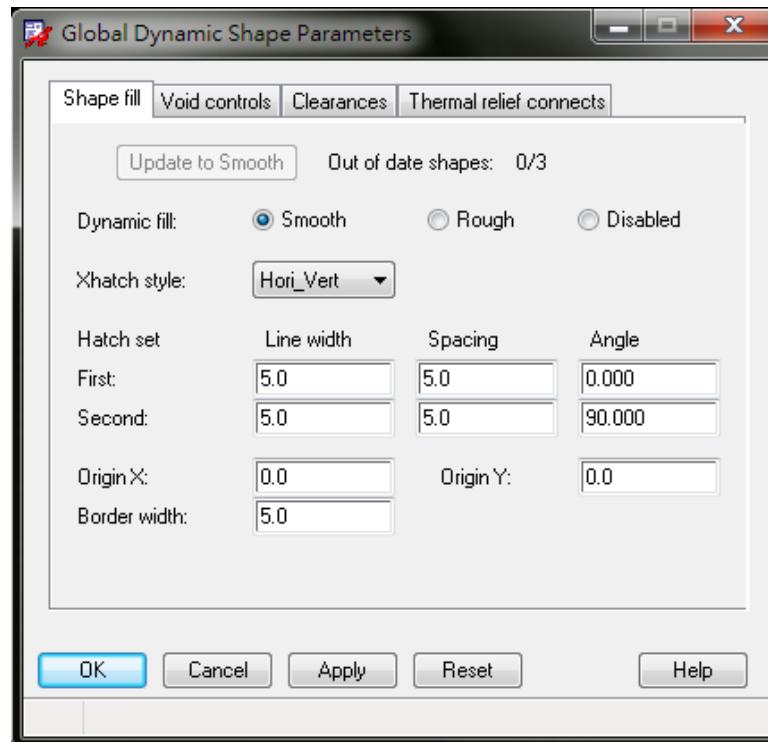
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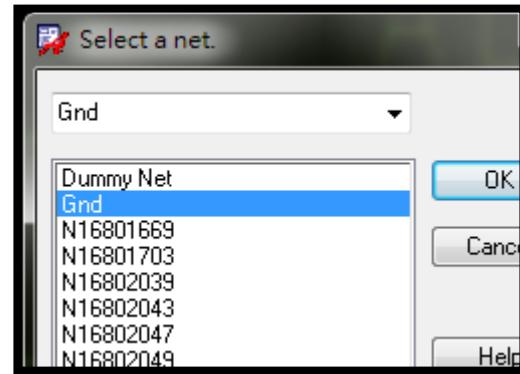
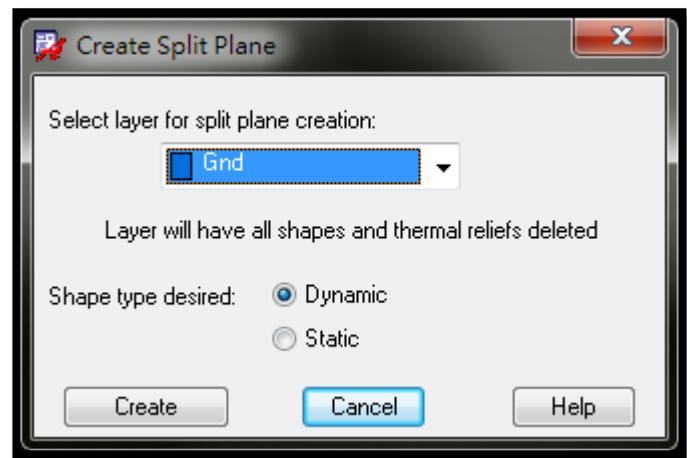
# Dynamic shape

- When DRC rules (constraints) are updated, click “Update to Smooth”



# Split Plane

- 走完線之後，接下來要鋪地平面和VDD平面
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- 照上面兩圖設定後按OK
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- 改設定
  - 最小最大線寬
  - 各種間距
  - VIA



Allegro Constraint Manager (connected to Allegro PCB Design GXL 16.3) - [Spacing Constraint Sets: All Layers [DUALBAND\_TX\_v3]]

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Dsn	DUALBAND_TX_v3	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0	3.0

Allegro Constraint Manager (connected to Allegro PCB Design GXL 16.3) - [Physical Constraint Sets: All Layers [DUALBAND\_TX\_v3]]

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		Min	Max	Min Width	Max Length	Min Line Spac	Primary Gap	Neck Gap	(+)Tolerance	
*	*	*	*	*	*	*	*	*	*	*
Dsn	DUALBAND_TX_v3	3.0	20.0	5.0	0.0	0.0	0.0	0.0	0.0	VIA20:VIA14:VIA14_GND...
PCS	DEFAULT	3.0	20.0	5.0	0.0	0.0	0.0	0.0	0.0	VIA20:VIA14:VIA14_G...

# NCTU IEE 5046

# 高頻電路設計與實驗

# Finalizing PCB Design

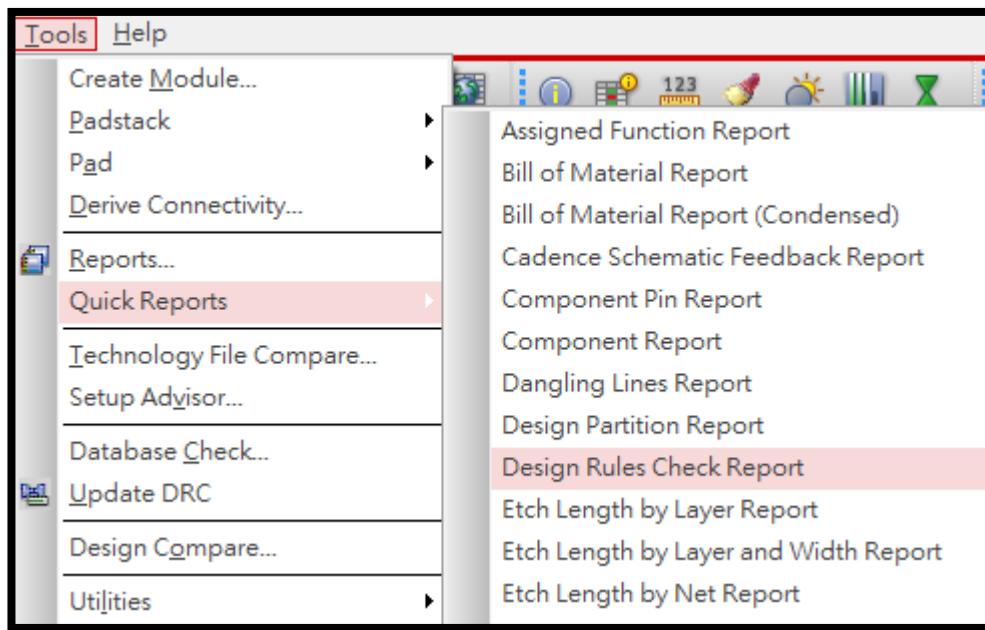
Lecturer: Professor Yu-Jiu Wang

TA: 李道一 [michael@rfvlsi.ee.nctu.edu.tw](mailto:michael@rfvlsi.ee.nctu.edu.tw)

Document coauthor: Jon-Jin Chen

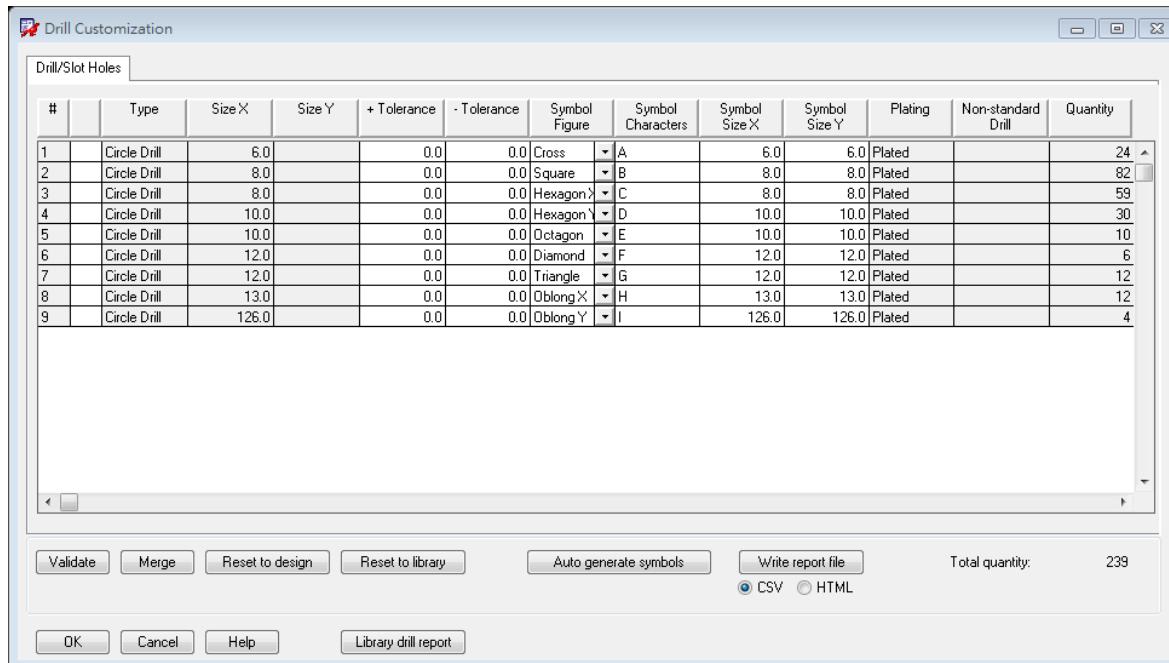
# Design Rule Checking (DRC)

- 按按鈕 
- 看報告
- 做修正



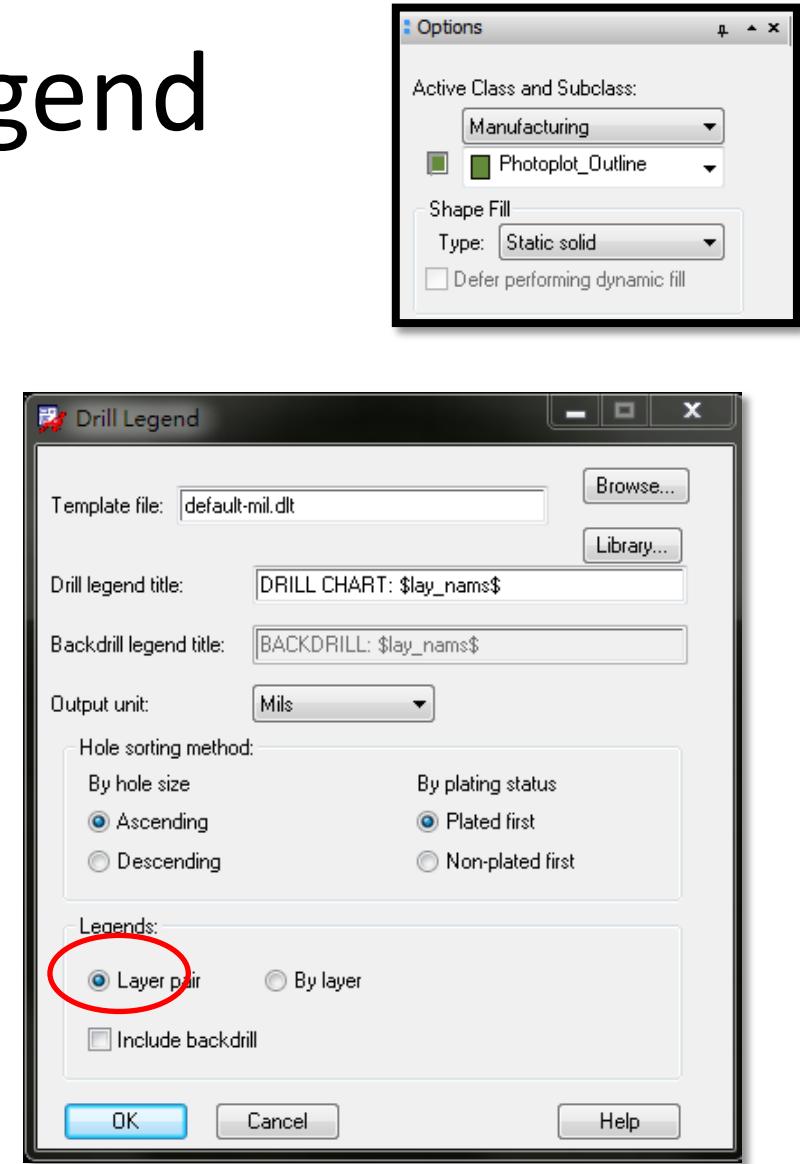
# Drill Legend - Drill Customization

- ***Drill Legend is not required for panelization (併版)***
- 設定鑽孔標記的圖例
- Manufacture -> NC->Drill Customization



# Drill Legend

- 每一層都鋪好後, 應該就不會有淡藍色的細線(有的話要檢查有沒有錯)
- 接下來如果使用的元件有鑽孔, 就要列出鑽孔表
- Manufacture -> NC -> Drill Legend
- OK後把表放到圖上, 如果有很多個表一開始會重疊, 此時先把框框拉開(只有框框,裡面的線不會動),排列成想要的形狀後
- 再重新呼叫Drill Legend, 這時候他就會自己排好了
- 排好以後選擇Add Rectangle, 用Manufacturing的Photoplot\_Outline
- 把板子還有Drill Legend 通通框起來

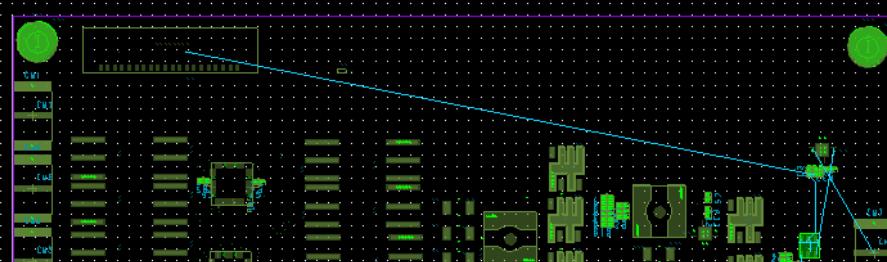


# Drill Legend - \*.dlt 設定檔範本

- 預設放在  
C:\Cadence\SPB\_16.3\share\pcb\text\nclegend
- 可以把裡面的dlt檔複製，然後用文字編輯器修改
- 若要併版，則不需要在個別的PCB加入Drill Legend

# Drill Legend

Photoplot Outline ↑



Drill Legend

BY LAYER: VDD to BOTTOM			
FIGURE	ALL UNITS ARE IN MILS	PLATED	QTY
.	8.0	PLATED	10
.	8.0	PLATED	44
.	12.0	PLATED	6
①	126.0	PLATED	4

BY LAYER: TOP to GND			
FIGURE	ALL UNITS ARE IN MILS	PLATED	QTY
.	6.0	PLATED	24
.	8.0	PLATED	72
.	8.0	PLATED	59
.	10.0	PLATED	30
.	10.0	PLATED	30
.	12.0	PLATED	6
.	12.0	PLATED	32
.	13.0	PLATED	32
①	126.0	PLATED	4

# Gerber RS-274X Artwork

- The file format used by PCB industry software to describe the images of a printed circuit board (copper layers, solder mask, legend, drill holes, etc.).
- The de-facto industry standard for printed circuit board image transfer

```
G04 Film Name: paste_top* G04 Origin Date:  
Thu Sep 20 15:54:22 2007* G04 Layer:  
PIN/PASTEMASK_TOP* %FSLAX55Y55*MOIN*%  
%IR0*IPPOS*OFA0.00000B0.00000*MIA0B0*SFA1.00  
000B1.00000*%  
%ADD28R,.11X.043*% %ADD390,.07X.022*%  
...  
%AMMACRO19* 21,1,.0512,.0512,0.0,0.0,45.*%  
%ADD19MACRO19*%  
%LPD*%
```

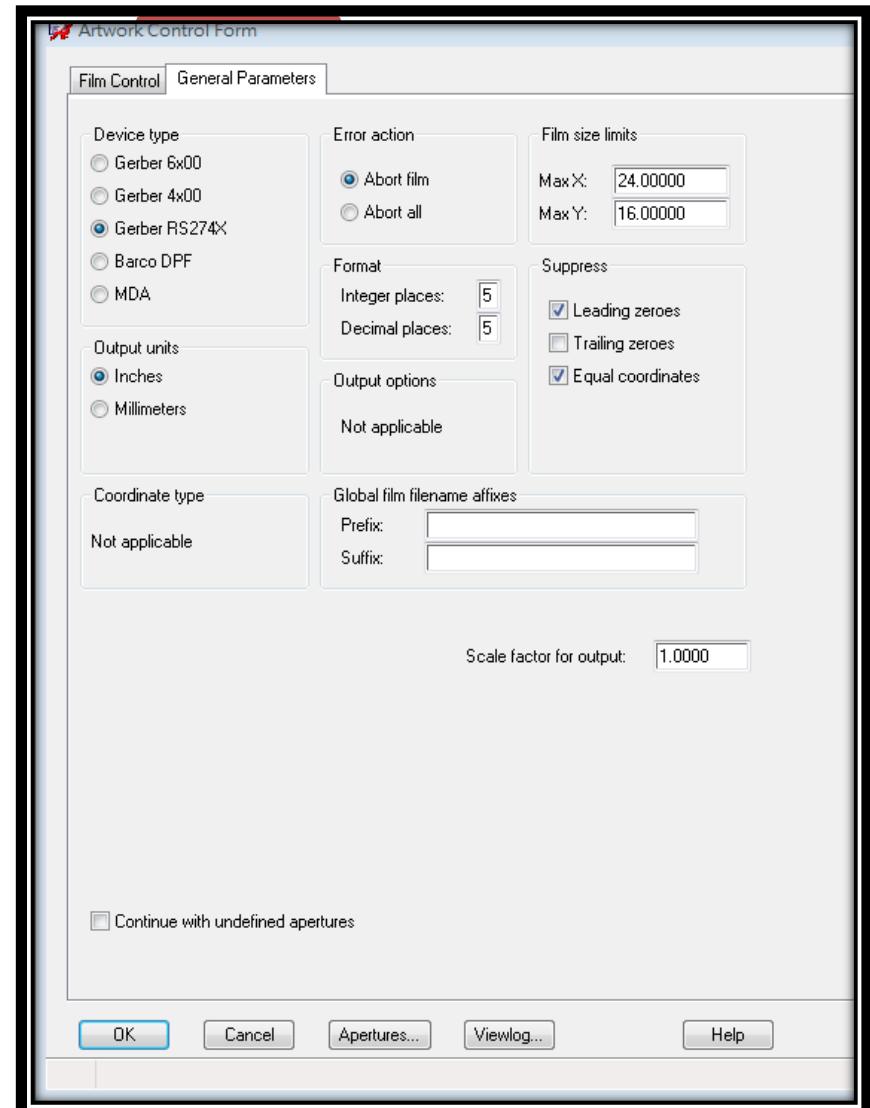
# Gerber RS-274X Artwork

- For double sided PCB, following Gerber files are usually submitted to fabrication company
  - Top Copper Etching
  - Bottom Copper Etching
  - Top Soldermask
  - Bottom Soldermask(optional)
  - Top Silkscreen
  - Bottom Silkscreen
- If you are designing paste stencil, following Geber files are needed
  - Top Pastemask
  - Bottom Pastemask

# Artwork(底片)產生

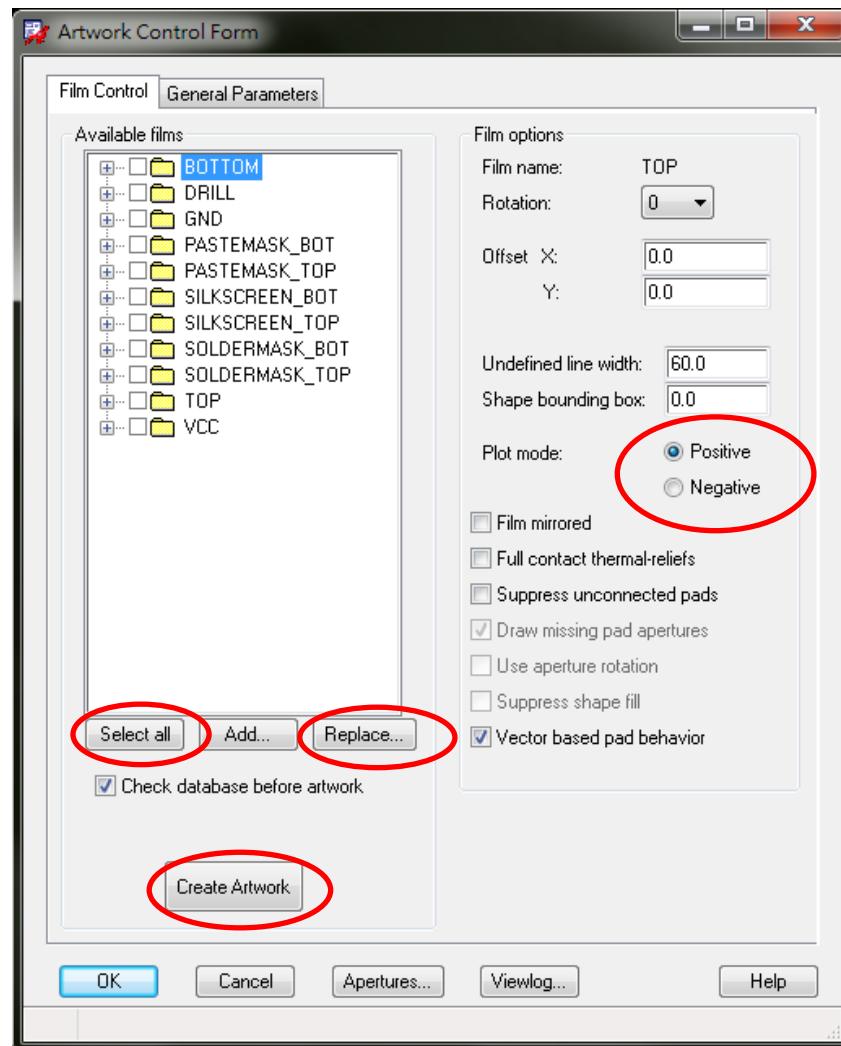


- 按按鈕
- 設定精確度，要比 design 的小數位數多一位。
- 選擇 GERBER 274X 格式



# Artwork(底片)產生(cont'd)

- 最後要輸出成Artwork
- Manufacture -> Artwork
- 預設只有板子所以先按Replace
- 每一層Layer需要和cross section 設定成一樣正片或負片
- 選擇FILM\_SETUP.txt (內容如下)
- 接著選Select all再選Create Artwork並按OK
- 就完成了



# FILM\_SETUP.txt

```
(axlfcreate "SILKSCREEN_BOT" '(0 0 0 30 0 1 0 0 0 1 0 0 1) '("REF  
DES/SILKSCREEN_BOTTOM" "PACKAGE GEOMETRY/SILKSCREEN_BOTTOM"  
"MANUFACTURING/PHOTOPILOT_OUTLINE" "BOARD GEOMETRY/OUTLINE" "BOARD  
GEOMETRY/SILKSCREEN_BOTTOM" ))  
(axlfcreate "PASTEMASK_BOT" '(0 0 0 30 0 1 0 0 0 1 0 0 1)  
'("PIN/PASTEMASK_BOTTOM" "MANUFACTURING/PHOTOPILOT_OUTLINE" "BOARD  
GEOMETRY/OUTLINE" ))  
(axlfcreate "VCC" '(0 0 0 30 0 0 0 1 0 1 0 0 1)  
'("MANUFACTURING/PHOTOPILOT_OUTLINE" "BOARD GEOMETRY/OUTLINE" ))  
(axlfcreate "SOLDERMASK_TOP" '(0 0 0 30 0 1 0 0 0 1 0 0 1) '("VIA  
CLASS/SOLDERMASK_TOP" "PIN/SOLDERMASK_TOP" "PACKAGE GEOMETRY/SOLDERMASK_TOP"  
"MANUFACTURING/PHOTOPILOT_OUTLINE" "BOARD GEOMETRY/OUTLINE" "BOARD  
GEOMETRY/SOLDERMASK_TOP" ))  
(axlfcreate "SOLDERMASK_BOT" '(0 0 0 30 0 1 0 0 0 1 0 0 1) '("VIA  
CLASS/SOLDERMASK_BOTTOM" "PIN/SOLDERMASK_BOTTOM" "PACKAGE  
GEOMETRY/SOLDERMASK_BOTTOM" "MANUFACTURING/PHOTOPILOT_OUTLINE" "BOARD  
GEOMETRY/OUTLINE" "BOARD GEOMETRY/SOLDERMASK_BOTTOM" ))  
(axlfcreate "SILKSCREEN_TOP" '(0 0 0 30 0 1 0 0 0 1 0 0 1) '("REF  
DES/SILKSCREEN_TOP" "PACKAGE GEOMETRY/SILKSCREEN_TOP"  
"MANUFACTURING/PHOTOPILOT_OUTLINE" "BOARD GEOMETRY/OUTLINE" "BOARD  
GEOMETRY/SILKSCREEN_TOP" ))
```

# FILM\_SETUP.txt

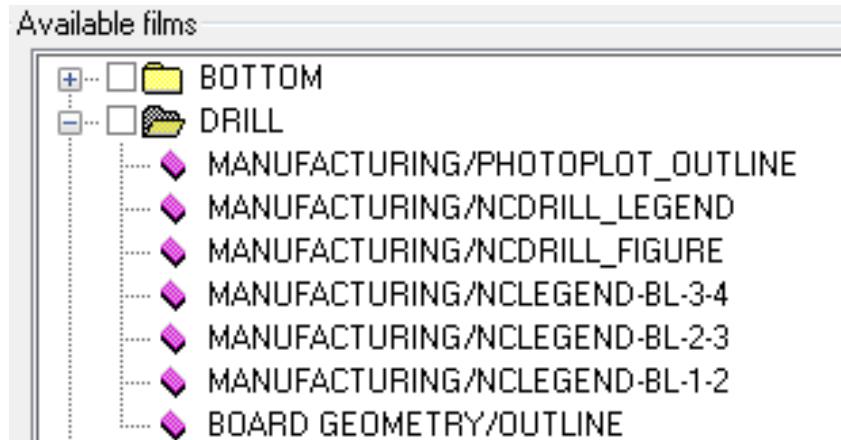
```
(axlfcreate "PASTEMASK_TOP" '(0 0 0 30 0 1 0 0 0 1 0 0 1)
' ("PIN/PASTEMASK_TOP" "MANUFACTURING/PHOTOPLOT_OUTLINE" "BOARD
GEOMETRY/OUTLINE" ))
(axlfcreate "GND" '(0 0 0 3 0 0 0 1 0 1 0 0 1) ' ("ANTIETCH/GND" "VIA
CLASS/GND" "PIN/GND" "MANUFACTURING/PHOTOPLOT_OUTLINE" "ETCH/GND" "BOARD
GEOMETRY/OUTLINE" ))
(axlfcreate "DRILL" '(0 0 0 1 0 0 1 0 0 0 1 0 0 1)
' ("MANUFACTURING/NCLEGEND-BL-3-4" "MANUFACTURING/NCLEGEND-BL-2-3"
"MANUFACTURING/NCLEGEND-BL-1-2" "MANUFACTURING/PHOTOPLOT_OUTLINE"
"MANUFACTURING/NCDRILL_LEGEND" "MANUFACTURING/NCDRILL_PICTURE" "BOARD
GEOMETRY/OUTLINE" ))
(axlfcreate "BOTTOM" '(0 0 0 30 0 1 0 0 0 1 0 0 1) ' ("VIA CLASS/BOTTOM"
"PIN/BOTTOM" "MANUFACTURING/PHOTOPLOT_OUTLINE" "ETCH/BOTTOM" "BOARD
GEOMETRY/OUTLINE" ))
(axlfcreate "TOP" '(0 0 0 30 0 1 0 0 0 1 0 0 1) ' ("VIA CLASS/TOP"
"PIN/TOP" "MANUFACTURING/PHOTOPLOT_OUTLINE" "ETCH/TOP" "BOARD
GEOMETRY/OUTLINE" ))
(axlfcreate "VDD" '(0 0 0 0 30 0 0 0 0 0 0 1 1) ' ("ETCH/VDD" "PIN/VDD"
"VIA CLASS/VDD" ))
```

# FILM\_SETUP每個欄位的意義

```
Field 1 = ROTATION
Field 2 = OFFSET X
Field 3 = OFFSET Y
Field 4 = UNDEFINED LINE WIDTH (e.g. 30=30mil)
Field 5 = SHAPE BOUNDING BOX
Field 6 = PLOT MODE
Field 7 = MIRRORED
Field 8 = FULL CONTACT THERMAL RELIEFS
Field 9 = SUPPRESS UNCONNECTED PADS
Field 10= DRAW MISSING APERTURES
Field 11= USE APERTURE ROTATION
Field 12= FILL OUTSIDE SHAPES
Field 13= VECTOR BASED PAD BEHAVIOR
ROTATION 0 = 0 DEG 2 = 90 DEG 4 = 180 DEG 6 = 270 DEG
OFFSET X OFFSET Y UNDEFINED LINE WIDTH
SHAPE BOUNDING BOX PLOT MODE 1 = POS 0 = NEG
MIRRORED 1= YES ( CHECKED ) 2 = NO
```

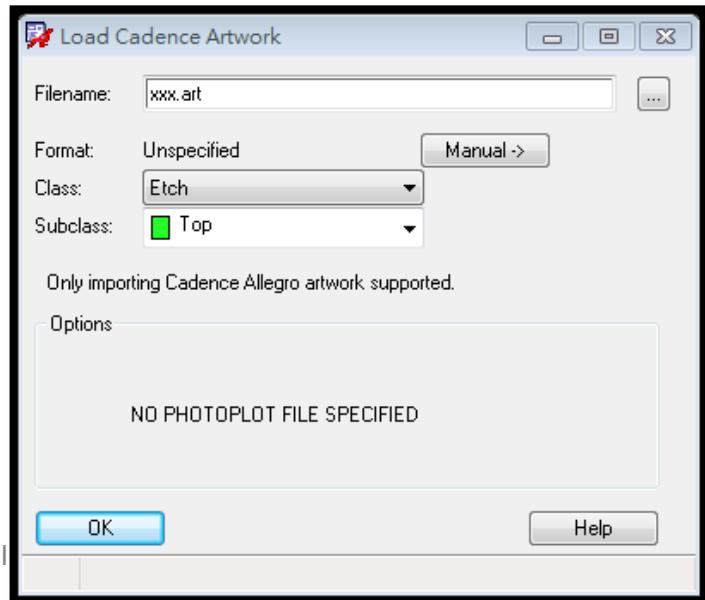
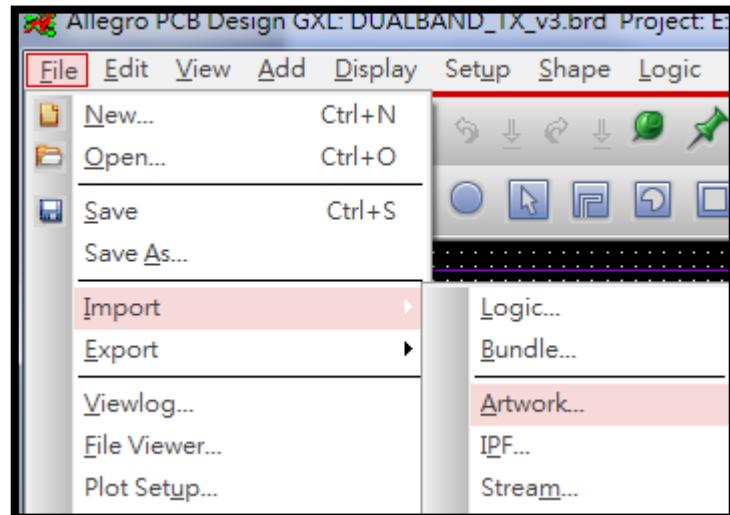
# Artwork中的Drill層

- MANUFACTURING/  
NCLEGEND-BL-1-2
- MANUFACTURING/  
NCLEGEND-BL-2-3
- MANUFACTURING/  
NCLEGEND-BL-3-4
- 不同層的Drill  
Legend都要出現這樣用CAM軟體才看的到



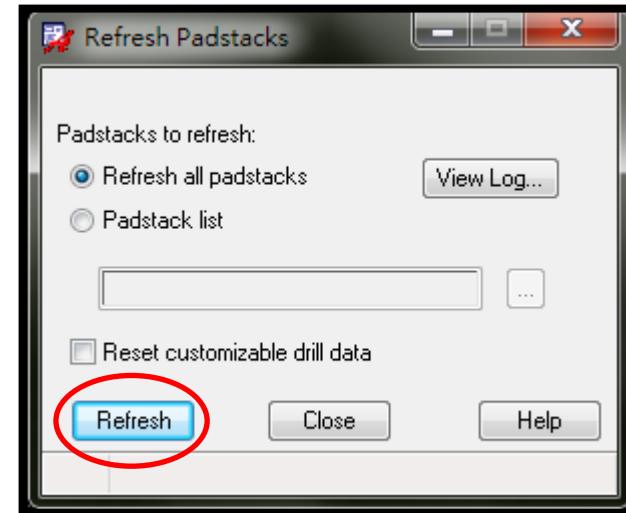
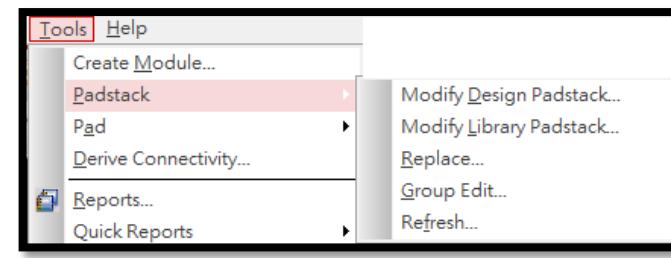
# 檢查底片

- Import Artwork
- 用CAM軟體去開 artwork



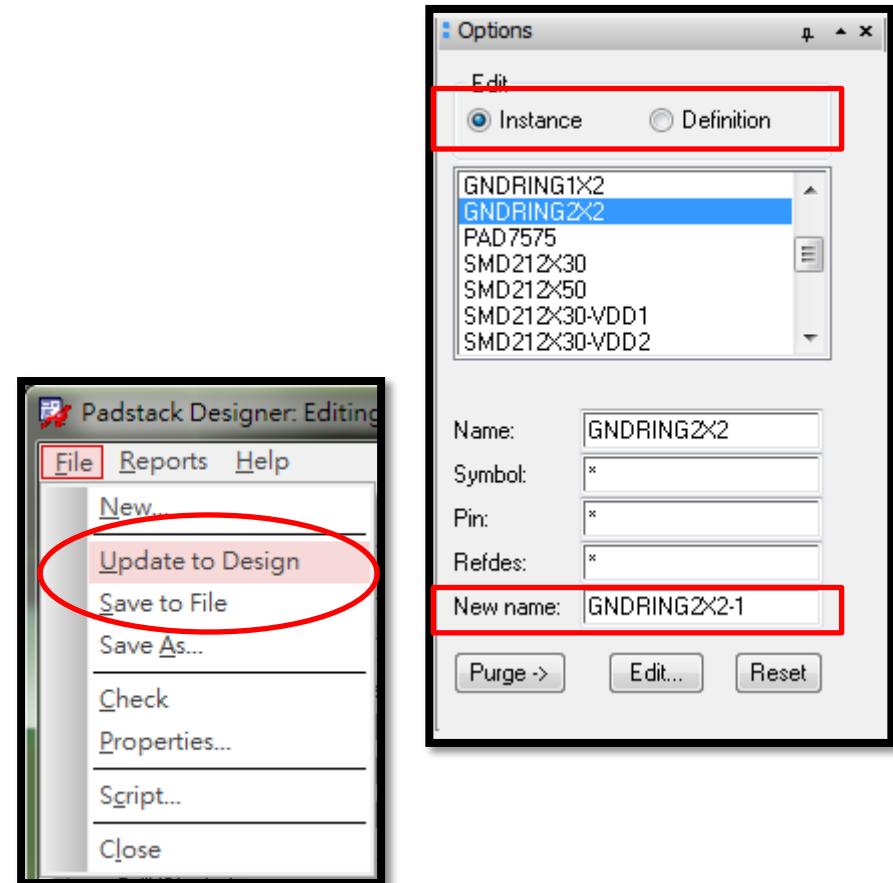
# 想修改Padstack怎麼辦？

- 在Tools -> Padstack底下有許多選項可以使用
- 如果在Pad Designer更改後想要更新可選擇Refresh後,選擇Refresh all padstacks然後按Refresh就會更新囉~



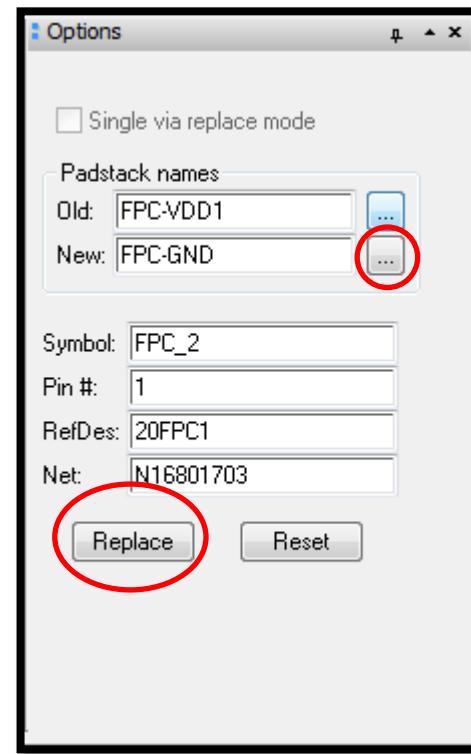
# Modify Design Padstack

- 可以更改板子上曾經用過的Pad
- 直接在Option的列表中點兩下就可以開始更改了~
- 如果選Instance就要另存成另外一個新的Pad
- 選Definition則是可以直接更改原本的檔案
- 改好之後再Pad Designer 選擇
- File -> Update to Design就可以看到更改的結果
- 另外也要Save to File
- Modify Library Padstack
- 和Modify Design Padstack類似
- 只是可以更改所有的Padstack



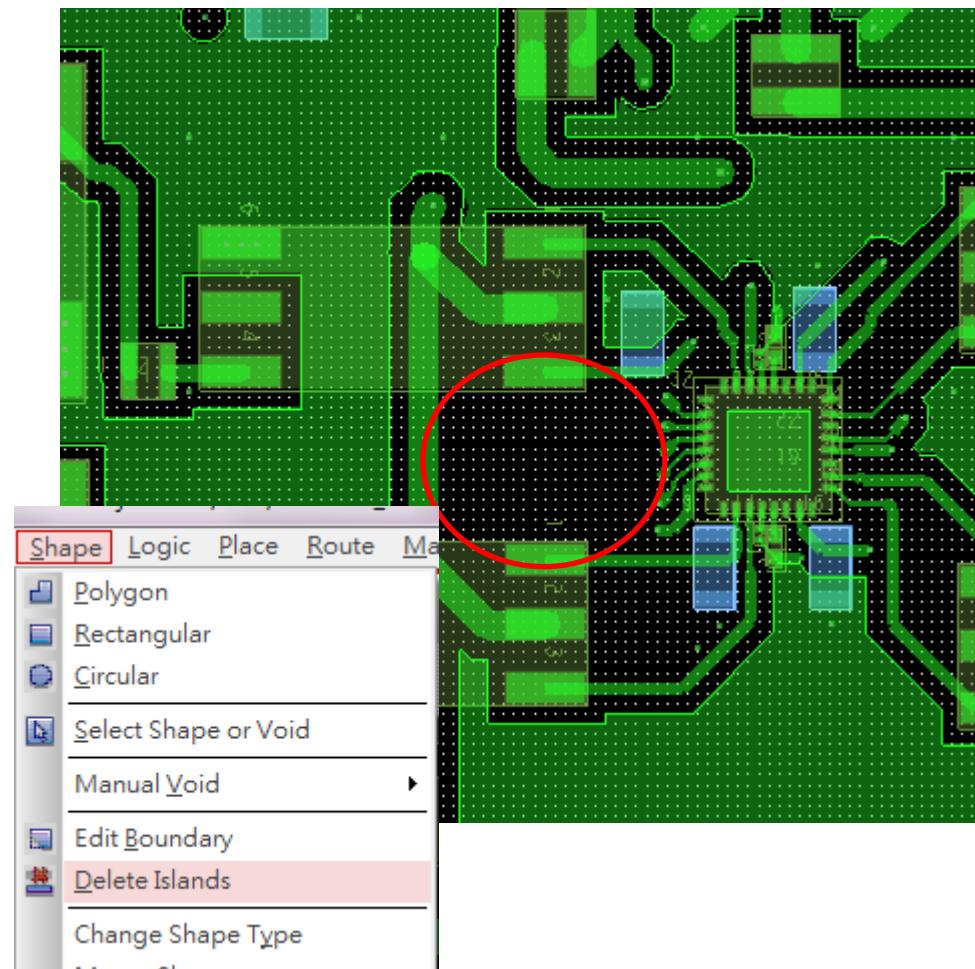
# Padstack Replace

- 可以取代板子上的Pad成其他Pad
- 除了New:的欄位以外
- 其他的欄位可以直接點選想要取代的Pad的位置
- 就會自動填入該有的值了
- 都點選好後再New的欄位選擇想要取代成的Pad
- 最後按Replace就完成了~



# Island removal

- 紅圈區為自動split plane後island產生的地方
- 利用“Delete Islands”將全部island刪除
- 或像紅圈上方處利用VIA確保island grounded



# Note

- 從另外板子的外圍要放20mil的AntiEtch。避免板子邊緣的導體外露，造成ESD
- 可直接用Add -> Rectangle
  - Subclass選擇要畫的layer(有鋪整層的都要畫)
  - 或選取All
- 建議全部使用英制單位
- GND和VDD之間要加上若干bypass capacitors
- 不同層的GND要打上若干個via或air bridge以確保GND shape的電位均勻