



## Isolated 5V RS-485 Transceiver With Integrated Transformer Driver

Check for Samples: [ISO3086T](#)

### FEATURES

- 3000 V<sub>RMS</sub> / 4242 V<sub>PK</sub> Isolation
- Bus-Pin ESD Protection
  - 11 kV HBM Between Bus-Pins and GND2
  - 6 kV HBM Between Bus-Pins and GND1
- 1/8 Unit Load – Up to 256 Nodes on a Bus
- Designed for RS-485 and RS-422 Applications
- Signaling Rates up to 20 Mbps
- Thermal Shutdown Protection
- Typical Efficiency > 60% (I<sub>LOAD</sub> = 100 mA) - see [SLUU469](#)
- Low Bus Capacitance 7 pF (Typ)
- 50 kV/μs Typical Transient Immunity
- UL 1577, IEC 60747-5-2 (VDE 0884, Rev. 2) Approvals Pending
- Fail-safe Receiver for Bus Open, Short, Idle
- Logic Inputs are 5-V Tolerant

### APPLICATIONS

- Isolated RS-485/RS-422 Interfaces
- Factory Automation
- Motor/Motion Control
- HVAC and Building Automation Networks
- Networked Security Stations

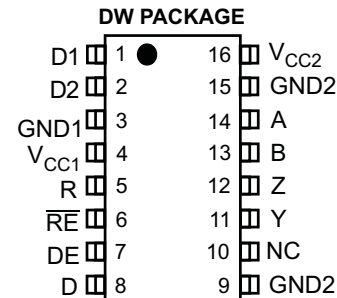
### DESCRIPTION

The ISO3086T is an isolated differential line transceiver with integrated oscillator outputs that provide the primary voltage for an isolation transformer. The device is a full-duplex differential line transceiver for RS-485 and RS-422 applications that can easily be configured for half-duplex operation by connecting pin 11 to pin 14, and pin 12 to pin 13.

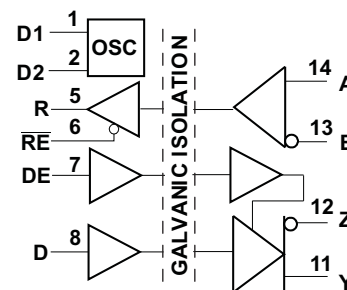
These devices are ideal for long transmission lines since the ground loop is broken to allow for a much larger common-mode voltage range. The symmetrical isolation barrier of the device is tested to provide 3000 V<sub>RMS</sub> or 4242 V<sub>PK</sub> of isolation for 1 minute per VDE between the bus-line transceiver and the logic-level interface.

Any cabled I/O can be subjected to electrical noise transients from various sources. These noise transients can cause damage to the transceiver and/or near-by sensitive circuitry if they are of sufficient magnitude and duration. These isolated devices can significantly increase protection and reduce the risk of damage to expensive control circuits.

The ISO3086T is specified for use from –40°C to 85°C.



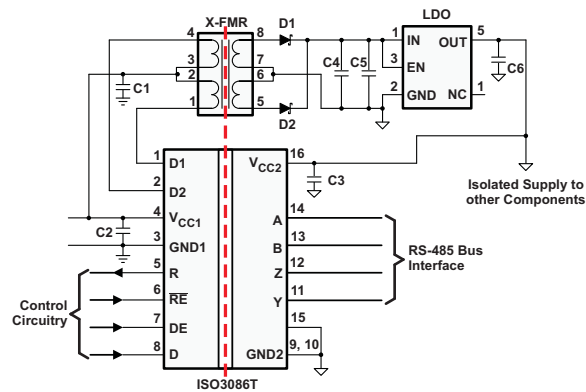
### FUNCTION DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



**Figure 1. Typical Application Circuit (For Details See [SLUU469](#))**

## PIN DESCRIPTIONS

NAME	PIN No.	FUNCTION
D1	1	Transformer Driver Terminal 1, Open Drain Output
D2	2	Transformer Driver Terminal 2, Open Drain Output
GND1	3	Logic-side Ground
V <sub>CC1</sub>	4	Logic-side Power Supply
R	5	Receiver Output
$\overline{R}$	6	Receiver Enable Input. This pin has complementary logic.
DE	7	Driver Enable Input
D	8	Driver Input
GND2	9, 15	Bus-side Ground. Both pins are internally connected.
NC	10	No Connect. This pin is not connected to any internal circuitry.
Y	11	Non-inverting Driver Output
Z	12	Inverting Driver Output
B	13	Inverting Receiver Input
A	14	Non-inverting Receiver Input
V <sub>CC2</sub>	16	Bus-side Power Supply

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

				VALUE	UNIT	
V <sub>CC1</sub> , V <sub>CC2</sub>	Input supply voltage <sup>(2)</sup>			−0.3 to 6	V	
V <sub>A</sub> , V <sub>B</sub> , V <sub>Y</sub> , V <sub>Z</sub>	Voltage at any bus I/O terminal (A, B, Y, Z)			−9 to 14	V	
V <sub>D1</sub> , V <sub>D2</sub>	Voltage at D1, D2			14	V	
V <sub>(TRANS)</sub>	Voltage input, transient pulse through 100Ω, see <a href="#">Figure 12</a> (A, B, Y, Z)			−50 to +50	V	
V <sub>I</sub>	Voltage input at D, DE or $\overline{RE}$ terminal			−0.5 to 7	V	
I <sub>O</sub>	Receiver output current			±10	mA	
I <sub>D1</sub> , I <sub>D2</sub>	Transformer Driver Output Current			450	mA	
ESD	Electrostatic discharge	Human Body Model	JEDEC Standard 22, Test Method A114-C.01	Bus pins and GND1	±6	kV
				Bus pins and GND2	±11	kV
				All pins	±4	kV
		Charged Device Model	JEDEC Standard 22, Test Method C101	All pins	±1.5	kV
		Machine Model	ANSI/ESDS5.2-1996		±200	V
T <sub>J</sub>	Maximum junction temperature			170	°C	
T <sub>STG</sub>	Storage temperature			−65 to 150	°C	

- (1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.

**RECOMMENDED OPERATING CONDITIONS**

			MIN	TYP	MAX	UNIT
V <sub>CC1</sub>	Logic-side supply voltage	3.3 V Operation	3	3.3	3.6	V
		5 V Operation	4.5	5	5.5	
V <sub>CC2</sub>	Bus-side supply voltage		4.5	5	5.5	V
V <sub>I</sub> or V <sub>IC</sub>	Voltage at any bus terminal (separately or common-mode)		−7		12	V
V <sub>IH</sub>	High-level input voltage	RE	2		V <sub>CC1</sub>	V
		D, DE	0.7 V <sub>CC1</sub>			
V <sub>IL</sub>	Low-level input voltage	RE	0		0.8	V
		D, DE	0.3 V <sub>CC1</sub>			
V <sub>ID</sub>	Differential input voltage	A with respect to B	−12		12	V
		Dynamic	See <a href="#">Figure 15</a>			
R <sub>L</sub>	Differential load resistance		54	60		Ω
I <sub>O</sub>	Output Current	Driver	−60		60	mA
		Receiver	−8		8	
T <sub>A</sub>	Ambient temperature		−40		85	°C
T <sub>J</sub>	Operating junction temperature		−40		150	°C
1 / t <sub>UI</sub>	Signaling Rate				20	Mbps

## SUPPLY CURRENT and COMMON-MODE TRANSIENT IMMUNITY

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I <sub>CC1</sub> <sup>(1)</sup>	Logic-side quiescent supply current	DE and $\overline{RE} = 0\text{ V}$ or $V_{CC1}$ (Driver and Receiver Enabled or Disabled), D = 0 V or $V_{CC1}$ , No load	$V_{CC1} = 3.3\text{ V} \pm 10\%$		5	8	mA
			$V_{CC1} = 5\text{ V} \pm 10\%$		7	12	
I <sub>CC2</sub> <sup>(1)</sup>	Bus-side quiescent supply current	$\overline{RE} = 0\text{ V}$ or $V_{CC1}$ , DE = 0 V (driver disabled), No load			10	15	mA
		$\overline{RE} = 0\text{ V}$ or $V_{CC1}$ , DE = $V_{CC1}$ (driver enabled), D = 0 V or $V_{CC1}$ , No Load			10	15	
CMTI	Common-mode transient immunity	See Figure 13, V <sub>I</sub> = V <sub>CC1</sub> or 0 V		25	50		kV/μs

(1)  $I_{CC1}$  and  $I_{CC2}$  are measured when device is connected to external power supplies,  $V_{CC1}$  and  $V_{CC2}$ . In this case, D1 and D2 are open and disconnected from external transformer.

## DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>OD</sub>	Differential output voltage magnitude	$I_O = 0$ mA, no load	3	4.3	$V_{CC2}$	V
		$R_L = 54\ \Omega$ (RS-485), See Figure 2	1.5	2.3		
		$R_L = 100\ \Omega$ (RS-422), See Figure 2	2	2.3		
		$V_{test}$ from -7 V to +12 V, See Figure 3	1.5			
$\Delta V_{OD} $	Change in magnitude of the differential output voltage	See Figure 2 and Figure 3	-0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	Figure 4	1	2.6	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage		-0.1		0.1	V
$V_{OC(pp)}$	Peak-to-peak common-mode output voltage	See Figure 4		0.5		V
$I_I$	Input current	D, DE, $V_I$ at 0 V or $V_{CC1}$	-10		10	$\mu$ A
$I_{OZ}$	High-impedance state output current, Y or Z pin	$V_Y$ or $V_Z = 12V$ , $V_{CC2} = 0V$ or 5 V, DE = 0 V			1	$\mu$ A
		$V_Y$ or $V_Z = -7V$ , $V_{CC2} = 0V$ or 5 V, DE = 0 V			-1	
$I_{OS}^{(1)}$	Short-circuit output current	-7 V $\leq V_Y$ or $V_Z \leq 12V$ Other bus pin at 0 V	-250		250	mA

(1) This device has thermal shutdown and output current limiting features to protect in short-circuit fault condition.

## DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$ , $t_{PHL}$	Propagation delay	See Figure 5		25	45	ns
PWD <sup>(1)</sup>	Pulse width distortion ( $ t_{PHL} - t_{PLH} $ )			1	7.5	
$t_r$ , $t_f$	Differential output signal rise time and fall time			7	15	
$t_{PZH}$ , $t_{PHZ}$	Propagation delay, high-impedance-to-high-level output, Propagation delay, high-level-to-high-impedance output	See Figure 6 DE at 0 V		25	55	ns
$t_{PLZ}$ , $t_{PZL}$	Propagation delay, low-level to high-impedance output, Propagation delay, high-impedance to low-level output	See Figure 7, DE at 0 V		25	55	ns

(1) Also known as pulse skew

## RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT(+)}$	Positive-going input threshold voltage	$I_O = -8 \text{ mA}$		-85	-10	mV
$V_{IT(-)}$	Negative-going input threshold voltage	$I_O = 8 \text{ mA}$	-200	-115		mV
$V_{hys}$	Hysteresis voltage ( $V_{IT+} - V_{IT-}$ )			30		mV
$V_{OH}$	High-level output voltage	$V_{ID} = 200 \text{ mV}$ , $I_O = -8 \text{ mA}$ , See Figure 8	$V_{CC1} = 3.3 \text{ V}$	$V_{CC1} - 0.4$	3.1	V
			$V_{CC1} = 5 \text{ V}$	4	4.8	
$V_{OL}$	Low-level output voltage	$V_{ID} = 200 \text{ mV}$ , $I_O = 8 \text{ mA}$ , See Figure 8	$V_{CC1} = 3.3 \text{ V}$	0.15	0.4	V
			$V_{CC1} = 5 \text{ V}$	0.15	0.4	
$I_{O(Z)}$	High-impedance state output current	$V_O = 0$ or $V_{CC1}$ , $\overline{RE} = V_{CC1}$	-1		1	$\mu\text{A}$
$I_A, I_B$	Bus input current	$V_A$ or $V_B = 12 \text{ V}$		40	100	$\mu\text{A}$
		$V_A$ or $V_B = 12 \text{ V}$ , $V_{CC2} = 0$		60	130	
		$V_A$ or $V_B = -7 \text{ V}$	-100	-40		
		$V_A$ or $V_B = -7 \text{ V}$ , $V_{CC2} = 0$	-100	-30		
$I_{IH}$	High-level input current, $\overline{RE}$	$V_{IH} = 2. \text{ V}$	-10		10	$\mu\text{A}$
$I_{IL}$	Low-level input current, $\overline{RE}$	$V_{IL} = 0.8 \text{ V}$	-10		10	
$R_{ID}$	Differential input resistance	A, B	96			k $\Omega$
$C_{ID}$	Differential input capacitance	$V_I = 0.4 \sin(4E6\pi t) + 0.5 \text{ V}$		7		pF

## RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}, t_{PHL}$	Propagation delay	See Figure 9		103	125	ns
$t_{sk(p)}$	Pulse skew ( $ t_{PHL} - t_{PLH} $ )			3	15	
$t_r, t_f$	Output signal rise and fall time			1		
$t_{PHZ}, t_{PZH}$	Propagation delay, high-level to high-impedance output Propagation delay, high-impedance to high-level output	See Figure 10, DE at 0 V		11	22	ns
$t_{PLZ}, t_{PZL}$	Propagation delay, low-level to high-impedance output Propagation delay, high-impedance to low-level output	See Figure 11, DE at 0 V		11	22	

## TRANSFORMER DRIVER CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{OSC}$	Oscillator frequency	$V_{CC1} = 5 \text{ V} \pm 10\%$ , D1 and D2 connected to transformer	350	450	610	kHz
		$V_{CC1} = 3.3 \text{ V} \pm 10\%$ , D1 and D2 connected to transformer	300	400	550	
$R_{ON}$	Switch on resistance	D1 and D2 connected to 50 $\Omega$ pull-up resistors		1	2.5	$\Omega$
$t_{r_D}$	D1, D2 output rise time	$V_{CC1} = 5 \text{ V} \pm 10\%$ , see Figure 14, <sup>(1)</sup>		80		ns
		$V_{CC1} = 3.3 \text{ V} \pm 10\%$ , see Figure 14, <sup>(1)</sup>		70		
$t_{f_D}$	D1, D2 output fall time	$V_{CC1} = 5 \text{ V} \pm 10\%$ , see Figure 14, <sup>(1)</sup>		55		ns
		$V_{CC1} = 3.3 \text{ V} \pm 10\%$ , see Figure 14, <sup>(1)</sup>		80		
$f_{St}$	Startup frequency	$V_{CC1} = 2.4 \text{ V}$ , D1 and D2 connected to transformer		350		kHz
$t_{BBM}$	Break before make time delay	$V_{CC1} = 5 \text{ V} \pm 10\%$ , see Figure 14, <sup>(1)</sup>		38		ns
		$V_{CC1} = 3.3 \text{ V} \pm 10\%$ , see Figure 14, <sup>(1)</sup>		140		

<sup>(1)</sup> D1 and D2 connected to 50 $\Omega$  pull-up resistors

## PARAMETER MEASUREMENT INFORMATION

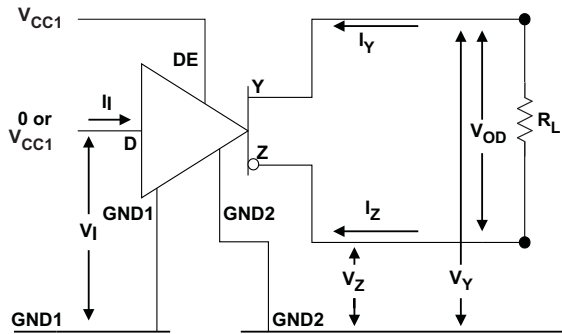


Figure 2. Driver  $V_{OD}$  Test and Current Definitions

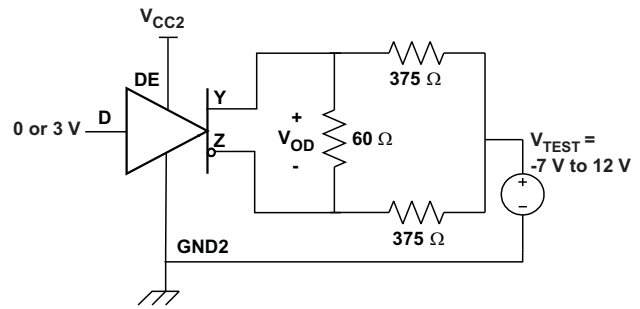


Figure 3. Driver  $V_{OD}$  With Common-Mode Loading Test Circuit

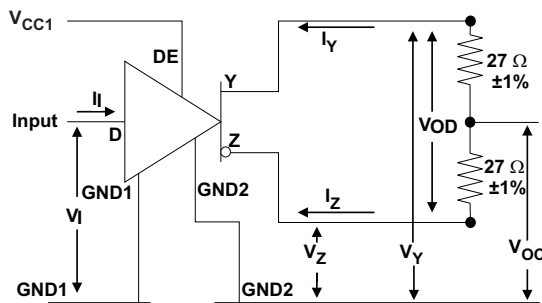


Figure 4. Test Circuit and Waveform Definitions For The Driver Common-Mode Output Voltage

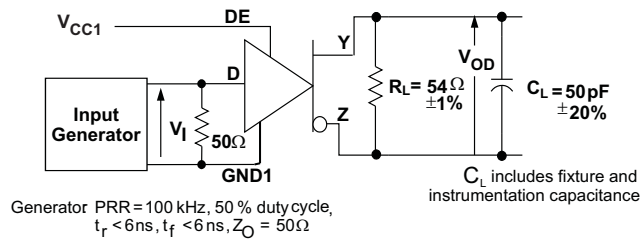
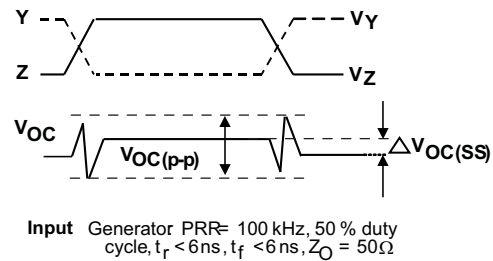


Figure 5. Driver Switching Test Circuit and Voltage Waveforms

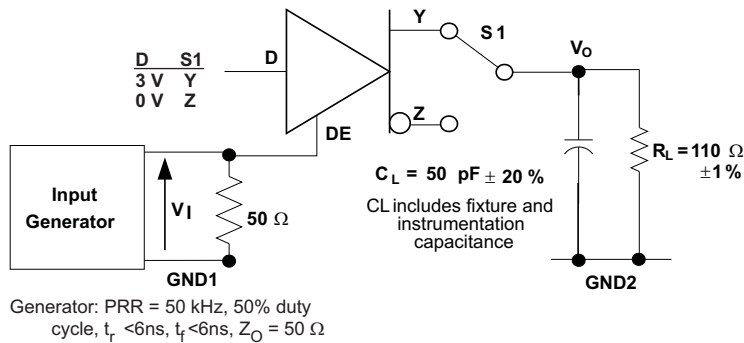
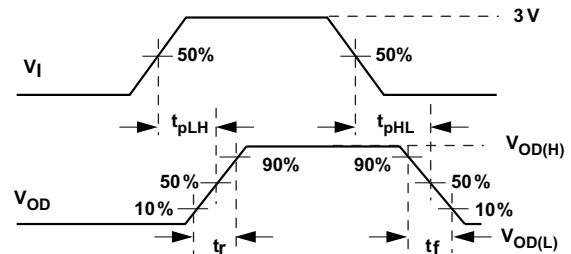


Figure 6. Driver High-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

## PARAMETER MEASUREMENT INFORMATION (continued)

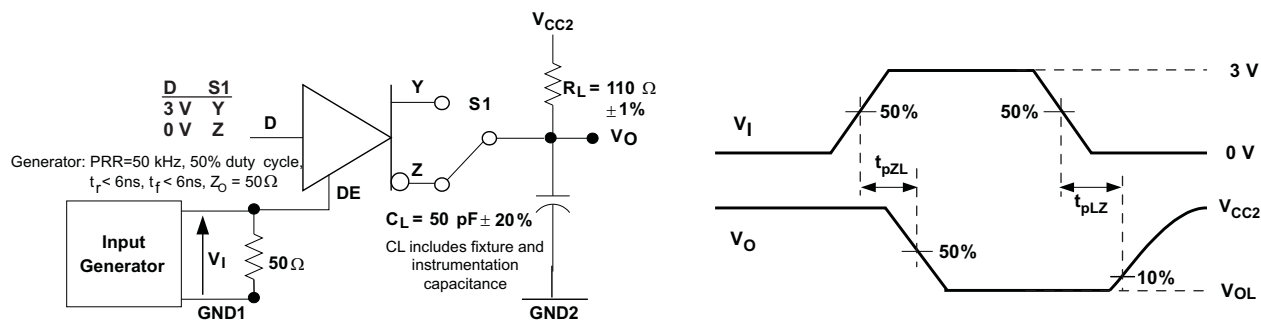


Figure 7. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveform

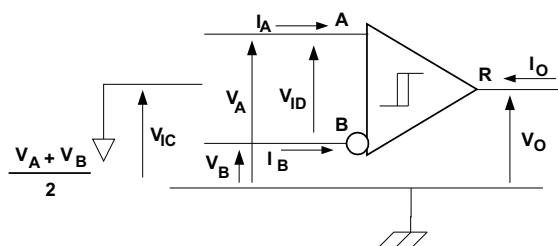


Figure 8. Receiver Voltage and Current Definitions

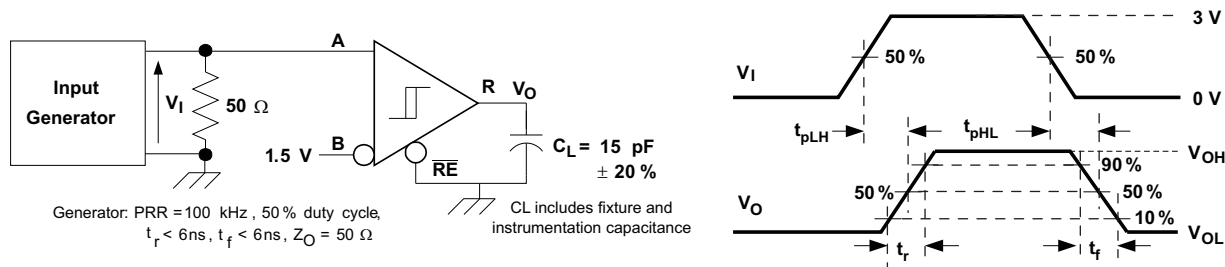


Figure 9. Receiver Switching Test Circuit and Waveforms

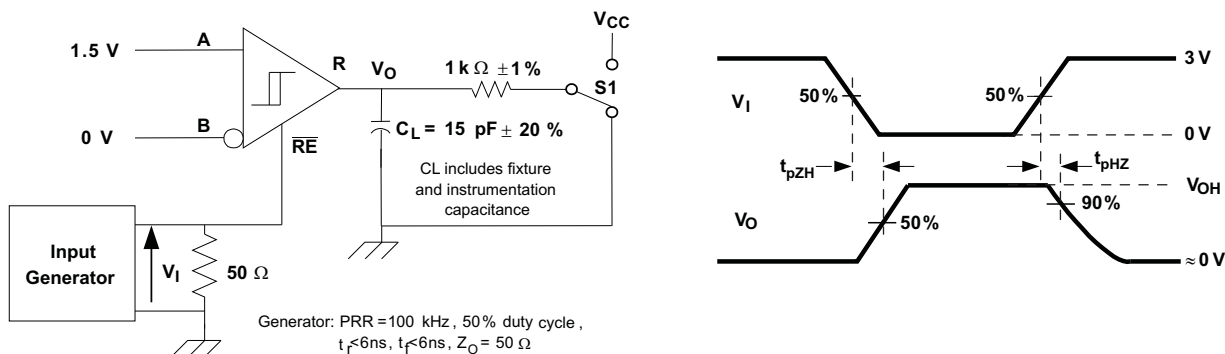
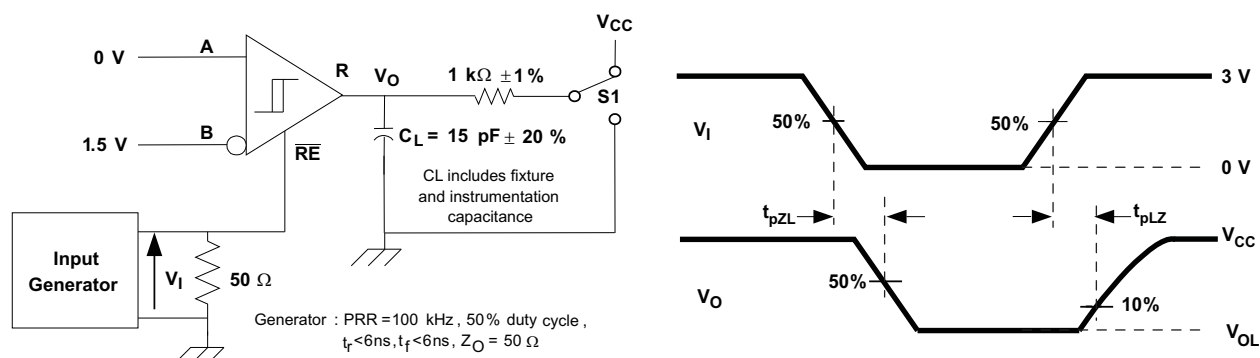
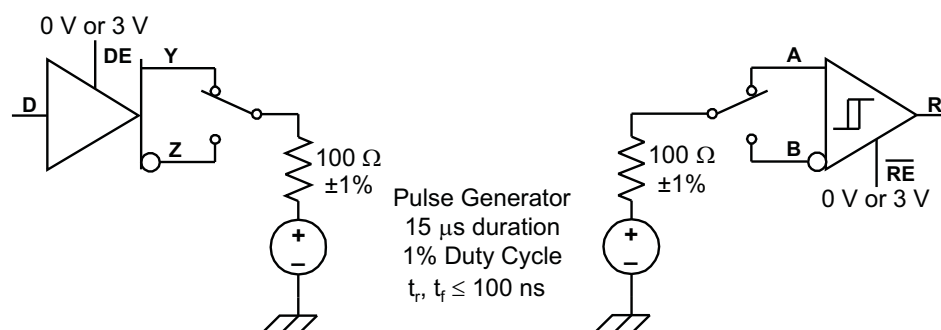
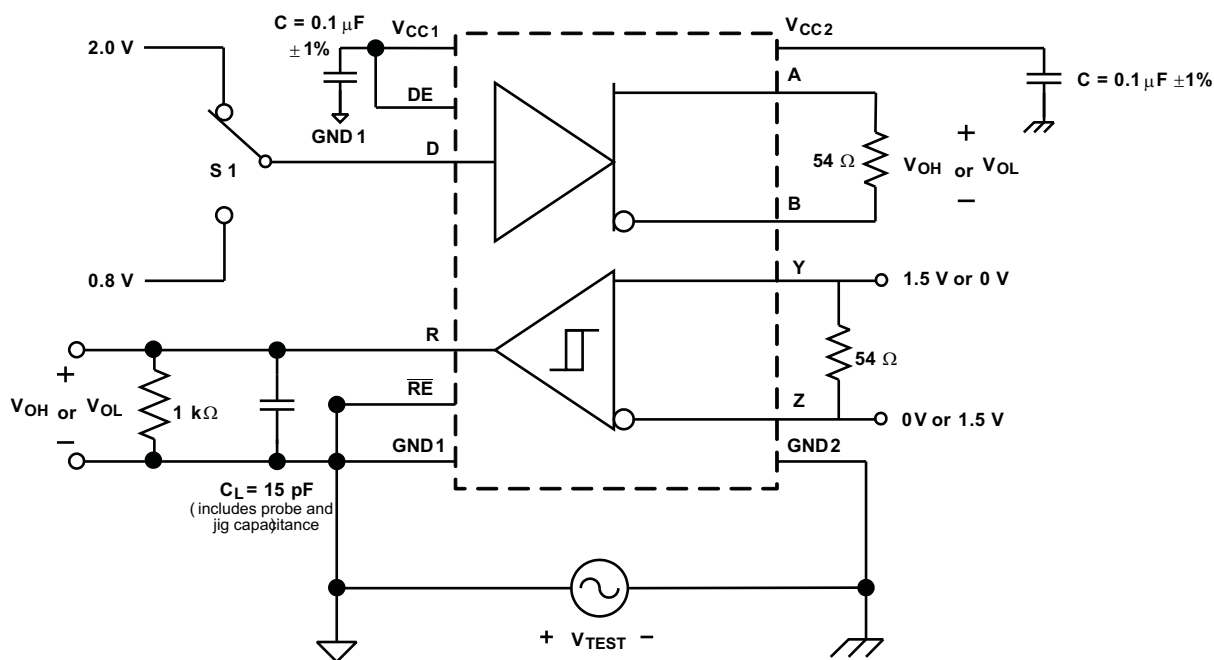
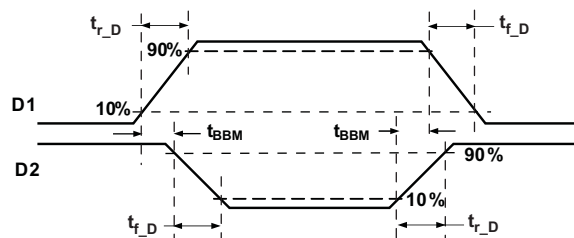


Figure 10. Receiver Enable Test Circuit and Waveforms, Data Output High

**PARAMETER MEASUREMENT INFORMATION (continued)**

**Figure 11. Receiver Enable Test Circuit and Waveforms, Data Output Low**

**Figure 12. Transient Over-Voltage Test Circuit**

**Figure 13. Common-Mode Transient Immunity Test Circuit**



## PARAMETER MEASUREMENT INFORMATION (continued)



**Figure 14. Transition Times and Break-Before-Make Time Delay for D1, D2 Outputs**

## DEVICE INFORMATION

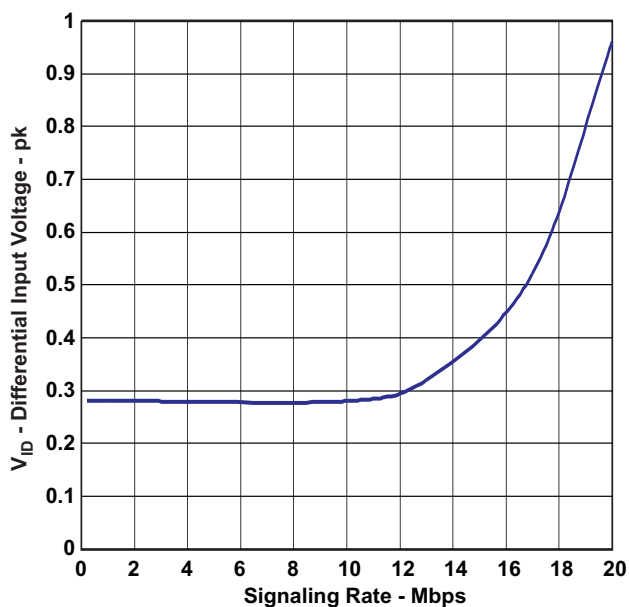


Figure 15. ISO3086T Recommended Minimum Differential Input Voltage vs Signaling Rate

Table 1. Driver Function Table<sup>(1)</sup>

INPUT	ENABLE	OUTPUTS	
(D)	(DE)	Y	Z
H	H	H	L
L	H	L	H
X	L	hi-Z	hi-Z
X	OPEN	hi-Z	hi-Z
OPEN	H	H	L

(1) H = High Level, L = Low Level, X = Don't Care, hi-Z = High Impedance (off)

Table 2. Receiver Function Table<sup>(1)</sup>

DIFFERENTIAL INPUT $V_{ID} = (V_A - V_B)$	ENABLE (RE)	OUTPUT (R)
$-0.01 \text{ V} \leq V_{ID}$	L	H
$-0.2 \text{ V} < V_{ID} < -0.01 \text{ V}$	L	?
$V_{ID} \leq -0.2 \text{ V}$	L	L
X	H	hi-Z
X	OPEN	hi-Z
Open circuit	L	H
Short Circuit	L	H
Idle (terminated) bus	L	H

(1) H = High Level, L = Low Level, X = Don't Care, hi-Z = High Impedance (Off), ? = Indeterminate

## IEC INSULATION AND SAFETY RELATED SPECIFICATIONS FOR 16-DW PACKAGE

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance <sup>(1)</sup> )	Shortest terminal to terminal distance through air	8.3			mm
L(I02)	Minimum external tracking (Creepage <sup>(1)</sup> )	Shortest terminal to terminal distance across the package surface	8.1			mm
CTI	Tracking resistance(Comparative Tracking Index)	DIN IEC 60112 / VDE 0303 Part 1	400			V
	Minimum Internal Gap (Internal Clearance)	Distance through the insulation	0.008			mm
R <sub>IO</sub>	Isolation resistance	Input to output, V <sub>IO</sub> = 500 V, all pins on each side of the barrier tied together creating a two-terminal device	>10 <sup>12</sup>			Ω
C <sub>IO</sub>	Barrier capacitance Input to output	V <sub>I</sub> = V <sub>CC</sub> /2 + 0.4 sin (2πft), f = 1 MHz, V <sub>CC</sub> = 5 V		2		pF
C <sub>I</sub>	Input capacitance to ground	V <sub>IO</sub> = 0.4 sin (2πft), f = 1 MHz		2		pF

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance.

Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

### IEC 60664-1 RATINGS TABLE

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	II
Installation classification	Rated mains voltage ≤ 150 V <sub>RMS</sub>	I-IV
	Rated mains voltage ≤ 300 V <sub>RMS</sub>	I-III
	Rated mains voltage ≤ 400 V <sub>RMS</sub>	I-II

### IEC 60747-5-2 INSULATION CHARACTERISTICS<sup>(1)</sup>

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SPECIFICATION	UNIT
V <sub>IORM</sub>	Maximum working insulation voltage	566	V <sub>PK</sub>
V <sub>PR</sub>	Input to output test voltage	Method b1, V <sub>PR</sub> = V <sub>IORM</sub> × 1.875, 100% Production test with t = 1 s, Partial discharge < 5 pC	V <sub>PK</sub>
		Method a, After environmental tests subgroup 1, V <sub>PR</sub> = V <sub>IORM</sub> × 1.6, t = 10 s, Partial discharge < 5pC	
		After Input/Output Safety Test Subgroup 2/3, V <sub>PR</sub> = V <sub>IORM</sub> × 1.2, t = 10 s, Partial discharge < 5 pC	
V <sub>IOTM</sub>	Maximum transient overvoltage	t = 60 s	V <sub>PK</sub>
V <sub>IOSM</sub>	Maximum surge voltage	Tested per IEC 60065 (Qualification Test)	V <sub>PK</sub>
R <sub>S</sub>	Insulation resistance	V <sub>IO</sub> = 500 V at T <sub>S</sub>	> 10 <sup>9</sup> Ω
	Pollution degree		2

- (1) Climatic Classification 40/125/21

# ISO3086T

SLLSE27C – JANUARY 2011 – REVISED JULY 2011

[www.ti.com](http://www.ti.com)

## REGULATORY INFORMATION

VDE	UL
Certified according to DIN EN / IEC 60747-5-2 (VDE 0884 Part 2)	Recognized under 1577 Component Recognition Program
Basic Insulation Maximum Transient Overvoltage, 4242 V <sub>PK</sub> Maximum Surge Voltage, 4242 V <sub>PK</sub> Maximum Working Voltage, 566 V <sub>PK</sub>	Single / Basic Isolation Voltage, 2500 V <sub>RMS</sub> <sup>(1)</sup>
File Number: 40016131 (Approval Pending)	File Number: E181974 (Approval Pending)

(1) Production tested  $\geq 3000$  V<sub>RMS</sub> for 1 second in accordance with UL 1577.

## IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply. Without current limiting, sufficient power is dissipated to overheat the die; and, damage the isolation barrier—potentially leading to secondary system failures.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>S</sub> Safety input, output, or supply current	DW-16 $\theta_{JA} = 80.5^{\circ}\text{C/W}$ , V <sub>I</sub> = 5.5 V, T <sub>J</sub> = 170°C, T <sub>A</sub> = 25°C			327	mA
T <sub>S</sub> Maximum case temperature				150	°C

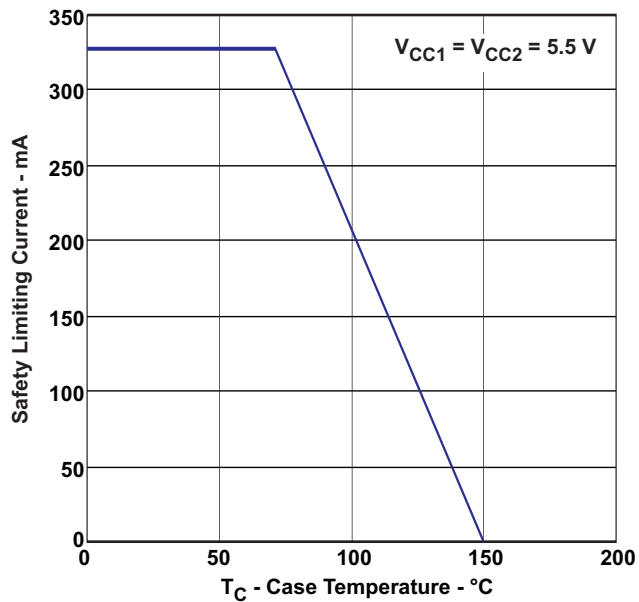
The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the Thermal Characteristics table is that of a device installed on a High-K Test Board for Leaded Surface Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

## THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		ISO3086T	UNITS
		DW	
		16 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance	80.5	°C/W
$\theta_{JC(TOP)}$	Junction-to-case(top) thermal resistance	43.8	
$\theta_{JB}$	Junction-to-board thermal resistance	49.7	
$\psi_{JT}$	Junction-to-top characterization parameter	13.8	
$\psi_{JB}$	Junction-to-board characterization parameter	41.4	
$\theta_{JC(BOTTOM)}$	Junction-to-case(bottom) thermal resistance	n/a	
P <sub>D</sub> <sup>(2)</sup>	V <sub>CC1</sub> = V <sub>CC2</sub> = 5.5V, T <sub>J</sub> = 150°C, R <sub>L</sub> = 54Ω, C <sub>L</sub> = 50pF (Driver), C <sub>L</sub> = 15pF (Receiver), Input a 10 MHz 50% duty cycle square wave to Driver and Receiver	490	mW

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

(2) P<sub>D</sub> = Maximum device power dissipation



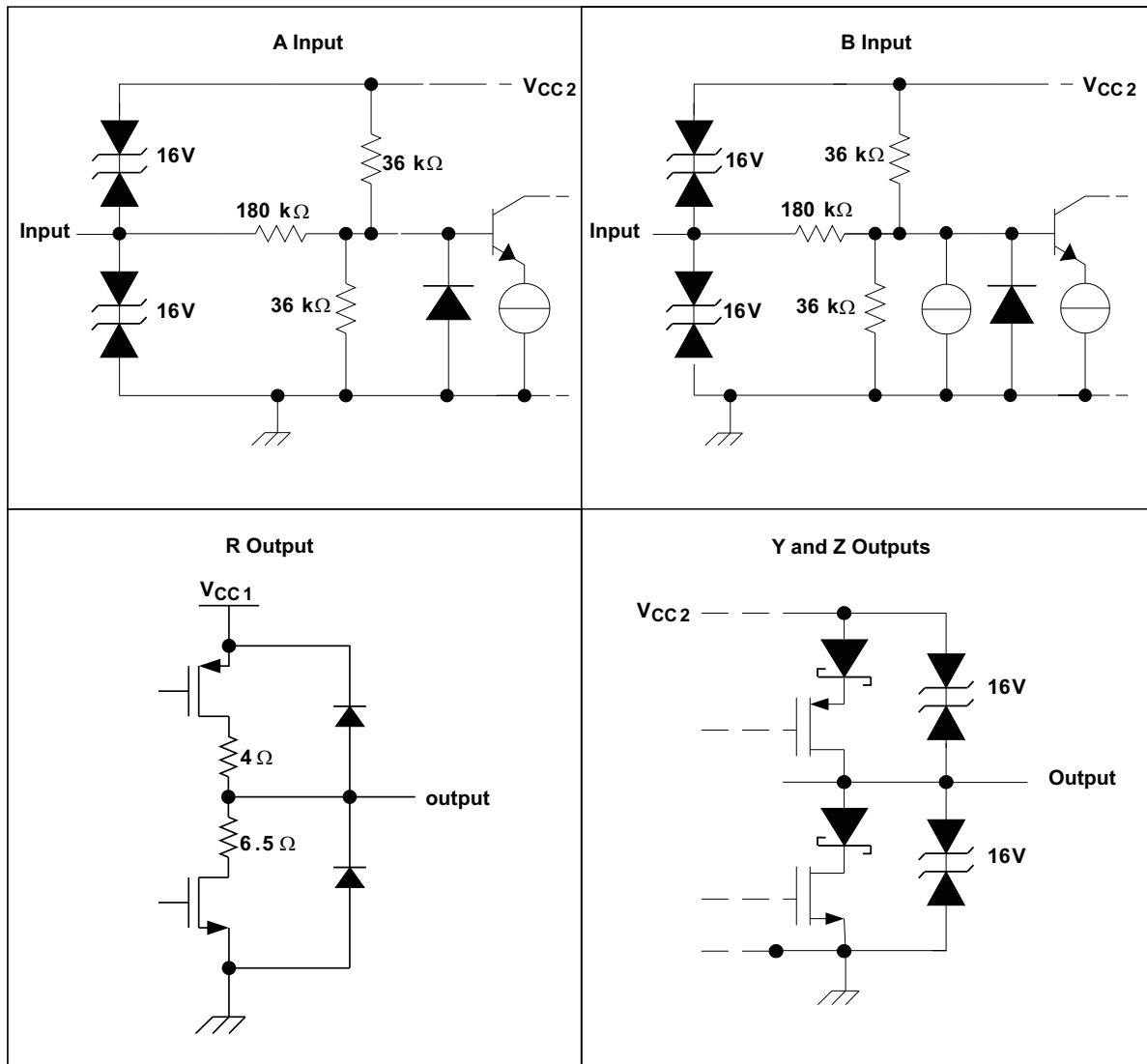
**Figure 16. DW-16  $\theta_{JC}$  Thermal Derating Curve per IEC 60747-5-2**

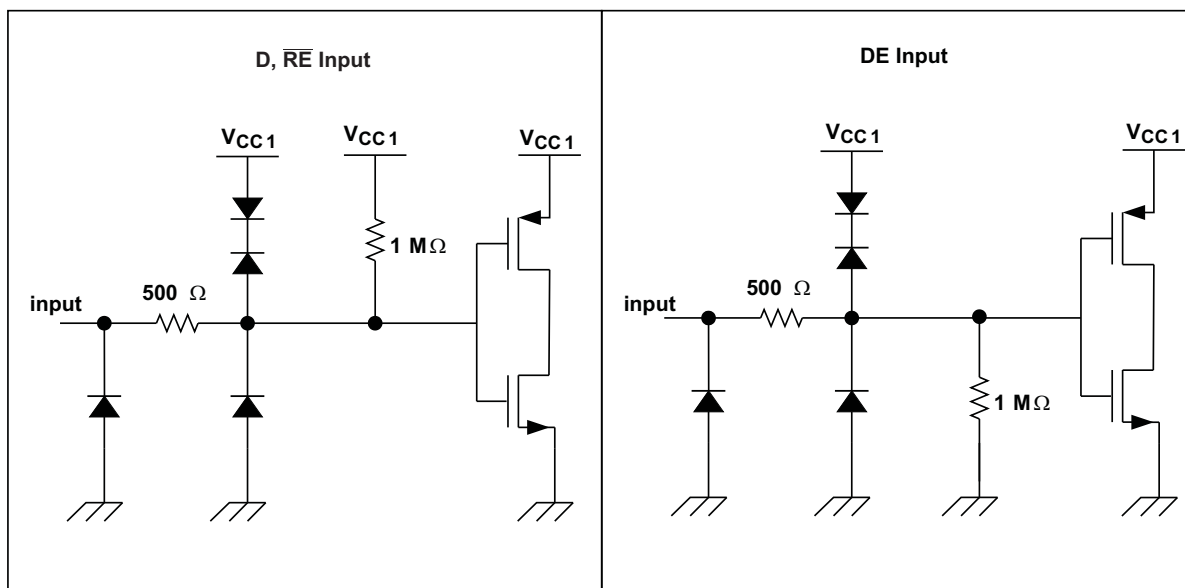
# ISO3086T

SLLSE27C – JANUARY 2011 – REVISED JULY 2011

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## EQUIVALENT CIRCUIT SCHEMATICS





## TYPICAL CHARACTERISTICS

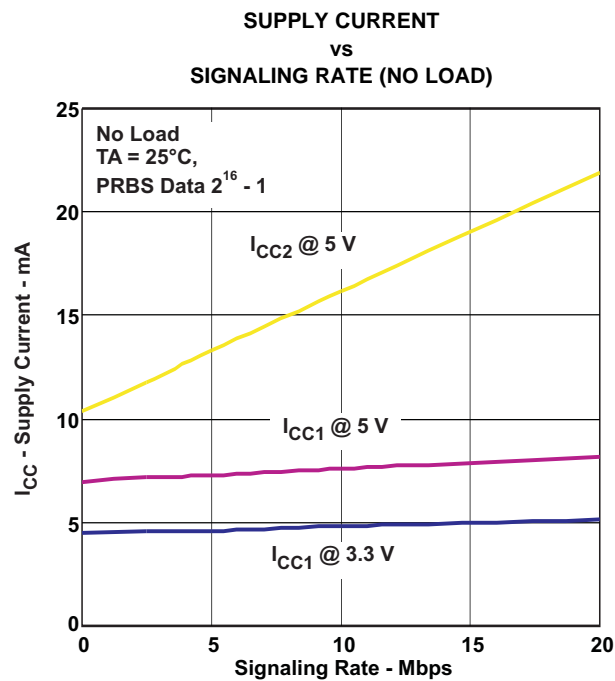


Figure 17.

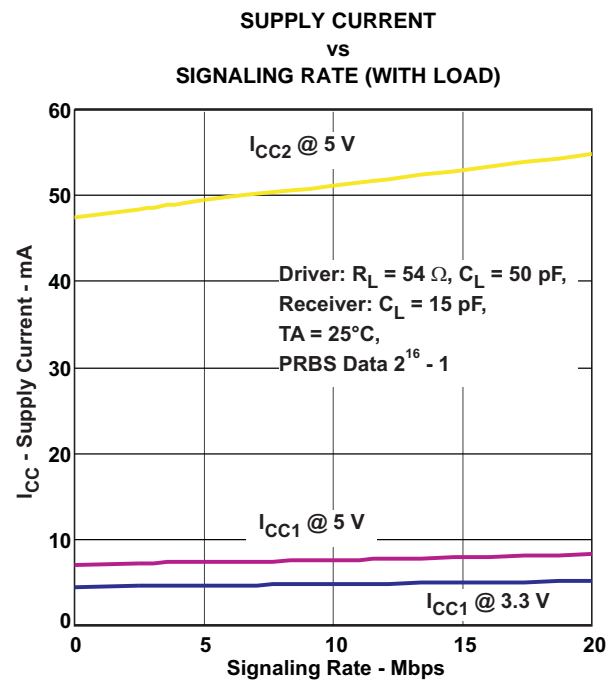


Figure 18.

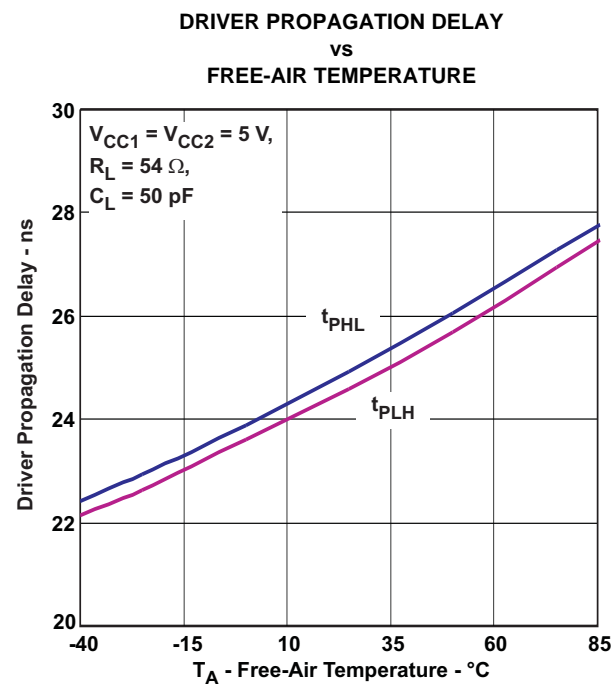


Figure 19.

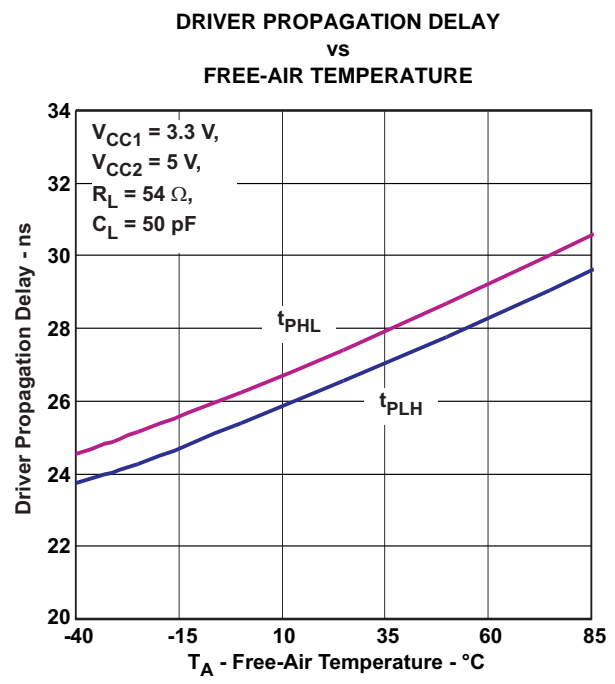


Figure 20.



## TYPICAL CHARACTERISTICS (continued)

RECEIVER PROPAGATION DELAY  
vs  
FREE-AIR TEMPERATURE

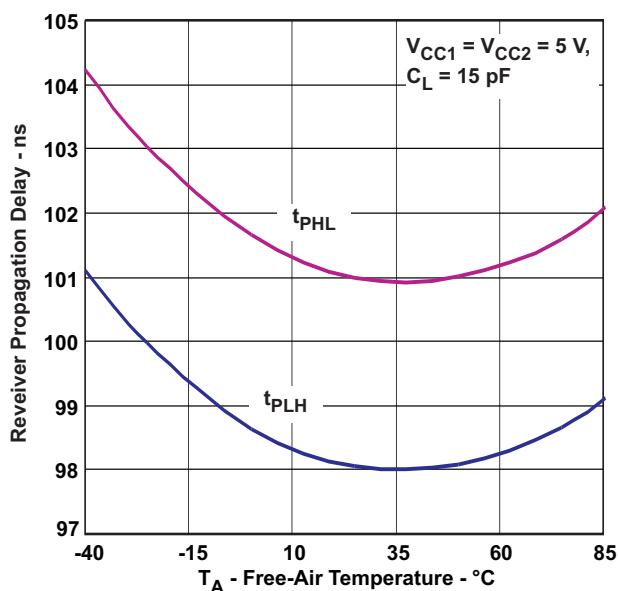


Figure 21.

RECEIVER PROPAGATION  
vs  
FREE-AIR TEMPERATURE

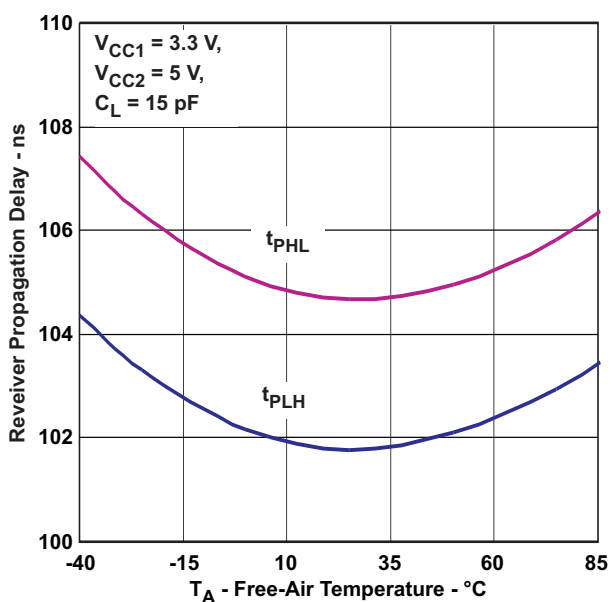


Figure 22.

DRIVER RISE, FALL TIME  
vs  
FREE-AIR TEMPERATURE

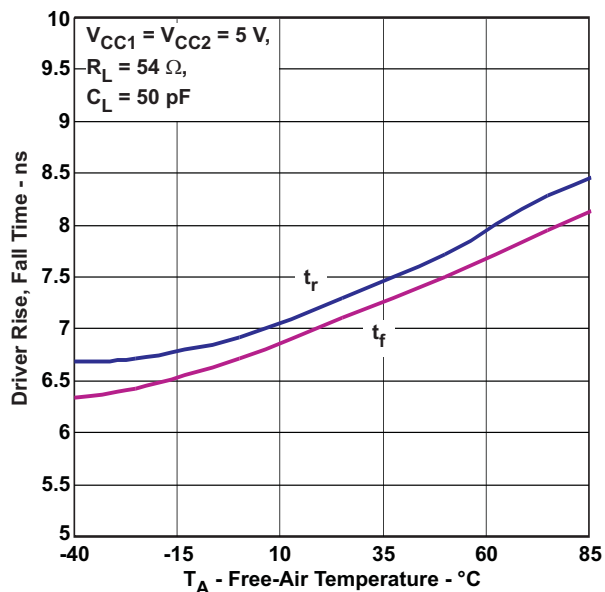


Figure 23.

DRIVER RISE, FALL TIME  
vs  
FREE-AIR TEMPERATURE

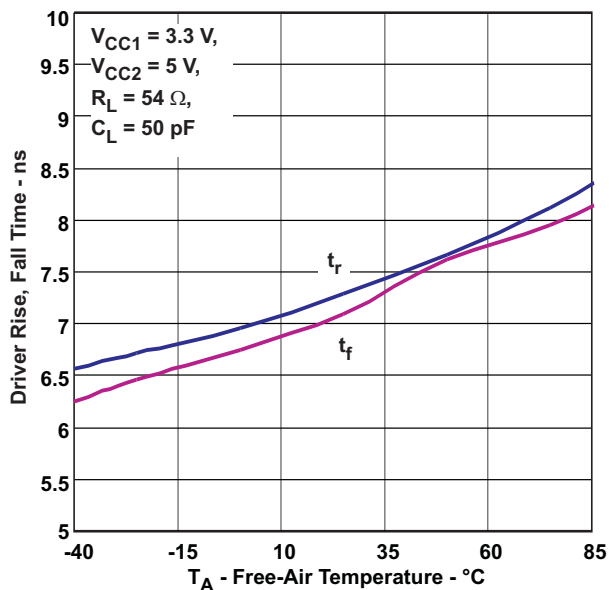


Figure 24.

**TYPICAL CHARACTERISTICS (continued)**

RECEIVER RISE, FALL TIME  
vs  
FREE-AIR TEMPERATURE

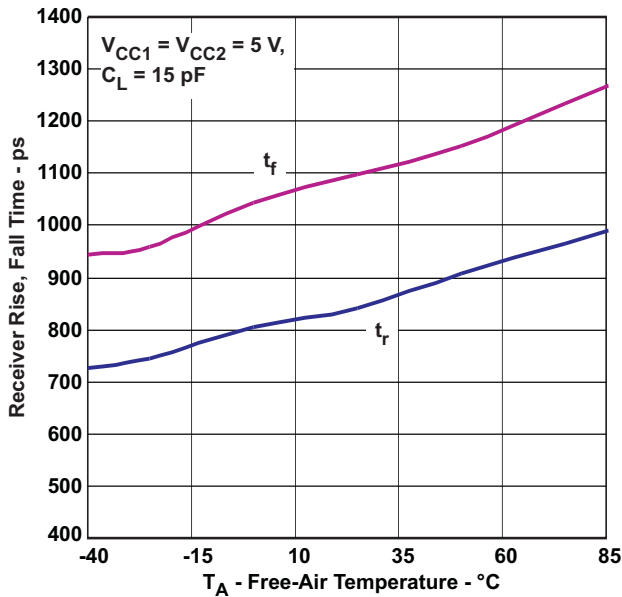


Figure 25.

RECEIVER RISE, FALL TIME  
vs  
FREE-AIR TEMPERATURE

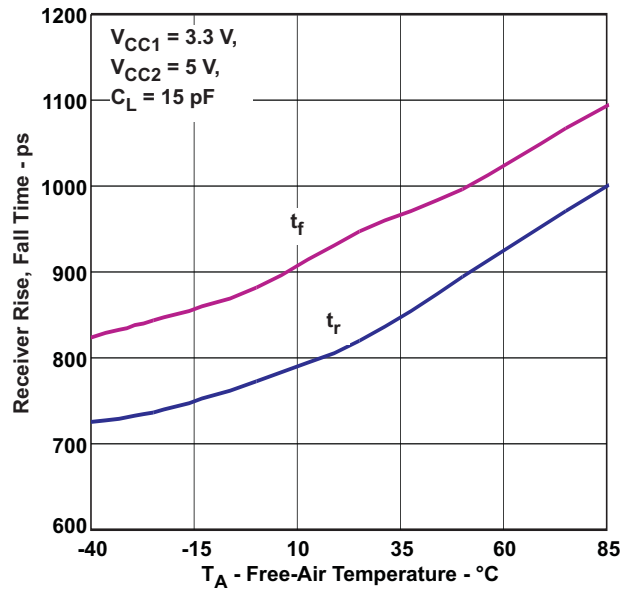


Figure 26.

DRIVER DIFFERENTIAL OUTPUT VOLTAGE  
vs  
LOAD CURRENT

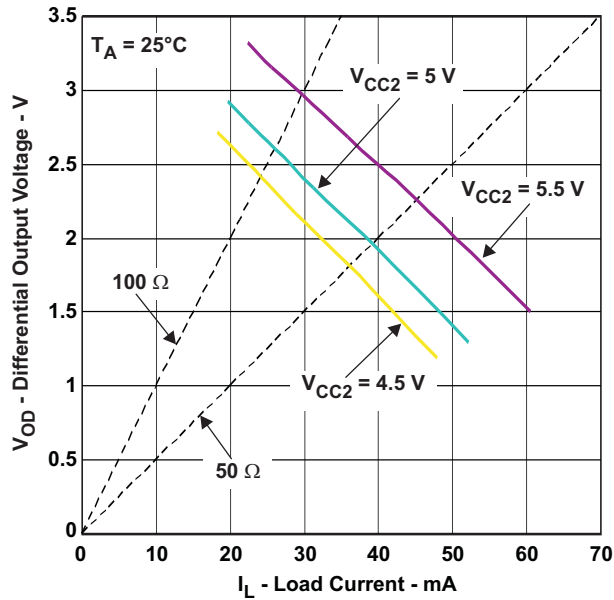


Figure 27.

RECEIVER HIGH-LEVEL OUTPUT CURRENT  
vs  
HIGH-LEVEL OUTPUT VOLTAGE

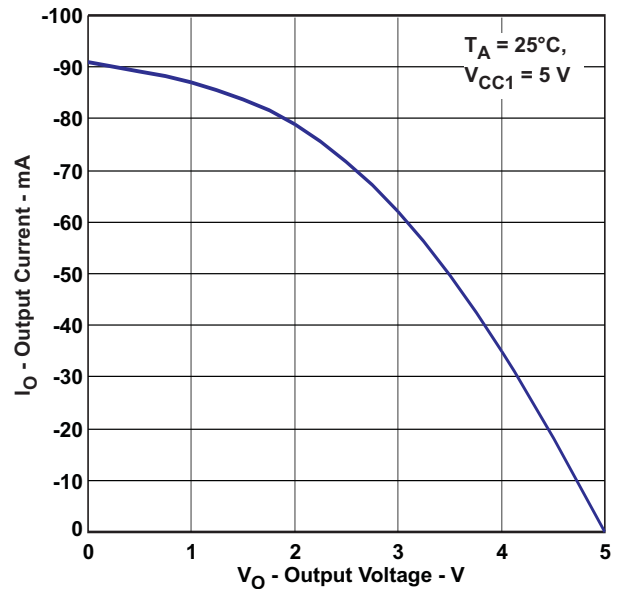


Figure 28.

## TYPICAL CHARACTERISTICS (continued)

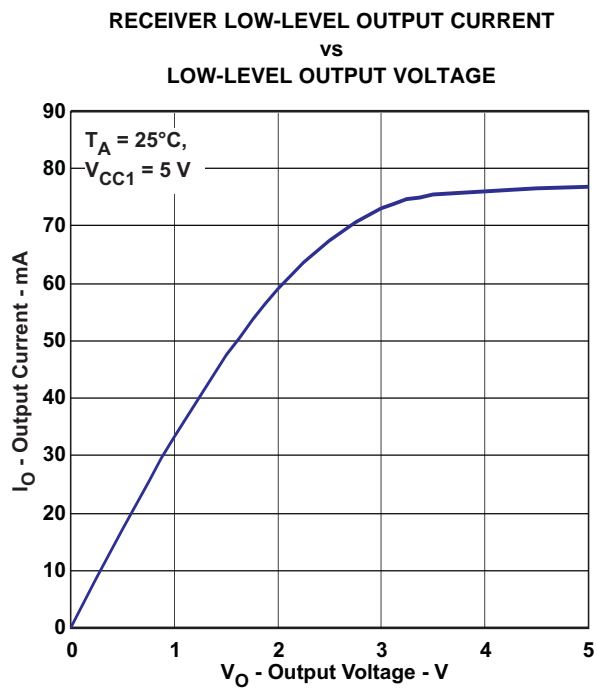


Figure 29.

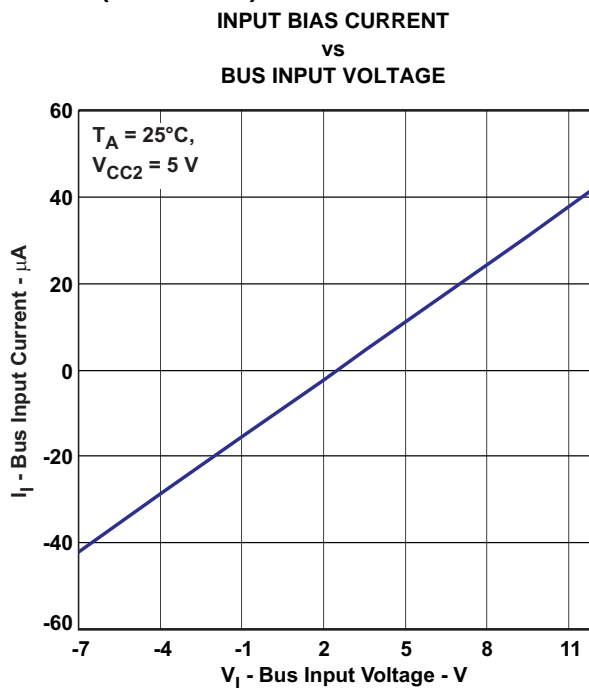


Figure 30.

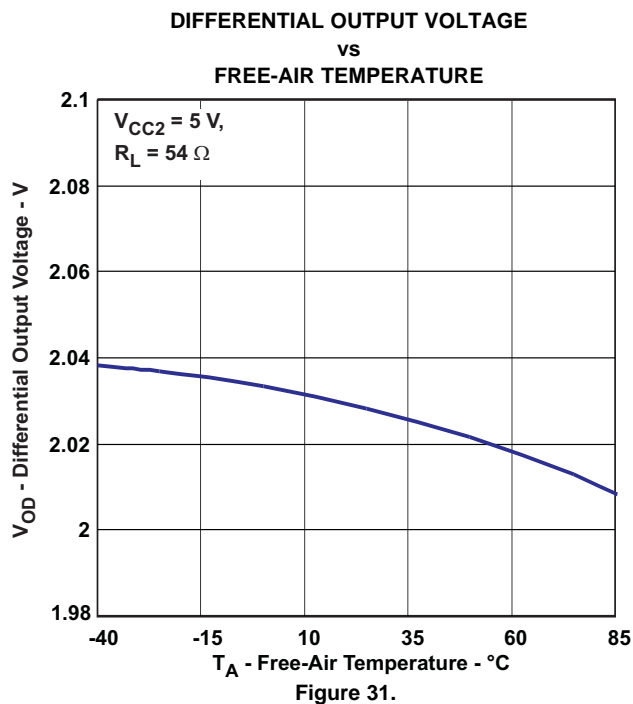


Figure 31.

## APPLICATION INFORMATION

### REFERENCE DESIGN

ISO3086T Reference design ([SLUU469](#)) and miniature evaluation boards are available.

### TRANSIENT VOLTAGES

Isolation of a circuit insulates it from other circuits and earth so that noise develops across the insulation rather than circuit components. The most common noise threat to data-line circuits is voltage surges or electrical fast transients that occur after installation and the transient ratings of the ISO3086T are sufficient for all but the most severe installations. However, some equipment manufacturers use their ESD generators to test transient susceptibility of their equipment and can easily exceed insulation ratings. ESD generators simulate static discharges that may occur during device or equipment handling with low-energy but very high voltage transients.

**Figure 32** models the ISO3086T bus IO connected to a noise generator.  $C_{IN}$  and  $R_{IN}$  is the device and any other stray or added capacitance or resistance across the A or B pin to GND2,  $C_{ISO}$  and  $R_{ISO}$  is the capacitance and resistance between GND1 and GND2 of the ISO308x plus those of any other insulation (transformer, etc.), and we assume stray inductance negligible. From this model, the voltage at the isolated bus return is

$$V_{GND2} = V_N \frac{Z_{ISO}}{Z_{ISO} + Z_{IN}}$$
 and will always be less than 16 V from  $V_N$ . If the ISO3086 are tested as a stand-alone device,  $R_{IN} = 6 \times 10^4 \Omega$ ,  $C_{IN} = 16 \times 10^{-12} \text{ F}$ ,  $R_{ISO} = 10^9 \Omega$  and  $C_{ISO} = 10^{-12} \text{ F}$ .

Note from **Figure 32** that the resistor ratio determines the voltage ratio at low frequency and it is the inverse capacitance ratio at high frequency. In the stand-alone case and for low frequency,

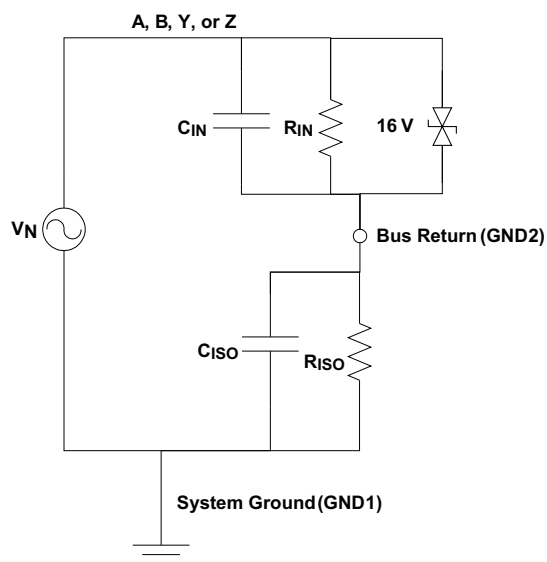
$$\frac{V_{GND2}}{V_N} = \frac{R_{ISO}}{R_{ISO} + R_{IN}} = \frac{10^9}{10^9 + 6 \times 10^4}$$

or essentially all of noise appears across the barrier. At very high frequency,

$$\frac{V_{GND2}}{V_N} = \frac{\frac{1}{C_{ISO}}}{\frac{1}{C_{ISO}} + \frac{1}{C_{IN}}} = \frac{1}{1 + \frac{C_{ISO}}{C_{IN}}} = \frac{1}{1 + \frac{1}{16}} = 0.94$$

and 94% of  $V_N$  appears across the barrier. As long as  $R_{ISO}$  is greater than  $R_{IN}$  and  $C_{ISO}$  is less than  $C_{IN}$ , most of transient noise appears across the isolation barrier, as it should.

We recommend the reader **not** test equipment transient susceptibility with ESD generators or consider product claims of ESD ratings above the barrier transient ratings of an isolated interface. ESD is best managed through recessing or covering connector pins in a conductive connector shell and installer training.



**Figure 32. Noise Model**

## REVISION HISTORY

Changes from Original (January 2011) to Revision A	Page
• Changed the data sheet From: Preview To: Production .....	1
• Changed the Features and Description .....	1
• Added <a href="#">Figure 1</a> Typical Application Circuit .....	2
<hr/>	
Changes from Revision A (March 2011) to Revision B	Page
• Deleted the MIN and MAX values from rows, $t_{r_d}$ , $t_{f_D}$ , and $t_{BBM}$ of the TRANSFORMER DRIVER CHARACTERISTICS table .....	5
<hr/>	
Changes from Revision B (July 2011) to Revision C	Page
• Added Note 1 to the TRANSFORMER DRIVER CHARACTERISTICS table .....	5
• Changed the TRANSFORMER DRIVER CHARACTERISTICS table - $f_{st}$ Test Conditions From: $V_{CC1} = 9V$ To: $V_{CC1} = 2.4$ and Changed the TYP value From: 230 To: 350 kHz .....	5

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
ISO3086TDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ISO3086TDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

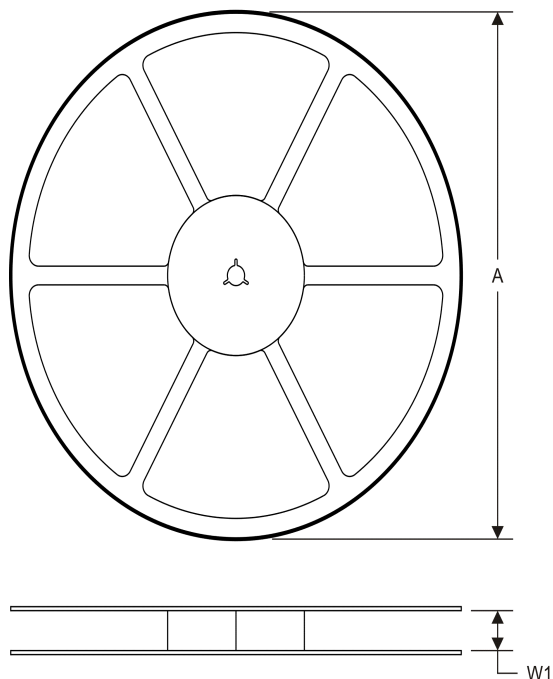
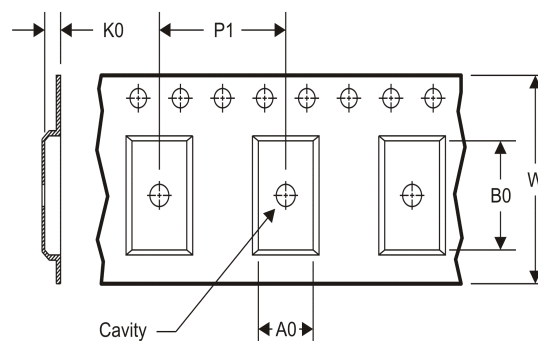
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


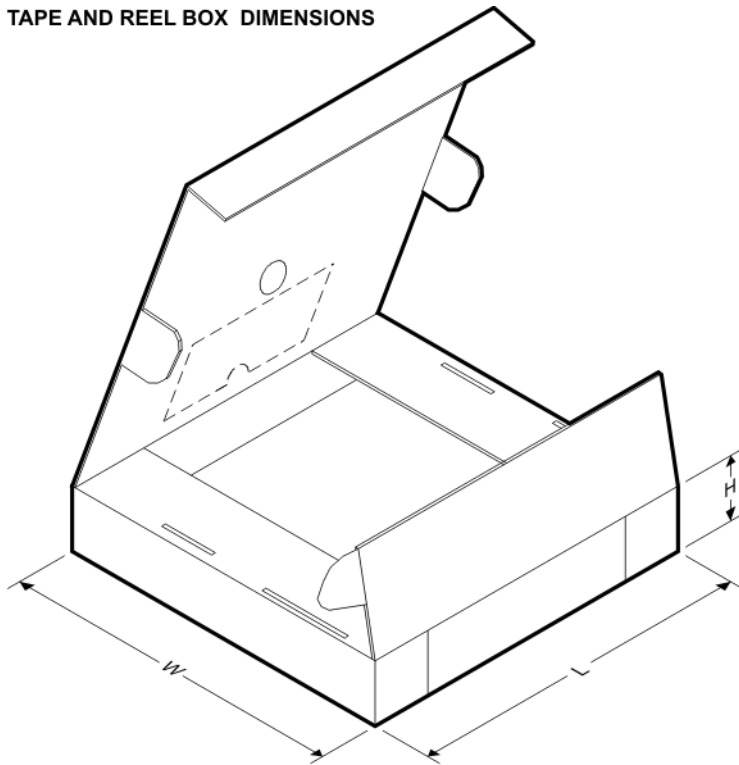
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO3086TDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



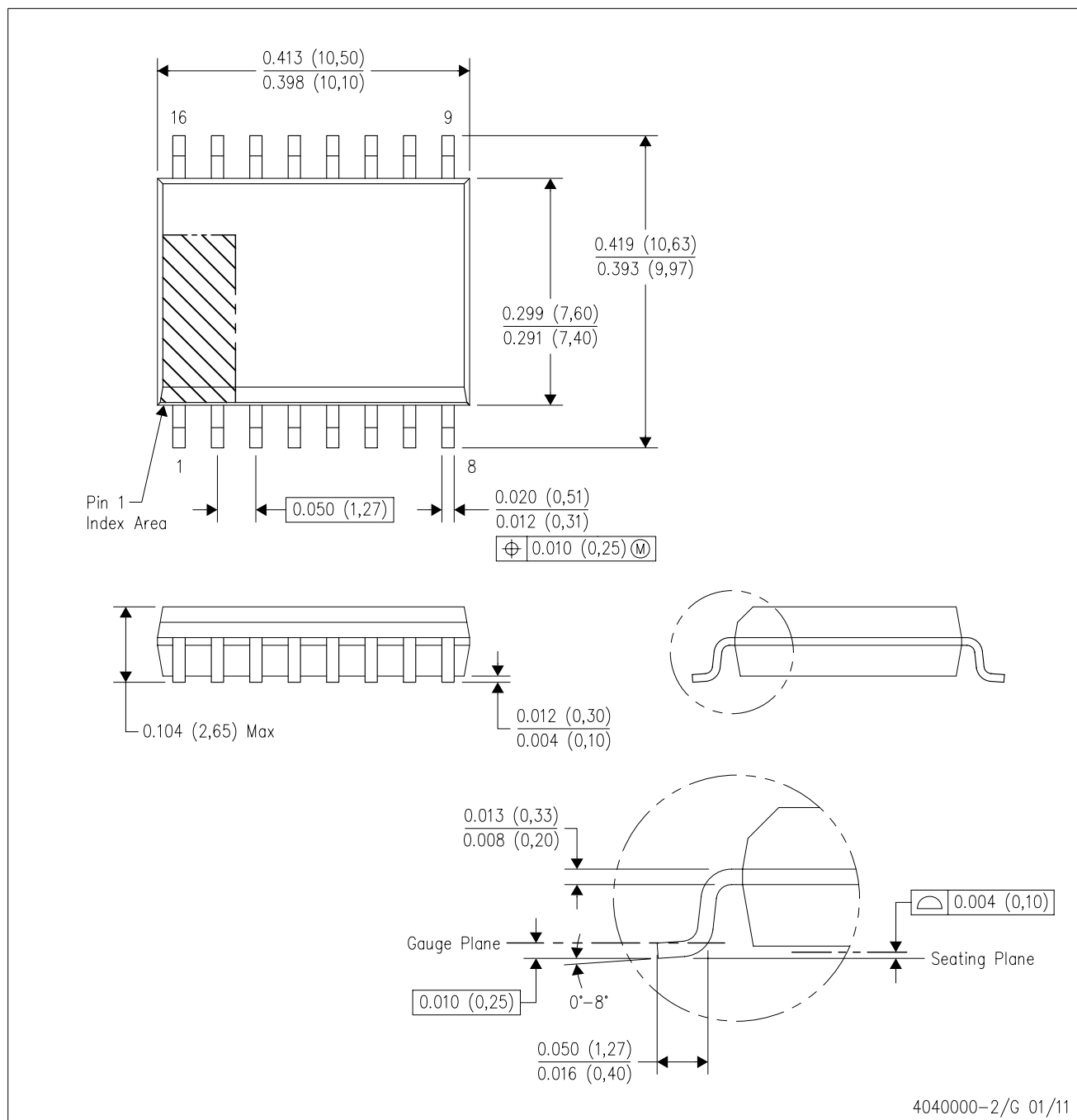
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO3086TDWR	SOIC	DW	16	2000	533.4	186.0	36.0



DW (R-PDSO-G16)

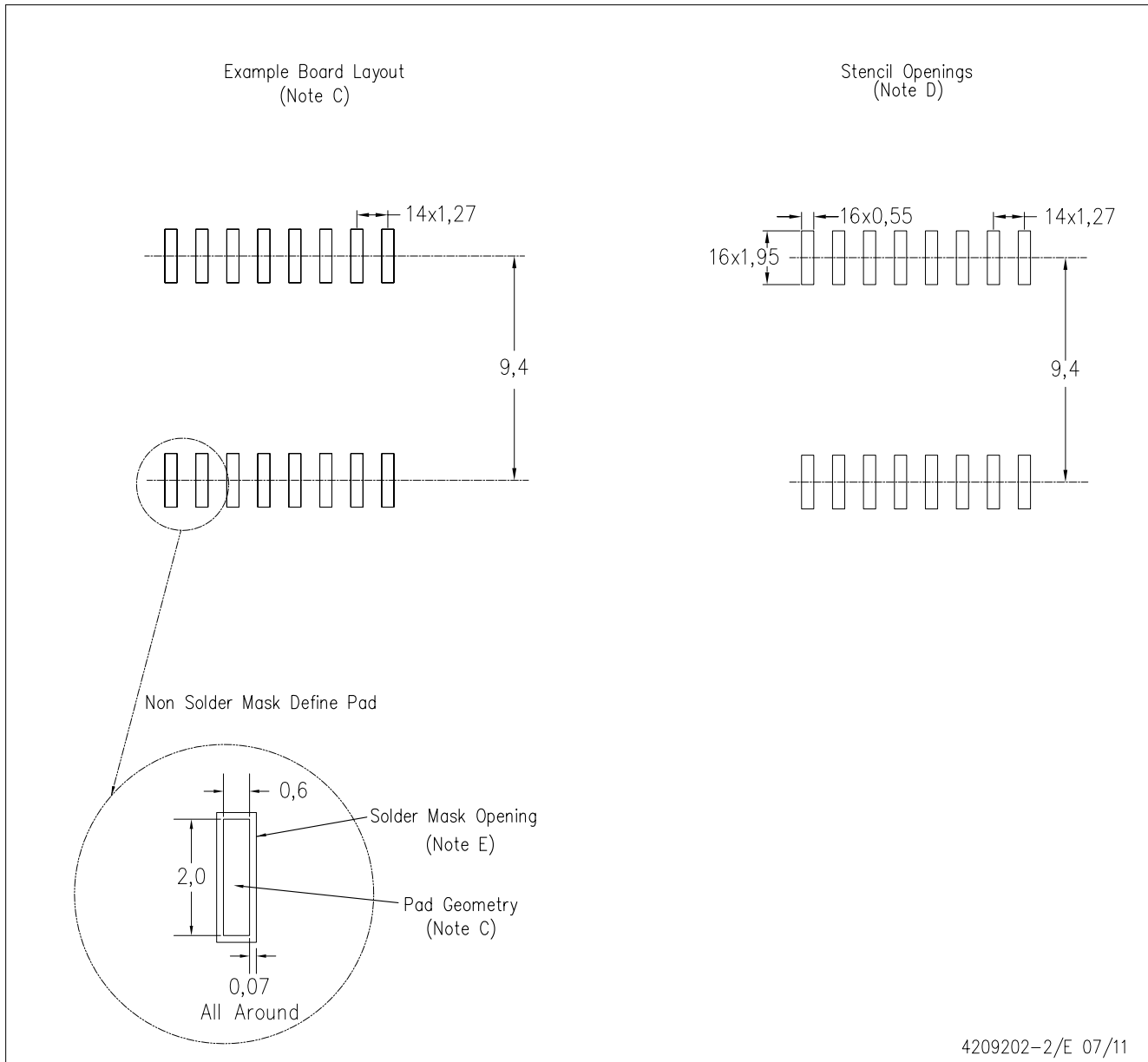
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AA.

DW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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