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Automatic Calibration of Micro-Architecture Description Models

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UT ECE

Outline

- Background
- Related Work
- Challenges and Solutions
- Automatic Calibration Flow
- Results and Conclusion
- Technology Transfer

Background

- **Increasing design complexities**
  - Rapid design space exploration for system prototyping
  - Instruction Set Simulator (ISS) is the key component
  - Fast generation of accurate performance models
- **Traditional approaches**
  - Open source ISSs: e.g. gem5, OVP, Simplescalar
  - Manually built processor models in C or C++
  - Inaccurate or too hard to explore new features
- **Automatic performance model generation**
  - Parameterize (micro-)architecture description models
  - Calibrate parameterized micro-architecture models against low level implementations

Related Work

- **Abstract performance model calibration**
  - On-line tuning of application performance prediction models [Augonnet09]
  - Analysis models without implementation details [Pimentel08, Haid09]

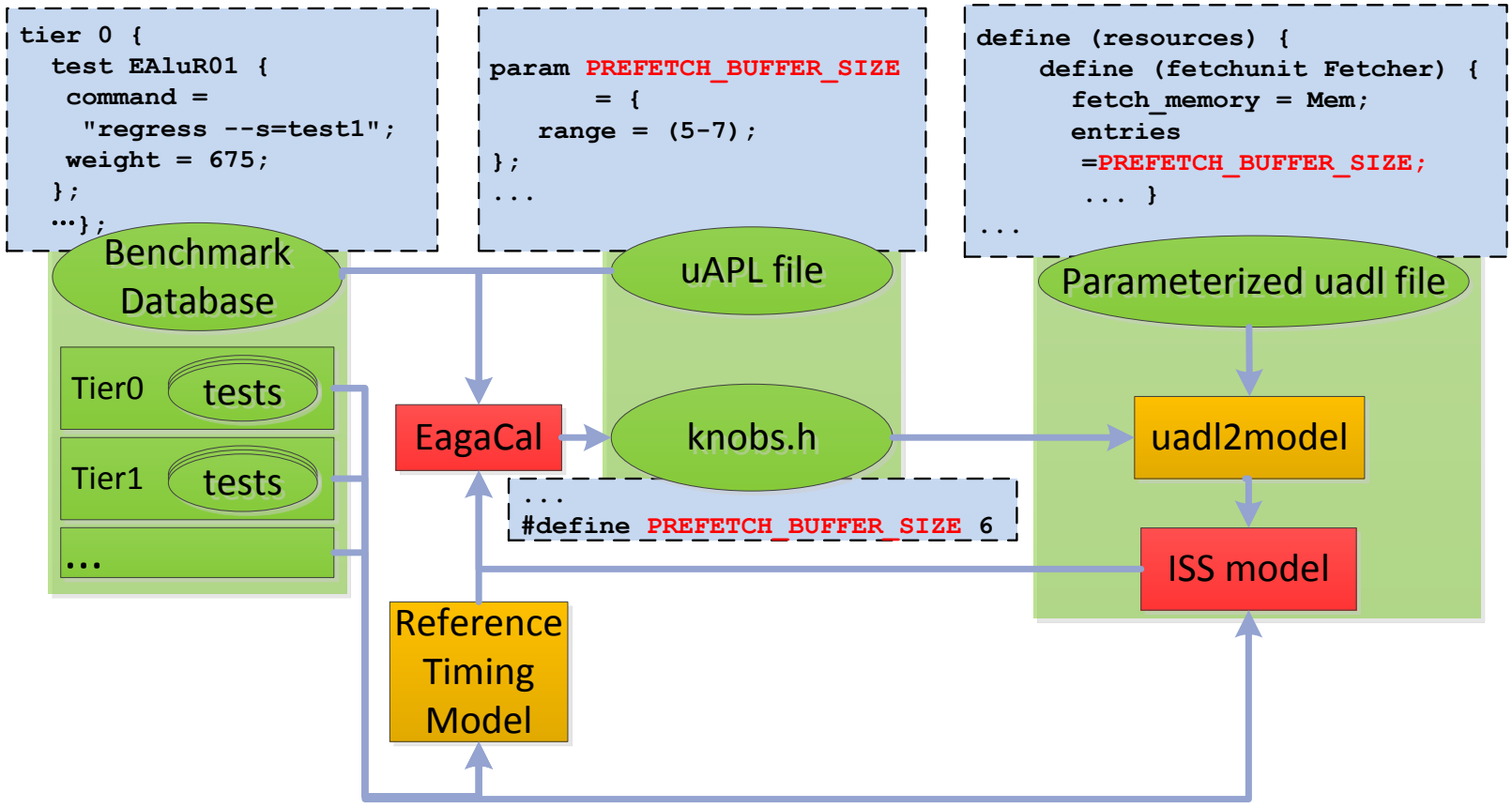
- **Architecture description languages (ADLs)**
  - Rapid prototyping of (micro-)architecture models [LISA, TARGET, nML]
  - Need tedious manual calibration to match RTL timing behaviors
  - Require automatic calibration of high-level description models against existing RTL

Challenges and Solutions

- **How to efficiently model micro-architecture performance?**
  - Easy to be parameterized for calibration
  - Reflect real structures which are tunable for further exploration
  - Freescale open source Architecture/Micro-architecture Description Language (ADL/uADL)
    - Decouple timing and functionality
    - Reconfigurable and reusable declarative definition blocks
- **How to speed up the search strategy?**
  - Reduce ISS instances evaluation time
  - Prune searching spaces by hierarchically calibrating various aspects of processor model
  - Evolutionary, iterative exploration across multi-tiered benchmark sets

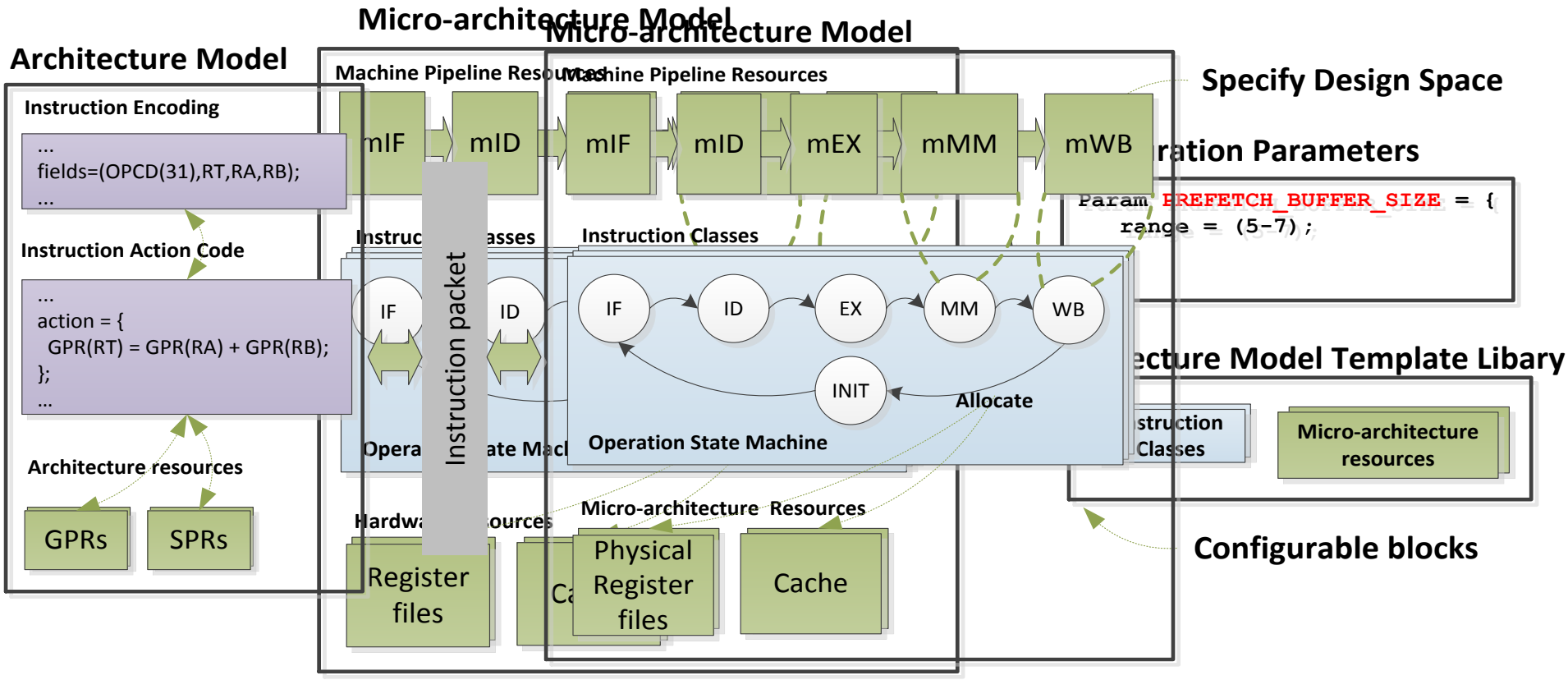
Calibration Infrastructure Overview

- **Evolutionary/Genetic Algorithm CALibration (EagaCal)**
  - Calibrate manually parameterized uADL model
  - Parameters specification in μArchitecture Parameterization Language (uAPL) file format
  - Multi-tiered benchmark set

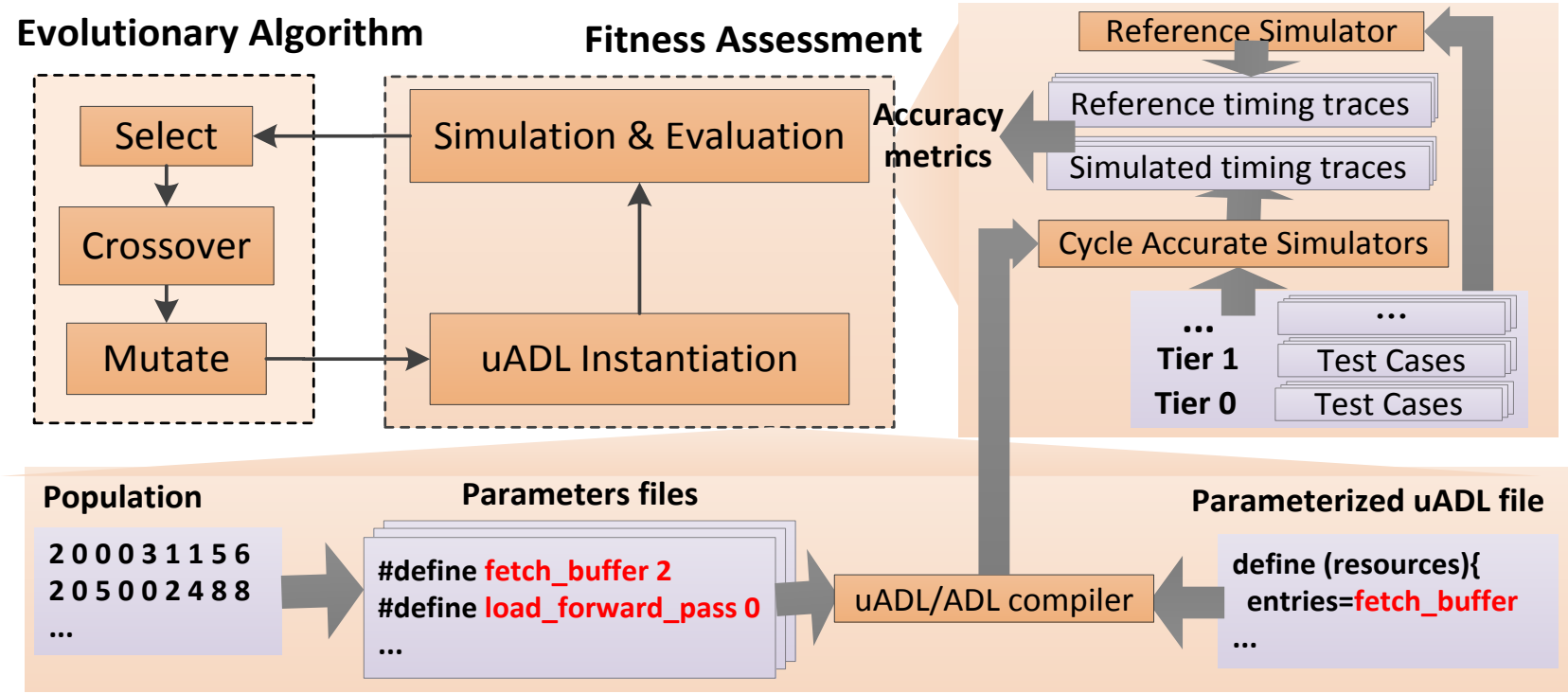


uADL Model Parameterization

- **uADL model characterization**
  - Separate behavior and resource blocks
  - Generate (micro-)architecture template model libraries
- **Specify search space by configuration parameters**



Evolutionary Calibration and Exploration



- **Iterative exploration across multi-tier benchmarks**
  - Encode parameterized micro-architecture knobs into genome
  - Micro-benchmarks with reference RTL traces for fitness assignment
  - Genetic algorithm to discover optimal set of uADL parameters

Successive Multi-Tiered Pruning

- **Multiple tiers of benchmarks**
  - Benchmark hierarchy with emphasis on different calibration aspects
  - Quickly prune design space by incrementally adding tiers instead of running whole set of benchmarks
  - Introduce a new tier when best individual is not improved for a consecutive generations
- **Fast fitness assessment of each candidate parameter set**

$$Accuracy = 1 - \frac{\sum_{i=1}^{n} W_i \times E_i}{\sum_{i=1}^{n} W_i}$$

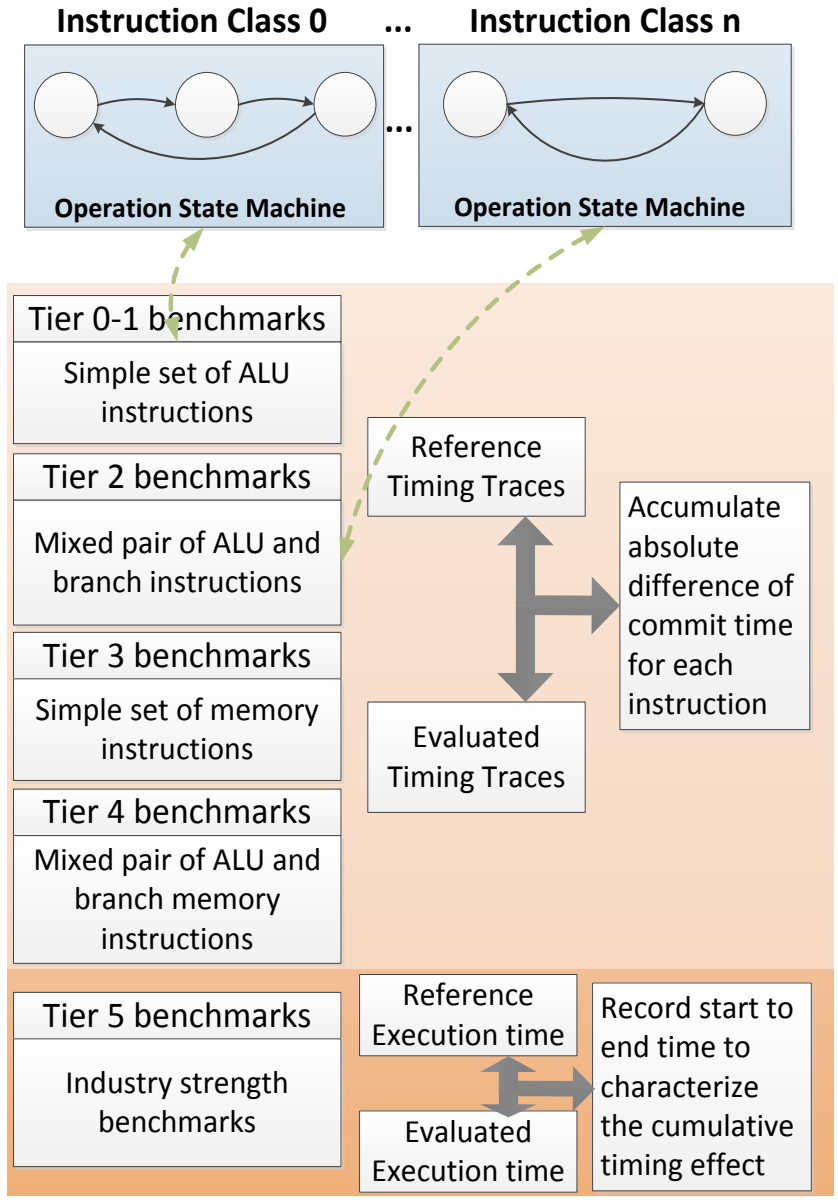
W_i: instruction count of *benchmark*$_i$
E_i: timing error of *benchmark*$_i$

For tier0 - tier4 :

$$E_i = \frac{\sum_{j=1}^{W_i} |t_j - t_j'|}{t_{W_i}'}$$

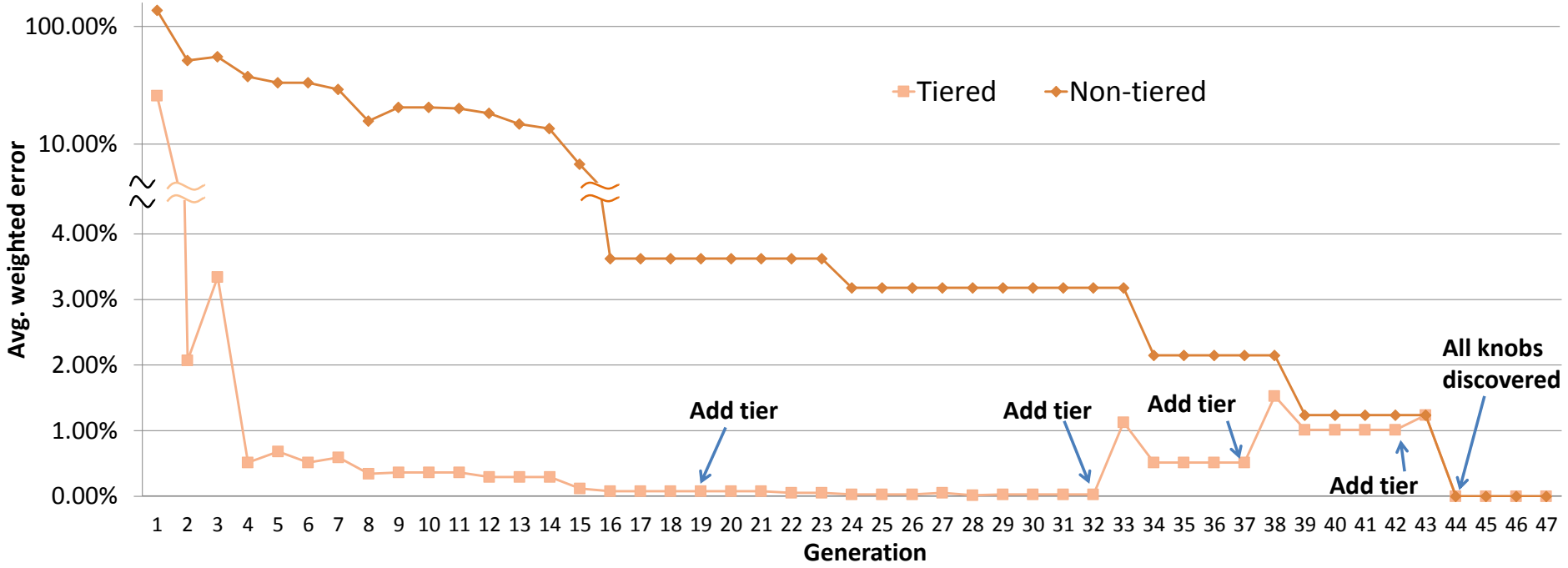
For tier5 :

$$E_i = \frac{|t_{W_i} - t_{W_i}'|}{t_{W_i}'}$$



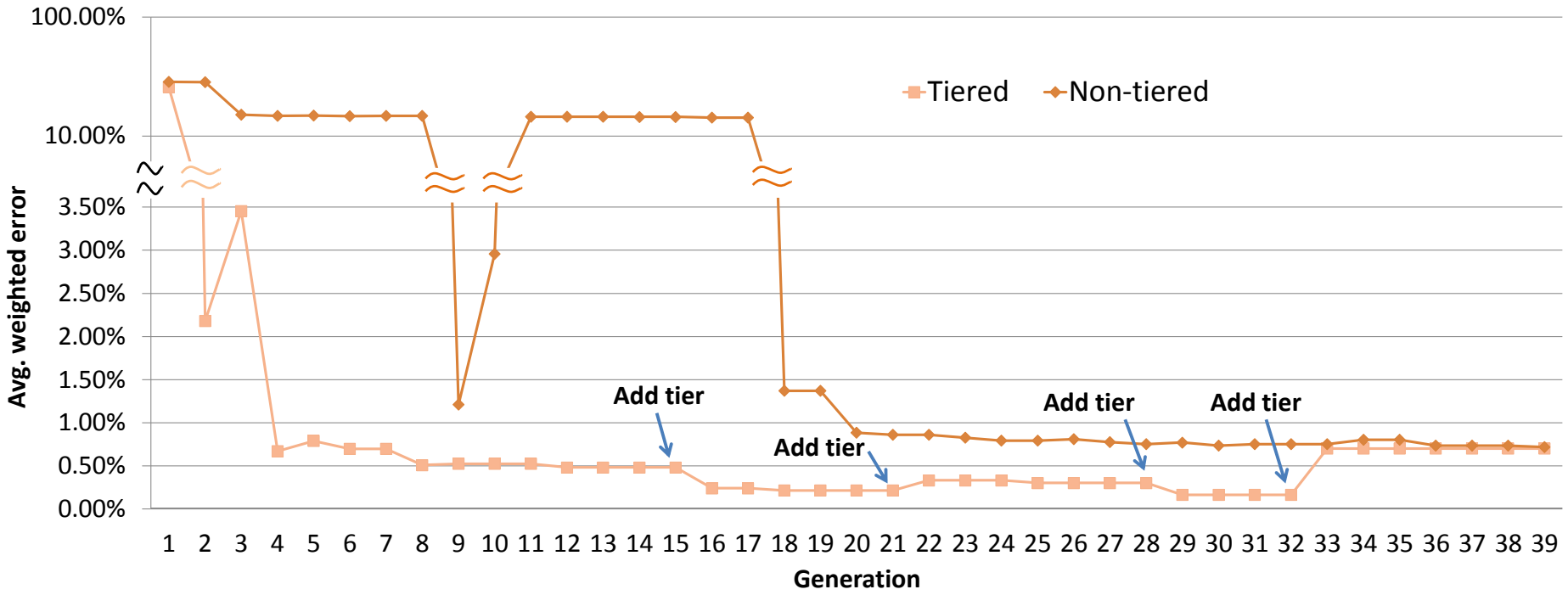
Calibration Results (1)

- **Automated calibration against reference ADL model**
  - uADL model for e200z0 PowerPC core
    - 14 parameters specified in uAPL file
    - 29 million possible candidates
  - Compare against timing traces generated from reference uADL model



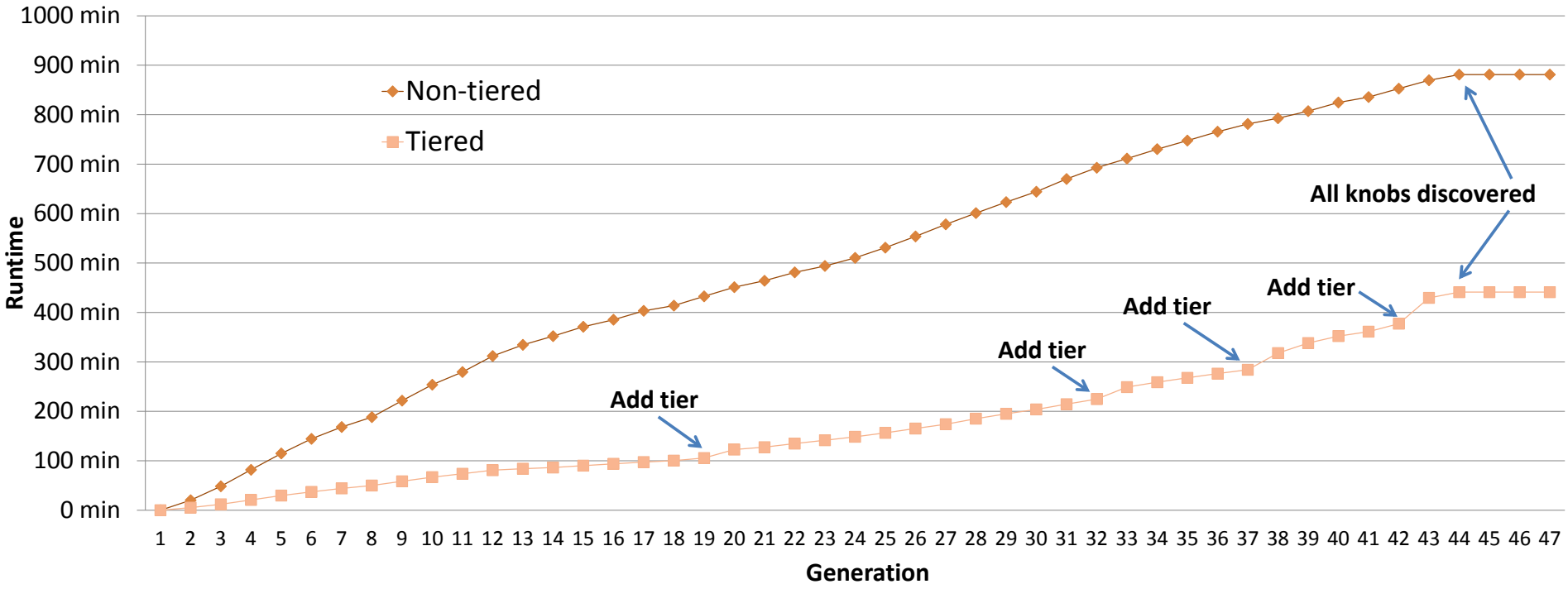
Calibration Results (2)

- **Automated calibration against RTL reference**
  - uADL model for e200z0 PowerPC core
  - Compare against RTL timing reference traces
    - >99% average accuracy across all benchmarks in 8-hour calibration



Calibration Results (3)

- **Calibration runtime**
  - Hierarchical benchmarks sets for evaluation and simulation
    - Add tier and re-evaluate when no more improvement of the population
  - Reduce calibration time by 46% compared to non-tiered approach



Summary & Conclusion

- **Automatically discover accurate processor models**
  - Architecture/Mcrio-architecutre Description Language (ADL/uADL)
    - Parameterized templates as a starting point
  - Calibrate high-level uADL models against existing RTL
    - Calibrate micro-architecture parameters in uADL template
- **Calibration results**
  - >99% average accuracy across all benchmarks in 8-hour calibration
- **Future work**
  - Calibrate more complicated and realistic processor models
  - Integrate other metrics into calibration framework (Power, thermal, reliability)
  - Automatic micro-architecture library characterization, classification and generation

Automatic micro-architecture model calibration framework

Technology Transfer

- **Automatic Platform Model Calibration and Tuning**
  - Task ID 2085.001
- **Reports and publications**
  - S. Chakravarty, A. Gerstlauer. “Performance and Power Modeling Case Study”, Report, Jan. 2011.
  - S. Chakravarty, A. Gerstlauer. “ADL Driven Back-Annotation and Simulation Methodology for Host Compiled Performance and Power Modeling”, Report, July 2011.
  - S. Chakravarty, A. Gerstlauer. “Host Compiled Performance and Power Modeling of Embedded Systems," SRC TECHCON, August 2011.
  - S. Chakravarty, A. Gerstlauer, “Automated, ADL-Driven Generation of Host-Compiled Platform Models,” Report, December 2012.
  - S. Chakravarty, Z. Zhao, A. Gerstlauer, “Automated, Retargetable Back-Annotation for Host-Compiled Power and Performance Modeling,” *CODES+ISSS*, Montreal, Canada, September 2013.
  - Z. Zhao, S. Chakravarty, A. Gerstlauer, “Automated, Retargetable Back-Annotation for Host-Compiled Performance and Power Modeling,” *SRC TECHCON*, Aug. 2013. ***(best in session)***
  - Z. Zhao, G. Morrison, A. Gerstlauer, “Automated ADL Model Calibration and Tuning,” Report, Dec. 2013.
- **Industrial interactions**
  - Leveraging Freescale’s open-source ADL technology
    - http://opensource.freescale.com/fsl-oss-projects/
  - Regular (bi-weekly) project discussions (Freescale, TI)
  - Internships at Freescale (6/2013-8/2013)
    - Automated discovery of ADL based cycle-accurate reference models