AC5715A Datasheet

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AC5715A Features

CPU Core

- Dual-core 32-bit CPU
- 32KB I-Cache
- 24KB D-Cache
- 96K On-chip SRAM
- The maximum operating frequency is 240MHz
- Peripherals can access external memory through cache
- Support IEEE-754 standard single-precision floating point

Interrupts

- 256 interrupt sources with 8 levels of programmable priority
- Support external I/O interrupt
- With soft interrupt (virtual interrupt) function, priority can be configured

Video Codec

- H.264 codec, encoding maximum support:
  - Single mode: 1920×1080@60fps
  - Dual mode: 1920×1080@30fps + 1280×720@30fps
- M-JPEG codec

Image Signal Processor

- Support maximum size: 2304×1296
- Support 8-bit / 10-bit / 12-bit RAW data
- Support 16-bit YUV / 24-bit RGB data
- Support RGBIR sensor
- Support AE / AWB
- Support WDR technology
- Support advanced color enhance
- Support 2D/3D noise reduction
- Support sharpness process
- Support video scaling and digital zoom
- Support video deinterlacing
- Support real time recording OSD
- Support true color logo OSD

Video input interface

- One MIPI CSI interface
  - Support 8-bit / 10-bit / 12-bit RAW data
  - Support 16-bit YUV / 24-bit RGB data
  - Support 1/2lane mode
  - Support DSI mode

Audio codec

- 2 PGA for MIC in
- 1 channels delta-sigma audio ADC with SNR > 85 dB
- 1 channels delta-sigma audio DAC with SNR > 95 dB
- Support 8/11.025/12/16/22.05/24/32/44.1/48KHz Sample Rate

Peripheral interface

- Peripheral pin select function
- Up to 22 programmable digital I/O pins
- Support 3 IO port wake-up MCU
- Support peripheral wake-up MCU
- 2 32-bit reloadable timers for timing / capture and PWM
- 1 SPI host controllers, support DMA
- 1 SDIO 2.0 interfaces, support DMA
- 2 I^2C controllers, support master and slave modes
- 1 UARTs, 2 of which support DMA loop buffer
- 4 channels motor PWM
- 1 high speed USB SIE, support HUB
- RTC, with alarm clock and time base to wake up the chip
- Support programable pipeline DMA copy
- Watchdog
- CRC check

Memory Interface

- DDRX controller, support DDR1
  - 16-bit data width
  - Support DDR1@200MHz
  - Maximum support 32×16Mbit
- 1 high-speed SPI flash interface
  - Support standard, dual and quad modes
  - Maximum support 16MB, 80MHz

Analog Peripheral Features

- 2 clock oscillation circuits
- One high speed USB 2.0 PHY
- 4 clock generators (PLLs), provide various system frequencies
- 5 channels 10-bit key general ADC
- 3 lanes MIPI CSI PHY
- 8-level low voltage detector
- Power-on reset

Package type

- AC5715A4: 16×16Mbit/DDR1
- QFN52(6mm×6mm)

1. Pin Defintion

1.1 Pin Assignment

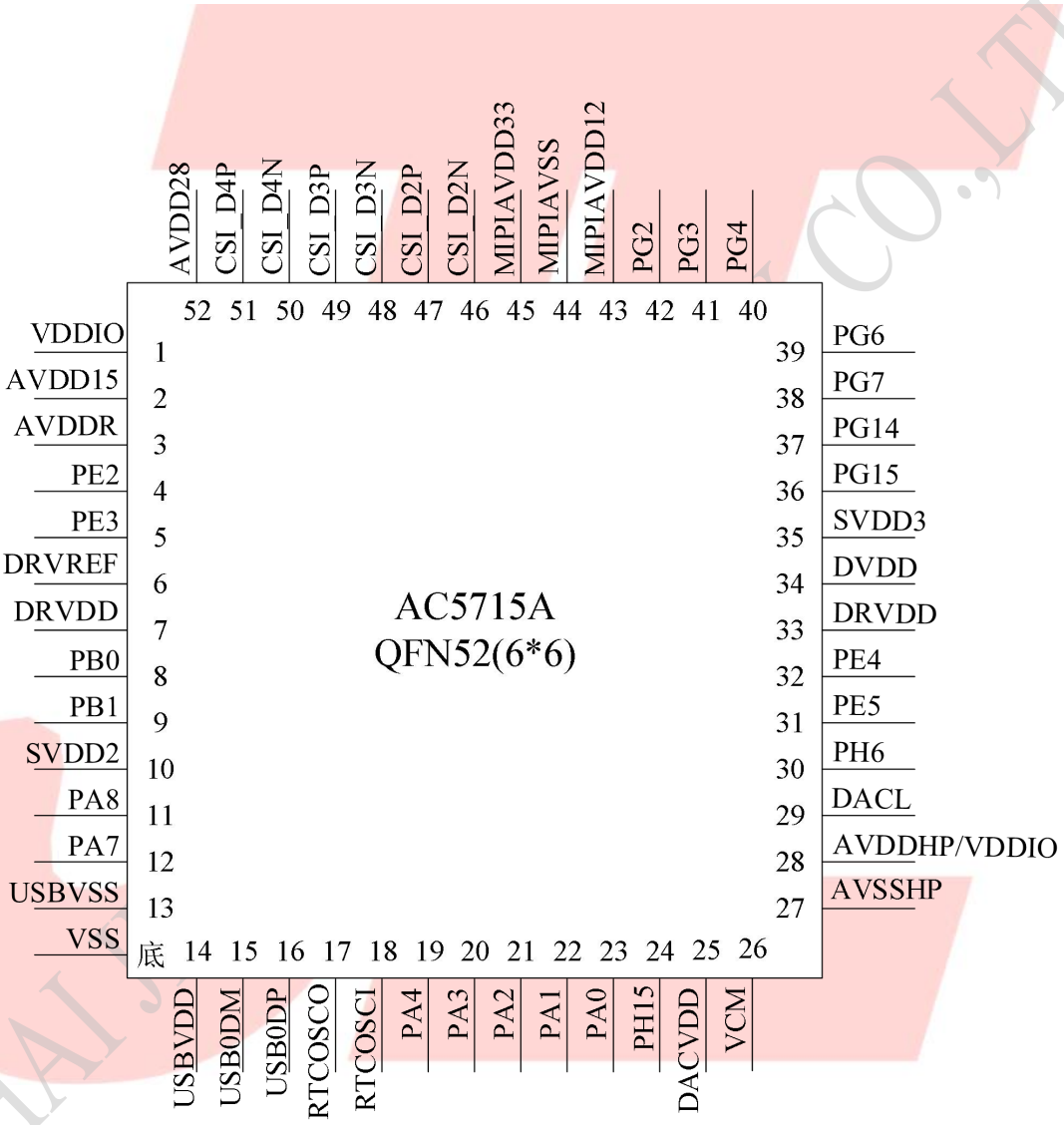


Figure 1-1 AC5715A_QFN52 Pin Assignment

★Note：SVDD2 is the power supply for IO(PB0, PB1, PA7, PA8)
SVDD3 is the power supply for IO(PG2-PG4, PG6, PG7, PG14, PG15)

1.2 Pin Description

Table 1-1 AC5715A_QFN52 Pin Description

No.	Name	I/O type	Function	Other Function
1	VDDIO	P	IO Power	——
2	AVDD15	P	AVDD15	——
3	AVDDR	P	Power	——
4	PE2	I/O	GPIO	VPP CLKOUT0: Clock Out0 PWM4: Timer4 PWM Output
5	PE3	I/O	GPIO	ADC5: ADC Input Channel 5
6	DRVREF	P	DDR REF	——
7	DRVDD	P	DDR Power	——
8	PB0	I/O	GPIO	ADC1: ADC Input Channel 1 IIC_SCL1_A: IIC SCLK(A)
9	PB1	I/O	GPIO	PWM0: Timer0 PWM Output IIC_SDA1_A: IIC Data1(A)
10	SVDD2	P	IO Power2	——
11	PA8	I/O	GPIO	UART0_RXA: UART0 Data In(A)
12	PA7	I/O	GPIO	UART0_TXA: UART0 Data Out(A)
13	USBVSS	P	USB Ground	——
14	USBVDD	P	USB Power	——
15	USB0DM	I/O	USB0DM	——
16	USB0DP	I/O	USB0DP	——
17	RTCOSCO	I/O	RTC OSCO	——
18	RTCOSCI	I/O	RTC OSCI	——
19	PA4	I/O	GPIO	SPI0_CLKA: SPI0 CLK(A) SD0_DAT0A: SD0 Data0(A)
20	PA3	I/O	GPIO	SPI0_DOA(0): SPI0 Data Out(A) SD0_DAT2A: SD0 Data2(A)
21	PA2	I/O	GPIO	SPI0_DAT2A(2): SPI0 Data2(A) SD0_CLKA: SD0 CLK(A) IIC_SCL1_B: IIC CLK(B) ADC0: ADC Input Channel 0
22	PA1	I/O	GPIO	SPI0_DIA(1): SPI0 Data In(A) SD0_CMDA: SD0 CMD(A) IIC_SDA1_B: IIC Data1(B)
23	PA0	I/O	GPIO	SPI0_CSA: SPI0 Chip Select(A)

No.	Name	I/O type	Function	Other Function
24	PH15	I/O	GPIO	SPI0_DAT3A(3): SPI0 Data3(A) SD0_DAT1A: SD0 Data1(A) CLKOUT2: Clock Out2 Wakeup15: Port Wakeup 15
25	DACVDD	P	DAC Power	——
26	VCM	P	VCM	——
27	AVSSHP	P	HP Ground	——
28	AVDDHP	P	HP Power	——
	VDDIO	P	IO Power	——
29	DACL	O	DAC Left Channel	——
30	PH6	I/O	GPIO	MICL: MIC Left
31	PE5	I/O	GPIO	ADC8: ADC Input Channel 8 IIC_SDA1_D: IIC1 Data(D) Wakeup11: Port Wakeup 11 MOTOR PWM_H4_B
32	PE4	I/O	GPIO	IIC_SCL1_D: IIC1 SCL(D) Wakeup10: Port Wakeup 10 MOTOR PWM_L4_B
33	DRVDD	P	DDR Power	——
34	DVDD	P	Core Power	——
35	SVDD3	P	IO Power3	——
36	PG15	I/O	GPIO	OSCO0 MOTOR PWM_H4_A
37	PG14	I/O	GPIO	OSCI0 MOTOR PWM_L4_A
38	PG7	I/O	GPIO	UART0_RXB: Uart0 Data In(B) ADC7: ADC Input Channel 7 IIC_SDA0_A: IIC0 Data(A)
39	PG6	I/O	GPIO	UART0_TXB: Uart0 Data Out(B) IIC_SCL0_A: IIC0 SCLK(A)
40	PG4	I/O	GPIO	SD0_DAT0C: SD0 Data0(C)
41	PG3	I/O	GPIO	SD0_CLKC: SD0 CLK(C)
42	PG2	I/O	GPIO	SD0_CMDC: SD0 CMD(C)
43	MIPIAVDD12	P	MIPI AVDD	——
44	MIPIAVSS	P	MIPI Ground	——
45	MIPIAVDD33	P	MIPI Power	——

No.	Name	I/O type	Function	Other Function
46	CSI_D2N	I	MIPI CSI Lane	MIPI CSI data(0/1) lane(P/N) MIPI CSI clock lane(P/N)
47	CSI_D2P	I	MIPI CSI Lane	MIPI CSI data(0/1) lane(P/N) MIPI CSI clock lane(P/N)
48	CSI_D3N	I	MIPI CSI Lane	MIPI CSI data(0/1) lane(P/N) MIPI CSI clock lane(P/N)
49	CSI_D3P	I	MIPI CSI Lane	MIPI CSI data(0/1) lane(P/N) MIPI CSI clock lane(P/N)
50	CSI_D4N	I	MIPI CSI Lane	MIPI CSI data(0/1) lane(P/N) MIPI CSI clock lane(P/N)
51	CSI_D4P	I	MIPI CSI Lane	MIPI CSI data(0/1) lane(P/N) MIPI CSI clock lane(P/N)
52	AVDD28	P	AVDD28	——

(★Note: 1. P----Power Supply 2. I----Input 3. I/O----Bi-direction)

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1

Symbol	Item	Range	Unit	Remarks
SVDD2/SVDD3	Special IO Logic Voltage	-0.3 to 3.6	V	---
VDDIO/USBVDD /MIPIAVDD33	Digital Voltage	-0.3 to 3.6	V	---
AVDDHP	Analog Voltage	-0.3 to 3.6	V	---
DVDD/MIPIAVDD12	Core Voltage	-0.3 to 1.3	V	---
DRVDD	DDR1 Voltage	-0.3 to 2.7	V	---
AVDDR	Digital Voltage	-0.3 to 3.3	V	---
V_{IO1}	Voltage applied on normal pin	-0.3 to VDDIO+0.3	V	Relative to ground
V_{IO2}	Voltage applied on special pin	-0.3 to SVDD2/3+0.3	V	Relative to ground
T_{OPE}	Operating Temperature	-40 to 85	℃	---
T_{STG}	Storage Temperature	-65 to 150	℃	---

2.2 Recommended Operating Conditions

Table 2-2

Symbol	Item	Min	Typ	Max	Unit
SVDD2/SVDD3	1.8V Logic Voltage	1.7	1.8	1.9	V
	3.3V Logic Voltage	3.0	3.3	3.6	V
VDDIO/USBVDD /MIPIAVDD33	Digital Voltage	3.0	3.3	3.6	V
AVDDHP	Analog Voltage	3.0	3.3	3.6	V
DVDD/MIPIAVDD12	Core Voltage	1.0	1.1	1.2	V
DRVDD	DDR1 Voltage	2.3	2.5	2.7	V
AVDDR	Digital Voltage	1.7	2.5	2.7	V

2.3 IO Input/Output Electrical Characteristics

Table 2-3

Input Characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input low (logic 0) voltage	-0.3	-	0.3* VDDIO	V	VDDIO = 3.3V
V_{IH}	Input high (logic 1) voltage	0.7* VDDIO	-	VDDIO+0.3	V	VDDIO = 3.3V
Output Characteristics						
V_{OL}	Output low (logic 0) voltage	-	-	0.1* VDDIO	V	VDDIO = 3.3V
V_{OH}	Output high (logic 1) voltage	0.9* VDDIO	-	-	V	VDDIO = 3.3V

2.4 IO Output Drive Strength Pull Up/Down Characteristics

Table 2-4

Port	Drive Strength	Pull Up Resistance	Pull Down Resistance	Note
PA0 - PA4 PA7, PA8 PB0, PB1 PE3, PE4, PE5 PG2 - PG4 PG6, PG7 PG14, PG15 PH6, PH15	Strong drive: 16mA / 21mA Weak drive: 2mA / 7mA	10K	10K	Test Conditions: VDDIO = 3.3V SVDD2 = 3.3V SVDD3 = 3.3V
PE2	7mA	10K	10K	---
USB_DP	10mA	1.5K	15K	Use as normal IO
USB_DM	10mA	---	15K	Use as normal IO

(★NOTE: precision of pull-up and pull-down resistor is ±20%)

2.5 LDO Characteristics

Table 2-5

Internal LDO	Output Voltage Range	Drive Stength	Test Conditions
AVDD15	1.3V-2.0V	~50 mA	AVDDR=2.5V
AVDD28	2.5V-3.2V	~100 mA	VDDIO=3.3V

2.6 Audio DAC Characteristics

Table 2-6

Symbol	Parameters	Min	Typ	Max	Unit	Test Conditions
SNR	Signal to Noise Ratio	-	95	-	dB	1KHz, SR=44.1K, Mute File, CR=192Kbps
THD+N	Total Harmonic Distortion + Noise	-	-73	-	dB	(-1.5dB) 1KHz, SR=44.1K, CR=192Kbps

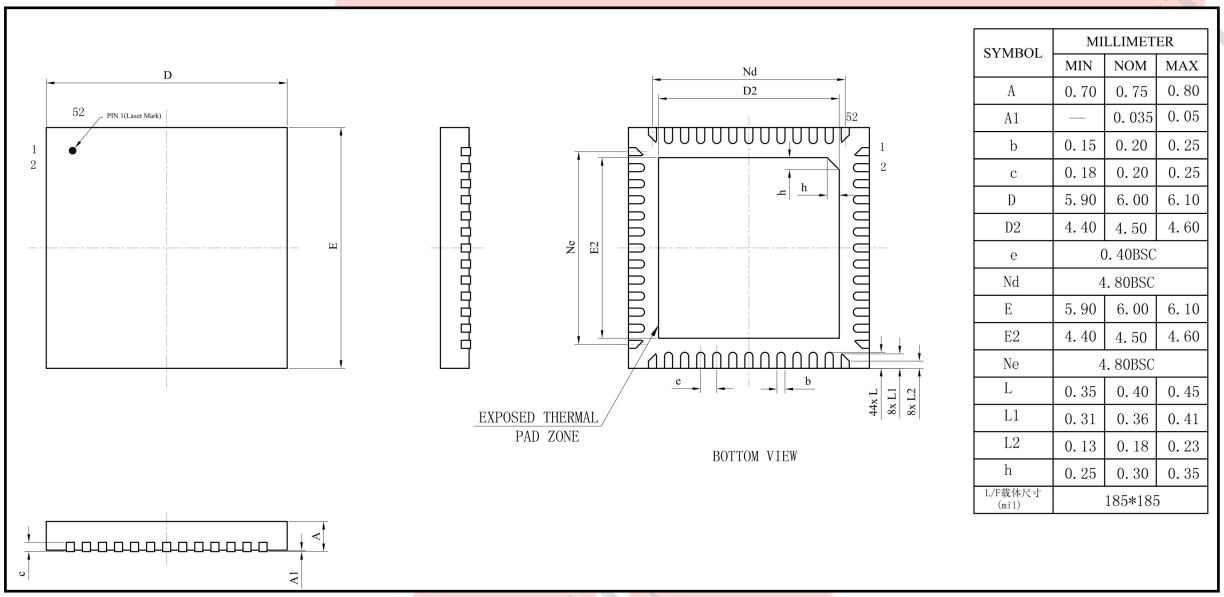
2.7 Audio ADC Characteristics

Table 2-7

Symbol	Parameters	Min	Typ	Max	Unit	Test Conditions
SNR	Signal to Noise Ratio	-	85	-	dB	1KHz, SR=44.1K, Mute File, CR=192Kbps
THD+N	Total Harmonic Distortion + Noise	-	-75	-	dB	(-1.5dB) 1KHz, SR=44.1K, CR=192Kbps

3. Package

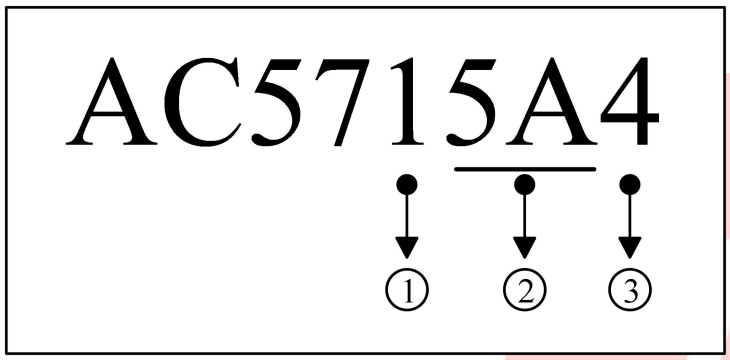
3.1 QFN_52PIN Package Diagram



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.035	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	5.90	6.00	6.10
D2	4.40	4.50	4.60
e	0.40BSC		
Nd	4.80BSC		
E	5.90	6.00	6.10
E2	4.40	4.50	4.60
Ne	4.80BSC		
L	0.35	0.40	0.45
L1	0.31	0.36	0.41
L2	0.13	0.18	0.23
h	0.25	0.30	0.35
L/F载体尺寸 (mil)	185*185		

Figure 3-1 AC5715A_QFN52 Package Diagram

4. Package Type Specification



① 0 represents DDR2 and 1 represents DDR1

② Different numbers and letters represent different packages

③ Represents the sdram size of the chip, 8 represents 512M, 4 represents 256M, 2 represents 128M and 1 represents 64M.

5. Version Information

Date	Version Number	Description
2023.02.13	V1.0	Initial draft