Operational Amplifier Design

EE618 Course Project

IIT Bombay

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- In this project you will design an Op-Amp inspired from TI OPA344/345.
- Reference for the Op-Amp internal circuit configuration: OPA344/345 data sheet uploaded on Moodle with highlights, also available from TI website: **DATA SHEET**
- Use PTM 180nm CMOS technology model file. V_{dd}= 1.8 V, V_{ss}= 0 V. PTM model file: Here
- Notice: Use the following relations (λ: Grid size = 90 nm).
  1. AS = 4λ×W (for single-finger transistor)
  2. PD = PS = 2× (4λ + W) (for single-finger transistor)
  3. AD = 2λ×W (for multi-finger transistor)
  4. PD = PS = 4λ + W (for multi-finger transistor)
- Maximum transistor length in the design should not be more than 2µm.
- In case, the transistor bulk connection is not mentioned: Bulk of NMOS transistor should be connected to VSS. Bulk of the PMOS transistor should be connected to the source of same transistor.
- **Note**: NGSPICE netlist for Op-amp is provided to you on Page 6 of this Project PDF. You can modify the template for your design. You have to mention the work contribution from each member of your group at the end of your report. The template for which is given on Page 5.

TARGET REQUIREMENTS AND SPECIFICATION

Note: This are different from data sheet specifications.

- Single ended output.
- Open loop small signal low-frequency voltage gain > 100 dB
- Unity gain bandwidth > 10 MHz
- Input CM voltage range: 100 mV to 1.7 V.
- Output voltage range: 100 mV to 1.7 V.
- Phase margin > 60º (Load capacitance = 5 pF).
- Slew rate > 2 V/µs (Load capacitance = 5 pF).

Parameters

1	$\lambda_n = 0.05V^{-1}$	4	$\lambda_p = 0.1V^{-1}$
2	$k_n = 300\ \mu A/V$	5	$k_p = 65\ \mu A/V^2$
3	$V_{tn} = 0.3999V$	6	$V_p = 0.42\ V$

Op-amp Architecture

The purpose of this course project is to design a rail-to-rail, two folded cascode stages Op-amp with Class-AB output stage

Circuit diagram (.PNG) is here

Xcircuit file (.ps) is here

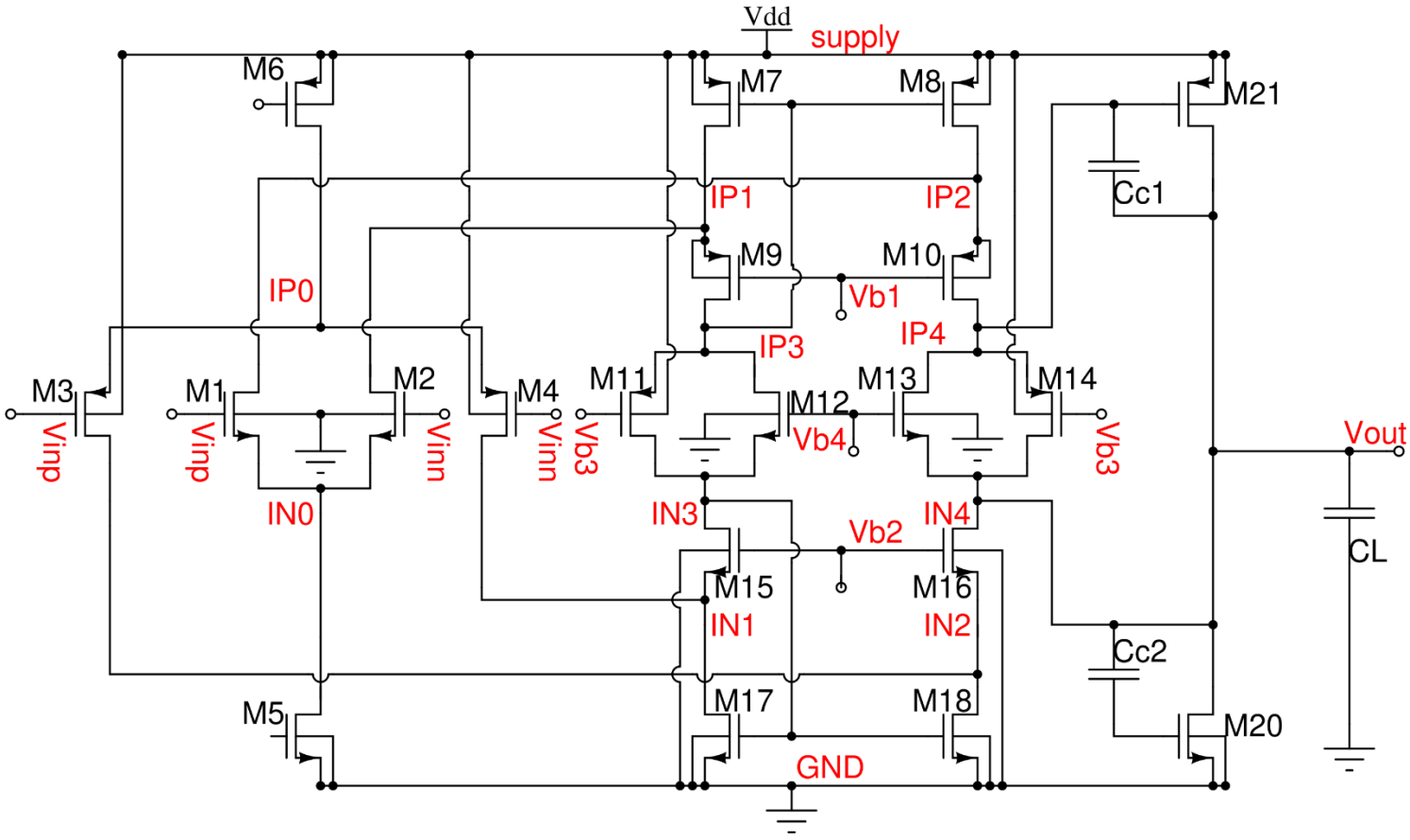


Figure 1: Two stage rail-to-rail folded cascode Op-amp with Class AB output stage

1- Op-amp Design flow

1.1 Report the design flow of the op-amp in the form of step by step procedure. Design flow involves determining bias currents, voltages and size of transistors compatible with section 2 of this project using the information from Assignment 2.

Step 1 Find the I_{bias} from slew rate.

$$\frac{dV_{out}}{dt} = \frac{I_{bias}}{C_L} > 2\ \frac{V}{\mu S}$$

$$\frac{I_{bias}}{5 \times 10^{-12}} > 2\ \frac{V}{\mu S}$$

$$I_{bias} > 10\ \times 10^{-6} A$$

$$\boldsymbol{I_{bias} = 60\ \times 10^{-6}\ A}$$

Step 2 Find the maximum output current I_{oss}

$$I_{oss} \geq\ I_{bias}\left(1 + \frac{C_L}{C_c}\right)$$

$$\boldsymbol{\therefore I_{oss} = 150\ \times 10^{-6}\ A}$$

Step 3 From unity gain bandwidth find minimum g_{m1}.

$$f_u = \frac{g_{m1}}{2\ \times \pi \times C_c}$$

$$f_u > 10\ MHz$$

$$g_{m1}\ > 2\ \times \pi \times C_c \times 10\ MHz$$

$$g_{m1}\ >\ 251 \times 10^{-6}\ S$$

Step 4 Frequency of non-dominant pole

$$f_{ND} =\ f_u\ \times \sqrt{3}$$

$$f_{ND} =\ \frac{g_{m19}}{2 \times \pi \times C_L}$$

$$\frac{g_{m19}}{2 \times \pi \times C_L} = \frac{g_{m1}}{2\ \times \pi \times C_c} \times\ \sqrt{3}$$

$$\therefore\ g_{m19} = \frac{g_{m1} \times C_L}{C_c} \times\ \sqrt{3}$$

$$\therefore\ |V_{dsatp19}| =\ \frac{I_{19} \times 2}{g_{m19}}$$

Step 5 Assuming $|V_{dsatp19}| = |V_{dsatp10}|$

$$g_{m10} = \frac{2 \times I_{10}}{V_{dsatp19}} = \sqrt{3} \times \frac{g_{m1} \times I_{10} \times C_L}{I_{19} \times C_c}$$

Step 6 Required gain $A_v\ > 100\ dB$

$$A_v =\ A_{v1} \times A_{v2}$$

$$A_{v1} =\ -g_{m1} \times [g_{m10}\ \times\ r_{010} \times (r_{08}||r_{01})]$$

$$A_{v2} =\ -g_{m19} \times (r_{019}||r_{020})$$

Step 7 Find the gain

A_v, A_{v1}, A_{v2}

$\lambda_n = 0.05V^{-1}\ ;\ \lambda_p = 0.1V^{-1}$

$I_{bias} = 60 \times 10^{-6}\ A\ ;\ I_1 =\ I_2 =\ 30 \times 10^{-6}\ A;\ I_7 =\ I_8 =\ 60 \times 10^{-6}\ A;$

$I_9 =\ I_{10} =\ 30 \times 10^{-6}\ A;\ I_{19} =\ I_{20} =\ 150 \times 10^{-6}\ A;$

$$r_{01} =\ r_{02} = \frac{1}{\lambda_n \times I_1} = 667\ k\Omega$$

$$r_{08} =\ r_{07} = \frac{1}{\lambda_p \times I_8} = 167\ k\Omega$$

$$r_{010} =\ r_{09} = \frac{1}{\lambda_p \times I_{10}} = 334\ k\Omega$$

$$r_{019} = \frac{1}{\lambda_p \times I_{19}} = 69\ k\Omega$$

$$r_{020} = \frac{1}{\lambda_n \times I_{20}} = 134\ k\Omega$$

$$\therefore\ A_{v1} = -g_{m1} \times [g_{m10}\ \times\ r_{010} \times (r_{08}||r_{01})]$$

But $g_{m10} = \sqrt{3} \times \frac{g_{m1} \times I_{10} \times C_L}{I_{19} \times C_c}$

$$\therefore\ A_{v1} = -g_{m1} \times \left[\sqrt{3} \times \frac{g_{m1} \times I_{10} \times C_L}{I_{19} \times C_c}\ \times\ r_{010} \times (r_{08}||r_{01})\right]$$

$$A_{v1} = -g_{m1}^2 \times 1.9379 \times 10^{10}$$

$$A_{v2} = -g_{m19} \times (r_{019}||r_{020})$$

But $g_{m19} = \frac{g_{m1} \times C_L}{C_c} \times \sqrt{3}$

$$\therefore A_{v2} = -\frac{g_{m1} \times C_L}{C_c} \times \sqrt{3} \times (r_{019}||r_{020})$$

$$\therefore A_{v2} = -97.4278 \times 10^3 \times g_{m1}$$

$$\therefore A_v = 1.888 \times 10^{15} \times g_{m1}^3$$

But $A_v > 100\ dB = 100000$

$$\therefore \sqrt[3]{\frac{100000}{1.888 \times 10^{15}}} < g_{m1}$$

$$\therefore \mathbf{375.54 \times 10^{-6} S < g_{m1}}$$

Step 8 Finding the g_{m1} value

Let choose the $|V_{dsatp19}| = 0.25\ or\ 3V$

$$|V_{dsatp19}| = \frac{I_{19} \times 2}{g_{m19}} = \frac{I_{19} \times 2}{\frac{g_{m1} \times C_L}{C_c} \times \sqrt{3}}$$

For $|V_{dsatp19}| = \mathbf{0.3V}$

$g_{m1} = 460 \times 10^{-6}\ S$

$g_{m19} = g_{m20} = \frac{g_{m1} \times C_L}{C_c} \times \sqrt{3} = 996 \times 10^{-6}\ S$

$f_{ND} = \frac{g_{m19}}{2 \times \pi \times C_L} = 31.70 \times 10^6 Hz$

$f_u = \frac{g_{m1}}{2\ \times \pi \times C_c} = 18.30 \times 10^6 Hz$

$PM = 180° - 90° - tan^{-1}\left[\frac{w_u}{w_{ND}}\right] > 60°$

For $|V_{dsatp19}| = \mathbf{0.25V}$

$g_{m1} = 555 \times 10^{-6}\ S$

$g_{m19} = g_{m20} = \frac{g_{m1} \times C_L}{C_c} \times \sqrt{3} = 1.2 \times 10^{-3}\ S$

$f_{ND} = \frac{g_{m19}}{2 \times \pi \times C_L} = 38.197 \times 10^6 Hz$

$f_u = \frac{g_{m1}}{2\ \times \pi \times C_c} = 22.08 \times 10^6 Hz$

$PM = 180° - 90° - tan^{-1}\left[\frac{w_u}{w_{ND}}\right] = 59.96° < 60°$

$$\therefore \mathbf{g_{m1} = 460 \times 10^{-6}}$$

$$\therefore \mathbf{A_{v1} = -4100}$$

$$\therefore \mathbf{A_{v2} = -42.81}$$

$$\therefore \mathbf{A_v = 183748.8308 = 105.28dB}$$

Step 9 Find required g_m values to calculate W/L ratio

$$g_{m19} = g_{m20} = \frac{g_{m1} \times C_L}{C_c} \times \sqrt{3} = \sqrt{3}\ \times \frac{460 \times 10^{-6} \times 5}{4} = 996 \times 10^{-6}\ S$$

$$\therefore f_u = \frac{460 \times 10^{-6}}{2\ \times \pi \times 4 \times 10^{-12}}$$

$$\therefore \mathbf{f_u = 18.30 \times 10^6\ Hz}$$

$$\therefore f_{ND} = \frac{996 \times 10^{-6}}{2 \times \pi \times 5 \times 10^{-12}}$$

$$\therefore \mathbf{f_{ND} = 31.70 \times 10^6\ Hz}$$

Step 10 Calculate V_{dsat} and $\frac{W}{L}$ of all transistors.

$$|V_{dsatp19}| = \frac{I_{19} \times 2}{g_{m19}} = \frac{150 \times 10^{-6} \times 2}{996 \times 10^{-6}} \cong 0.3V$$

$$\therefore |V_{dsatp19}| = |V_{dsatn20}| = 0.3V$$

Assuming, $|V_{dsatp11}| = |V_{dsatn14}| = 0.3$ and $I_{11} = I_{14} = 30 \times 10^{-6}A$

$$\therefore g_{m11} = \frac{2 \times I_{11}}{V_{dsatp11}} = 200 \times 10^{-6}S$$

$$\left(\frac{W}{L}\right)_{11} = \left(\frac{W}{L}\right)_{14} = \frac{g_{m11}^2}{2 \times I_{11} \times k_p} = \frac{(200 \times 10^{-6})^2}{2 \times 30 \times 10^{-6} \times k_p} = \frac{10.25}{1}$$

$$\left(\frac{W}{L}\right)_{12} = \left(\frac{W}{L}\right)_{13} = \left(\frac{W}{L}\right)_{11} \times \frac{k_p}{k_n} = \frac{2.22}{1}$$

$$V_{dsatn12} = V_{dsatn13} = \sqrt{\frac{2 \times I_{12}}{k_n \times \left(\frac{W}{L}\right)_{12}}} = 0.3V$$

Assuming, $|V_{dsatp10}| = |V_{dsatn9}| = 0.3$ and $I_{10} = I_9 = 30 \times 10^{-6}A$

$$\therefore g_{m10} = g_{m9} = \frac{2 \times I_{10}}{V_{dsatp10}} = 200 \times 10^{-6}S$$

$$\left(\frac{W}{L}\right)_{10} = \left(\frac{W}{L}\right)_{9} = \frac{g_{m10}^2}{2 \times I_{10} \times k_p} = \frac{(200 \times 10^{-6})^2}{2 \times 30 \times 10^{-6} \times k_p} = \frac{10.25}{1}$$

Assuming, $|V_{dsatp8}| = |V_{dsatn7}| = 0.3$ and $I_8 = I_7 = 60 \times 10^{-6}A$

$$\therefore g_{m8} = g_{m7} = \frac{2 \times I_8}{V_{dsatp8}} = 400 \times 10^{-6}S$$

$$\left(\frac{W}{L}\right)_{8} = \left(\frac{W}{L}\right)_{7} = \frac{g_{m8}^2}{2 \times I_8 \times k_p} = \frac{(400 \times 10^{-6})^2}{2 \times 60 \times 10^{-6} \times k_p} = \frac{20.51}{1}$$

$$\left(\frac{W}{L}\right)_{18} = \left(\frac{W}{L}\right)_{17} = \left(\frac{W}{L}\right)_{8} \times \frac{k_p}{k_n} = \frac{4.5}{1}$$

$$I_{18} = I_{17} = 60 \times 10^{-6}A$$

$$V_{dsatn17} = V_{dsatn18} = \sqrt{\frac{2 \times I_{17}}{k_n \times \left(\frac{W}{L}\right)_{17}}} = 0.3V$$

$$\left(\frac{W}{L}\right)_{1} = \left(\frac{W}{L}\right)_{2} = \frac{g_{m1}^2}{2 \times I_1 \times k_n} = \frac{(460 \times 10^{-6})^2}{2 \times 30 \times 10^{-6} \times k_n} = \frac{11.75}{1}$$

$$V_{dsatn1} = V_{dsatn2} = \sqrt{\frac{2 \times I_1}{k_n \times \left(\frac{W}{L}\right)_{1}}} = 0.13V$$

$$\left(\frac{W}{L}\right)_{3} = \left(\frac{W}{L}\right)_{4} = \left(\frac{W}{L}\right)_{1} \times \frac{k_n}{k_p} = \frac{54.23}{1}$$

$$V_{dsatp3} = V_{dsatp4} = \sqrt{\frac{2 \times I_3}{k_p \times \left(\frac{W}{L}\right)_{3}}} = 0.13V$$

$I_5 = I_6 = 60 \times 10^{-6} A$; $V_{dsatn5} = V_{dsatn6} = 0.3V$

$$\left(\frac{W}{L}\right)_5 = \frac{2 \times I_5}{k_n \times {V_{dsatn5}}^2} = \frac{4.5}{1}$$

$$\left(\frac{W}{L}\right)_6 = \frac{2 \times I_6}{k_p \times {V_{dsatn6}}^2} = \frac{20.51}{1}$$

$$\left(\frac{W}{L}\right)_{15} = \left(\frac{W}{L}\right)_{16} = \left(\frac{W}{L}\right)_{10} \times \frac{k_p}{k_n} = \frac{2.22}{1}$$

$$V_{dsatn15} = V_{dsatn16} = \sqrt{\frac{2 \times I_{15}}{k_n \times \left(\frac{W}{L}\right)_{15}}} = 0.3V$$

$$\left(\frac{W}{L}\right)_{19} = \frac{g_{m19}^2}{2 \times I_{19} \times k_p} = \frac{(996 \times 10^{-6})^2}{2 \times 150 \times 10^{-6} \times k_p} = \frac{50.87}{1}$$

$$\left(\frac{W}{L}\right)_{20} = \left(\frac{W}{L}\right)_{19} \times \frac{k_p}{k_n} = \frac{11.02}{1}$$

$$V_{dsatp19} = \sqrt{\frac{2 \times I_{19}}{k_p \times \left(\frac{W}{L}\right)_{19}}} = 0.3V$$

$$V_{dsatn20} = \sqrt{\frac{2 \times I_{20}}{k_n \times \left(\frac{W}{L}\right)_{20}}} = 0.3V$$

Step 11 Calculation of biasing voltages

$V_{bp} = V_{dd} - V_{dsatp6} - |V_{Tp}|$

$\therefore V_{bp} = 1.8 - 0.2956 - 0.42 = 1.085V$

$V_{bn} = V_{dsatn5} - V_{Tn} = 0.6971V$

$V_{b1} = V_{dd} - |V_{dsatp7}| - |V_{dsatp7}| - |V_{Tp}| \cong 0.78$

$V_{b2} = V_{dsatn15} + V_{dsatn17} + V_{Tn} = 0.9799$

Calculation for V_{b3}

$V_{s11} = 1.2V$; $V_{d11} = 0.6V$

$\therefore 1.2 - 0.6 = 1.2 - V_{b3} - 0.42$

$V_{b3} = 0.18V$

Calculation for V_{b4}

$V_{b4} = V_{dsatn12} + V_{dsatn15} + V_{dsatn17} + V_{Tn} = 1.2628V$

1.2 Write size of transistors in a table.
Conclusion of above calculation and simulation values

Transistor	V_{dsat} (V)	I_D (μA)		g_m (μS)		W/L	
		Calc.	Sim.	Calc.	Sim.	Calc.	Sim.
1	0.13	30	18.18	460	262.66	11.75	12
2	0.13	30	18.18	460	262.66	11.75	12
3	0.13	30	16.97	460	287	54.23	54
4	0.13	30	16.97	460	287	54.23	54
5	0.3	60	36.37	400	246	4.5	4.5
6	0.3	60	33.96	400	254	20.51	21
7	0.3	60	37.74	400	266	20.51	21
8	0.3	60	37.74	400	266	20.51	21
9	0.3	30	19.56	200	141.9	10.25	11
10	0.3	30	19.56	200	141.9	10.25	11
11	0.3	30	19.21	300	138	10.25	11
12	0.3	30	34.36	300	7.50	2.22	2.5
13	0.3	30	34.36	300	7.50	2.22	2.5
14	0.3	30	19.21	300	138	10.25	11
15	0.3	30	19.56	200	135	2.22	2.5
16	0.3	30	19.56	200	135	2.22	2.5
17	0.3	60	36.54	400	231	4.5	4.5
18	0.3	60	36.54	400	231	4.5	4.5
19	0.3	150	98.59	996	698	50.87	51
20	0.3	150	98.59	996	656	11.02	11

Biasing Voltages	Calculated (V)	Observed in Simulation
V_{bp}	1.085	1.091
V_{bn}	0.6971	0.6917
V_{b1}	0.78	0.7875
V_{b2}	0.9799	0.984
V_{b3}	0.18	0.186
V_{b4}	1.2628	0.1279

Observation: While simulating OPAMP circuit. We came to know that the constant parameter taken as constants are changing in simulation environment. The calculations of W/L is approximated as few of the other parameters like body bias effect and channel length modulation were ignored during hand calculation. Therefore, we are getting output as per specified requirements of Unity gain bandwidth, Phase margin, gain and slew rate. But the current and overdrive voltage are deviated from their actual values due to change in constant parameters. Because of this transconductance is also changed in simulation environment.

1.3 The design procedure may not succeed in one step. So simply show how you repeated the design to finally achieve the target specifications.

As mention in above in observation, Calculated Values not matching with simulation.
So, the calculation done few times to get close to required output with minimum deviation

1. Iteration is done for different I_{bias} like 30 μA, 40 μA, and 60 μA. From this we calculated g_m values which suitable for unity gain bandwidth, frequency of 1st non-dominant pole.
2. After assuming each branch currents. Iteration is done for different overdrive voltages like 0.2V, 0.25V, 0.3V. These voltages are assumed for some transistors and rest overdrive calculated. From Overdrive voltages W/L and g_m for all transistors calculated.
3. We faced a problem while calculating Biasing voltage. Specifically, V_{b3} and V_{b4} . As we mention considered constant parameters are deviating their mention values. In the circuit 0.01V change in biasing voltages caused significant changes in current, gain and phase margin. It was difficult to set this biasing voltage as small changes in their voltages showing resulted in undesired simulation output.

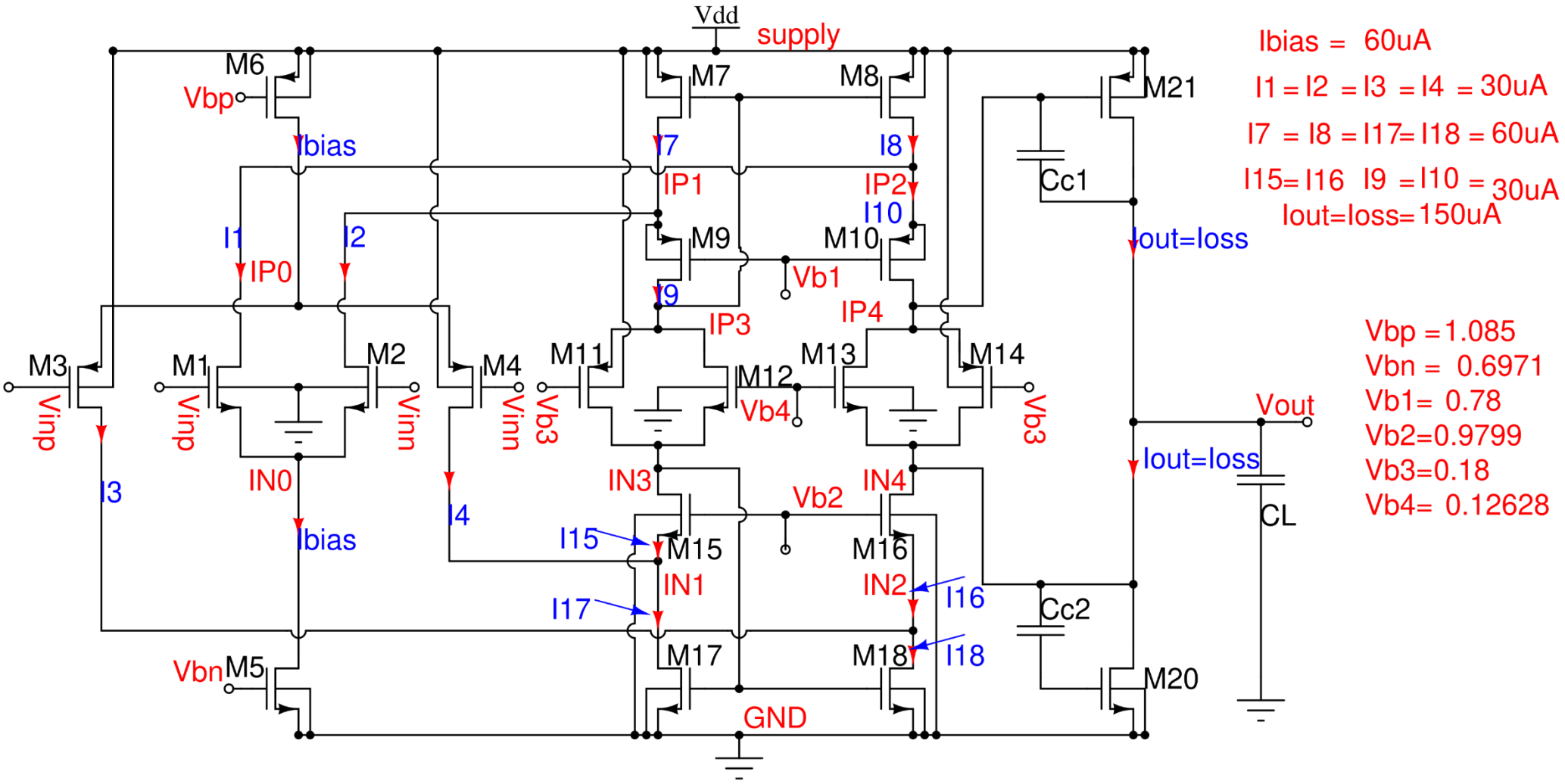
Design Procedure:

- Find the minimum current for bias current and output current.
- Determine minimum transconductance of transistor M1(input).
- State the parameters like transconductance, overdrive voltages, gains in terms of the bias current, output current and transconductance of transistor M1 or input transistor transconductance.
- Keeping in mind output swing assuming the values of overdrive voltages of last stage or output stage. Find the as many parameters as possible. Compare them, take which look optimum.
- Assumption is all transistor in saturation. So, using saturation region equations find the parameters from designing.

1.4 Clearly show bias currents and voltages on the schematic.

Circuit diagram (.PNG) is here

Xcircuit file (.ps) is here



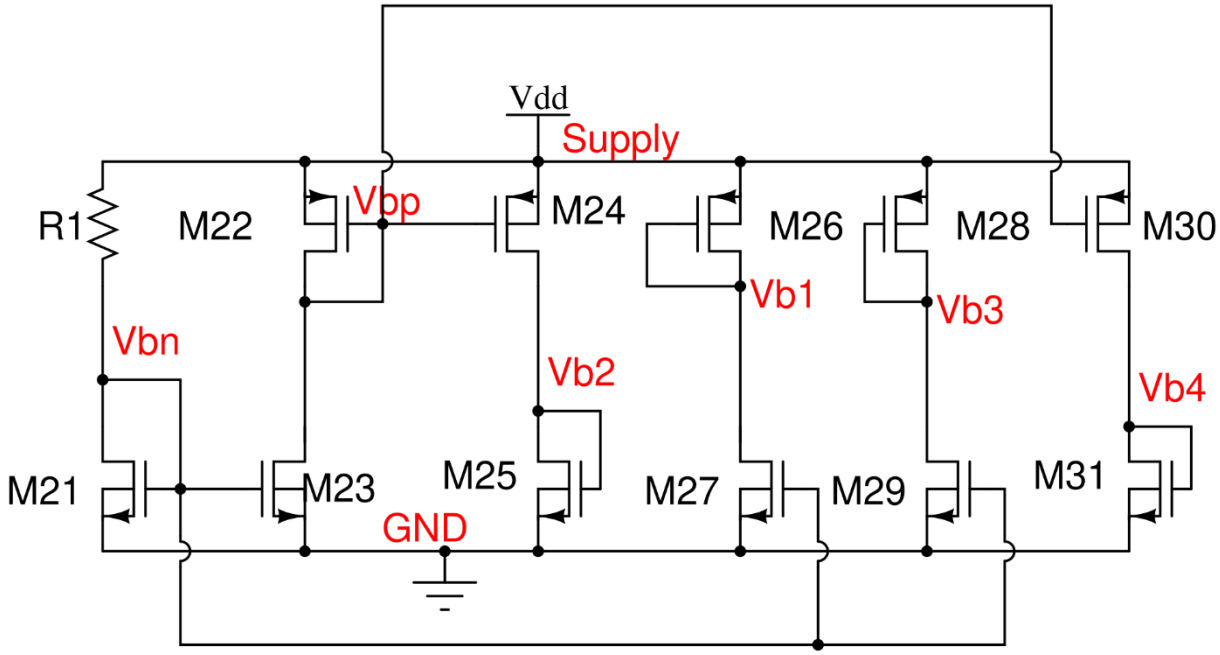
2- Reference Generator Circuit Design

In this section of the project, you will design a reference generator circuit of your choice. Reference generator circuit includes generating reference current (I_{ref}) first and then use current mirroring to generate bias voltages: V_{bn}, V_{bp} and $V_{b1}$to V_{b4}

Circuit diagram (.PNG) is here.

Xcircuit file (.ps) is here.

2.1 Draw the reference generator circuit which includes generating reference current (I_{ref}) and use current mirroring to generate other bias voltages for Op-amp.



2.2 Report the step by step design procedure for reference generator circuit.

Step 1 Current through M21 is $I_{21} = 60\mu A$

Current mirroring using Biasing voltage V_{bn}, V_{bp}.

$$I_{21} = \frac{k_n}{2} \times \left(\frac{W}{L}\right)_{21} \times (V_{bn} - V_{Tn})^2$$

$$60 \times 10^{-6} = \frac{300 \times 10^{-6}}{2} \times \left(\frac{W}{L}\right)_{21} \times (0.697 - 0.399)^2$$

$$\left(\frac{W}{L}\right)_{21} = \frac{4.504}{1}$$

M21 copies current into M23 branch therefor current through M22 is $I_{22} = 60\mu A$

For M_{22},

$$I_{22} = \frac{k_p}{2} \times \left(\frac{W}{L}\right)_{22} \times (V_{dd} - V_{bp} - |V_{Tp}|)^2$$

$$60 \times 10^{-6} = \frac{65 \times 10^{-6}}{2} \times \left(\frac{W}{L}\right)_{22} \times (1.8 - 1.085 - 0.42)^2$$

$$\left(\frac{W}{L}\right)_{22} = \frac{21.21}{1}$$

Step 2 Calculation for half current thorough M24

For $M_{23}, I_{23} = 60\mu A$

$$I_{23} = \frac{k_n}{2} \times \left(\frac{W}{L}\right)_{23} \times (V_{bn} - V_{Tn})^2$$

$$30 \times 10^{-6} = \frac{300 \times 10^{-6}}{2} \times \left(\frac{W}{L}\right)_{23} \times (0.697 - 0.3999)^2$$

$$\left(\frac{W}{L}\right)_{23} = \frac{4.5}{1}$$

For $M_{24}, I_{24} = 30\mu A$

$$I_{24} = \frac{k_p}{2} \times \left(\frac{W}{L}\right)_{24} \times \left(V_{dd} - V_{bp} - |V_{Tp}|\right)^2$$

$$30 \times 10^{-6} = \frac{65 \times 10^{-6}}{2} \times \left(\frac{W}{L}\right)_{24} \times (1.8 - 1.085 - 0.42)^2$$

$$\left(\frac{W}{L}\right)_{24} = \frac{10.60}{1}$$

Current mirroring using Biasing voltage V_{b2}

For $M_{25}, I_{25} = 30\mu A$

$$I_{25} = \frac{k_n}{2} \times \left(\frac{W}{L}\right)_{25} \times (V_{b2} - V_{Tn})^2$$

$$30 \times 10^{-6} = \frac{300 \times 10^{-6}}{2} \times \left(\frac{W}{L}\right)_{25} \times (0.9799 - 0.3999)^2$$

$$\left(\frac{W}{L}\right)_{25} = \frac{0.5945}{1}$$

Step 3 Calculation for half current thorough M27

For $M_{27}, I_{27} = 30\mu A$

$$I_{27} = \frac{k_n}{2} \times \left(\frac{W}{L}\right)_{27} \times (V_{bn} - V_{Tn})^2$$

$$30 \times 10^{-6} = \frac{300 \times 10^{-6}}{2} \times \left(\frac{W}{L}\right)_{27} \times (0.697 - 0.399)^2$$

$$\left(\frac{W}{L}\right)_{27} = \frac{2.26}{1}$$

Current mirroring using Biasing voltage V_{b1}

For $M_{26}, I_{26} = 30\mu A$

$$I_{26} = \frac{k_p}{2} \times \left(\frac{W}{L}\right)_{26} \times \left(V_{dd} - V_{b1} - |V_{Tp}|\right)^2$$

$$30 \times 10^{-6} = \frac{65 \times 10^{-6}}{2} \times \left(\frac{W}{L}\right)_{25} \times (1.8 - 0.78 - 0.42)^2$$

$$\left(\frac{W}{L}\right)_{26} = \frac{1.538}{1}$$

Step 4 Current mirroring using Biasing voltage V_{b3}

$$\left(\frac{W}{L}\right)_{29} = \left(\frac{W}{L}\right)_{21} = \frac{4.504}{1}$$

$$I_{28} = \frac{k_p}{2} \times \left(\frac{W}{L}\right)_{28} \times \left(V_{dd} - V_{b3} - |V_{Tp}|\right)^2$$

$$60 \times 10^{-6} = \frac{65 \times 10^{-6}}{2} \times \left(\frac{W}{L}\right)_{28} \times (1.8 - 0.19 - 0.42)^2$$

$$\left(\frac{W}{L}\right)_{28} = \frac{1.303}{1}$$

Step 5 Current mirroring using Biasing voltage V_{b4}

For M_{31}, $I_{31} = 60\mu A$

$$I_{31} = \frac{k_n}{2} \times \left(\frac{W}{L}\right)_{31} \times (V_{b4} - V_{Tn})^2$$

$$60 \times 10^{-6} = \frac{300 \times 10^{-6}}{2} \times \left(\frac{W}{L}\right)_{31} \times (1.28 - 0.3999)^2$$

$$\left(\frac{W}{L}\right)_{31} = \frac{0.5164}{1}$$

$$\left(\frac{W}{L}\right)_{30} = \left(\frac{W}{L}\right)_{22} = \frac{21.21}{1}$$

Step 6 Calculation of R

$$I_R = \frac{\mu_n \times C_{ox}}{2} \times \left(\frac{W}{L}\right) \times (V_{dd} - R \times I_R - V_{Tn})^2$$

$$R \times I_R = V_{dd} - V_{Tn} - \sqrt{\frac{2 \times I_R}{\mu_n \times C_{ox} \times \left(\frac{W}{L}\right)}} = 1.102857$$

$$\boldsymbol{R = 18.30k\Omega}$$

2.3 Tabulate the size of transistors used in the circuit.

Transistors	Sizes	Simulation Size
M21	4.504	7.5
M22	21.21	38
M23	4.504	7.5
M24	10.60	10.60
M25	0.5945	0.58
M26	1.538	2.3
M27	2.26	2
M28	1.303	2.1
M29	4.504	7.5
M30	21.21	38
M31	0.5164	1

Observation: In the simulation with calculated values of W/L is showing wrong biasing voltages which results in incorrect output of OPAMP circuit. Therefore, Transistor values are changed so the OPAMP will work properly.

Source code is here

For the following questions:

```
*CMOS PROJECT
.param lpn = 1u
.param lambda = 90n
.param w1 = 12u
*WL1 WL2
.param w2 = 54u
*WL3 WL4
.param w3 = 4.5u
*WL5
.param w4 = 21u
*WL6
.param w5 = 21u
*WL7 WL8
.param w6 = 11u
*WL9 WL10
.param w7 = 2.5u
*WL15 WL16
.param w8 = 4.5u
*WL17 WL18
.param w9 = 51u
*WL19
.param w10 = 11u
*WL20
.param w11 = 2.5u
*WL12 WL13
.param w12 = 11u
*WL11 WL14
.param w21 = 7.5u
.param w23 = 7.5u
.param w25 = 0.58u
.param w27 = 2u
.param w22 = 38u
.param w24 = 10.60u
.param w26 = 2.3u
.param w28 = 2.1u
.param w29 = 7.5u
.param w30 = 38u
.param w31 = 1u
***
```

In this snippet, All the W/L is mentioned for OPAMP and Reference current generator

Below snippet is for NMOS configuration in OPAMP.

```
M1 IP2 Vinp IN0 0 NMOS
+ L={lpn} W={w1} AD={4*lambda*w1} AS={4*lambda*w1}
+ PD={2*w1+8*lambda} PS={2*w1+8*lambda}
M2 IP1 Vinn IN0 0 NMOS
+ L={lpn} W={w1} AD={4*lambda*w1} AS={4*lambda*w1}
+ PD={2*w1+8*lambda} PS={2*w1+8*lambda}
M5 IN0 Vbn 0 0 NMOS
+ L={lpn} W={w3} AD={4*lambda*w3} AS={4*lambda*w3}
+ PD={2*w3+8*lambda} PS={2*w3+8*lambda}
****

M12 IP3 Vb4 IN3 0 NMOS
+ L={lpn} W={w11} AD={4*lambda*w11} AS={4*lambda*w11}
+ PD={2*w11+8*lambda} PS={2*w11+8*lambda}
M13 IP4 Vb4 IN4 0 NMOS
+ L={lpn} W={w11} AD={4*lambda*w11} AS={4*lambda*w11}
+ PD={2*w11+8*lambda} PS={2*w11+8*lambda}
M15 IN3 Vb2 IN1 0 NMOS
+ L={lpn} W={w7} AD={4*lambda*w7} AS={4*lambda*w7}
+ PD={2*w7+8*lambda} PS={2*w7+8*lambda}
M16 IN4 Vb2 IN2 0 NMOS
+ L={lpn} W={w7} AD={4*lambda*w7} AS={4*lambda*w7}
+ PD={2*w7+8*lambda} PS={2*w7+8*lambda}
M17 IN1 IN3 0 0 NMOS
+ L={lpn} W={w8} AD={4*lambda*w8} AS={4*lambda*w8}
+ PD={2*w8+8*lambda} PS={2*w8+8*lambda}
M18 IN2 IN3 0 0 NMOS
+ L={lpn} W={w8} AD={4*lambda*w8} AS={4*lambda*w8}
+ PD={2*w8+8*lambda} PS={2*w8+8*lambda}
***

M20 Vout IN4 0 0 NMOS
+ L={lpn} W={w10} AD={4*lambda*w10} AS={4*lambda*w10}
+ PD={2*w10+8*lambda} PS={2*w10+8*lambda}
****######################
```

Below snippet is for PMOS configuration in OPAMP.

```
M3 IN2 Vinp IP0 supply PMOS
+ L={lpn} W={w2} AD={4*lambda*w2} AS={4*lambda*w2}
+ PD={2*w2+8*lambda} PS={2*w2+8*lambda}
M4 IN1 Vinn IP0 supply PMOS
+ L={lpn} W={w2} AD={4*lambda*w2} AS={4*lambda*w2}
+ PD={2*w2+8*lambda} PS={2*w2+8*lambda}
M6 IP0 Vbp supply supply PMOS
+ L={lpn} W={w4} AD={4*lambda*w4} AS={4*lambda*w4}
+ PD={2*w4+8*lambda} PS={2*w4+8*lambda}
****
M7 IP1 IP3 supply supply PMOS
+ L={lpn} W={w5} AD={4*lambda*w5} AS={4*lambda*w5}
+ PD={2*w5+8*lambda} PS={2*w5+8*lambda}
M8 IP2 IP3 supply supply PMOS
+ L={lpn} W={w5} AD={4*lambda*w5} AS={4*lambda*w5}
+ PD={2*w5+8*lambda} PS={2*w5+8*lambda}
M9 IP3 Vb1 IP1 IP1 PMOS
+ L={lpn} W={w6} AD={4*lambda*w6} AS={4*lambda*w6}
+ PD={2*w6+8*lambda} PS={2*w6+8*lambda}
M10 IP4 Vb1 IP2 IP2 PMOS
+ L={lpn} W={w6} AD={4*lambda*w6} AS={4*lambda*w6}
+ PD={2*w6+8*lambda} PS={2*w6+8*lambda}
M11 IN3 Vb3 IP3 supply PMOS
+ L={lpn} W={w12} AD={4*lambda*w12} AS={4*lambda*w12}
+ PD={2*w12+8*lambda} PS={2*w12+8*lambda}
M14 IN4 Vb3 IP4 supply PMOS
+ L={lpn} W={w12} AD={4*lambda*w12} AS={4*lambda*w12}
+ PD={2*w12+8*lambda} PS={2*w12+8*lambda}
****
M19 Vout IP4 supply supply PMOS
+ L={lpn} W={w9} AD={4*lambda*w9} AS={4*lambda*w9}
+ PD={2*w9+8*lambda} PS={2*w9+8*lambda}

*****##################################################
```

Below snippet is for Transistor configuration in Reference generator.

```
*#####################################################
M21 Vbn Vbn 0 0 NMOS
+ L={lpn} W={w21} AD={4*lambda*w21} AS={4*lambda*w21}
+ PD={2*w21+8*lambda} PS={2*w21+8*lambda}
M23 Vbp Vbn 0 0 NMOS
+ L={lpn} W={w23} AD={4*lambda*w23} AS={4*lambda*w23}
+ PD={2*w23+8*lambda} PS={2*w23+8*lambda}
M22 Vbp Vbp supply supply PMOS
+ L={lpn} W={w22} AD={4*lambda*w22} AS={4*lambda*w22}
+ PD={2*w22+8*lambda} PS={2*w22+8*lambda}
M24 Vb2 Vbp supply supply PMOS
+ L={lpn} W={w24} AD={4*lambda*w24} AS={4*lambda*w24}
+ PD={2*w24+8*lambda} PS={2*w24+8*lambda}
M26 Vb1 Vb1 supply supply PMOS
+ L={lpn} W={w26} AD={4*lambda*w26} AS={4*lambda*w26}
+ PD={2*w26+8*lambda} PS={2*w26+8*lambda}
M25 Vb2 Vb2 0 0 NMOS
+ L={lpn} W={w25} AD={4*lambda*w25} AS={4*lambda*w25}
+ PD={2*w25+8*lambda} PS={2*w25+8*lambda}
M27 Vb1 Vbn 0 0 NMOS
+ L={lpn} W={w27} AD={4*lambda*w27} AS={4*lambda*w27}
+ PD={2*w27+8*lambda} PS={2*w27+8*lambda}

M28 Vb3 Vb3 supply supply PMOS
+ L={lpn} W={w28} AD={4*lambda*w28} AS={4*lambda*w28}
+ PD={2*w28+8*lambda} PS={2*w28+8*lambda}
M29 Vb3 Vbn 0 0 NMOS
+ L={lpn} W={w29} AD={4*lambda*w29} AS={4*lambda*w29}
+ PD={2*w29+8*lambda} PS={2*w29+8*lambda}

M30 Vb4 Vbp supply supply PMOS
+ L={lpn} W={w30} AD={4*lambda*w30} AS={4*lambda*w30}
+ PD={2*w30+8*lambda} PS={2*w30+8*lambda}
M31 Vb4 Vb4 0 0 NMOS
+ L={lpn} W={w31} AD={4*lambda*w31} AS={4*lambda*w31}
+ PD={2*w31+8*lambda} PS={2*w31+8*lambda}
******#####################################################
```

Snippet for resistor and capacitor connection.

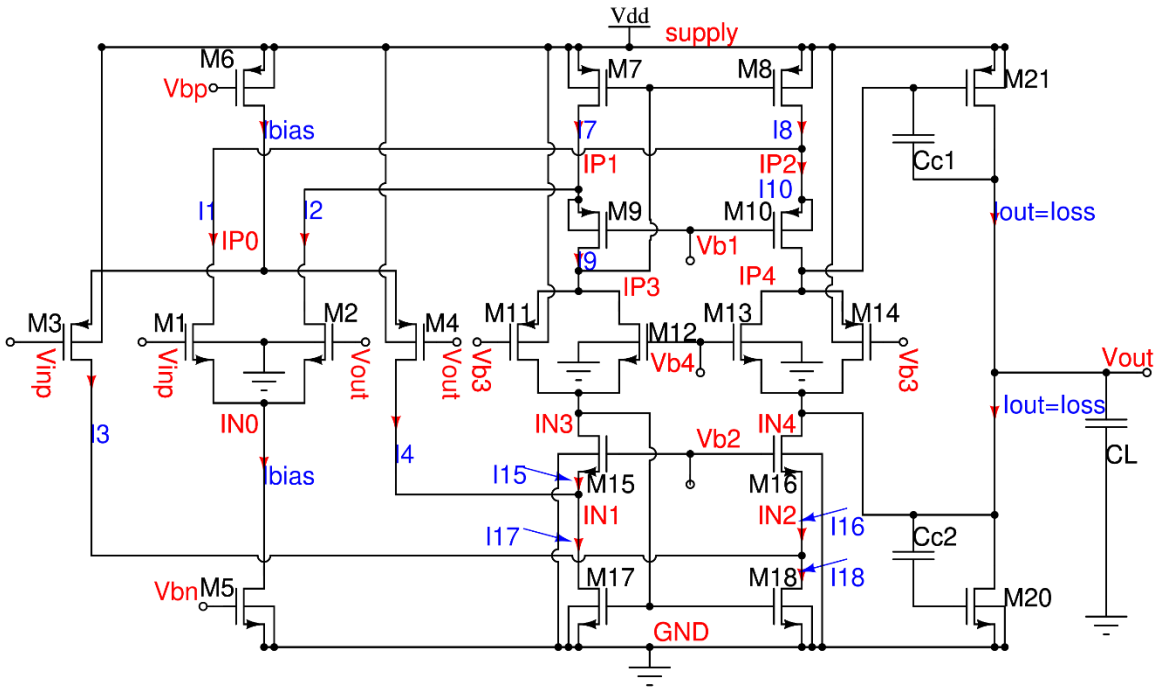
```
R1 supply Vbn 17.5k
Cc1 IP4 Vout 4p
Cc2 IN4 Vout 4p
CL Vout 0 5p
****************************************
```

3- DC Simulations

3.1 Connect the Op-amp in closed loop mode with voltage gain of -1 and apply DC common mode voltage (V_{cm}) at positive terminal of Op-amp.

Xcircuit file is here.

Circuit Diagram is here.



3.2 Run DC simulations on Op-amp including reference generator and find DC operating points.

Snippet for the DC simulation

NGSPICE code for this question is here

```
**************************************
VDD supply 0 dc 1.8
vd Int6 0 dc 0 ac 2
Evid1 Vinp Int Int6 0 0
Evid2 Vinn Int Int6 0 0
vcm Int 0 dc 0.9
.include 180nm_bulk.txt
.dc vcm 0.9 0.9 0.9
.control
run
PRINT V(Vout) V(Vinn) V(Vinp)
PRINT V(IN0) V(IN1) V(IN2) V(IN3) V(IN4)
PRINT V(IP0) V(IP1) V(IP2) V(IP3) V(IP4)
PRINT @M1[ID] @M2[ID] @M3[ID] @M4[ID]
PRINT @M5[ID] @M6[ID] @M7[ID] @M8[ID]
PRINT @M9[ID] @M10[ID] @M11[ID] @M12[ID]
PRINT @M13[ID] @M14[ID] @M15[ID] @M16[ID]
PRINT @M17[ID] @M18[ID] @M19[ID] @M20[ID]
PRINT V(Vbp) V(Vbn) V(Vb1) V(Vb2) V(Vb3) V(Vb4)
PRINT @M21[ID] @M23[ID] @M24[ID] @M27[ID] @M31[ID] @M30[ID]

.ENDC
.END
```

3.3 DC operating points should clearly show all the node voltages and currents.

- **Node voltages and currents for reference current circuit.**

V_{bp}(V)	1.0911	$I_{21}(\mu A)$	63.30
V_{bn}(V)	0.6917	$I_{23}(\mu A)$	65.51
V_{b1}(V)	0.7875	$I_{24}(\mu A)$	18.51
V_{b2}(V)	0.98445	$I_{27}(\mu A)$	17.50
V_{b3}(V)	0.1862	$I_{30}(\mu A)$	63.95
V_{b4}(V)	1.279	$I_{31}(\mu A)$	63.95

- **Node voltages and currents for OPAMP circuit.**

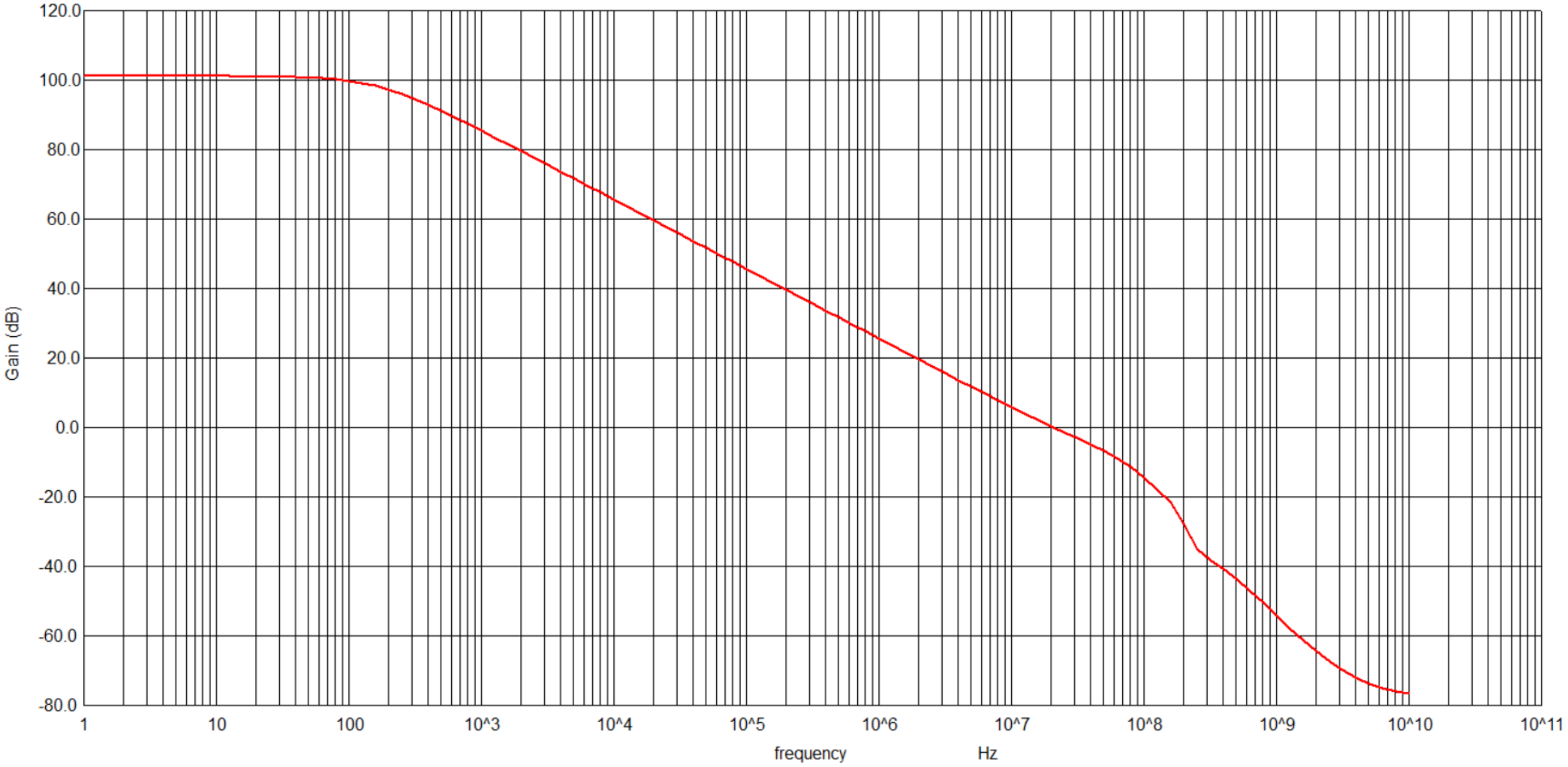
$I_1(\mu A)$	18.18	$I_{12}(\mu A)$	34.36	$V_{out}(V)$	0.9
$I_2(\mu A)$	18.18	$I_{13}(\mu A)$	32.18	$V_{in0}(V)$	0.296
$I_3(\mu A)$	16.98	$I_{14}(\mu A)$	19.24	$V_{in1}(V)$	0.22997
$I_4(\mu A)$	16.98	$I_{15}(\mu A)$	19.56	$V_{in2}(V)$	0.23
$I_5(\mu A)$	36.37	$I_{16}(\mu A)$	19.56	$V_{in3}(V)$	0.696866
$I_6(\mu A)$	33.96	$I_{17}(\mu A)$	36.54	$V_{in4}(V)$	0.69926
$I_7(\mu A)$	37.74	$I_{18}(\mu A)$	36.54	$V_{ip0}(V)$	1.525
$I_8(\mu A)$	37.74	$I_{19}(\mu A)$	99.47	$V_{ip1}(V)$	1.505
$I_9(\mu A)$	19.56	$I_{20}(\mu A)$	99.47	$V_{ip2}(V)$	1.505
$I_{10}(\mu A)$	19.56	$V_{inp}(V)$	0.9	$V_{ip3}(V)$	1.077
$I_{11}(\mu A)$	19.21	$V_{inn}(V)$	0.9	$V_{ip4}(V)$	1.077

4- AC Simulations

4.1 Plot the open loop differential voltage gain (in dB) as a function of frequency. Highlight the approximate location of poles and zeros. (Use common mode voltage: 0.9 V).
Following snippet for the open loop differential voltage gain (dB)
NGSPICE code for this question is here

```
VDD supply 0 dc 1.8
vd Int6 0 dc 0 ac 2
Evid1 Vinp Int Int6 0 0.5
Evid2 Vinn Int Int6 0 -0.5
vcm Int 0 dc 0.9
.include 180nm_bulk.txt
.control
run
ac dec 10 1 10G
set color0 = white
set color1 = black
set color2 = red
set color3 = black
set xbrushwidth = 2
plot Vdb(Vout) ylabel 'Gain (dB)' xlimit 1 1G
print MAXIMUM(Vdb(Vout))
print MAXIMUM(V(Vout))
PZ Int6 0 Vout 0 VOL PZ
Print all
.ENDC
.END
```

Differential gain (dB) VS frequency (Hz)



```
No. of Data Rows : 101
maximum(vdb(vout)) = 1.011109e+02
maximum(v(vout)) = 1.136415e+05,3.744110e-01
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
```

```
No. of Data Rows : 1
ngspice 30 -> print all
pole(1) = -1.07288e+09,0.000000e+00
pole(2) = -9.46175e+08,0.000000e+00
pole(3) = -7.12325e+08,0.000000e+00
pole(4) = -6.56887e+08,0.000000e+00
pole(5) = -4.47996e+08,0.000000e+00
pole(6) = -2.21576e+08,0.000000e+00
pole(7) = -4.22641e+07,0.000000e+00
pole(8) = -1.05178e+03,0.000000e+00
zero(1) = -1.14195e+09,0.000000e+00
zero(2) = -9.48400e+08,0.000000e+00
zero(3) = -8.24932e+08,0.000000e+00
zero(4) = -6.53769e+08,0.000000e+00
zero(5) = -4.48294e+08,0.000000e+00
zero(6) = -4.18037e+07,0.000000e+00
zero(7) = 1.668132e+08,0.000000e+00
ngspice 31 ->
Interrupted once . . .
Warning: clearing control structures
ngspice 31 ->
```

Pole	MHz	Zero	MHz
1	−1072	1	−1141.95
2	−946	2	−948.4
3	−712	3	−824.93
4	−657	4	−653.76
5	−448	5	−448.29
6	−221.5	6	−41.8
7	−42.26	7	−166.81
8	**−0.00105**		

By observation

- **Pole= $-1.05 \times 10^3\ Hz$ Dominant pole**
- **pair of pole-zero cancelling each other**
- **Other 3 pole-zero approximately close to each other.**
- **Pole -42.26Mhz and Zero -41.8Mhz are close to each other.**

4.2 Compare the results from simulation with estimated pole-zero locations from hand calculations ($C_L = 5$ pF)

Pole-Zero Calculation:

$$\omega_d = \frac{1}{\tau_d}$$

$$\tau_d = R_{eq} \times C_c \times (1 - A_{v2})$$

$$R_{eq} = g_{m10} \times r_{08} \times r_{010}$$

$$A_{v2} = -44.82$$

$$R_{eq} = 200 \times 10^{-6} \times 167 \times 10^3 \times 334 \times 10^3 = 11.15 \times 10^6 \Omega$$

$$\therefore \tau_d = 2.044 \times 10^{-3} s$$

$$\omega_d = 489.23$$

$$f_d = 77.86$$

$$f_{ND} = \frac{g_{m19}}{2 \times \pi \times C_L} = 31.70 \times 10^6\ Hz$$

$$f_Z = \frac{g_{m19}}{2 \times \pi \times C_c} = 39.62 \times 10^6\ Hz$$

Calculated Pole and zeros are:

- $f_d = 77.86Hz$
- $f_{ND} = 31.70 \times 10^6\ Hz$
- $f_Z = 39.62 \times 10^6\ Hz$

By comparing with simulated results

- $f_d = 1.05 \times 10^3 Hz$
- $f_{ND} = 42.26 \times 10^6\ Hz$
- $f_Z = 41.8 \times 10^6\ Hz$

4.3 Plot phase of open loop voltage gain as a function of frequency and specify the phase margin. Snippet for the Phase margin and phase plot.

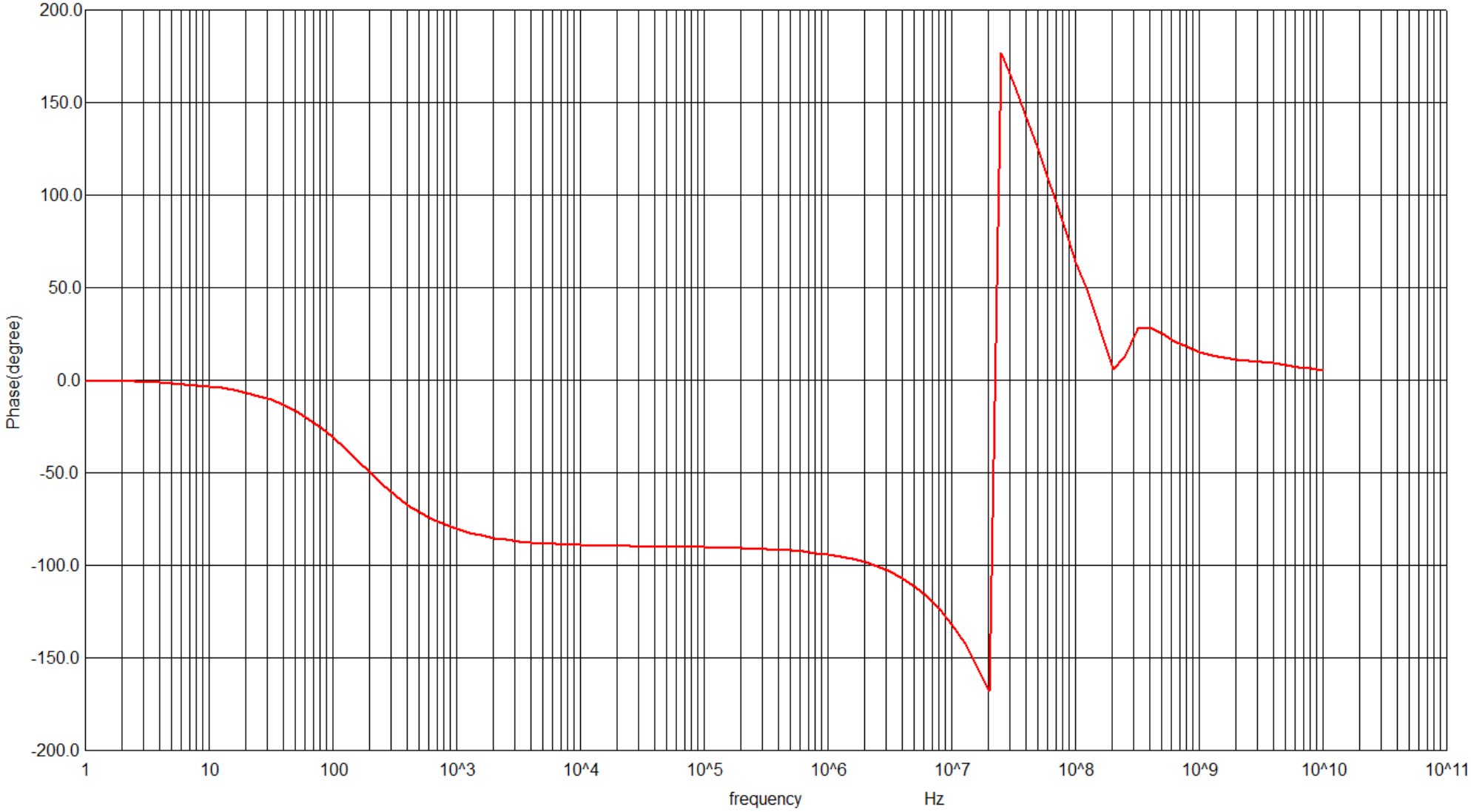
NGSPICE code for this question is here.

```
VDD supply 0 dc 1.8
vd Int6 0 dc 0 ac 2
Evid1 Vinp Int Int6 0 0.5
Evid2 Vinn Int Int6 0 -0.5
vcm Int 0 dc 0.9
.include 180nm_bulk.txt
.control
run
ac dec 10 1 10G
print MAXIMUM(Vdb(Vout))
let phase = 180/PI * ph(Vout)
plot phase ylabel 'Phase (degree)' xlimit 1 1G
MEAS AC Unity_Freq WHEN vdb(Vout) = 0
Let Double_Unity_Freq = 2*Unity_Freq
PRINT Double_Unity_Freq
Meas AC gain_at2xUGBW FIND Vdb(Vout) AT = Double_Unity_Freq
Let Roll_off = gain_at2xUGBW/log(2)
PRINT Roll_off

.ENDC
.END

```

```
No. of Data Rows : 101
maximum(vdb(vout)) = 1.011109e+02
unity_freq         =  2.094123e+07
double_unity_freq = 4.188246e+07
gain_at2xugbw      =  -5.410432e+00
roll_off = -7.80560e+00
ngspice 53 ->
```

- Unity gain Bandwidth 20.94Mhz
- Phase margin 78.10°

Phase (degree) VS frequency (Hz)



4.4 Calculate the roll-off at 1 octave above unity gain frequency.

1 octave above Unity gain frequency is equal to $f_{unity} \times 2 = 20.94 \times 10^6 \times 2 = 41.88Mhz$

```
plot Vdb(Vout)
MEAS AC Unity_Freq WHEN vdb(Vout) = 0
Let Double_Unity_Freq = 2*Unity_Freq
PRINT Double_Unity_Freq
Meas AC Gain FIND Vdb(Vout) AT = Double_Unity_Freq
Let Roll_off = Gain/log(2)
PRINT Roll_off
```

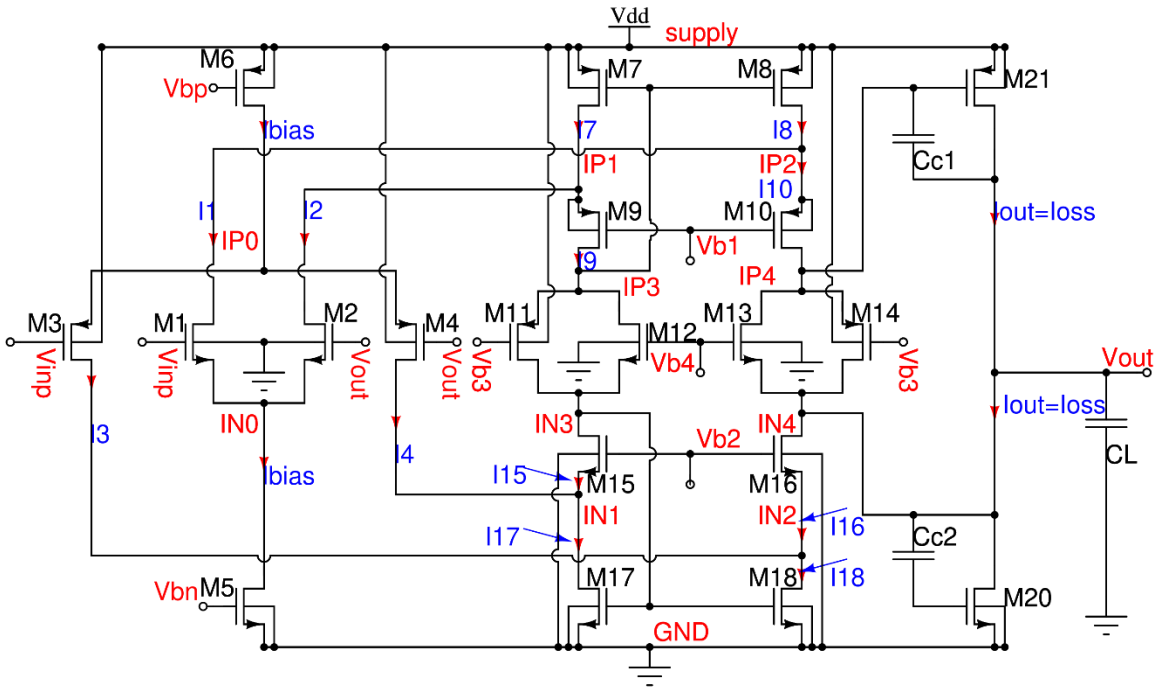
Roll-off at 1 octave above unity gain frequency is **-7.805 dB/oct**

5- Slew rate Simulation

5.1 Connect the Op-amp in closed loop mode with voltage gain of -1. (Use common mode voltage: 0.9 V).

Xcircuit file is here.

Circuit Diagram is here.



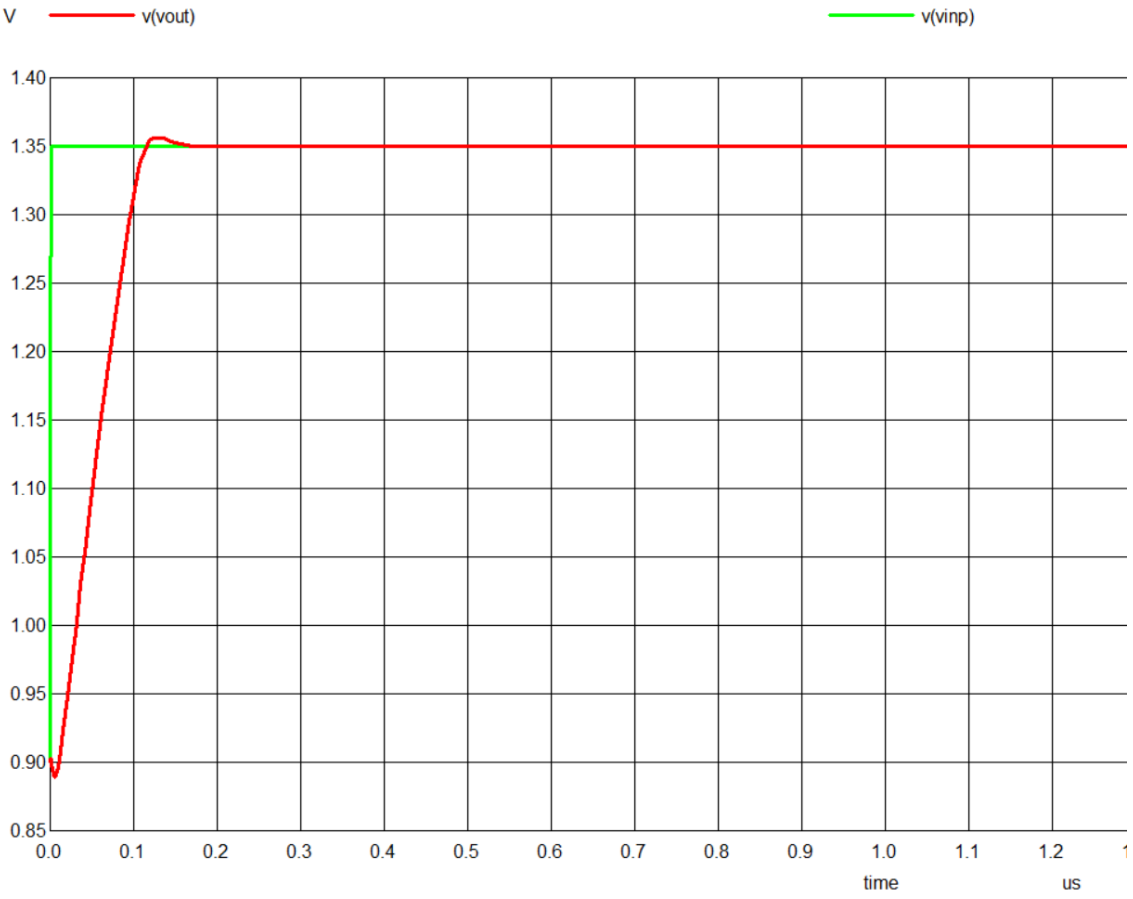
NGSPICE code for this question is here.

V_{inn} is shorted with V_{out}.

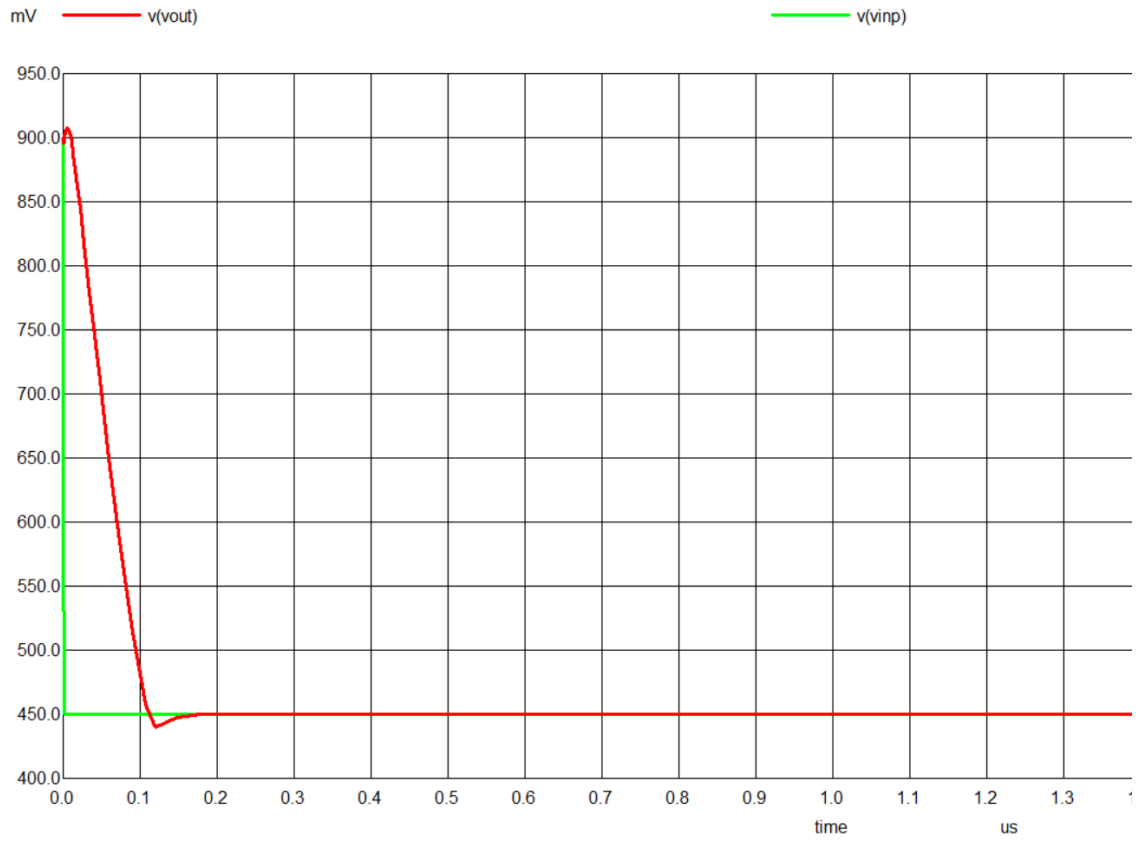
```
VDD supply 0 dc 1.8
Vin1 Int6 0 DC 0 PULSE(-0.9 0.9 0 1n 1n 4us 4us)
Evid1 Vinp Int Int6 0 0.5
Evid2 Vinn Int Int6 0 0
vcm Int 0 dc 0.9
.include 180nm_bulk.txt
.tran 0.1uS 2uS 0uS
.control
run
set color0 = white
set color1 = black
set color2 = red
set color3 = green
set xbrushwidth = 3
Plot  V(Vout) V(Vinp)
Let SR = deriv(V(Vout))
Print MAXIMUM(SR)
.ENDC
.END
```

5.2 Simulate step response to +450 mV and -450 mV differential input step voltage and calculate slew rate.

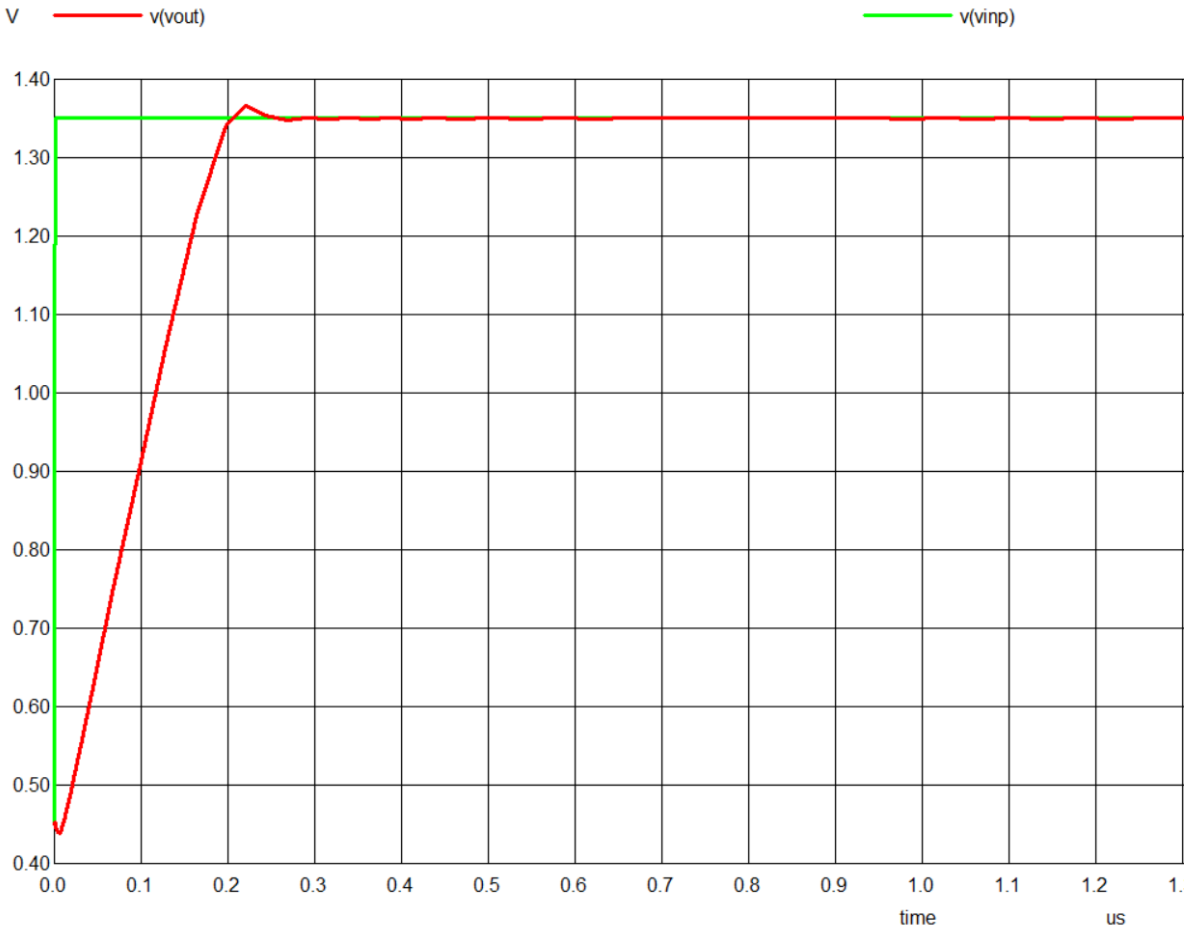
- Slew Rate is 8. 04 $\frac{V}{\mu s}$ with +450mV



- Slew Rate is 4. 52 $\frac{V}{\mu s}$ with -450mV



- Slew Rate is $14.81 \frac{V}{\mu s}$ with -450mV to +450mV swing

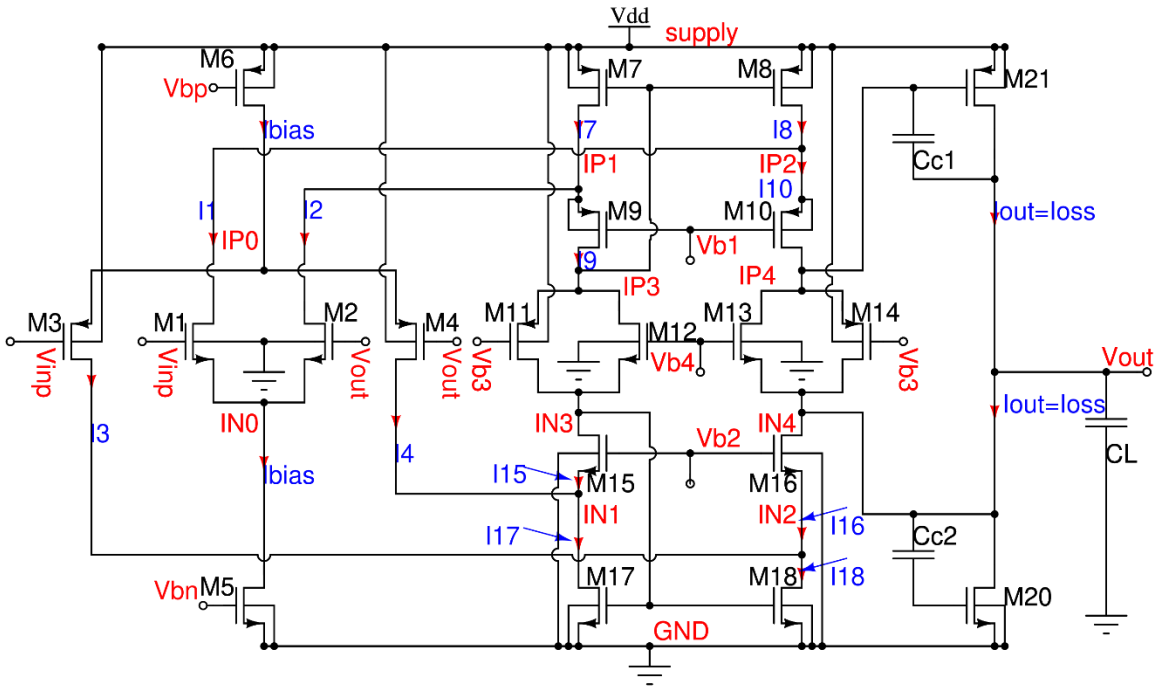


6- Transient Simulation

6.1 Connect the Op-amp in closed loop mode with voltage gain of -1. (Use common mode voltage: 0.9 V).

Xcircuit file is here.

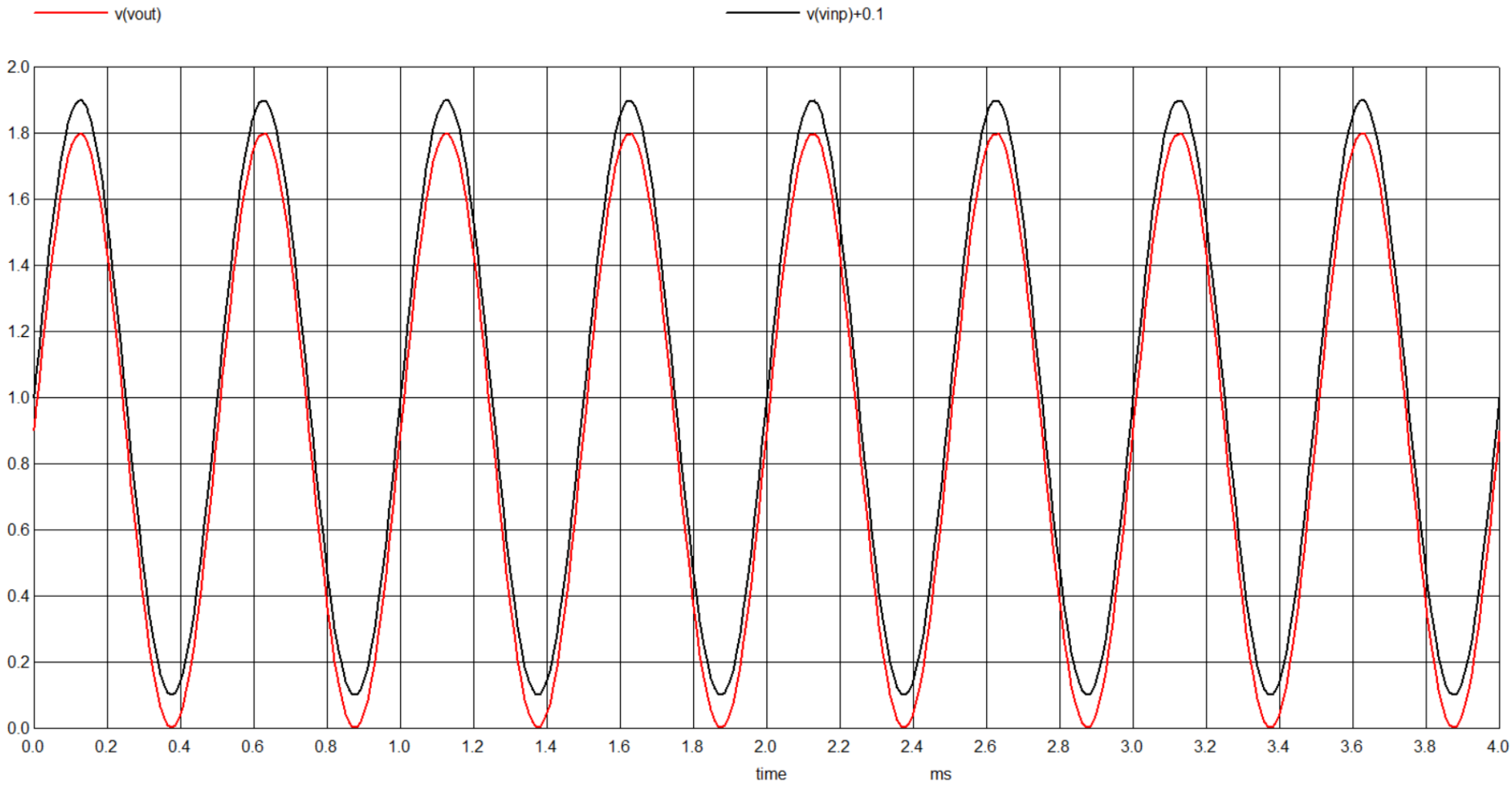
Circuit Diagram is here.



6.2 Run transient simulation for maximum output voltage swing.

NGSPICE code for this question is here

```
VDD supply 0 dc 1.8
VIN Int6 0 dc 0 SIN(0 1.8 2K 0 0)
*vd Int6 0 dc 0 ac 2
Evid1 Vinp Int Int6 0 0.5
Evid2 Vinn Int Int6 0 0
vcm Int 0 dc 0.9
.include 180nm_bulk.txt
.tran 0.1mS 4m 0uS

.control
run
print MAXIMUM(V(Vout))
print MINIMUM(V(Vout))
PLOT V(Vout) V(Vinp)+0.01
.ENDC
.END
```



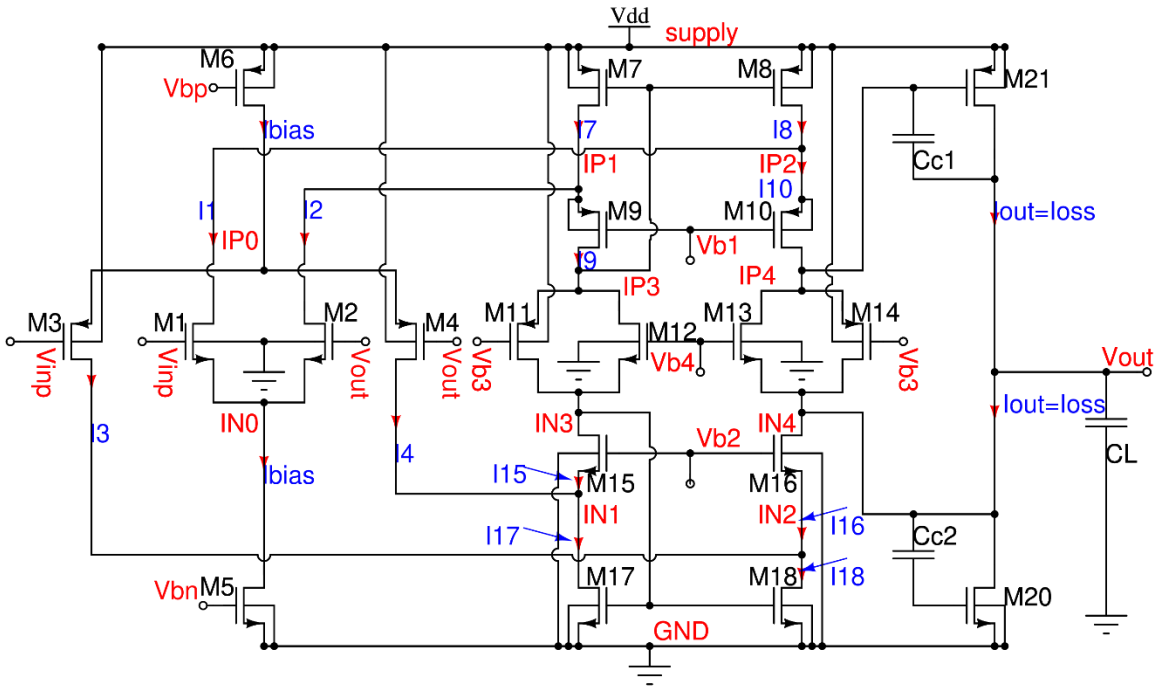
- Maximum Voltage swing is 1.8V

7- Common-mode (CM) DC Simulation

7.1 Connect the Op-amp in closed loop mode with voltage gain of -1.

Xcircuit file is here.

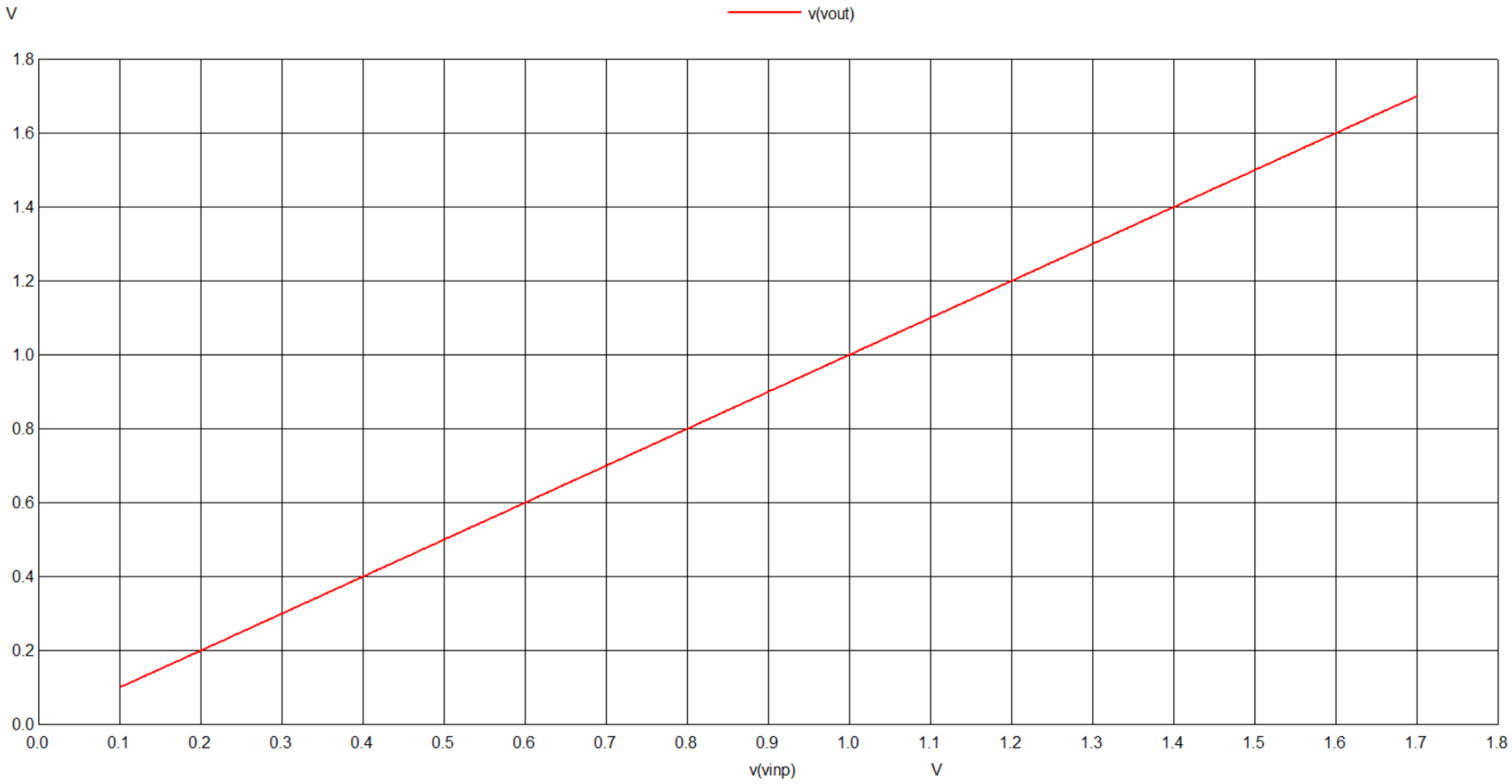
Circuit Diagram is here.



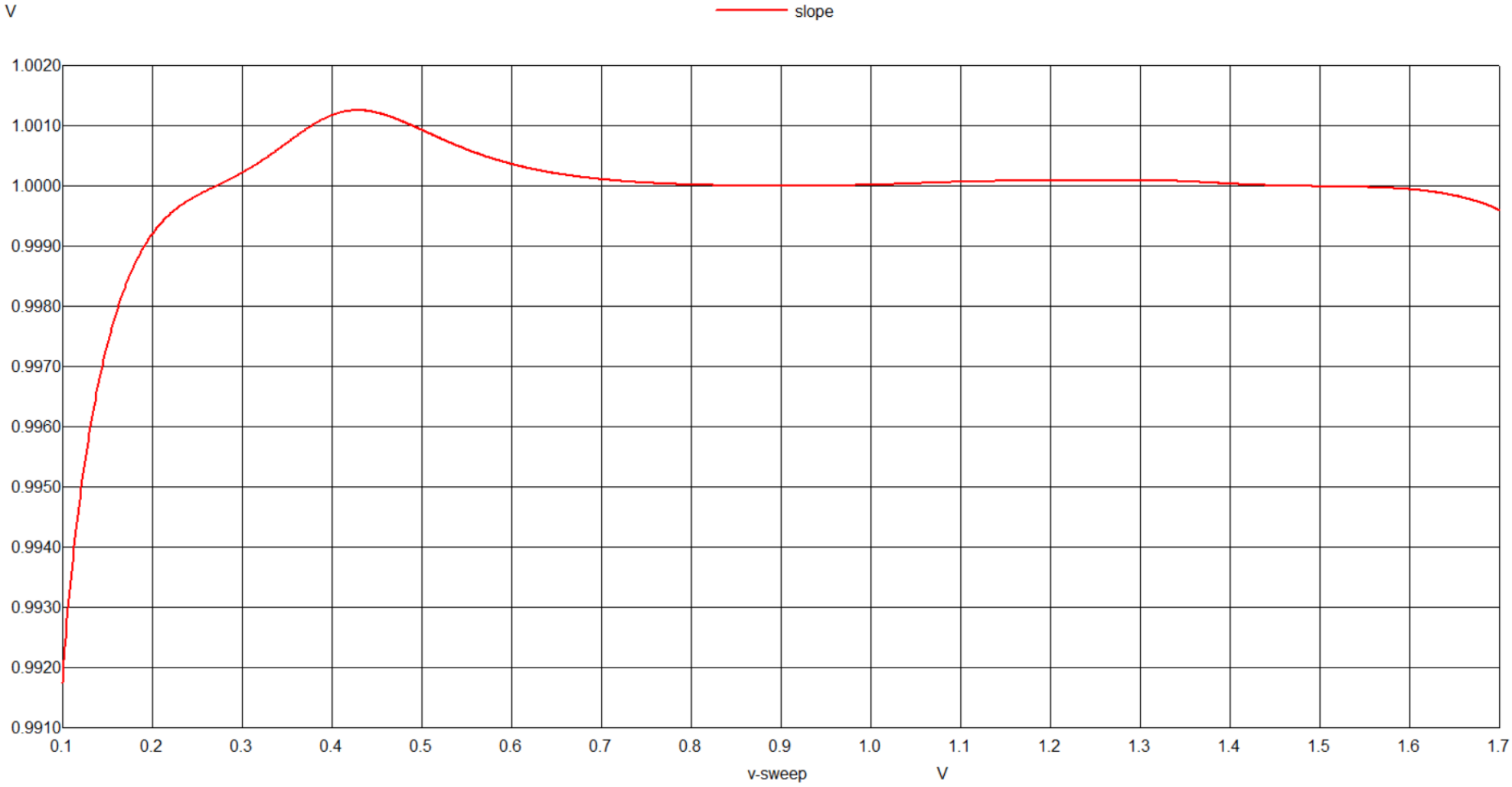
7.2 Sweep the common-mode DC input voltage from V_{cm-min} to V_{cm-max} (total range better than 50% of the V_{DD}). Plot output CM DC voltage as a function of input CM DC voltage.

Code for this question is here.

```
VDD supply 0 dc 1.8
vd Int6 0 dc 0 ac 2
Evid1 Vinp Int Int6 0 0.5
Evid2 Vinn Int Int6 0 0
vcm Int 0 dc 0.9
.include 180nm_bulk.txt
.dc vcm 0.1 1.7 0.1
.control
run
plot V(Vout) VS V(Vinp)
let slope = deriv(V(Vout))
plot slope
meas dc s100 FIND slope AT = 0.1
meas dc s09 FIND slope AT = 0.9
meas dc s16 FIND slope AT = 1.6
Print MAXIMUM(slope)
Print MINIMUM(slope)
.ENDC
.END
```


V
v(vout)
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
1.1
1.2
1.3
1.4
1.5
1.6
1.7
1.8
v(vinp)
V

7.3 Calculate the non-linearity of Op-amp by marking the values of slope at V_{cm}= 100 mV, 0.9 V and 1.6 V.



Slope at

- $V_{cm} = 100mV$ is 0.99174
- $V_{cm} = 0.9V$ *is* 0.9999987
- $V_{cm} = 1.6V$ *is* 0.9994

7.4 Report the maximum and minimum values of the slope calculated in 7.3 part.

```
No. of Data Rows : 1601
slope_100m           =  9.917433e-01
slope_900m           =  9.999987e-01
slope_1600m          =  9.999400e-01
maximum(slope) = 1.001253e+00
minimum(slope) = 9.917433e-01
ngspice 16 ->
```

- Maximum slope is 1.000
- Minimum slope is 0.9917

References

1. Pole Zero determination
   https://wordpress.nmsu.edu/pfurth/files/2015/06/Tutorial_Pole_Zero_2011.pdf
2. NGSPICE version-33 manual
   http://ngspice.sourceforge.net/docs/ngspice-manual.pdf
3. Design of 1V, 0.18μ FOLDED CASCODE OPAMP
   http://www.tjprc.org/publishpapers/2-15-1381147174-25%20.Design%20of%201%20V.FULL.pdf
4. A low voltage rail-to-rail operational amplifier with constant operation and improved process robustness
   https://lib.dr.iastate.edu/cgi/viewcontent.cgi?article=1719&context=etd
5. Rail-to-rail constant g_m input stage and class AB output stage for low-voltage CMOS OPAMP
   https://link.springer.com/article/10.1007/BF01239246

WORK CONTRIBUTION TEMPLATE

- You have to write work contribution from each member of your group at the end of project report using this template.
- Write the names of your group members in place of Member 1 and Member 2. For each question number, put a checkmark (✓) in Member 1 column or Member 2 column to specify whether the question is solved by Member 1 or Member 2 respectively.
- You may add any comments if you have in the same columns corresponding to every question

Q. no.	Prasad	Sagar
1.1	✓	✓
1.2	✓	✓
1.3	✓	✓
1.4	✓	✓
2.1	✓	✓
2.2	✓	
2.3	✓	✓
3.1	✓	✓
3.2		✓
3.3		✓
4.1	✓	✓
4.2	✓	✓
4.3	✓	
4.4	✓	
5.1	✓	✓
5.2		✓
6.1	✓	✓
6.2	✓	
7.1	✓	✓
7.2	✓	
7.3		✓
7.4		✓

- In his project, we proceeded with the design parameters first each team member designed individually for different bias current and came up with their W/L calculations and bias voltages. The final design was chosen which satisfied all the target requirements and specifications.
- To avoid any calculation mistakes both the team members did hand calculation and verified their result before simulating the design.
- Simulation part were done as mentioned in above table.
- In this pandemic time both the team members choose Google Meet, Google Colab and WhatsApp for collaborating and working together.