Design of Pipeline ADC based on Ring Amplifier

Submitted in partial fulfillment of the requirements
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by

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Thesis Approval

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Abstract

Designers moving to nanoscale technology nodes prefer ADC architectures like SAR because they downscale better than others. As for scaled technology, SAR ADC exhibits high accuracy and high resolution, but they take longer to convert. A pipeline ADC is beneficial for applications requiring moderate to high operating rates and high resolution. The thesis focuses on designing an 8-bit pipeline analog to digital converter (ADC).

The pipeline ADC consists of a 1.5-bit sub-ADC using a dynamic comparator and a multiplying DAC(MDAC). MDAC consumes most of the overall converter power, performing inter-stage residue amplification in the pipeline ADC. Traditionally, an operational amplifier configured in a switched-capacitor (SC) structure performs required inter-stage residue amplification.

The scaling down of CMOS technology challenges the performance of conventional operational amplifiers. It suffers from low output swing, dynamic range, and power consumption. Therefore, an alternative design of conventional OPAMP is required. A ring amplifier is an emerging circuit meant to replace the operational amplifier. The ring amplifier resembles a ring oscillator, which naturally incorporates the idea of scalability.

In the dissertation, different components of ADC are discussed and designed for the target specifications. The goal is to develop an 8-bit pipeline ADC using 1.5-bit per stage using 65nm CMOS technology and implement the system at a 200MHz sampling rate. The pipeline ADC consumes a total power of 22 mW with a 1.2 V power supply and achieves an SNDR of 49.3dB, resulting in an Effective Number of Bits (ENOB) of 7.9 bits. A DNL and INL are within $\pm$ 1 LSB, ensuring all ADC bits are available. The designed pipeline ADC achieves a Figure of Merit (FoM) of 460fJ/conversion rate.

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List of Abbreviations

DNL	Differential Non-linearity
ENOB	Effective Number of bits
INL	Integral Non-linearity
MDAC	Multiplying Digital-to-Analog Converter
RAMP	Ring Amplifier
SC	Switched-Capacitor
SHA	Sample and Hold Amplifier
SNDR	Signal-to-Noise- and Distortion Ratio

Chapter 1

Introduction

1.1 Background

Information in the physical world is analog form. Our senses tell us if a sound is high-pitched, loud, or muted and whether the temperature is humid or cold. The human brain understands analog information and reacts accordingly. Gathering information from the physical world is not straightforward for computers or other digital systems. It is vital to convert analog signals to discrete, binary signals to utilize the benefits of digital signal processing. A high-performance ADC bridges the gap between continuous and discrete-time domain.

1.2 Motivation

Typically, ADCs are analyzed based on three parameters: sampling rate, resolving bits, and consumed power. Various ADC configurations have evolved, including the Flash-type ADC, Successive Approximation Register (SAR) ADC, Σ-Δ ADC, and Pipeline ADC. The ADCs

must be able to operate at high speed, resolve a higher number of bits and have a minimal power consumption. Figure 1.1 shows the typical ADC architectures used as a base for converter design.

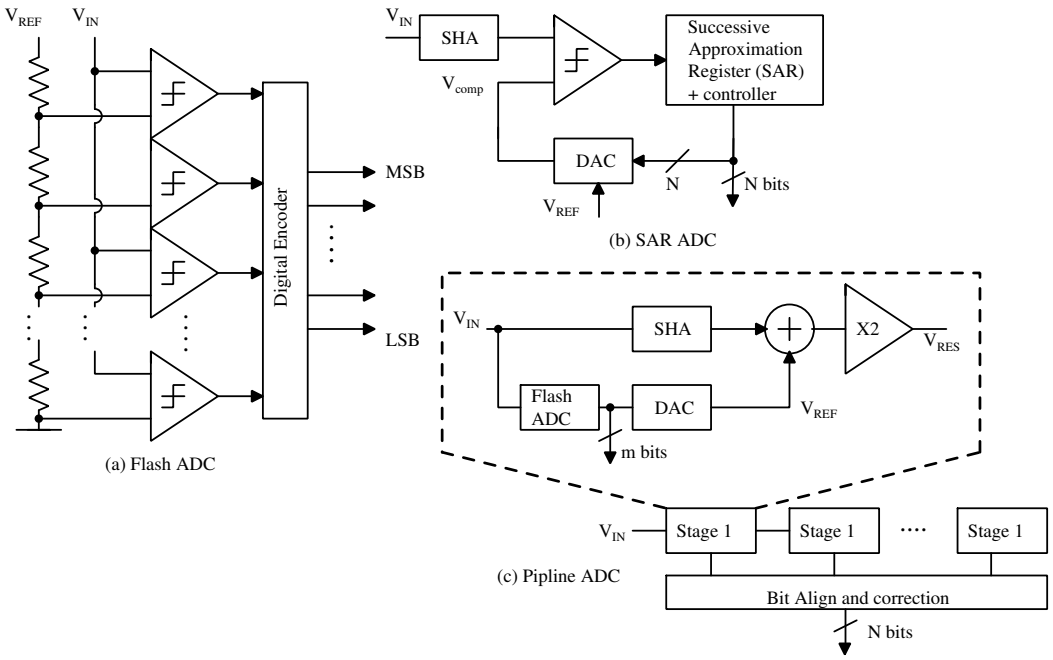


Figure 1.1: Typical ADC architectures [1]

- Flash ADC: Flash ADC has one of the highest sampling rates of all ADCs. This design uses a resistive ladder for the reference voltages to the parallel comparators encoded to produce the digital output. The circuits consist of 2^n resistors and 2^n-1 comparators, making the design power-intensive when applied at high resolution. The Flash ADC is typically only used for high-frequency applications when there is no other choice to address the specification.

- SAR ADC: The successive approximation-register (SAR) ADC can operate at medium resolution with a low sampling rate and power consumption. The typical design consists of a comparator, DAC, shift register, and encoders. SAR ADC employs the single comparator in cyclic architecture. The ADC will require N cycles to generate the digital output for N-bit resolution. A SAR ADC can be used in many applications.

- Pipeline ADC: This complex design that offers a moderate to high sampling rate and high resolution. The typical design is based on multiple stages consisting of an SHA, DAC, and sub-Flash ADC. The digital logic block is used to realign the digital code. Although

the Pipelined architecture cannot reach the sampling rate of a conventional Flash ADC, this architecture can save a significant power.

Researchers developed figures of merit (FoM) to measure the energy efficiency of ADCs with various parameters fairly. ADC FoMs combine parameters, such as power consumption, conversion speed, and effective resolution, into one for easy comparison. These metrics directly affect energy efficiency. The Walden FoM (FoMW) [3] is one of the most frequently used FoMs and is based on an empirical relationship from extensive ADC performance survey data. In his study of resolution and conversion rate, Walden discovered a pattern showing that for every twofold increase in conversion rate, the resolution falls by one bit. In light of this discovery, he proposed the following FoMW:

$$FOM_w = \frac{P}{f_s \times 2^{ENOB}} \tag{1.1}$$

Where P is power consumption, f_s is conversion rate, and ENOB is the effective number of bits. ENOB is derived from Signal-to-noise and distortion ratio (SNDR).

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{1.2}$$

The pipeline ADC is a famous architecture among various ADCs, including flash, pipeline, successive approximation register (SAR), and $\sum$-Δ. This is because it covers a wide range of conversion rates (1 MHz to 10 GHz) with a resolution range from moderate to high resolution (6 to 16b), as shown in Figure 1.2 [2]

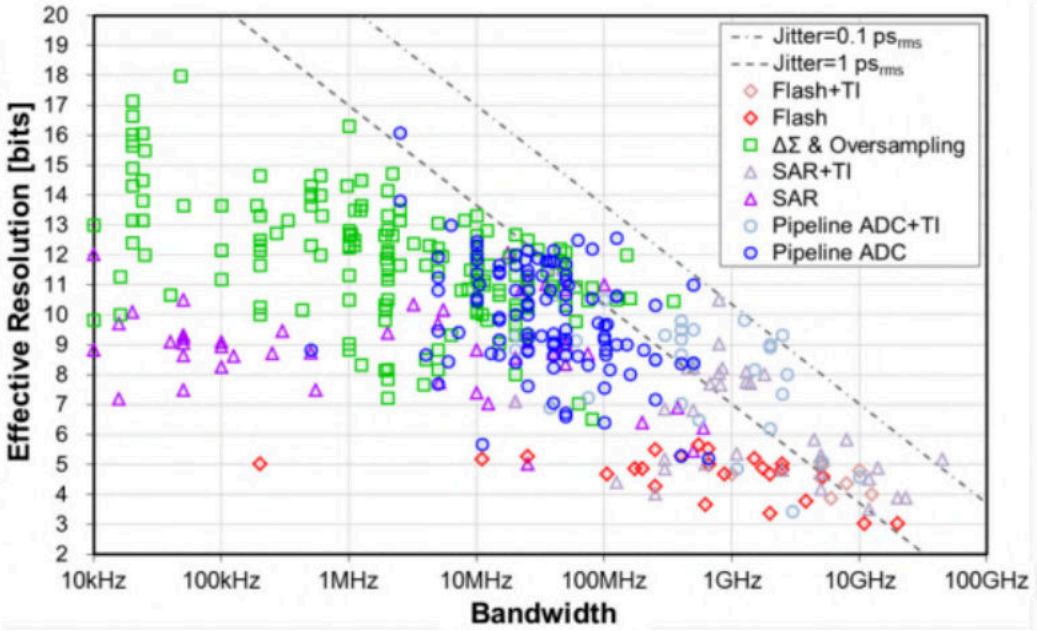


Figure 1.2: Conversion rate vs Effective bits [2]

1.3 Thesis objectives

The residue amplifier used in the conventionally OPAMP-based pipeline must be optimized to achieve higher energy efficiency. However, process scaling makes it more challenging to design the traditional OPAMP. Technology scaling reduces supply requirements and downgrades intrinsic device gain. Therefore, achieving a high gain for residue amplification in pipeline ADC is getting more challenging. As supply voltage is scaled down, using a cascode structure is highly problematic because it affects the output swing of an amplifier.

The shortcomings of traditional OPAMP-based SC circuits have been addressed using various alternative strategies, such as zero-crossing- and inverter-based circuits. The ring amplifier is another intriguing substitute. The ring amplifier in the SC circuits uses feedback just as conventional opamp SC circuits do; therefore, the accuracy relies on the gain of the ring amplifier. The desired gain can be easily achieved from three gain stages.

Self-biased ring amplifier is discussed and designed in the given dissertation, which is robust to PVT variation. A conventional ring amplifier is used as a backbone to explain the inner workings of the amplifier. The simple design methodology is illustrated to construct a

Self-bias class AB-style Ring amplifier. Also, the design tradeoff is discussed.

This thesis is organized into 6 chapters as follows

1. Chapter-1: This chapter gives an overview of the advantages of pipeline ADC. Factors affecting ADC performance are highlighted. Ring amplifier is briefly introduced chapter.

2. Chapter-2: Typical block diagram of pipeline ADC architecture is explained. This chapter also explains the working of Multiplying DAC, sub-ADC, ring amplifier, comparator, and digital error correction techniques.

3. Chapter-3: In-depth analysis of the ring amplifier using a conventional ring amplifier model is explained. Self-bias ring amplifier is explained using switched capacitor MDAC structure.

4. Chapter-4: The design methodology of the ring amplifier is presented. Complete pipeline ADC with the design of clocked comparator for a 1.5-bit sub-ADC, design of the switch is presented with clock phases.

5. Chapter-5: Various ring amplifier analyses are presented to design suitable residue amplifiers for the pipeline ADC. The test bench of the pipeline ADC is explained. The Monte-Carlo Simulations determine the static performance of the ADC. Dynamic performance for typical and other corners is tested.

6. Chapter-6: The chapter concludes the thesis and compares ADC performance with published ADC work. It also proposes the possible work that can be done on the ring amplifier to improve the efficiency of the ADC.

Chapter 2

Overview of Pipeline ADC

2.1 Introduction

In this chapter, the pipeline ADC architecture is detailed. The various building block of the pipeline ADC is described. The presented ADC uses SHA-less architecture. The resolution of pipeline ADC is easily adjusted by adding or removing the number of stages. For each additional stage, power consumption increases drastically.

2.2 Pipeline Architecture

Figure 4.12 represents a block diagram of pipeline ADC architecture which consists of 8 identical stages, each stage resolving 2 bits. The stages are successively connected. Every 2 bits from all stages are aligned and combined using digital logic to obtain high-resolution 8-bit results results. [4]

Each stage of pipeline ADC operates in two phases, sampling and amplification,which

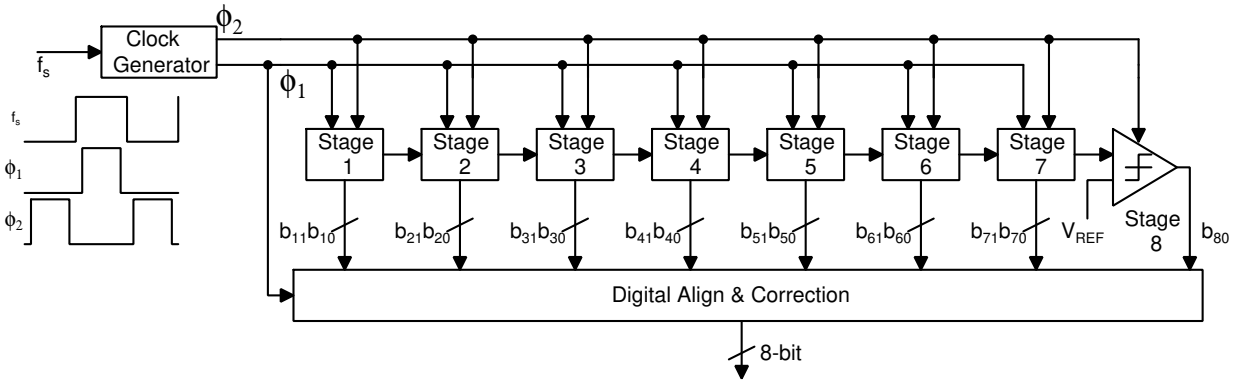


Figure 2.1: Pipeline ADC architecture

are non-overlapping clock phases, as shown in Figure 4.12. The input signal is sampled in the sampling phase. Sub-ADC within a non-overlapping period quantifies the sampled signal into three levels. This digital output bits are applied to DAC, which generates reference voltages. In the amplification phase, sampled input and reference voltage are compared and the residue signal is generated for the next stage as shown in Figure 2.2. The gain of the residue amplifier is 2^m, where m is the number of bits generated in the stage.

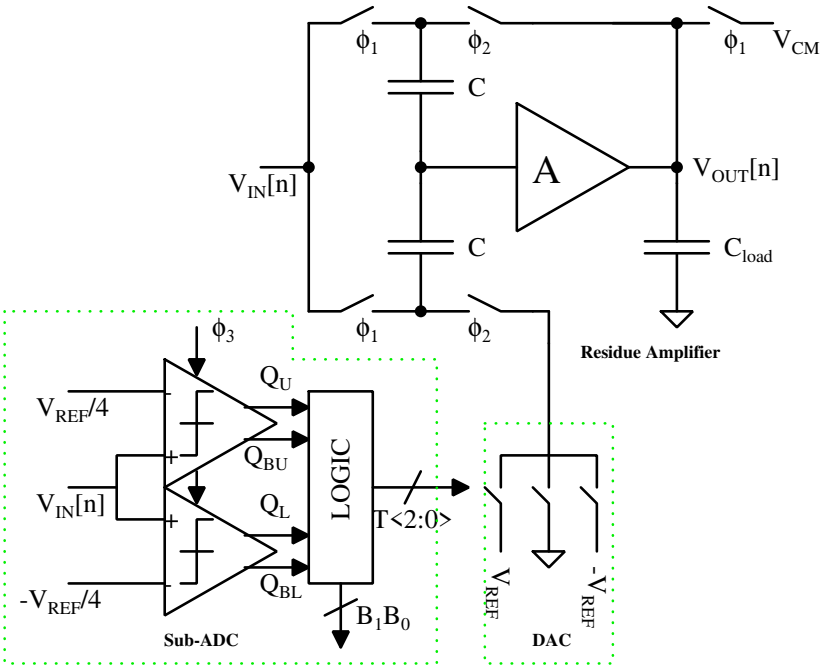


Figure 2.2: Single Stage of Pipeline ADC

All the stages operate parallelly in pair of non-overlapping phases ϕ_1 and ϕ_2. Sub-ADC to perform accurately, sampling of the input signal must be completed in the sampling phase and DAC must generate the reference signal in the amplification. Therefore sub-ADC is enabled at

the start of the non-overlapping period of ϕ_1 and ϕ_2. The proposed ADC architecture does not have any SHA. When any pipeline ADC stage enters the amplification phase, the consequent stage enters the sampling phase. If an i^{th} stage is in the amplification phase, then the $i+1^{th}$ stage will be in the sampling phase. Because of this sampling capacitor of the $i+1^{th}$ stage works as load capacitor for the i^{th} stage. Therefore, the need for SHA is avoided. Conventionally the latency of pipeline ADC depends on the number of stage because every stage consumes one clock cycle to convert. Nevertheless, in the proposed thesis, latency is half because single cycle two stages work. In the first half of the cycle, i^{th} stage samples, generate 2-bit output bits then in the next half of cycle $i+1^{th}$ stage the samples the residue generated at same time and resolved two more bits at the end of the cycle as shown in Figure 2.3.

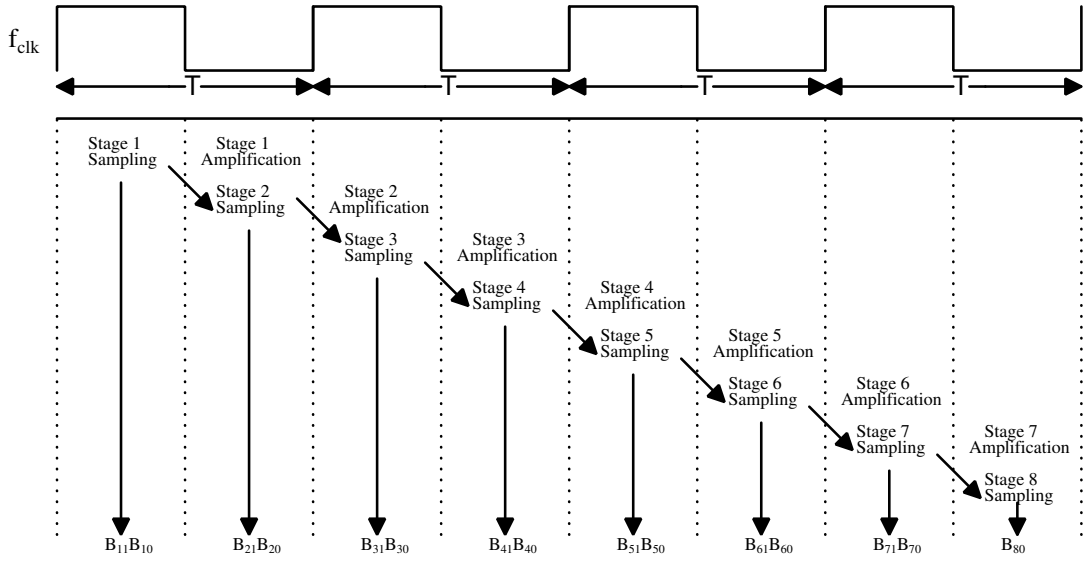


Figure 2.3: Pipeline Stages Operation Modes

2.3 Multiplying Digital-to-Analog Converter (MDAC)

The operation of MDAC is an equivalent sample and hold (S/H), summer ,and switched-capacitor amplifier. With switched-capacitor MDAC, basic operations like addition, subtraction ,and multiplication with constant are possible. In the proposed thesis, pseudo-differential MDAC is designed, but for explanation purposes, single-ended MDAC is shown in Figure.2.2.

The proposed pipeline ADC resolves 1.5 bits per stage, as shown in Figure 4.12. let us examine pipeline ADC, which resolves 1 bit per stage, to understand the importance of this 0.5-bit redundancy.

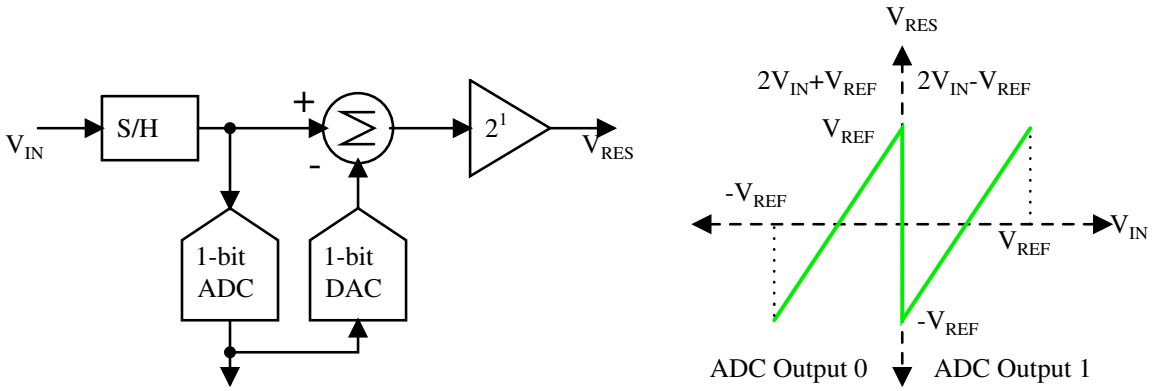


Figure 2.4: 1-bit per pipeline stage and stage transfer function

Figure 2.4 describes the pipeline stage, which resolves 1 bit and, the transfer function of the stage is given. Due to mismatches, the offset can occur and alter the transfer function, as shown in Figure 2.5. This error leads to stage output exceeding full-scale range causing a loss of information. The errors can be eliminated by limiting the transfer function within $\pm V_{REF}/2$. The addition of an extra comparator achieves this. The Pipeline stage resolves 2 bits With the additional comparator, which divides the stage operations into three regions.

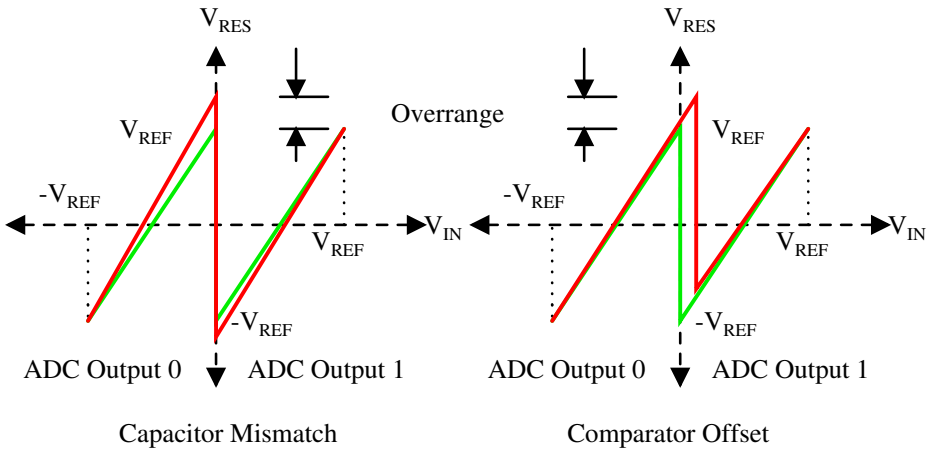


Figure 2.5: Transfer altered due to mismatches and offset

Three unique digital output alters the transfer function of the pipeline stage shown in Figure 2.6. The internal working of the switched capacitor residue amplifier is explained in chapter-3.

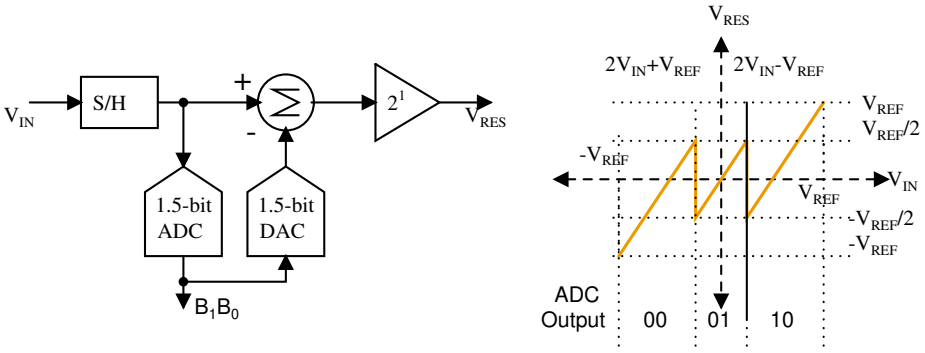


Figure 2.6: 1.5bits/stage block diagram and Transfer function

2.4 Sub-ADC

In the pipeline ADC, each stage consists of a sub-ADC implemented using simple flash ADC architecture. The proposed sub-ADC generates 1.5 bits with two dynamic comparators, an encoder ,and a resistive ladder, as given in below in Figure 2.7. The comparator compares the input signal with a reference signal and gives a decision in the binary digits, which should have minimum power consumption, minimum offset, and resolve the bits shortest possible time. The output of the comparators is encoded into a binary format from the thermometer code using the basic logic circuit. MSB is directly taken from upper comparator output Q_1. LSB is calculated from the logical expression $Q_{1B} \wedge Q_2$. Comparator outputs directly control DAC switches to select the reference voltages in the amplification phase.

Sub-ADC Input(V_{IN})	$\mathbf{Q_1}$	$\mathbf{Q_2}$	$\mathbf{Q_{1B}}$	$\mathbf{Q_{2B}}$	$\mathbf{B_1}$	$\mathbf{B_0}$
$V_{IN} \leq -V_{REF}/4$	0	0	1	1	0	0
$-V_{REF}/4 \leq {}_{IN} \leq V_{REF}/4$	0	1	1	0	0	1
$V_{IN} \geq V_{REF}/4$	1	1	0	0	1	0

Table 2.1: Truth Table for encoder

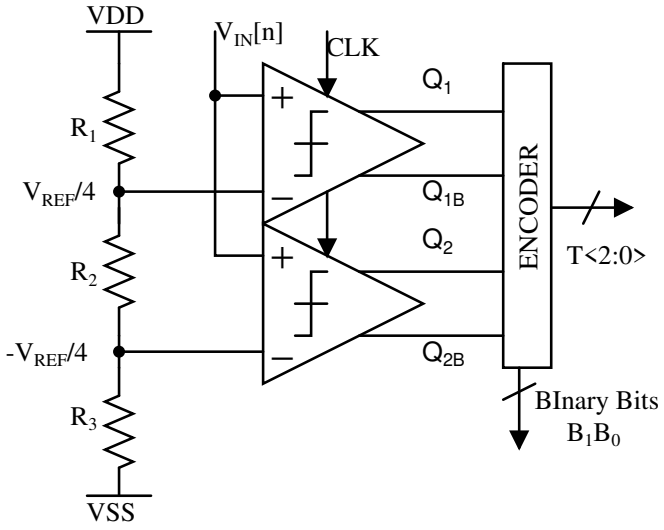


Figure 2.7: 1.5 bits Sub-ADC

The resolution requirement of the sub-ADC is very low; therefore, primarily, flash ADC is used. The Comparator thresholds ($\pm V_{REF}/4$) are derived from the resistive ladder network given in Figure 2.7. The error correction algorithm relaxes the tolerance of offset in the comparator. For V_{REF} = 500 mV, an offset of 125 mV $_{REF}/4$ is tolerable.

2.4.1 Preamplifier based Clocked Comparator

Comparator is one of the vital building blocks of any converter. In the proposed thesis preamplifier-based dynamic comparator is illustrated. This type of comparator is fast and has a low input-referred offset.Preamplifier amplifies the difference between input sufficiently high, so latch can quickly decide.

- **Preamplifier**: The preamplifier used in the thesis is a dual input differential amplifier. It has two differential input terminals and two differential reference input terminals. Just for explanation purposes, single input pair is shown in Figure 2.8. The preamplifier's design was done so that the decision circuit(Latch) could detect the input in the shortest possible time. The gain of the preamplifier is compromised to achieve high bandwidth.

- **Decision Circuit**:The latch must become susceptible to differentiate the mV level signal. The circuit uses regenerative feedback (positive feedback) from the cross-gate connection,

as shown in Figure 2.8. Latches are designed from the back to back inverters connections. Decision circuits work2 in two modes. When the preamplifier is disabled, the internal nodes of the latch are set to V_{DD}. It is called pre-charging. When the preamplifier is enabled, the differential output of the preamplifier is applied to the latch. The differential output of the preamplifier decides which one of the output are set to V_{DD} and the other to ground potential.[4]

- **Output buffer**: The purpose of the output buffer remove the glitches and convert the output of decision circuit into logical signal (V_{DD} or 0).

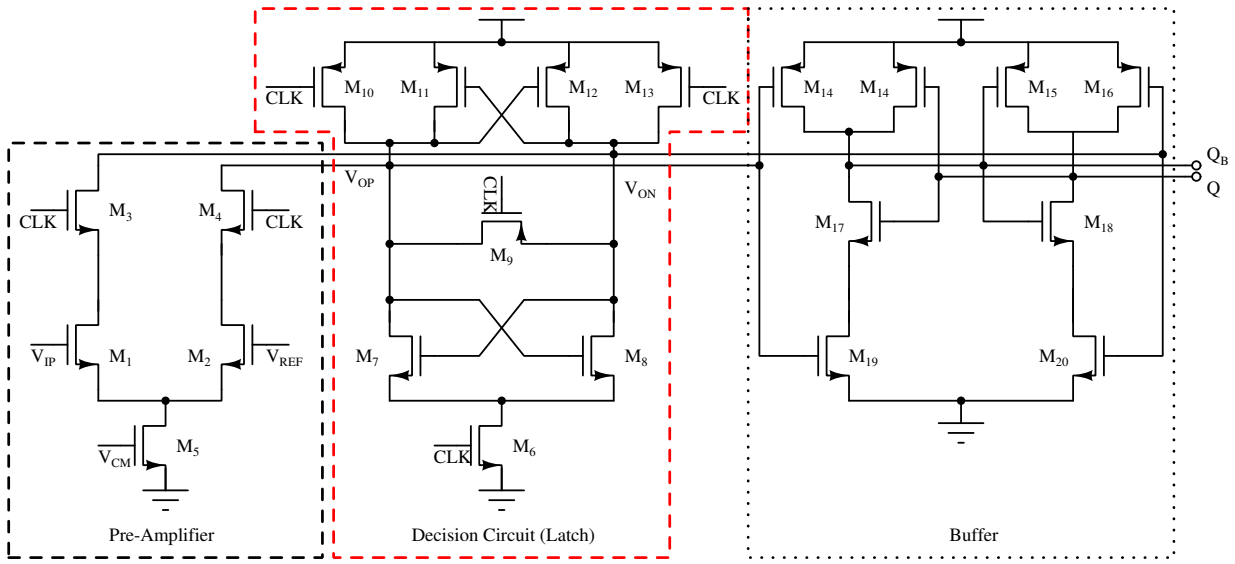


Figure 2.8: Preamplifier based Dynamic Comparator

2.5 1.5 bit Digital to Analog Converter

Proposed pipeline ADC generate 1.5bits/stage and residue signal is propagated. The residue signal is output of MDAC which scales the difference signal between input and reference voltage. The three different reference voltages are required to produce 1.5 bits resolution. The reference voltages are $+V_REF$, 0 and $-V_REF$. Selection of these reference voltages are done by thermometer code generated at the comparators output. The reference voltage generated using resistive ladder with rail voltages as V_{DD} and 0. Hence, This reference signals are generated with respect to analog ground, i.e, $V_{DD}/2$. The 1.5 bit DAC also called a 3:1 ana-

Q_1	Q_2	Q_{1B}	Q_{2B}	CTRL1	CTRL0	CTRL2	V_{DAC}
0	0	1	1	1	0	0	V_{CM} -V_{REF}
0	1	1	0	0	1	0	V_{CM}
1	1	0	0	0	0	1	V_{CM}+V_{REF}

Table 2.2: Truth Table of 1.5 bit DAC

log Multiplexer. Q_1 and Q_2 are control signals shown in Truth table Table 2.2 are the output of comparator which are thermometric in nature. Figure 2.9 shown below is schematic of 3:1 analog mux

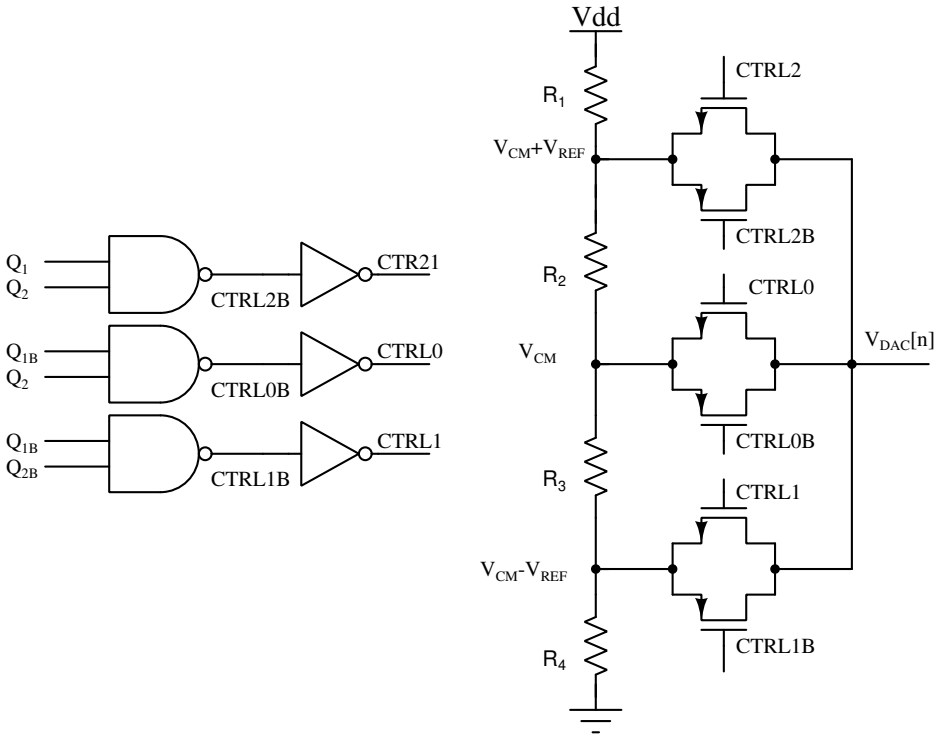


Figure 2.9: 1.5-bit DAC (3:1 Analog Mux)

2.6 Digital Bit Alignment and Correction

The output of the pipeline stages is evaluated at different clock cycles. Until all the digital bits are not present, the bit correction algorithm cannot be applied. Conventionally, i^{th} stage data must be stored for N-i clock cycles. Output bits from all the stages are buffered until all are unavailable, as shown in Figure 2.10. D flip flop is one solution to store or buffer the output bits for few cycles. Once all the bits are synchronized, they are applied to a series of full adders and half adder. The sum is the converted data bit, and carry is propagated.

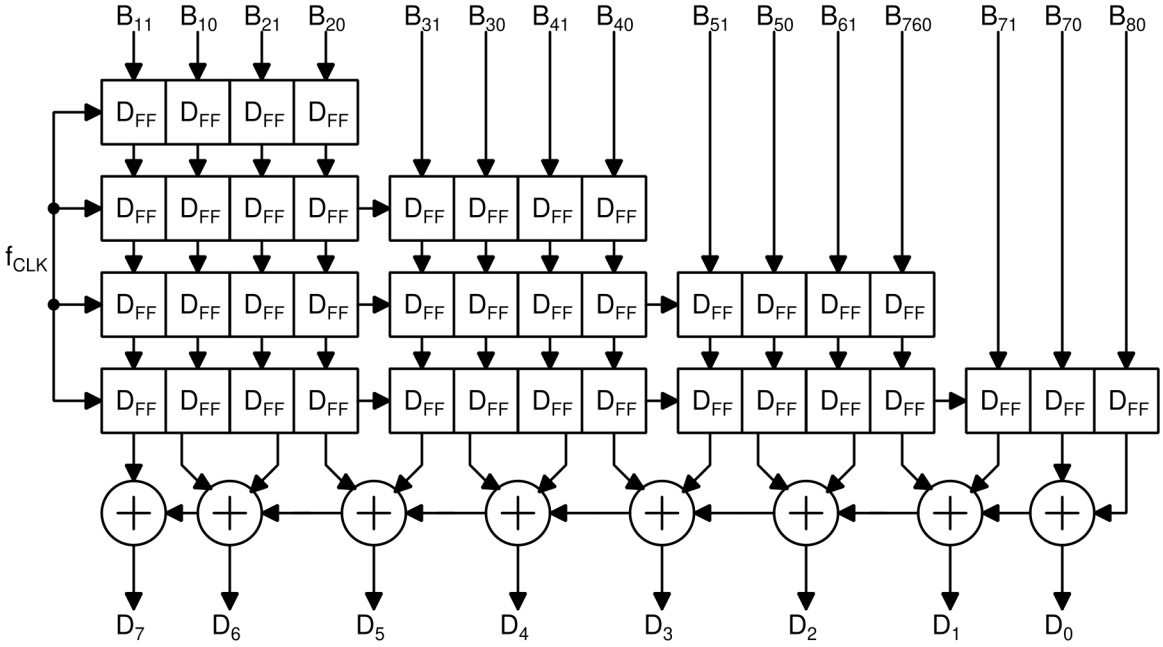


Figure 2.10: Bit Align and Correction Unit

Chapter 3

Ring Amplifier Theory

The pipeline ADC is a better choice for high-speed, high-performance applications. However, conventional pipeline ADC designs rely on the operational amplifier. With scaling in technology, supply scales too, which causes a lower signal swing. The power requirement is increased to compensate for the gain degraded due to scaling. Innovating a new compensation technique can resolve the problems faced by amplifiers, but it consumes more power. These methods will not provide the ability to scale with technology. Features like high speed, high bandwidth, high gain, rail-to-rail output swing, and performance which technology scaling like Digital circuits, are essential for designing amplifiers in the current time. Several approaches are explored, and one of them is the Ring Amplifier.

3.1 Conventional Ring Amplifier

The ring amplifier charges the large load capacitance through slew-based charging. It performs the dynamic current adjustment using the class-AB structure as the output stage. During amplification, only one of the transistors is on (either PMOS or NMOS). Hence, It can achieve

rail-to-rail output swing.A ring amplifier's basic building block is an inverter that takes advantage of technology scaling very efficiently. The ring amplifier structure resembles with ring oscillator. Fundamentally, it is three inverters cascaded, which provide very high gain. The single inverter could not provide the very high gain required for switched capacitor amplifier, and the two cascaded inverters will not provide the 180° phase shift required for feedback action. These three cascaded inverters are unstable in the switch-capacitor network because this structure fails to create any dominant pole. All the poles are close to each other may result in a negative phase margin. The addition of external load capacitance can a create pole at output dominant, which is required for any SC circuit. Increasing the sizes of stage 1 and 2 transistors moves the poles at high frequencies. However, This is not the optimum solution.

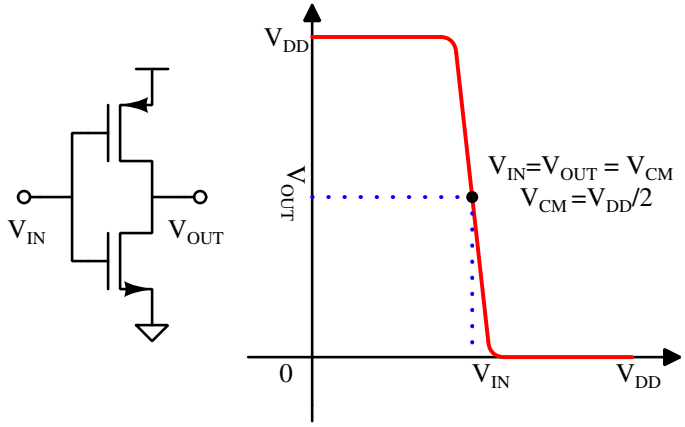


Figure 3.1: Inverter

Before moving to ring amplifier operation, let us look at the inverter and its characteristics, as shown in Figure 3.1. Inverter sizes are chosen so that the trip point (V_{trip}) is equal to V_{CM} ($V_{DD}/2$). When the input and the output of the inverter are at equal potential, the operating point is called V_{trip}. The common-mode voltage V_{CM} serves as the analog ground for the whole pipeline ADC. Inverters shown in Figure 3.1 are used in conventional ring amplifiers in Figure 3.2.

When the ϕ_{RST} is high, V_{IN} and V_A are V_{CM}. Input to the second stage inverters is V_{CM} - V_{OS} and V_{CM} + V_{OS}. The voltage difference across capacitors C_1 and C_2 are stored. This stored potential is called offset. It shifts the DC level of the output of the first stage inverter. The input of the second stage upper inverter is V_{CM} - V_{OS} resulting in $V_{BP} \approx V_{DD}$ due to inverter action. Hence, M_{CP} is off. Similarly, NMOS is off because the second-stage lower inverter is at the

V_{CM} + V_{OS} potential, as shown in Figure 3.3. **Transistors of the last class AB stage are turned off whenever the V_{IN} node moves towards to V_{CM} potential, which is steady-state condition of the ring amplifier.** This state is called reset mode.In this mode, output resistance increases as the Class AB stage moves towards a non-conducting state, causing a dominant pole at the output and stabilizing the ring amplifier. As NMOS and PMOS are turned off in the reset phase, there is no current path to charge the load capacitor. V_{OUT} potential is held at the common mode voltage V_{CM}.[5]

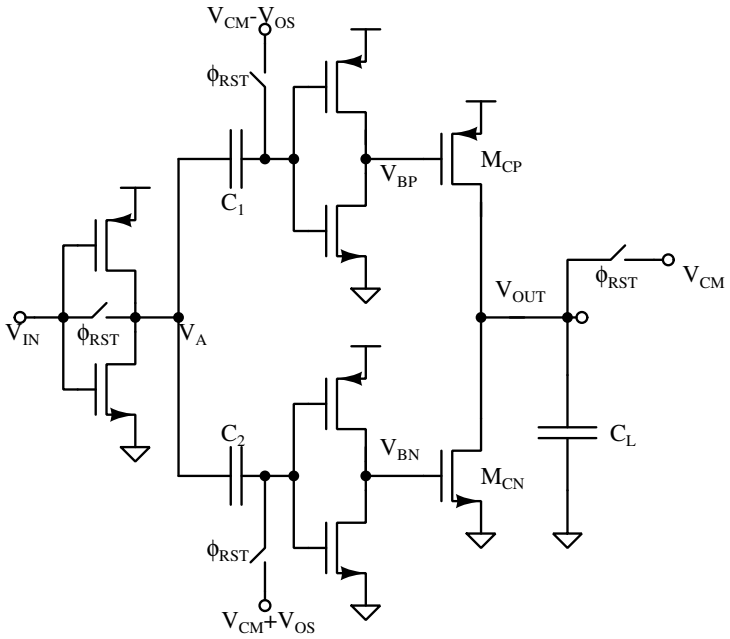


Figure 3.2: Conventional Ring Amplifier

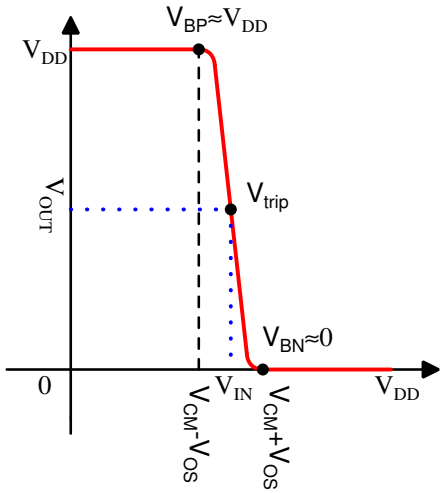


Figure 3.3: Second Stage Inverter Transfer Function

Equation 3.1 shows the condition for the ring amplifier to achieve stability. When the input is not equal to the V_{CM} then amplification action starts. Figure 3.4 depicts the dynamic current adjustment with respect to input of the ring amplifier.

$$V_{BP} > V_{DD} - |V_{thp}|, V_{BN} < V_{thn} \tag{3.1}$$

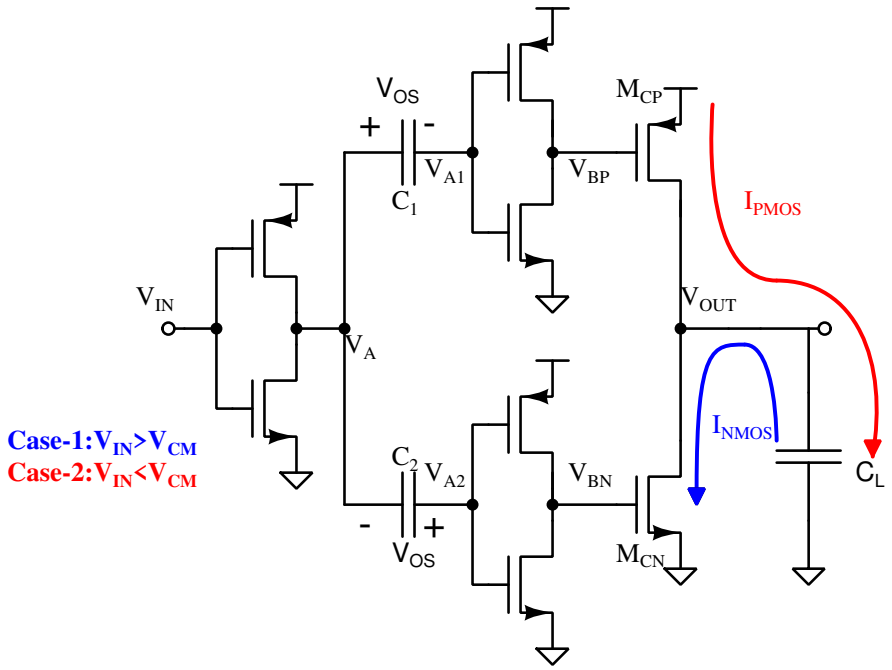


Figure 3.4: Class AB Action of Stage 3 Inverter of the Ring Amplifier

When the input node is deflected from V_{CM} potential, the first two stages of the ring amplifier activate one of the transistors of the third stage inverter, which charges or discharges the load capacitance.

- **Case-1** ($V_{IN} > V_{CM}$): Figure 3.5 illustrates the operation of the first two stages of the ring amplifier when $V_{IN} > V_{CM}$. Output of first stage inverter is given by the equation: $V_A = -(g_{mp}+g_{mn})(r_{op}||r_{on})$. Therefore node V_A will be lower than the common-mode potential. V_A with DC offset of $\pm V_{OS}$ given to the next inverter stage, which causes V_{BP} and V_{BN} transition to V_{DD}. PMOS of the third stage inverter is turned off, and NMOS is turned on. Load capacitance will start to discharge from common-mode potential, which is held in the reset phase as shown in Figure 3.4 with the blue color curve.Without feedback, load capacitance keeps discharging until it reaches the ground potential.

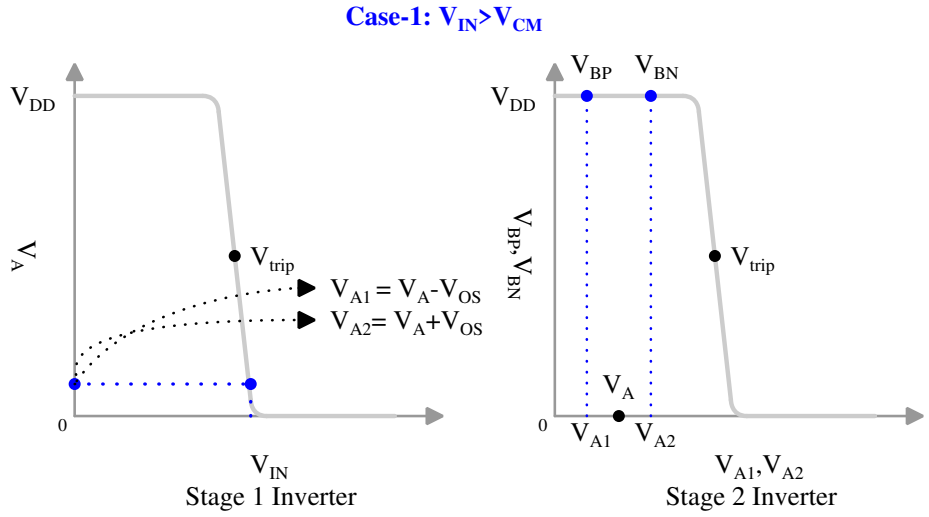


Figure 3.5: Stage 1 and Stage 2 Inverters Operation in Case-1: $V_{IN}>V_{CM}$

- **Case-2**($V_{IN} > V_{CM}$): Figure 3.6 illustrate the operation of the first two stages of the ring amplifier when $V_{IN} < V_{CM}$. Now, node V_A will be higher than common-mode potential. V_A with DC offset of $\pm V_{OS}$ given to next inverter stage causes V_{BP} and V_{BN} transition to 0. PMOS of the third stage inverter is turned on. and NMOS is turned off.Load capacitance starts charging from common-mode potential, which is held in the reset phase, as shown in Figure 3.4 with red color curve. Without feedback, load capacitance keeps charging until it reaches the V_{DD}.

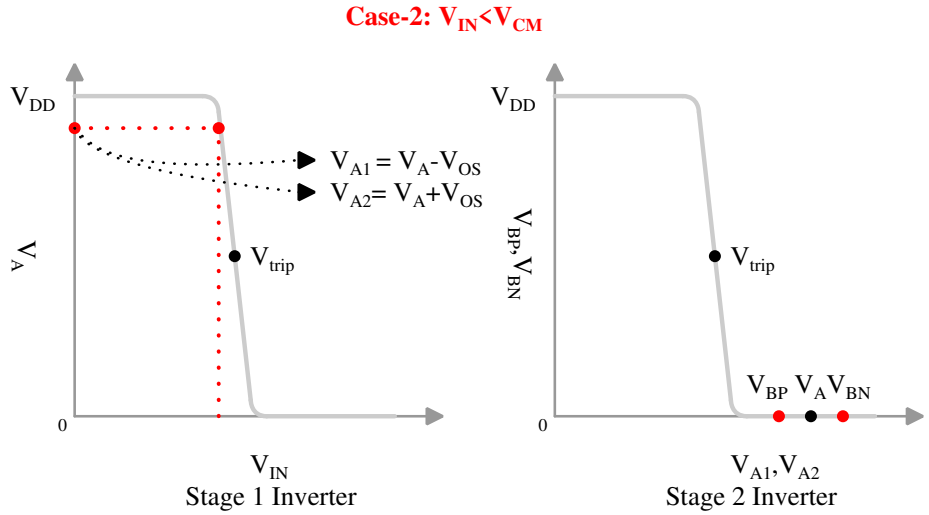


Figure 3.6: Stage 1 and Stage 2 Inverters Operation in Case-2: $V_{IN}<V_{CM}$

3.2 Self-Biased Ring Amplifier

The conventional ring amplifier achieves a very high gain with easy structure. In the third stage, PMOS and NMOS transistors are digitally controlled current sources; therefore, the ring amplifier efficiently provides a very high slew rate. However, the ring amplifier depends on the external bias voltages V_{OS}. Conventional ring amplifier is highly affected by the PVT variation. This section introduces the self-biased ring amplifier and explains its benefits. The offset is dynamically applied using an embedded resistor between the drain terminal of the second stage inverter. The below figure is a self-biased ring amplifier used to construct MDAC.[6]

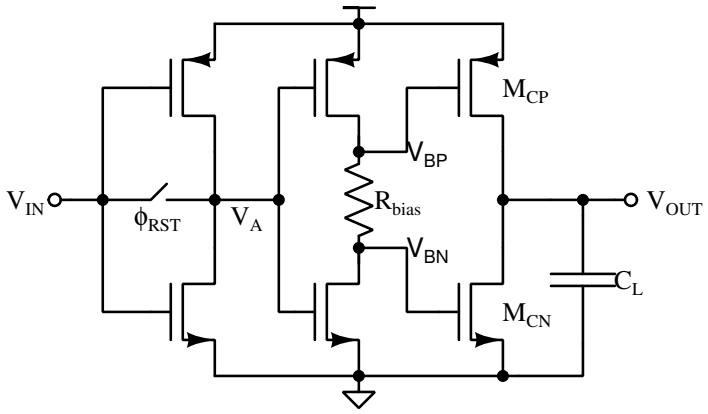


Figure 3.7: Self-Biased Ring Amplifier

Figure 3.7 has less number of inverters and offset capacitors also removed. Hence, power consumption can be reduced. R_{bias} dynamically applies the offset to the transistors M_{CP} and M_{CN}. The offset is easily varied using resistor value. The working of the self-biased ring amplifier is similar to the conventional ring amplifier. The current flowing through the resistor is equivalent to when a resistor is short-circuited. When the R_{bias} is short-circuited, the second stage inverter balanced at the trip point.

The condition limits the R_{bias} value that the steady-state NMOS of the second stage inverter must be in saturation. Otherwise, the ring amplifier's gain will reduce as the NMOS enters the triode region.

$$I_D = 0.5\mu_n C_{ox}\frac{W_n}{L_n}(V_{CM} - V_{thn})^2 \tag{3.2}$$

3.3 Multiplying DAC using Self-Biased Ring Amplifier

Section 3.2 describes the operation of MDAC, which is used in the pipeline ADC. This section discusses the detailed analysis of MDAC using the ring amplifier.

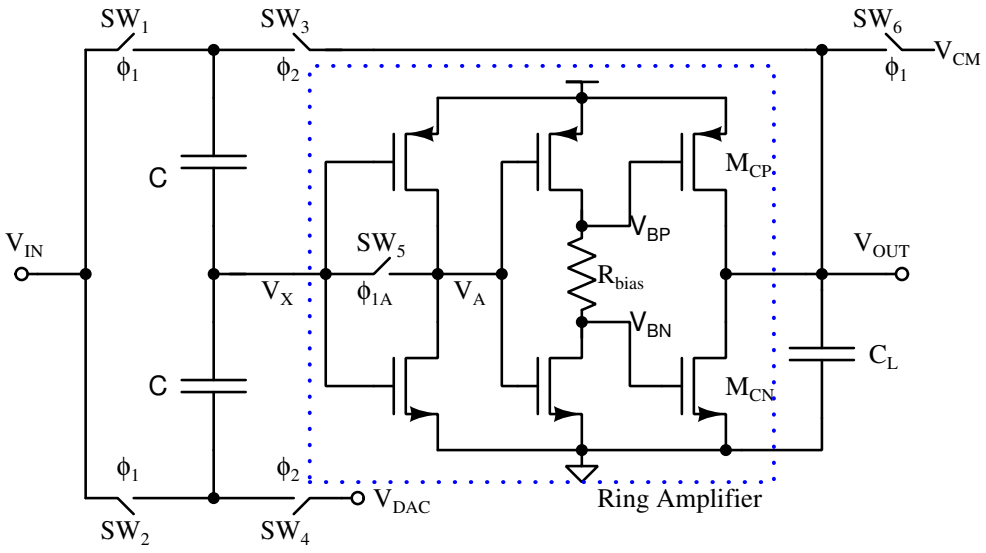


Figure 3.8: Single-Ended MDAC using ring Amplifier

The input signals V_{IN} and V_{DAC} are applied with respect to V_{CM} (analog ground). V_{CM} is also the trip point of the inverter described in section 3.1. The MDAC operates in two phases, one is the sampling phase, and the other is the amplification phase. Both the phases are non-overlapping clocks to avoid errors due to clock feed through and charge injection of switches.

Reset Phase: Switch SW_5 is closed , and the ring amplifier's first stage is balanced at the trip point ($V_X = V_A = V_{CM}$). Input is sampled in the sampling capacitor C. Charge at node X is given by equation 3.3.

$$Q_X = -2C(V_{IN} - V_{CM}) \tag{3.3}$$

If the bias resistor is short-circuited, the output of the second stage inverter would be V_{CM}. However, due to the presence of a resistor, the output is split into two different potential levels, V_{BP} and V_{BN}. The PMOS of the second stage has to be in saturation, so $V_{BP} \leq V_{DD}/2 + V_{thp,2}$. The maximum value of V_{BN} is given by $V_{BN} \geq V_{DD}/2 - V_{thn,2}$ to keep the NMOS in

saturation. While keeping second-stage transistors in saturation, V_{BP} and V_{BN} must keep third-stage transistors in the sub-threshold or cut-off region. The maximum value of V_{BP} required to make PMOS of the third stage off is given by V_{DD} - $V_{thp,3} \leq V_{BP}$. V_{BN} has to be smaller than $V_{thn,3}$ to maintain NMOS of the third stage in the cut-off region.

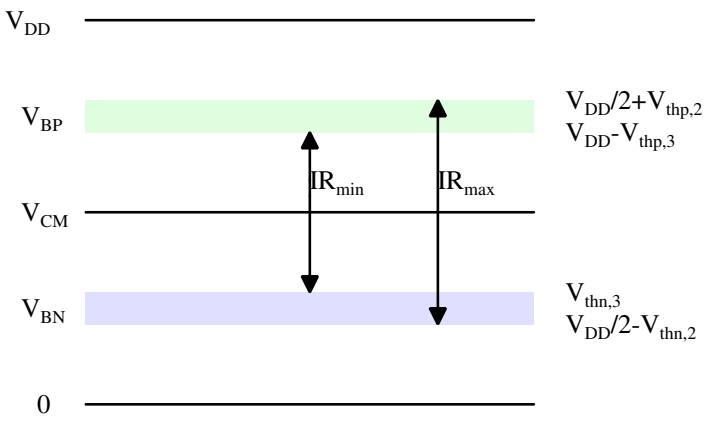


Figure 3.9: Available Range of V_{BP} and V_{BN}

Figure 3.9 shows an available range of V_{BP} and V_{BN}, which maintains the ring amplifier steady when V_{IN} moves towards V_{CM}. If the difference between V_{BP} and V_{BN} is smaller than IR_{min}, then the last stage doesn't turn off properly, and the stability of the ring amplifier is compromised. If the difference between V_{BP} and V_{BN} is more extensive,, then the ring amplifier will stabilize anywhere in the given range, which can cause an accuracy problem.[6]

When ϕ_1 is low, all the switches are opened. This is a non-overlapping period. Node V_X is stable at the V_{CM}, and the ring amplifier is off. Node V_{OUT} is also held at the V_{CM}. **Amplification Phase:** When ϕ_2 is high, SW_3 and SW_4 are closed. Node V_X is now floating, and the charge at node V_X is given by equation 3.4

$$Q_X = -2C(V_{DAC} - V_X) - C(V_{OUT} - V_X) \tag{3.4}$$

Equating Equations 3.3 and 3.4 and solving the equation to determine the value of the node V_X when the ϕ_2 is just high. At this instant, V_{OUT} is still held at V_{CM}.

$$V_X = -V_{IN} + V_{DAC}/2 + 3V_{CM}/2 \tag{3.5}$$

As defined before, V_{CM} is analog ground, therefore removing all the V_{CM} component and reevaluating equation 3.5,

$$V_X = -V_{in} + V_{dac}/2 \tag{3.6}$$

Values generated at the output of the DAC, as explained in section 2.5, are $+V_{REF}$, 0, and $-V_{REF}$ with respect to V_{CM}. As explained in section 3.1, When $V_X < V_{CM}$, PMOS of the last stage inverter is on, and NMOS is turned on when $V_X > V_{CM}$. As per equation 3.6, the ring amplifier decides and provides the current to charge or discharge the load capacitance.

V_{OUT} starts to charge or discharge, and feedback action emerges. Input node V_X starts to move towards the V_{CM}. Using equations 3.3, 3.4 and substituting $V_X = V_{CM}$ where ring amplifier is stable and last stage inverter is turned off. Equation 3.7 provides the output level with respect to V_{CM}.

$$V_{out} = 2V_{in} - V_{dac} \tag{3.7}$$

Output of Sub-ADC	**Output of DAC**	**Output of MDAC**
00	$-V_{REF}$	$2V_{IN}+V_{REF}$
01	0	$2V_{IN}$
10	V_{REF}	$2V_{IN}-V_{REF}$

Table 3.1: Residue Output with sub-ADC Output

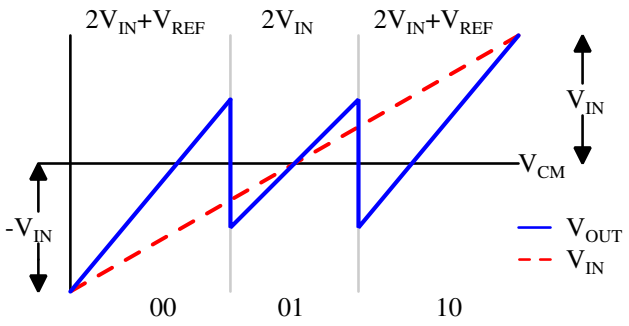


Figure 3.10: Residue Output

Chapter 4

Design Methodology

The proposed pipeline ADC uses differential input signals and generates residue signals throughout the pipe lining process for further processing while producing 1.5 bits per stage. Switched-capacitor and the latched comparator are the main blocks of the process. In this chapter, Ring amplifier design, comparator and switches are presented.

4.1 Ring Amplifier Design

Following parameters are considered for ring amplifier design:

Gain: Inverter gain is given by Equation 4.1. The small-signal gain is a function of the channel length(L). If L is increased, the gain increases, but the bandwidth reduces. Hence, the smallest length must be chosen to satisfy the gain and bandwidth requirement. Gain and bandwidth requirement is fulfilled by the length equal to 90nm for the first two stages. The third stage is operating as current sources; the length is kept 60nm. R_{bias} affects the gain of the ring amplifier directly. NMOS of the second stage inverter work in the triode region if the R_{bias} is large.[7]

$$A_v = (g_{mN} + g_{mP})(r_{oN} || r_{oP}) \tag{4.1}$$

Noise: The first stage is the dominant source of the noise. Thermal noise is given by equation 4.3. The power of the first stage can be minimized by maximizing trans-conductance.

$$\overline{v_{n,in}^2} = \frac{8kT}{3(g_{mN} + g_{mP})} \tag{4.2}$$

Stability: Every inverter stage contributes a pole -the dominant pole created by the third stage, biased in the low conduction region. As the difference between V_{BP} and V_{BN} increases, the phase margin improves but reduces the bandwidth.

$$\frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{g_{m1}.r_{o1}.g_{m2}.r_{o2}.g_{m3}.r_{o3}}{(1+s/P_1)(1+s/P_2)(1+s/P_3)} \tag{4.3}$$

Where, $P_1 = 1/r_{o1}C_1$, $P_2 = 1/r_{o2}C_2$ and $P_3 = 1/r_{o3}C_L$. The value R_{bias} is selected such way that with r_{o3} and C_L forms a dominant pole without affecting gain and accuracy.

Speed: The settling time required for the ring amplifier depends on slewing time and stabilization time. The slew rate is given by equation 4.4 The stabilization period is the time from the first overshoot to steady-state output. For proper operation, the overshoot needs to be minimized.

$$SR = \frac{I_{RAMP}}{C_L} = \frac{\mu C_{ox} W_3 (V_{GS} - V_{th})^2}{2.C_L L_3} \tag{4.4}$$

$$V_{overshoot} = I_{ramp}.\frac{T_{delay}}{C_{load}} \tag{4.5}$$

Whereas, T_{delay} is total loop delay. Therefore, optimum values has to found between slew rate and delay.[5]

4.1.1 Implementation of the Ring Amplifier

High gain, high bandwidth, and the trip point balanced at the V_{CM} are the critical parameters for the inverters used in the ring amplifier. Stage 1 and stage 2 inverters are identical, but the only parameter variable is multipliers of the transistors depending upon their functionality.[7]

A higher multiplier number is required for the first stage to increase the gain because stage 1 is the primary noise source. The parasitic capacitance seen from the input terminal is kept to a minimum, so the effect is minimal in the amplification phase. Stage 2 multiplier contributes to the dead zone and delays the amplification process. The higher the multiplier, the faster the response to the voltage change, but the current will be higher. The IR drop will cause the turning off of the third-stage transistors at lower input levels. Stage 3 inverter sizes are decided by the slew rate requirement to charge the load capacitance. For the proposed ADC, the slew rate is 0.5mV/ps, and Load capacitance is 300fF. The target current from the last stage should be greater than 150μA. Therefore, device sizes are selected as shown in Table 4.2. R_{bias} value is determined by the lower bound of third stage PMOS and upper bound of the third stage NMOS as mentioned in Figure 3.9.

	$\mathbf{R}_{bias}$	$\mathbf{C}_{load}$
Value	8k	300f

Table 4.1: Resistor and Load Capacitor Sizes

Transistor	**MP1**	**MN1**	**MP2**	**MN2**	**MP3**	**MN3**
W	2.805μ	1.11μ	2.805μ	1.11μ	300n	135n
Multiplier	12	12	2	2	2	2
L	90n	90n	90n	90n	60n	60n

Table 4.2: Device Sizes of the Ring Amplifier

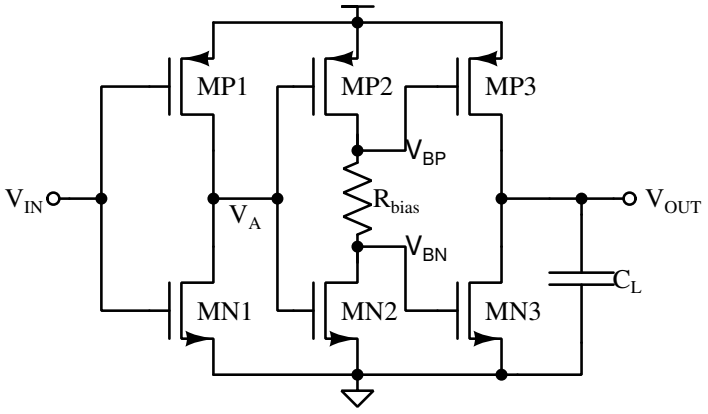


Figure 4.1: Schematic of the Ring Amplifier

4.2 Switch Design

Switches are used in the proposed pipeline ADC are complementary switches. The switch designs are limited due to Charge injection, clock feed through, thermal noise, and input dependent on resistance. In this section, this problems is discussed, and device sizes are presented.[8]

- **Charge Injection Error:** Switch designed using MOS transistor carries a finite amount of charges in 'on' state. When the switch is turned off, charges redistribute between the source and drain terminal of the transistor. This redistribution of charges causes errors in the output terminal. This error is known as a Charge injection error. This error can cause a dc offset error in the pipeline ADC.

- **Clock Feed-Through:** Capacitance between gate-source and gate-drain are coupled when clock edge arrives. This error is independent of the input as gate-source, and gate-drain capacitance is constant.

- **Thermal Noise:** Poor switch design is a dominant source of thermal noise in the switch-capacitor circuits. The on-resistance of the switch generates thermal noise. RMS noise voltage is given by $\sqrt{kT}/C$. The thermal noise limits many high-precision applications. It can be minimized by increasing the sampling capacitor but simultaneously degrading the operation's speed.

One of the solutions to minimize the charge injection and clock feed through error is

complementary switches. PMOS and NMOS possess charges that are opposite in polarity. If the PMOS compensates for the charge injected by NMOS while turning off, the charge injection problem can be minimized. Differential sampling circuits are one approach to mitigate the charge injection error.

Bottom plate sampling is used in the switched capacitor MDAC to minimize the supply-dependent charge errors. Figure 3.8 illustrate the operation of the bottom plate sampling. During ϕ_1, input is sampled on the sampling capacitor. Before the sampling phase ends. reset switch of the ring amplifier is opened so when ϕ_1 ends, the path has already cut off for the supply-dependent leakage charges.

One of the primary parameters of harmonic distortion is the non-linearity of the switch. When the device works in the linear region, the R_{on} resistance is dependent on the input voltage. This is quite undesirable in the conversion process. The device sizes are kept high to minimize this phenomenon, so the variation in on-resistance does not affect the overall performance.

In section 3.3, the operation of MDAC is explained, and Table 4.3 gives the sizes used to construct the complementary switches for the MDAC circuit.

Switch Name	**PMOS W**	**NMOS W**	**L**
Sampling Switch SW1, SW2	5u	5u	60n
Reset Switch SW5	1.8u	1.8u	60n
Output Switch SW6	5u	5u	60n
Amplification Switch SW3,SW4	2.05u	2.05u	60n

Table 4.3: Device Sizes of the Switches used in MDAC

4.3 Comparator Design

In this section, the comparator design approach is presented. In the pipeline ADC, the accuracy requirement of the comparator is relaxed.

Preamplifier: For the presented thesis, the main design requirement for the preamplifier is the bandwidth. The gain and bandwidth product is directly proportional to the tail current. Preamplifier gain reduces the latch offset when seen from the input end. Therefore, 50 μA is chosen so that the bias voltage required is common-mode voltage—no need for a biasing circuit. Figure 4.2 shows the decision circuit represented by load[9].

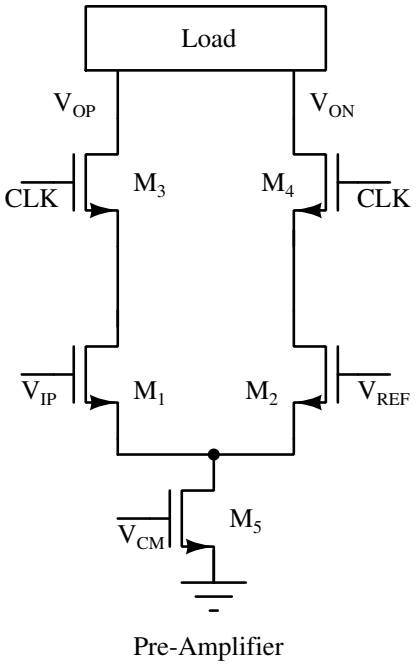


Figure 4.2: Schematic of the preamplifier

Latch or Decision Circuit: The amplified signal from the preamplifier is applied to the latch when the clock is high. The regenerative action starts, and the decision circuit produces the result. To work faster and efficiently, the difference between the output of the preamplifier has to be larger. Figure 4.3 shows the schematic of the latch. Once the decision process is completed, the output is buffered to remove the glitches for the further process. Figure 2.8 is given in subsection 2.4.1. Table 4.4 gives the sizes of the devices used in the preamplifier based on clocked comparator.

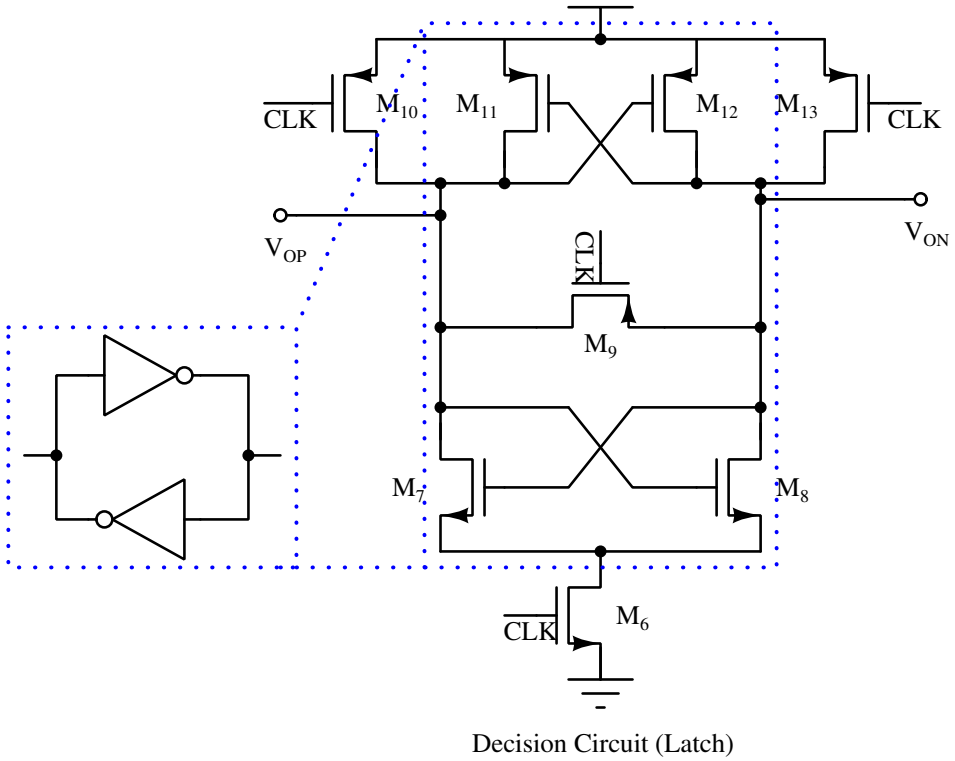


Figure 4.3: Schematic of the Latch

	W	L
Preamplifier	3u	60n
Latch	2u	60n
Buffer	2u	60n

Table 4.4: Device Sizes of the Preamplifier based Comparator

4.4 Single Stage of the Pipeline

Figure 4.4 shows the operation of the single-stage in the pipeline ADC. This section integrates a single stage from modular blocks like MDAC, Sub-ADC, and the DAC.In the earlier chapter, the concepts are illustrated using the single-ended components. In this section, all the components shown are differential. Differential signals are used to minimize the processing errors and increase the pipeline ADC's full output swing. Figure 4.6, 4.7, and 4.8 represent differential MDAC, differential reference voltages select for MDAC, and dual input differential

comparator, respectively.

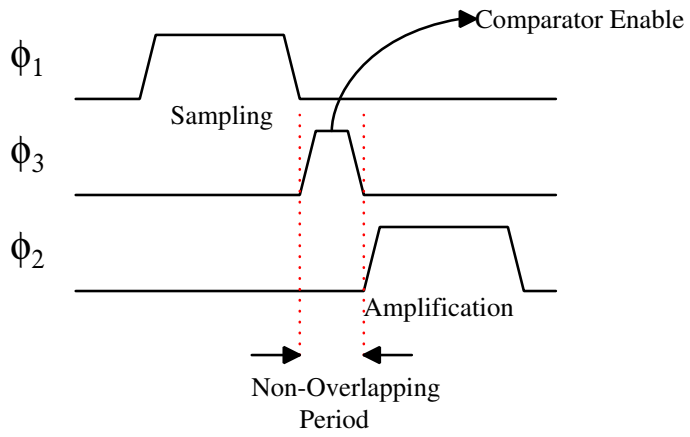


Figure 4.4: Operation of the Single Stage with Clock Phases

Compared to Figure 3.8, Figure 4.5 is modified for ϕ_2 operation. Control signals are enabled only when ϕ_2 is high, therefore SW4 is no longer required. Figure 4.5(b) represents symbolic view of the MDAC and it is also represents the functionality of the MDAC.

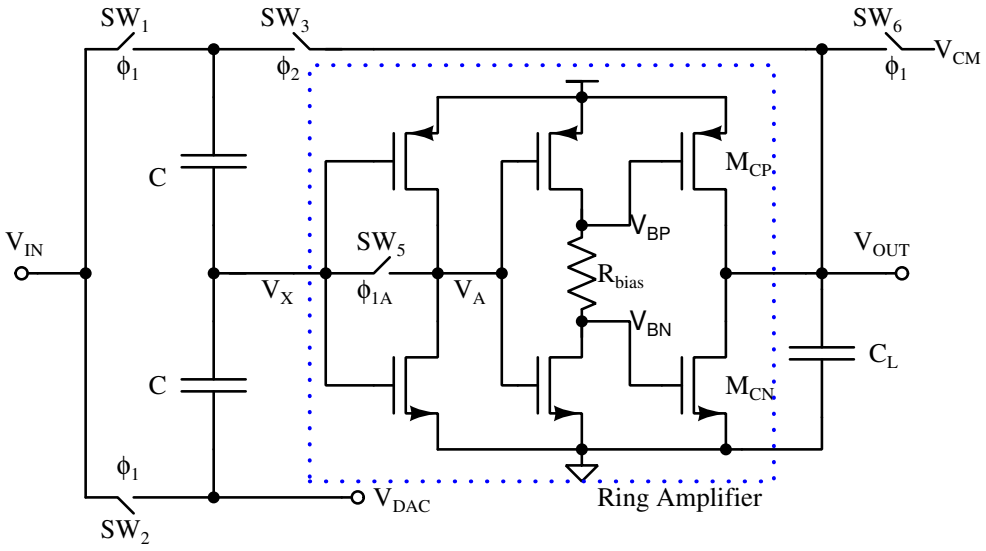
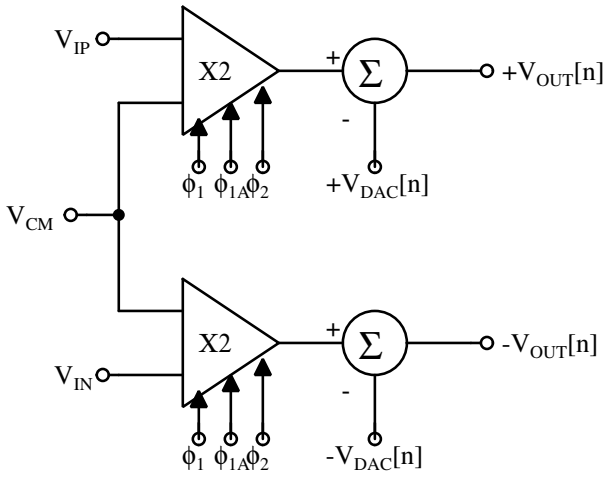


Figure 4.5: (a) Single Ended MDAC with Modified Schematic and (b) Symbolic Representation

Figure 4.6 represents construction of pseudo differential MDAC. Pseudo differential MDAC is used to minimize the errors arise due to switches and amplifier at the comparator input.



(a)

Figure 4.6: Symbolic Representation of the Pseudo-Differential MDAC

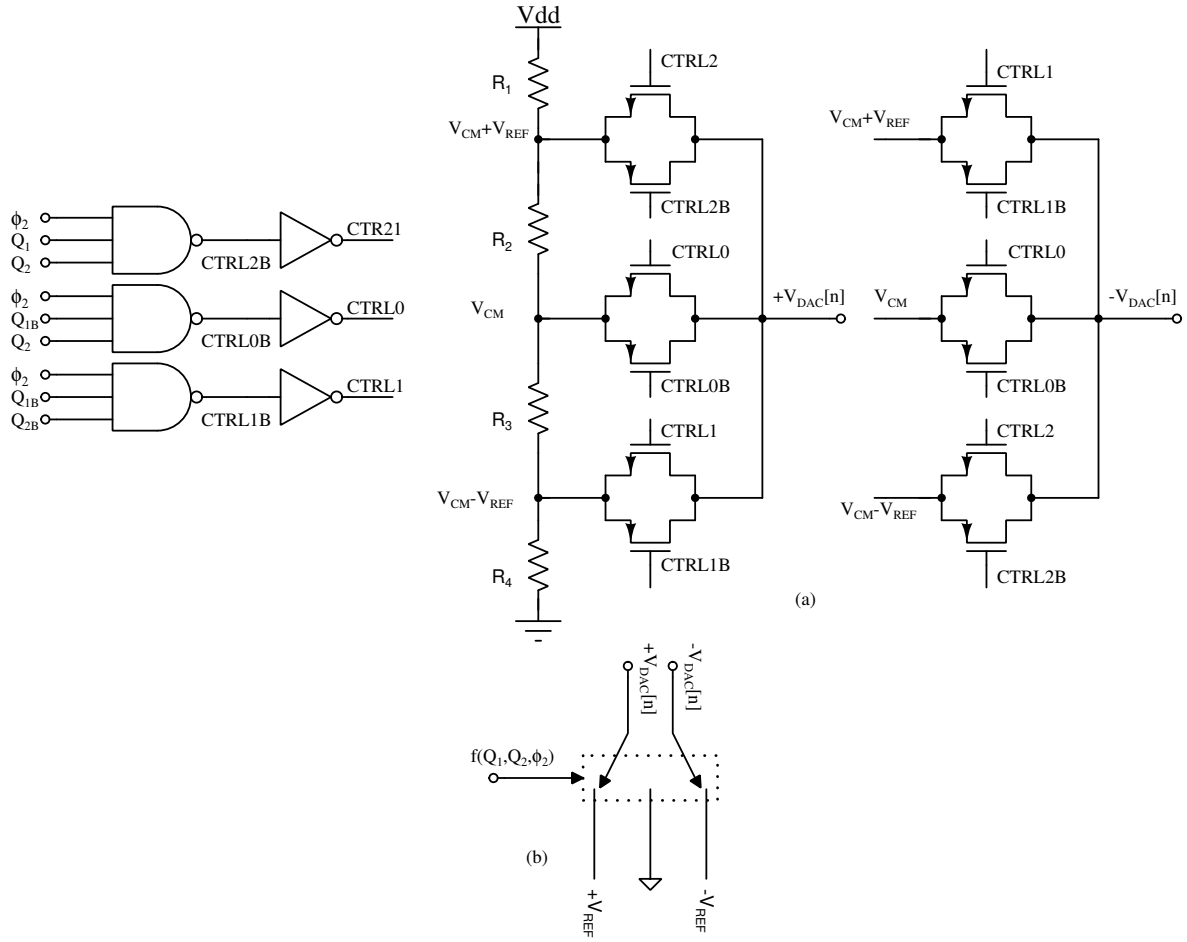


Figure 4.7: (a) Differential Reference Voltage Select for MDAC (b) Symbolic Representation

Figure 4.8 represents dual input differential comparator. The current flowing through transistor M_3 and M_4 are split into 2 different path each.

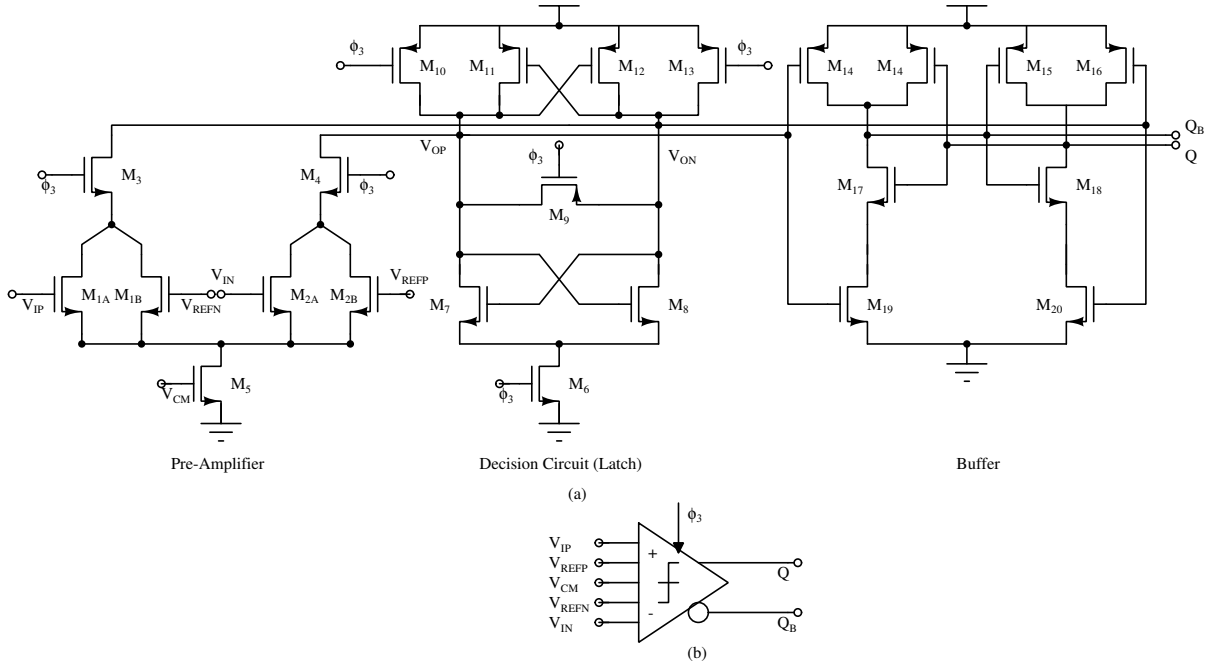


Figure 4.8: (a) Latched Comparator (b) Symbolic Representation

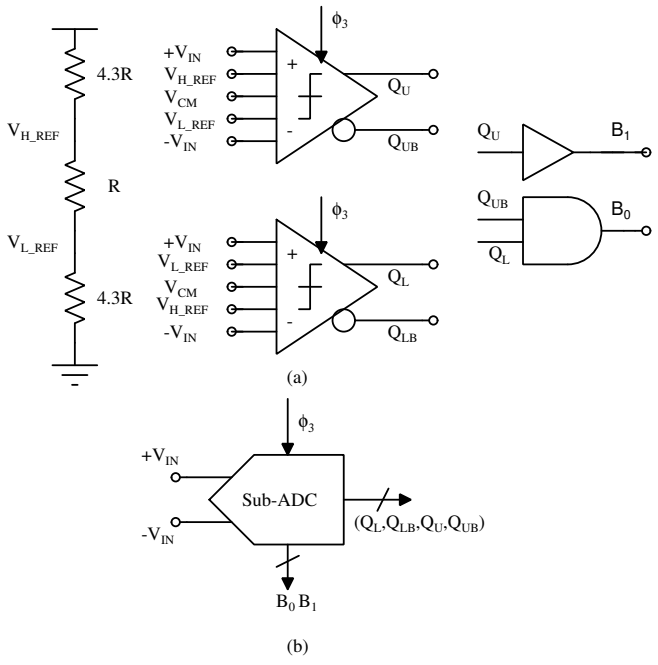


Figure 4.9: (a) Sub-ADC Schematic (b) Symbolic Representation

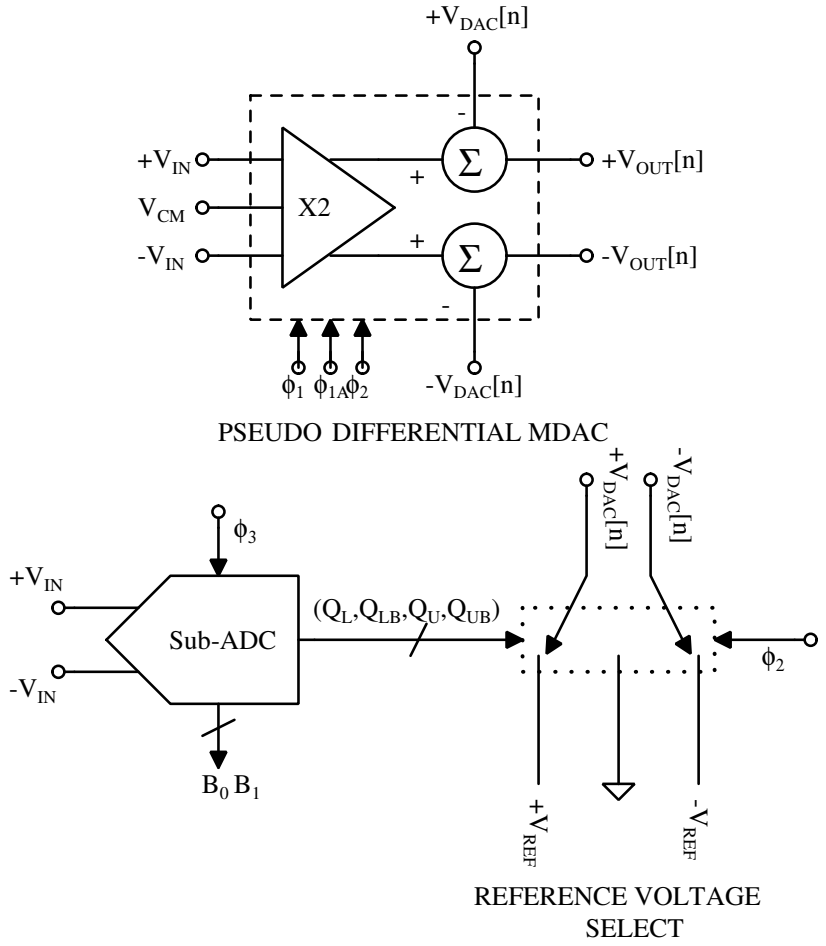


Figure 4.10: (a) Complete Schematic of the Single Stage of the Pipeline ADC

4.5 Complete Pipeline ADC

Section 2.2 explains the pipeline ADC and clocking scheme. In this section, pipeline stages are cascaded, and a complete schematic is presented with all the clock phases. Figure 4.11 represents the operation of pipeline ADC according to the clock scheme. There are four clock phases primarily. In the single clock cycle, two stages perform different operations and generate output bits. These bits are buffered using a D flip flop shown in Figure 2.10. This bits are corrected using half adder and full adders.

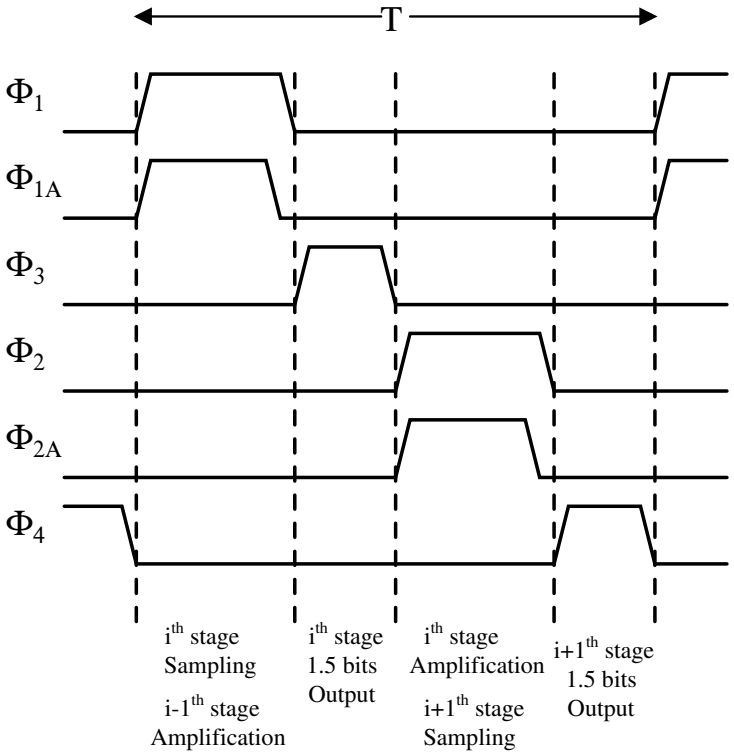


Figure 4.11: Pipeline Clock Scheme

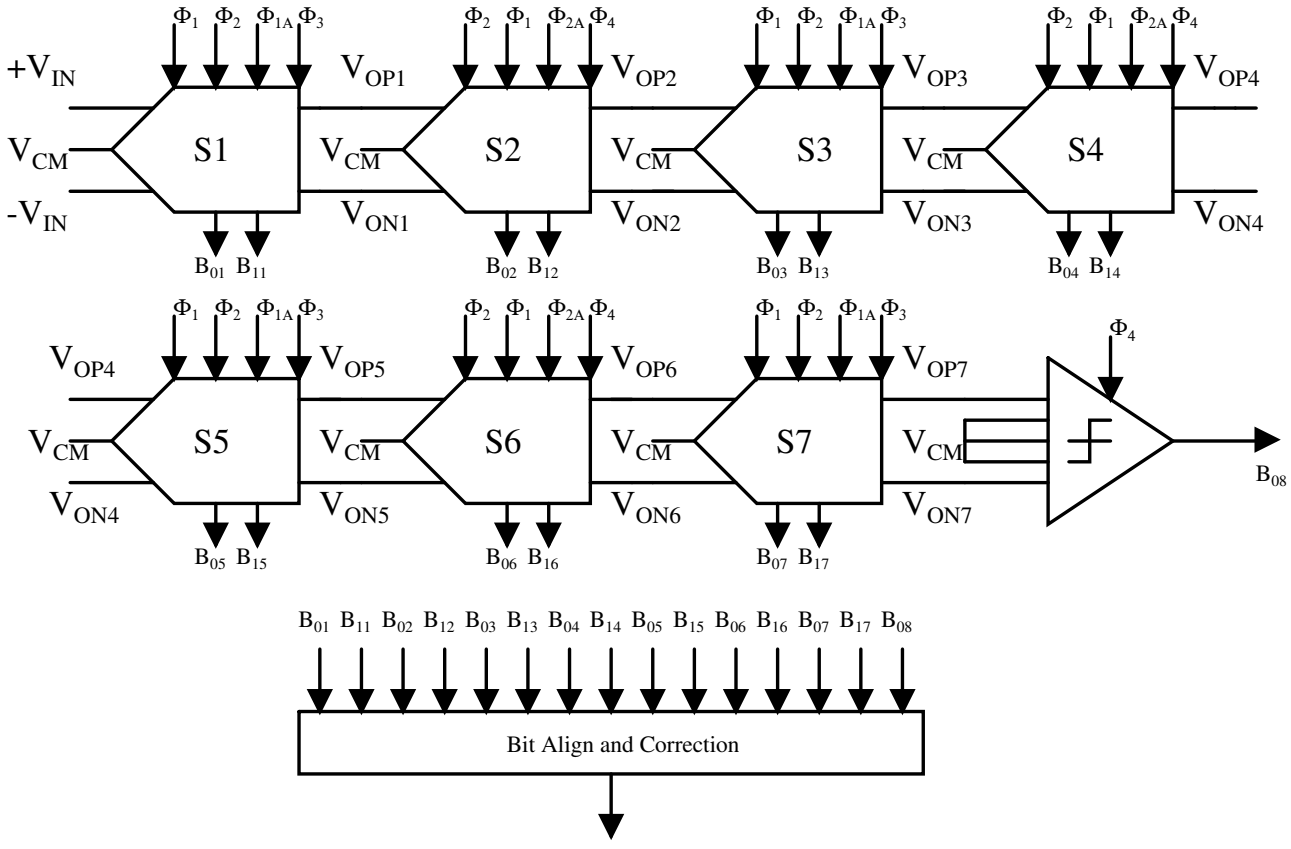


Figure 4.12: Complete Pipeline ADC

Chapter 5

Simulations and the Results

5.1 Switch

An 8-bit pipeline ADC has ideal SNR of (A^2/2)/(Δ^2/12), *Delta* is LSB. In the proposed thesis, LSB is $\Delta = V_{FS}/2^8$ = 1/256 = 3.90625mV. One source of SNR degradation is kT/C noise of the sampling circuit. Practical SNR is given by equation 5.1.

$$SNR = \frac{A^2/2}{(kT/C) + (\Delta^2/12)} \tag{5.1}$$

For Δ = 3.90625mV and at room temperature (300K), capacitor value is determined for SNR loss less than -0.1dB. Therefore, solving equation 5.2, sampling capacitor has to be less than 1.3×10^{-15}F. Sampling Capacitor value s decided to 100fF.

$$10\log\frac{\frac{\Delta^2}{12}}{\frac{\Delta^2}{12} + \frac{kT}{C}} < -1dB \tag{5.2}$$

The acquisition time of the sampling switch must be less than $T_{CLK}/2$. The difference between V_{IN} and V_{OUT} must be very less than Δ. Assuming worst condition, $V_{IN} = V_{FS}$, f_{sample} = 200MHz. The R_{on} of the switch is given by equation 5.3. The R_{on} should be very less than 4.5kΩ[10].

$$R_{on} << \frac{1}{C.N.f_{sample}.2\ln 2} \tag{5.3}$$

NMOS and PMOS device sizes are kept the same to create identical parasitic capacitance between gate-source and gate-drain terminal as clock feed through error is dominates at the 200MHz sampling frequency. All the switch sizes are decided such that R_{on} of the switch is less than 4.5kΩ.

5.1.1 On-Resistance of the Switch

Load resistance is kept high so the voltage drop across the switch can be accurately measured. Input voltage is swept, and the equation $R_{SW} = \frac{V_{IN}-V_{OUT}}{I}$ determines the value, where current I flows through the large resistance. Figure 5.1 represents the test bench to analyze the DC resistance of the switch. Average on-resistance for the reset switch, Amplification switch, and sampling switch are 811Ω, 710Ω and 288Ω, respectively.

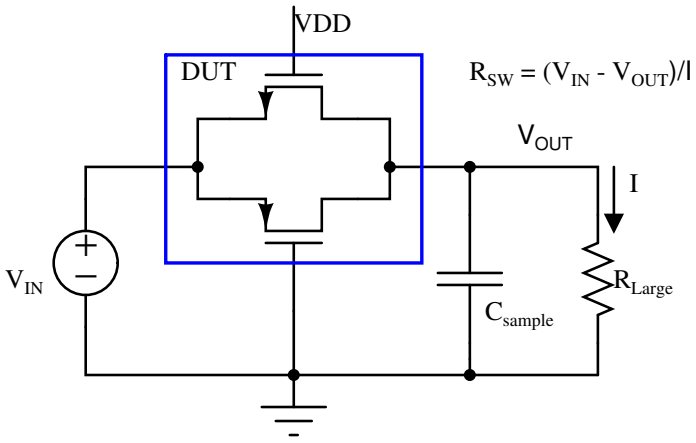


Figure 5.1: Test Bench for the R_{on} as function of input

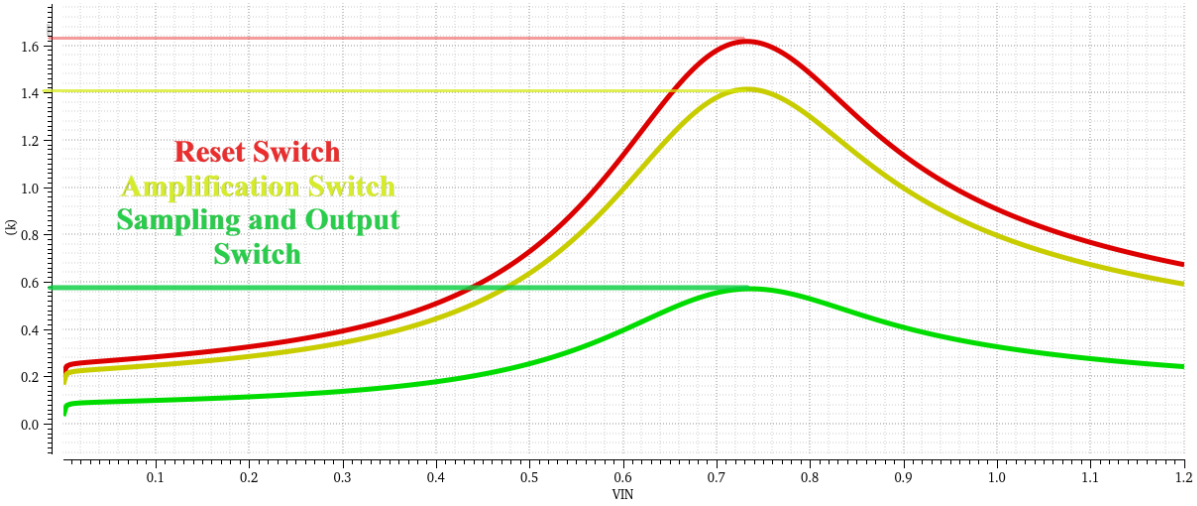


Figure 5.2: R_{on} Resistance of the Switches

5.2 Ring Amplifier

Ring amplifier is made of three cascaded inverter stage where every inverter have its own pole p = $1/(r_o C_p)$. This cascaded inverter achieves a high gain. Ring amplifier has aspects like slew rate, dead zone, and delay, which are analyzed using the simulations. Ring amplifier have three poles at each output node of the inverter. The stability of the ring amplifier depends on the location of the poles. Therefore the ac simulation is required. The dead-zone analysis is essential to understand the range of input where the ring amplifier is off—the third stage of the ring amplifier function as a current source. The effect of the different currents on how affects the dead zone is analyzed. Finally, transient simulation is performed with variable parameters.

5.2.1 Open Loop Gain Measurement

Figure 5.3 represents the AC simulation test bench. Open-loop gain and phase are plotted. Unity gain bandwidth, and the Phase margin is noted. The DC gain of the ring amplifier is 61.1 dB, and the unity-gain bandwidth (UGB) is 445.2MHz. The phase margin of the open-loop system is 71°[11].

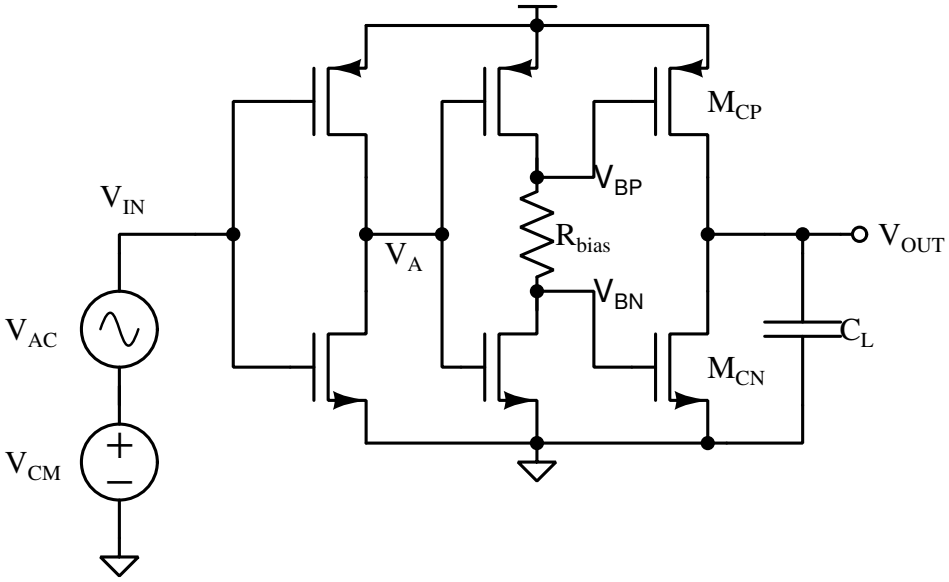


Figure 5.3: Test Bench for the Ac analysis

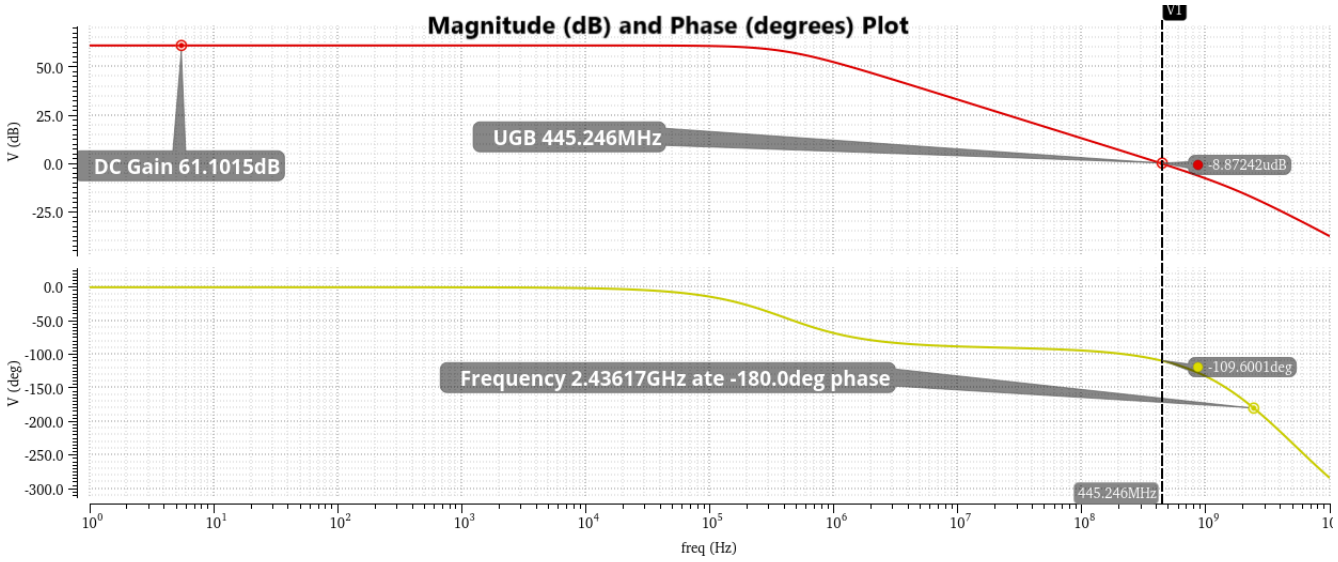


Figure 5.4: Magnitude(in dB) and Phase (in degrees) Plot

5.2.2 Dead Zone Variation

Figure 5.5 represents the test bench to analyze the dead zone dependence on the R_{bias}. DC input is swept, and current through the output node is measured and plotted. As R_{bias} is reduced, the voltage drop across the resistor will be less. Therefore, the input-referred range for which the ring amplifier turns off. This can cause oscillations during amplification because any

current source device fails to turn off. When R_{bias} is increased, the voltage drop results in faster turning off the current sources. This causes accuracy issues in ring amplification.[5]

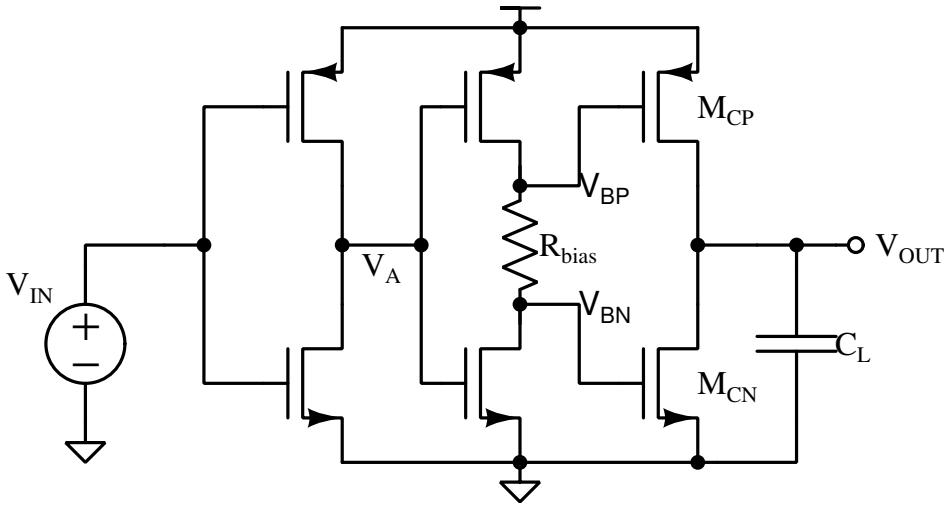


Figure 5.5: Dead Zone Analysis Test Bench for the Ring Amplifier

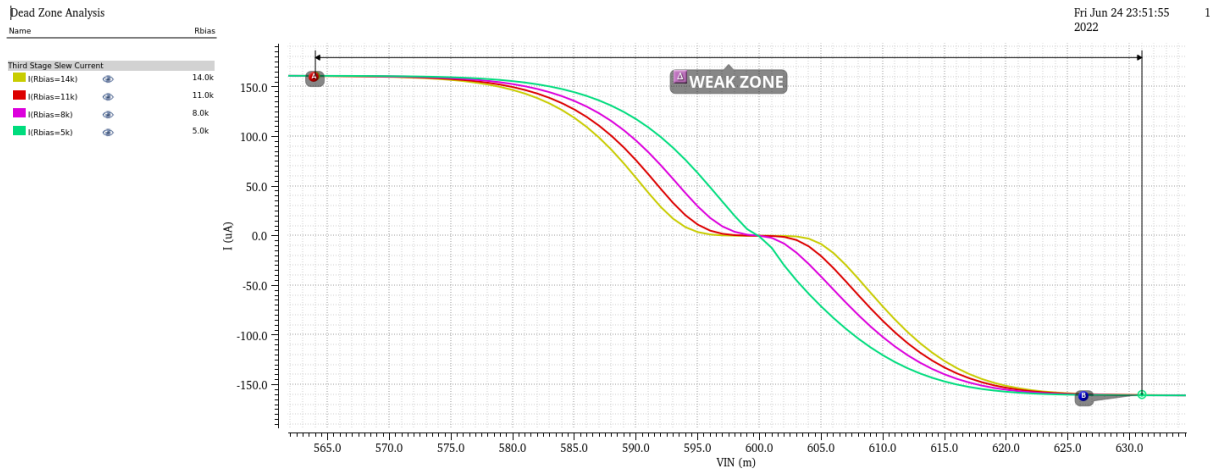


Figure 5.6: Dead Zone analysis using variation in the R_{bias}

When the width of the stage 2 inverter device is varied, the current flowing through the resistor will vary and cause a change in a dead zone. Figure5.7 shows the variation multiplier of the stage 2 inverter and proportionally change in a dead zone. The selection of the widths of the second stage inverter is essential for the transient analysis. Because stage 1 and stage 2 inverter sizes decide the propagation delay of the whole ring amplifier. If the widths are small, the propagation delay will be high, and Overshoot can be seen, which is explained in a transient simulation.

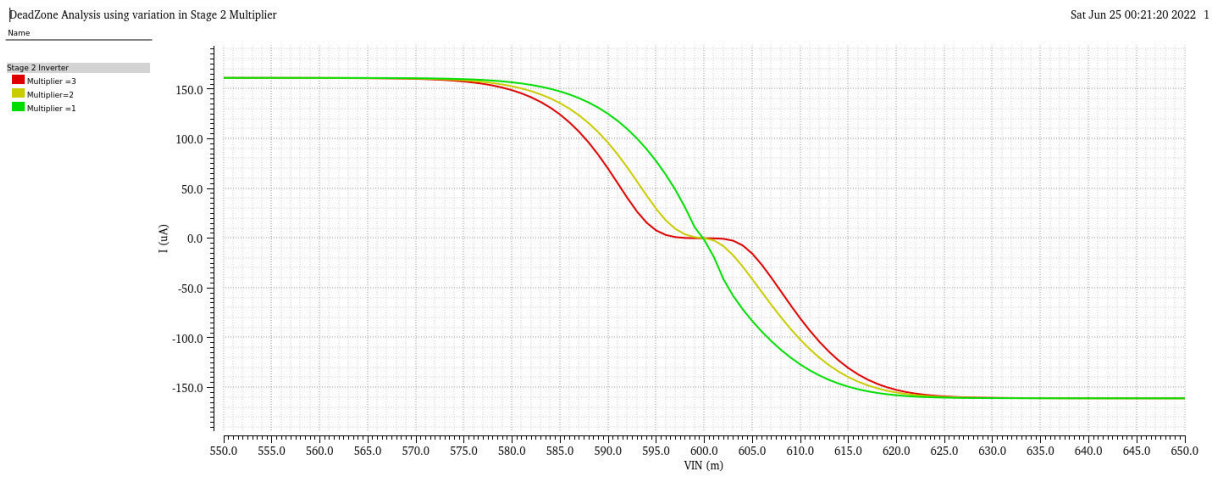


Figure 5.7: Dead Zone analysis using variation in the Stage 2 Multiplier

5.2.3 Variation in the Slew Current

The sizes of the third-stage devices are varied, directly affecting the load capacitor's charging and discharging current. The smaller the device sizes, the slower the response and more time to reach a steady-state, whereas the larger the device sizes, the higher the current and faster the response. Slew current is determined by the maximum output value reached by the capacitor in the smallest period.

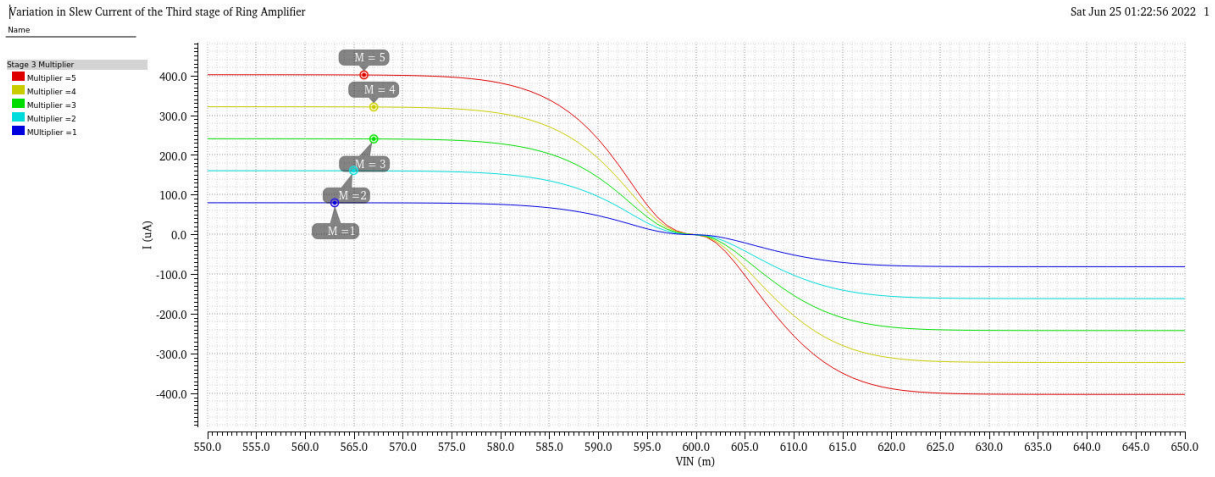


Figure 5.8: Slew Current Variation Due to Variation in Output Stage Multiplier

5.2.4 Transient Response of MDAC

In the above subsections, R_{bias}, multiplier of the second stage and third stage inverters varied and effect on the output current and dead zone are plotted. In this section this, same variation will be done and effect is shown in transient simulation.[12]

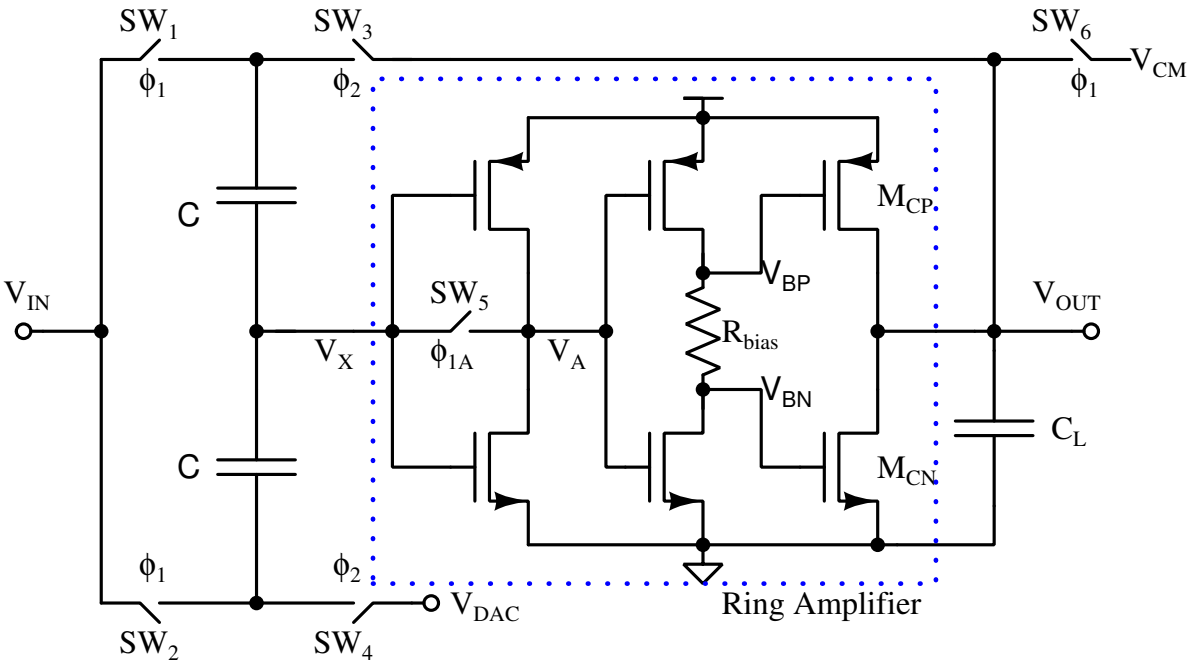


Figure 5.9: Test Bench for the Transient Simulation

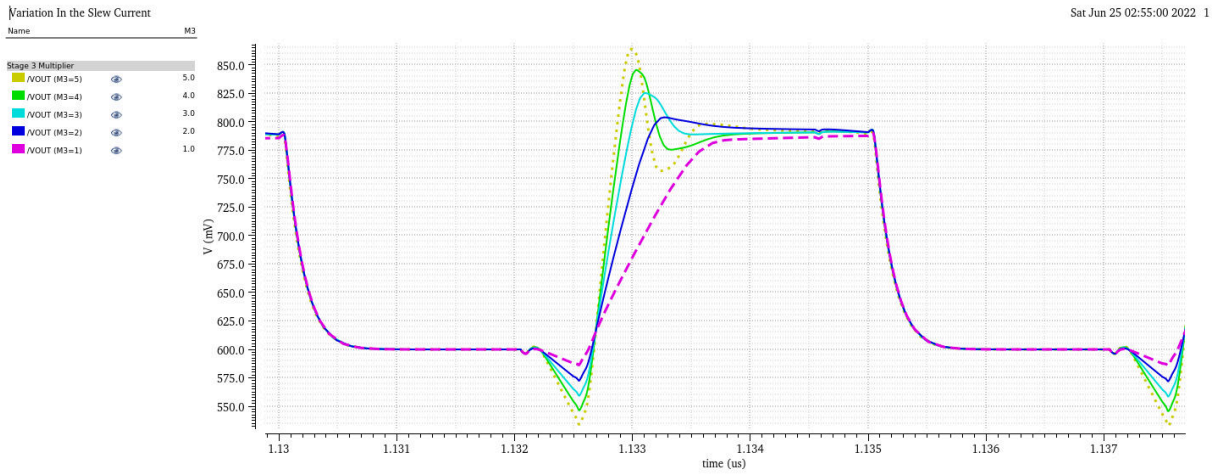


Figure 5.10: Transient Behaviour with Variation in Slew Current

Figure 5.10 represents variation in slew current and its effect on the transient simulation.

Higher the slew current, the faster the response, but when the V_{OUT} reaches desired output level at the same time input node of the ring amplifier should have reached V_{CM}. Due to propagation delay of Stage 1 and stage 2 inverter, it never happens at the same instant, and that causes overcharge. It is called Overshoot.

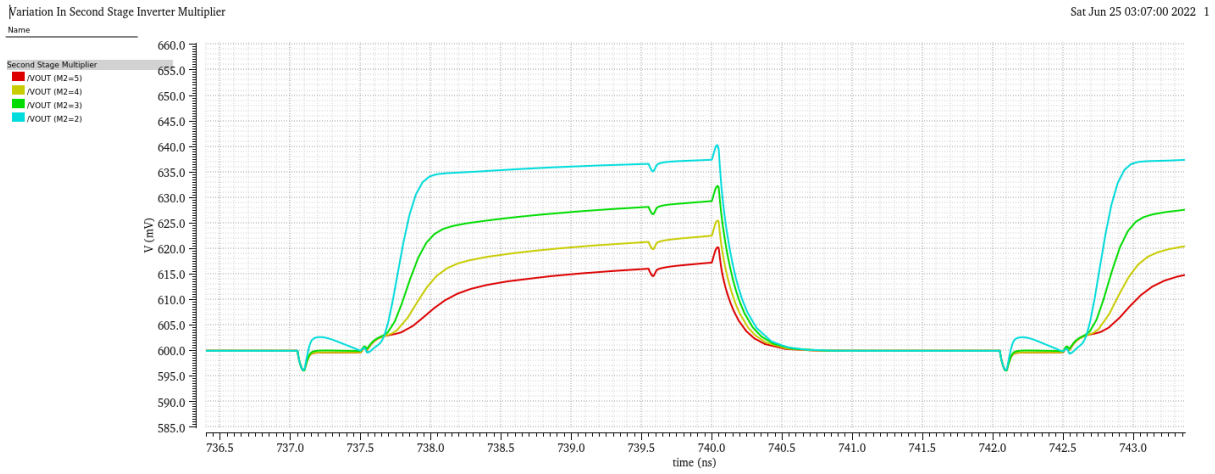


Figure 5.11: Transient Behaviour with Variation in Second Stage Inverter

Figure 5.11 represents variation in second stage multiplier. Second stage helps to tune the dead zone. Larger the dead zone poor the accuracy of ring amplifier. Smaller the dead zone, higher the overshoot and possibility of the oscillations. Similarly Figure 5.12 represents variation in R_{bias} which also contribute the dead zone range.

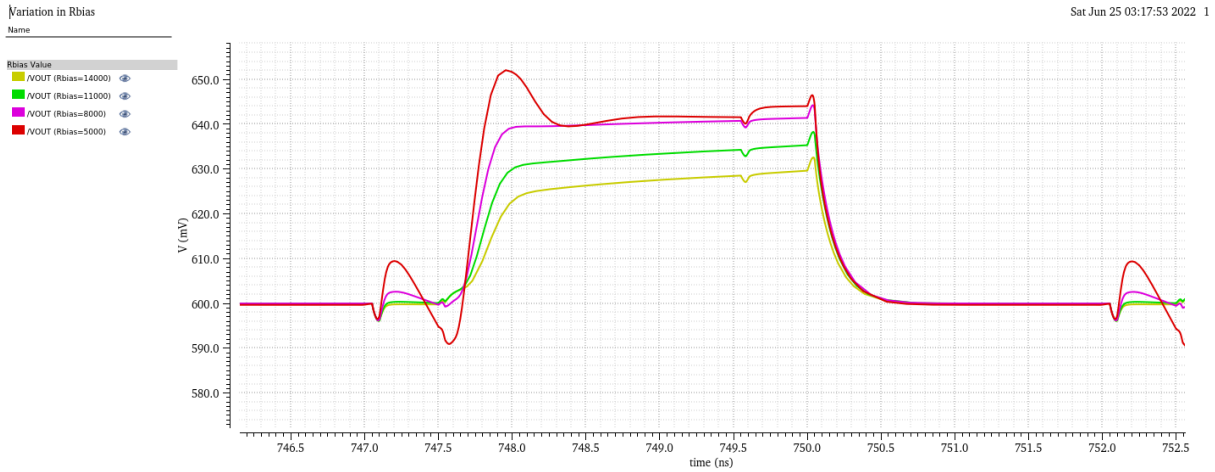


Figure 5.12: Transient Behaviour with Variation in R_{bias}

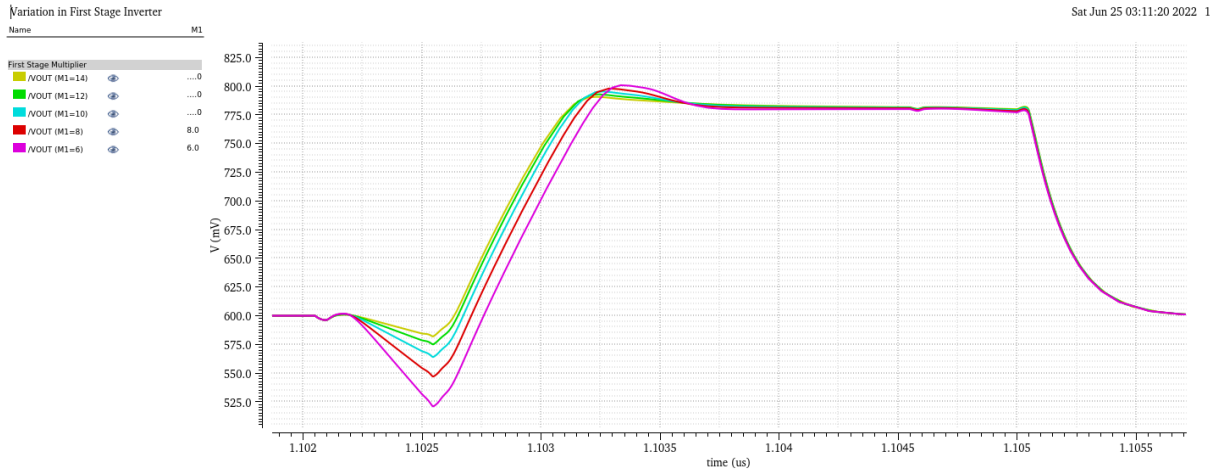


Figure 5.13: Transient Behaviour with Variation in First Stage Inverter

Figure 5.13 represents the variation in first stage multiplier, which results in the minimizing the propagation delay. Hence minimizing the overshoot and faster settling.

5.3 Simulation Results of Pipeline ADC

In this section, simulations are performed to articulate the performance of the pipeline ADC.

5.3.1 Transient Simulation

For the transient simulation, slow ramp input is applied to the ADC. Output value is evaluated using simple mathematical equation

$$V_{OUT} = \frac{D_7}{2} + \frac{D_6}{4} + \frac{D_5}{8} + \frac{D_4}{16} + \frac{D_3}{32} + \frac{D_2}{64} + \frac{D_1}{128} + \frac{D_0}{256} \tag{5.4}$$

Transient simulation result is shown in Figure 5.14. The simulation is performed for typical values of transistors and room temperature. There are no missing codes the typical simulations and the codes are switching with period of 5ns.

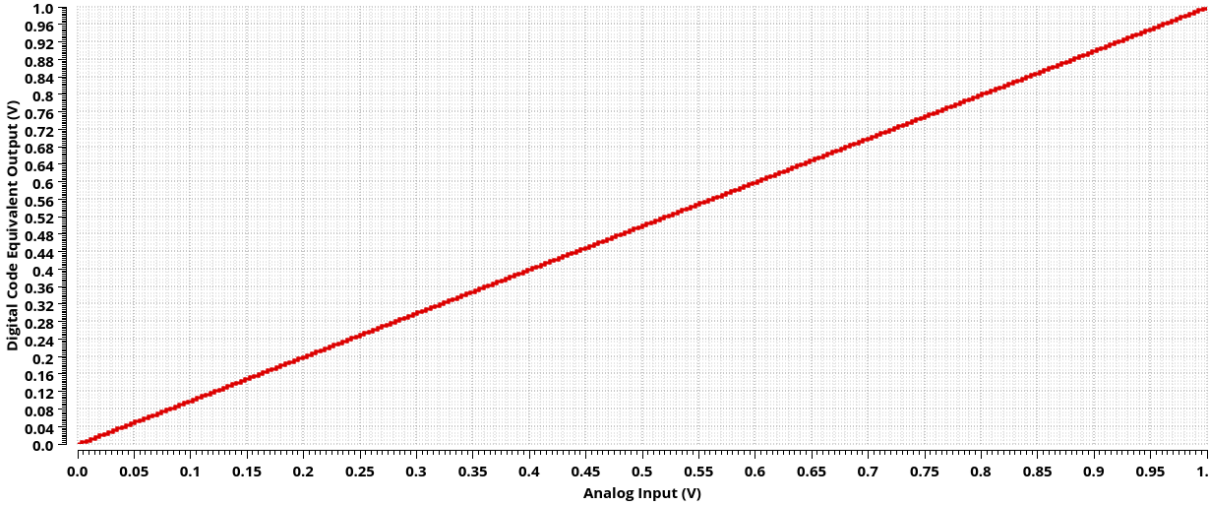


Figure 5.14: Transient Response for Ramp Input

5.3.2 Dynamic Performance of the Pipeline ADC

Dynamic performance of ADC is obtained for lower frequency and Nyquist frequency (100 MHz). To determine the dynamic performance of ADC, coherent sampling is used. f_{in}/f_{sample} = M/N, Where f_{sample} = 200MHz and N = 4096 points.

5.3.2.1 Low Frequency

For low frequency dynamic performance, M = 859 selected. f_{in} is calculated from as (200M×859)/4096. Figure 5.15 illustrates the dynamic performance of the Pipeline ADC at Low frequency in the typical conditions. The signaling system in the pipeline ADC is differential in the nature, hence the second harmonic tone have very small magnitude. However, third harmonics are present due to non-linearity of the switches and the comparators.

	M = 859
ENOB(bits)	7.738
SNDR(dB)	48.353
SFDR(dBc)	55.739

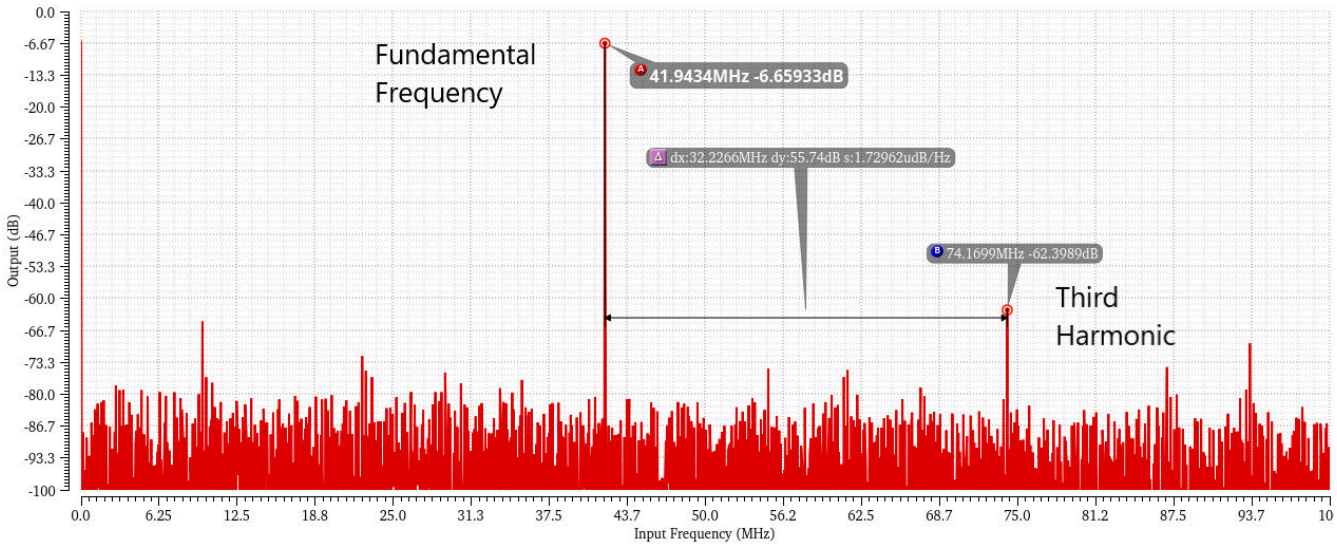


Figure 5.15: Dynamic Performance of ADC at Low Frequency

5.3.2.2 High Frequency

For High frequency(nyquist rate) dynamic performance, M = 2017 selected. The dynamic performance of the ADC is characterized using the performance of the ADC at the nyquist frequency. Below Figure 5.20 shows the FFT plot of the ADC at 98MHz. Fundamental tone at the 98.4MHz, But the different tones are also present at lower magnitude. Performance of the switches is degraded at the high frequency causing odd order harmonic tones at the output. Time difference between the rising edge of the comparator clock and the sampling clock of the first stage can add additional noise.

	M = 2017a
ENOB(bits)	7.627
SNDR(dB)	47.682
SFDR(dBc)	54.32

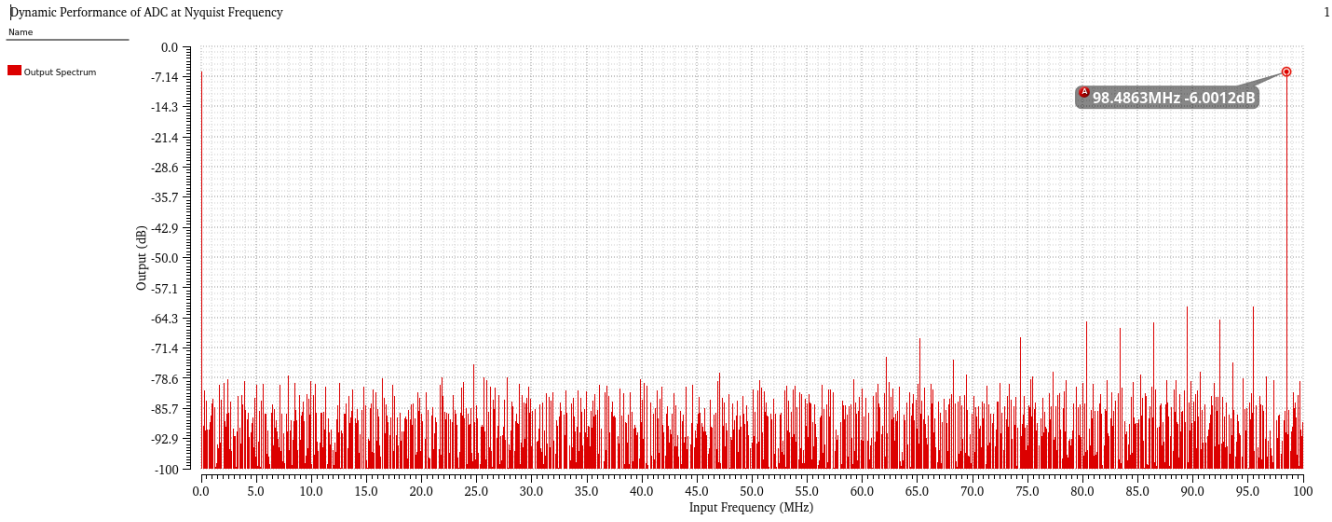


Figure 5.16: Dynamic Performance of ADC at Nyquist Frequency

5.3.3 Static Performance using Monte-Carlo Simulations

100 points Monte Carlo simulations were performed and the result illustrated below in the Figure 5.17. The main goal of the Monte Carlo simulation is to observe the static performance of the ADC while varying the process corners. Monte-Carlo simulations varies the parameters of the transistors, capacitor and resistors like Width, Length and the mobility in the incremental manner. Table 5.1 summarizes the static performance of the pipeline ADC. This results are extracted using the MATLAB code. Figure 5.18 demonstrates the distribution of the LSBs calculated from the Monte-Carlo Simulation.

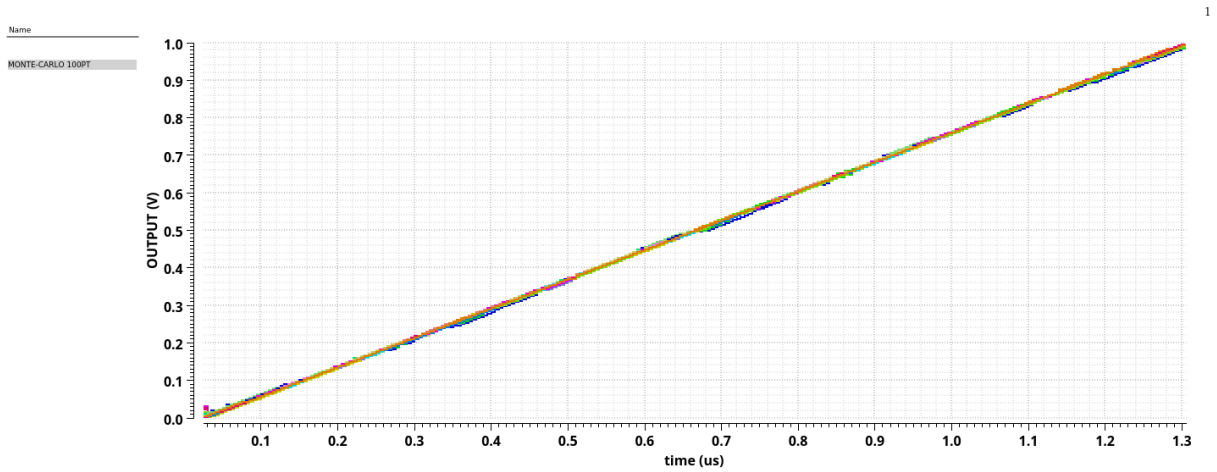


Figure 5.17: Transient Results of the 100 Point Monte-Carlo Simulation

	mV		**LSB**
MEAN (μ)	3.92	**DNL**$_{rms,max}$	0.65
SD (σ)	0.012	**INL**$_{rms,max}$	0.91

Table 5.1: Static Performance of Pipeline ADC

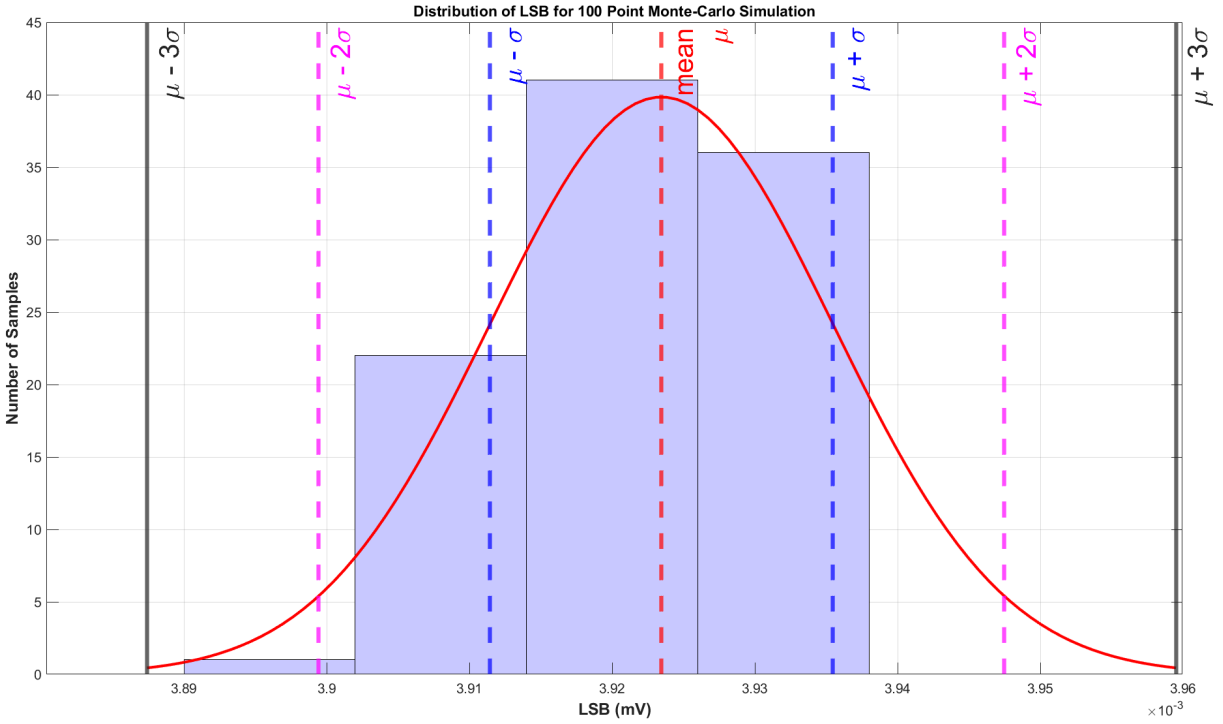


Figure 5.18: Distribution of the LSB(mV) in the Monte-Carlo Simulation

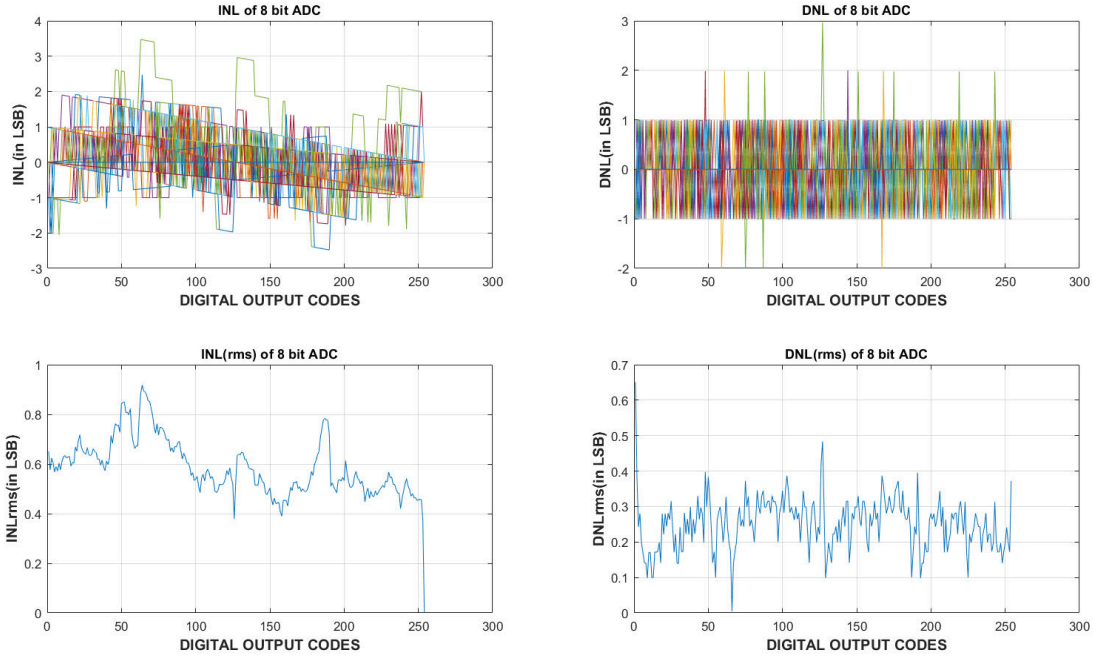


Figure 5.19: INL and DNL results of the 100 Point Monte-Carlo Simulation

5.3.4 Corner Simulations for the Dynamic Performance

Dynamic performance checked for the different process and temperature corners. Coherent sampling is used to decide the input frequency to get distinct 4096 sample points. SFDR, SNDR and ENOB is observed. Two frequencies are selected to characterize the dynamic performance such as 41.96MHz(M = 859) and 98.48MHz(M = 2017). Table 5.21 are recorded effective number of bits(ENOB) for the different corners. Three temperatures (-40°, 27° and 100°) and eight combinations of the process corners are selected to characterized the pipeline ADC. The abbreviations signifies the corner selection for transistor, resistor and capacitor respectively. The best results are observed for the fast transistor, fast resistor and flow capacitor at the temperature of -40°. The worst results are observed for the slow transistor, slow resistor and slow capacitor at the temperature of -40°.

Corner Performance (Effective Number of Bits [ENOB])							
Lowe Frequency (41.96MHz) M = 859				**Nyquist Frequency (98.48MHz) M = 2017**			
	Temperature				**Temperature**		
Corner	**-40**	**27**	**100**	**Corner**	**-40**	**27**	**100**
SSS	5.04	6.9	7.29	**SSS**	3.86	6.63	6.5
SSF	5.65	7.22	6.97	**SSF**	4.96	7.09	6.59
SFS	6.42	7.6	6.94	**SFS**	5.97	6.76	7.14
SFF	5.77	7.27	7.77	**SFF**	5.18	6.38	7.08
FSS	7.62	7.76	7.71	**FSS**	7.53	7.66	7.7
FSF	7.84	7.87	7.92	**FSF**	7.6	7.57	7.79
FFS	8.0	7.71	7.33	**FFS**	7.89	7.58	6.69
FFF	7.95	7.65	7	**FFF**	7.83	6.93	6.84
TTT	6.97	7.73	6.54	**TTT**	6.38	7.44	6.25

Table 5.2: ENOB(in bits) of Pipeline ADC under Process and Temperature Variation

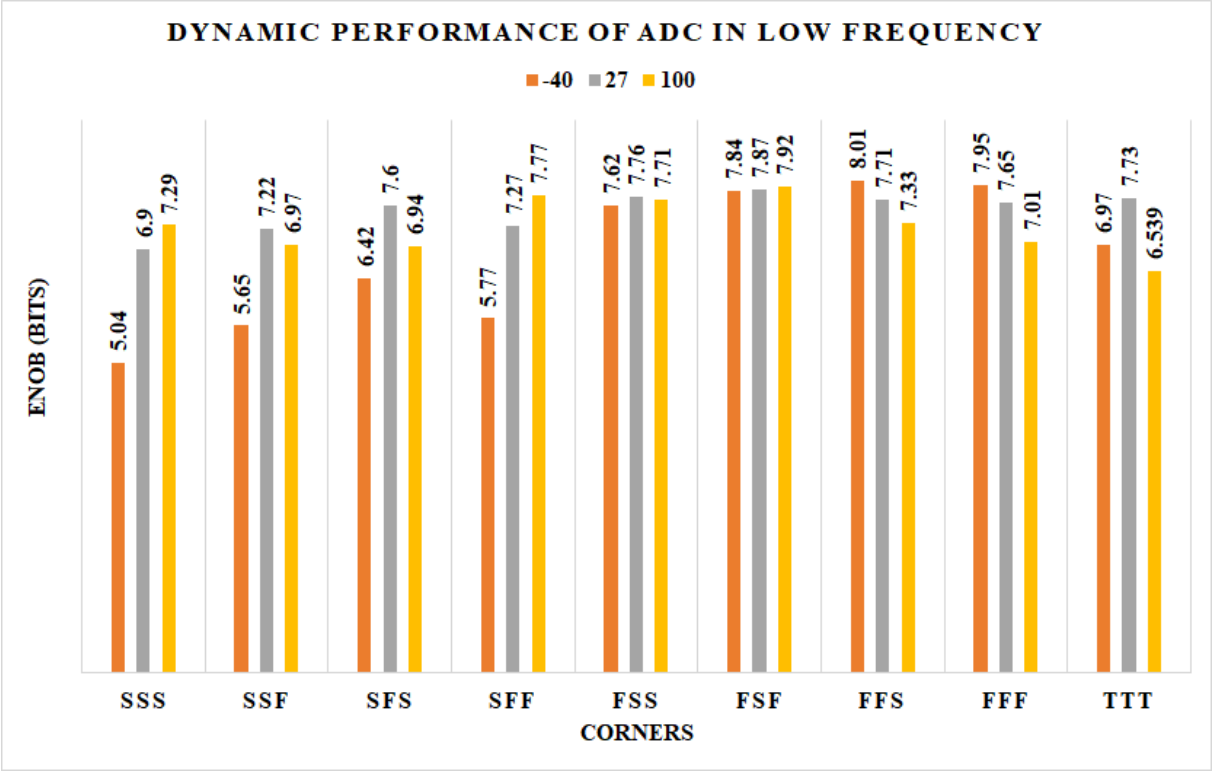


Figure 5.20: Corner Simulations of Pipeline ADC at Low Frequency (41.96MHz)

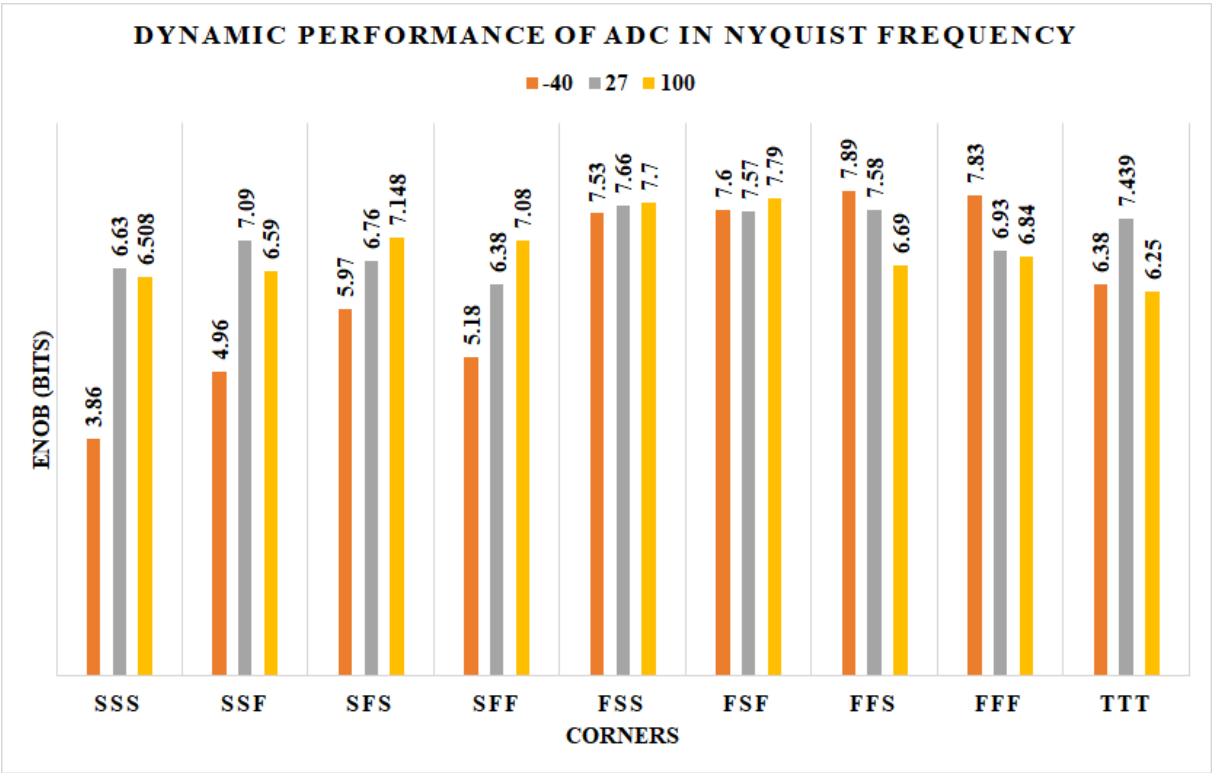


Figure 5.21: Corner Simulations of Pipeline ADC at Nyquist Frequency (98.48MHz)

Chapter 6

Conclusion

The ring amplifier in this thesis is designed for operating at 200MS/s, resolving 8-bit using pipeline ADC for the V_{FS} of 1V. At the temperature 27° in the typical values, ENOB (effective number of bits) is 7.65 bits. The ring amplifier is based on the ring oscillator; therefore amplifier is inclined to go under oscillation. The design procedure is not the same as the conventional opamp. The proposed ring amplifier design is very simple. The slew current and dead zone combination are performed to check the performance of ADC under different process and temperature corners. This combination is easily programmed from the test bench; such a facility is included in the ADC schematic.

The proposed ring amplifier consumes power because stage 1 and stage 2 are always on. Further research can be done, and the amplifier can be reconstructed using switches to minimize the power.

A conventional 8-bit pipeline ADC uses a simple ring amplifier where latency is four cycles in this proposed ADC. However, conventional ADC has a latency of eight clock cycles. On-resistance of the switches is required to be less than 4.5kΩ in the switched-capacitor circuit. By utilizing complementary switching structures, charge injection errors can be mitigated, but clock feed-through dominates in high-frequency operations, which is minimized by keeping

both PMOS and NMOS transistor sizes the same.

Ideally, the open-loop gain of the ring amplifier should be very high, but due to R_{bias}, third-stage devices are in a lower conduction region, causing the drop in the gain. In the third stage, on-resistance and the load capacitor form the dominant pole, stabilizing the ring amplifier in the close loop.

The operations of the ring amplifier are very different compared to the conventional operational amplifier. Its behavior changes dynamically throughout the operation. In the corners simulations, slew rate and propagation delays are varied, causing the degraded behavior, which affects the performance

The Pipeline ADC Designed using Ring Amplifier					
	JSSC[5] 2012	**JSSC[6] 2015**	**ICEIC[13] 2020**	**ISCAS[14] 2015**	**This Work**
Sampling Frequency(MHz)	30	100	100	70	200
Resolution(bits)	10.5	10.5	11	10	8
ENOB(bits)	9.9	9.33	10.8	8.36	7.44
SNDR(dB)	61.9	57.9	66.83	52	47.68
SFDR(dB)	74.2	71.9	76.03	-	54.3
POWER(mW)	2.6	2.46	18.6	3.65	22
FOM(fJ/C-step)	90	38.4	104	159.2	460
Technology	180	65	65	90	65

Table 6.1: Comparison of the Pipeline ADCs with Thesis Work

Appendix A

The Ring amplifier is very dynamic circuit, hence there is need to adjust the delay and the slew current such that ring amplifier has optimum accuracy and minimum overshoot. Below Figure A.1 is new design so pipeline ADC can work in the different corners. New dead zone and slew rate is selected with digitally controlled switches.

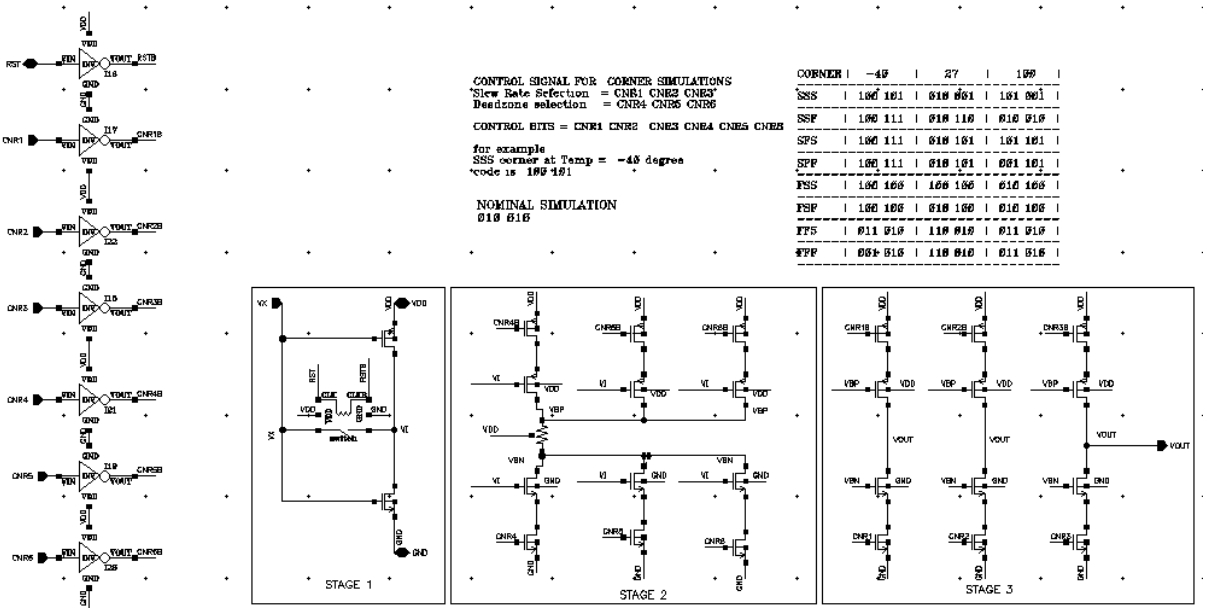


Figure A.1: New Design of the Ring Amplifier to operate ADC in the Different Corners

	Temperature		
Corners	**-40°**	**27°**	**100°**
SSS	100 101	010 001	101 001
SSF	100 111	010 011	010 010
SFS	100 111	010 101	101 101
SFF	100 111	010 101	001 101
FSS	100 100	100 100	010 100
FSF	100 100	010 100	010 100
FFS	011 010	110 010	011 010
FFF	001 010	110 010	011 010
NOM	010 010		

Table A.1: Digital Codes of the Ring Amplifier For Different Corners

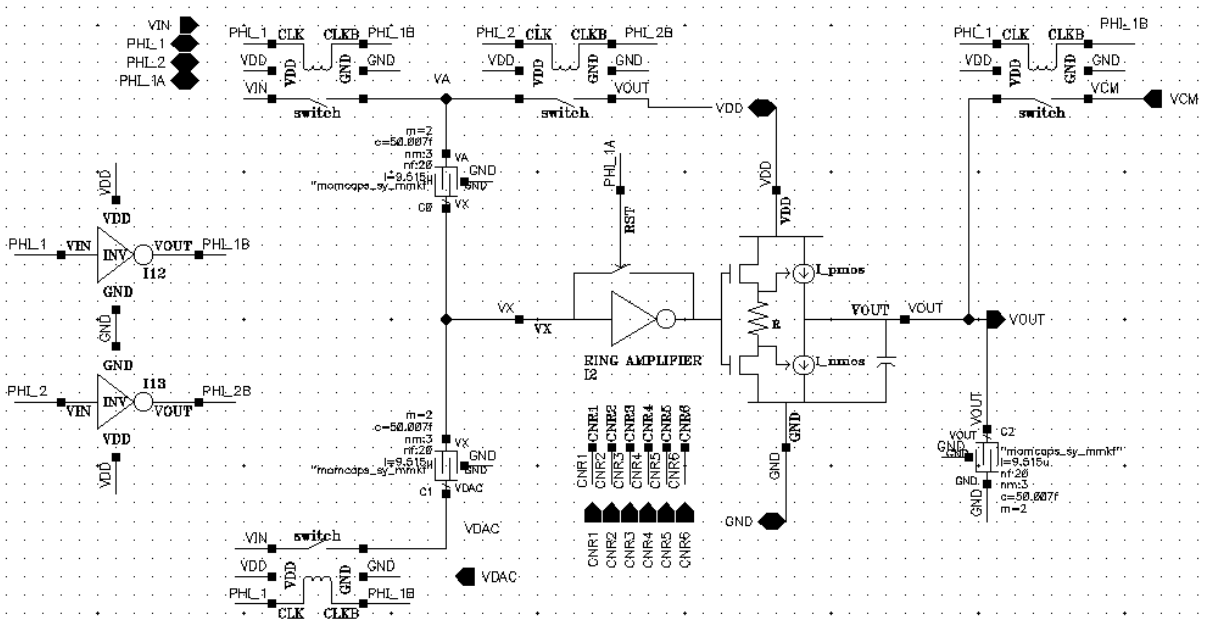


Figure A.2: Schematic of the MDAC

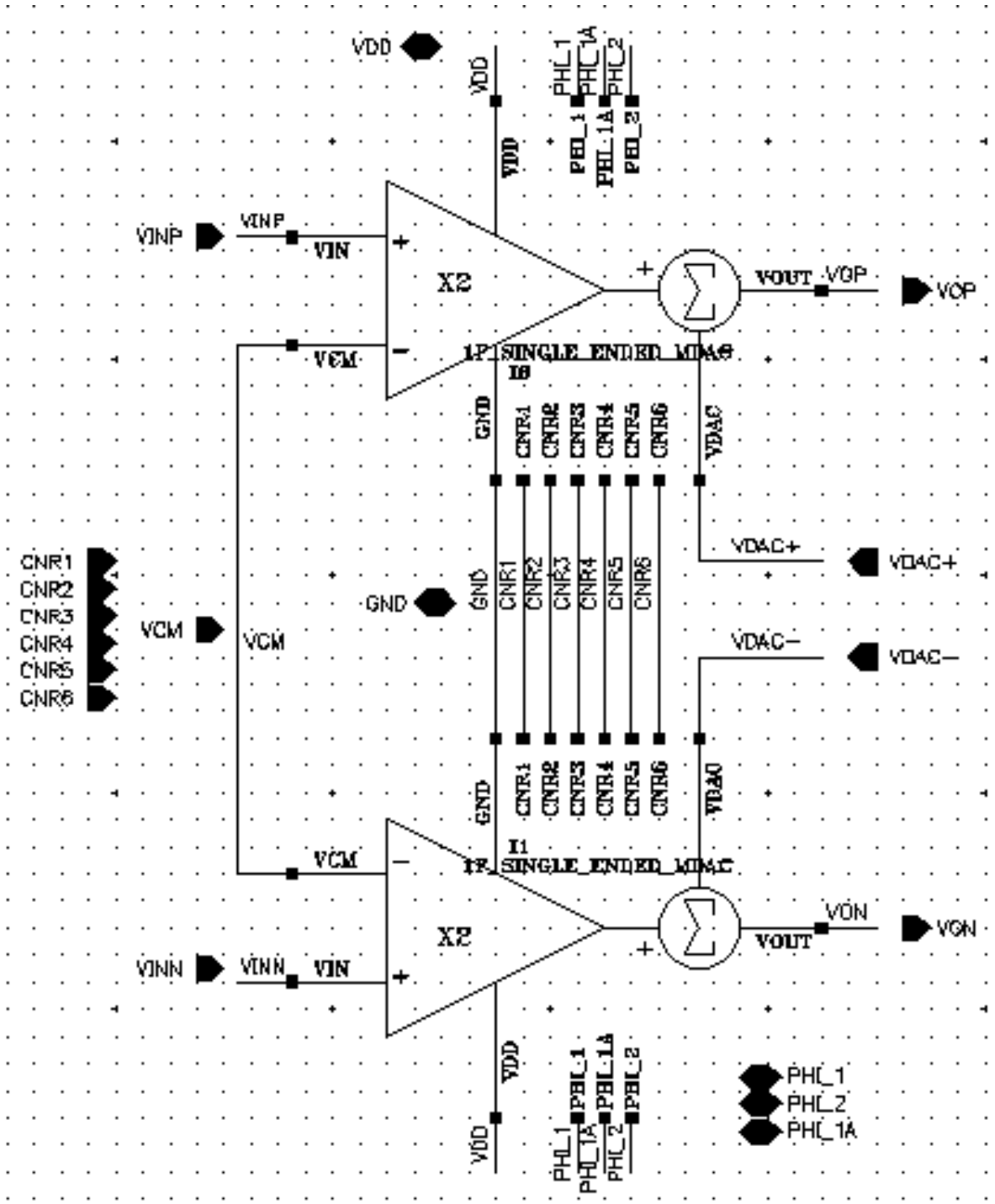


Figure A.3: Schematic of the Differential MDAC

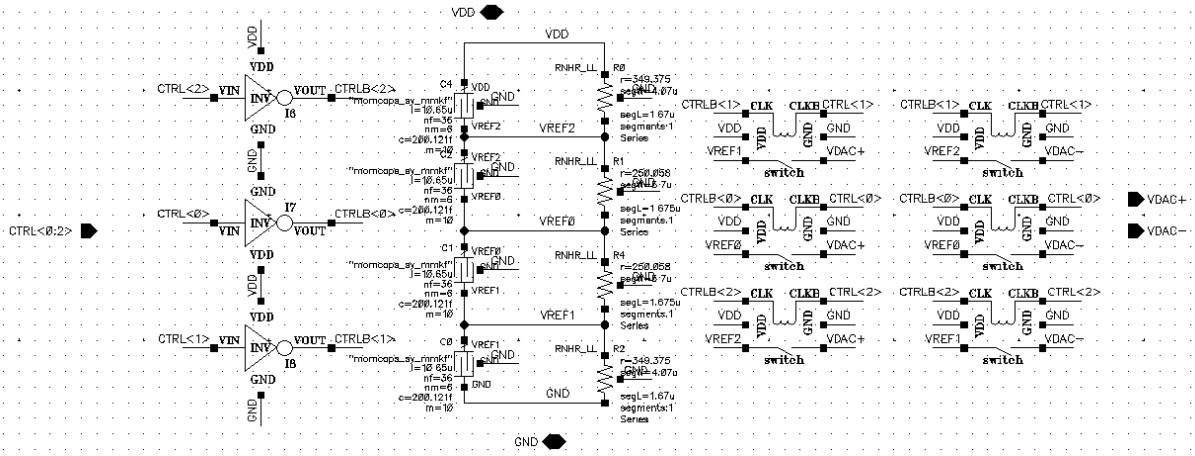


Figure A.4: Schematic of the 2-bit DAC

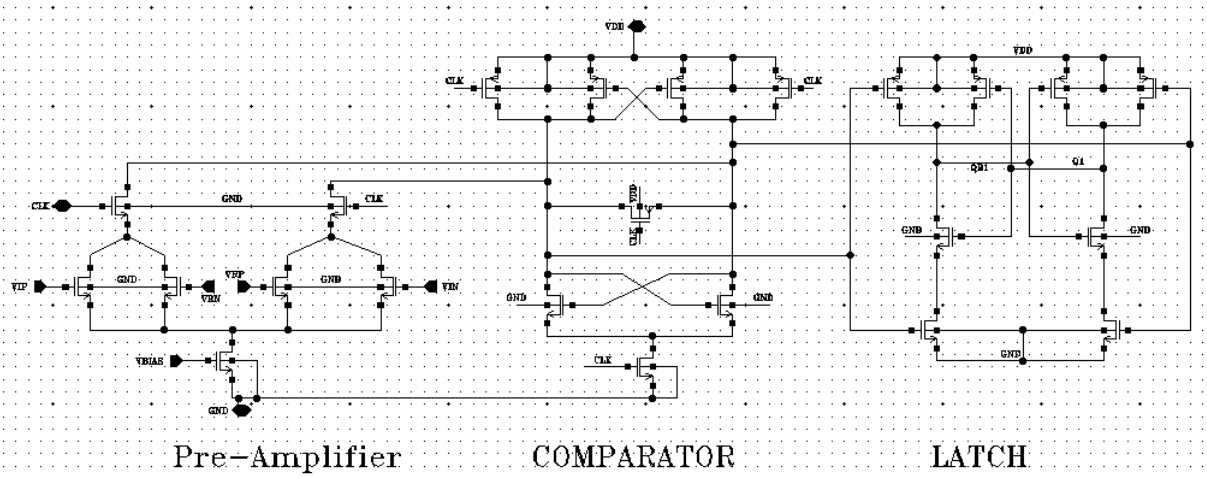


Figure A.5: Schematic of the Comparator

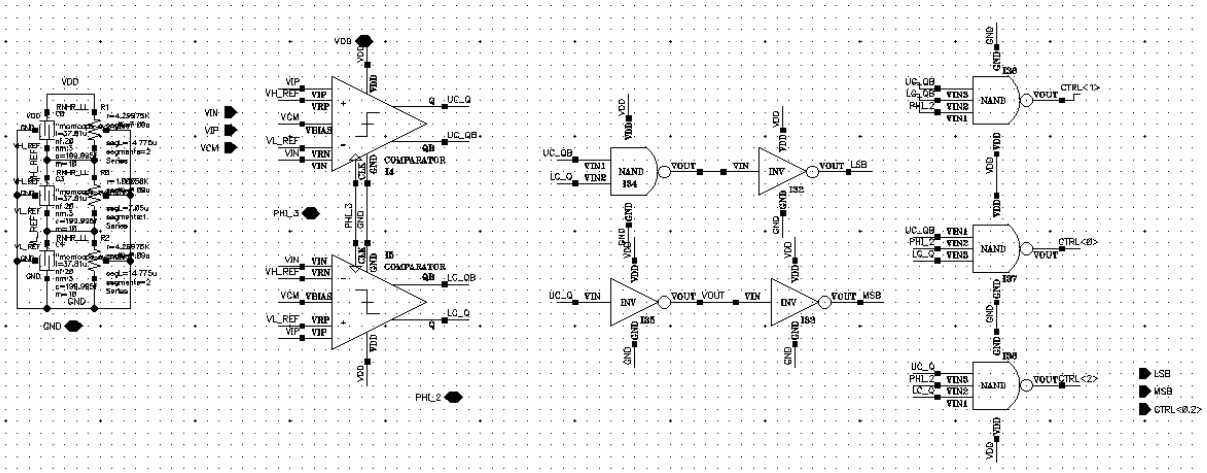


Figure A.6: Schematic of the 1.5-Bit ADC

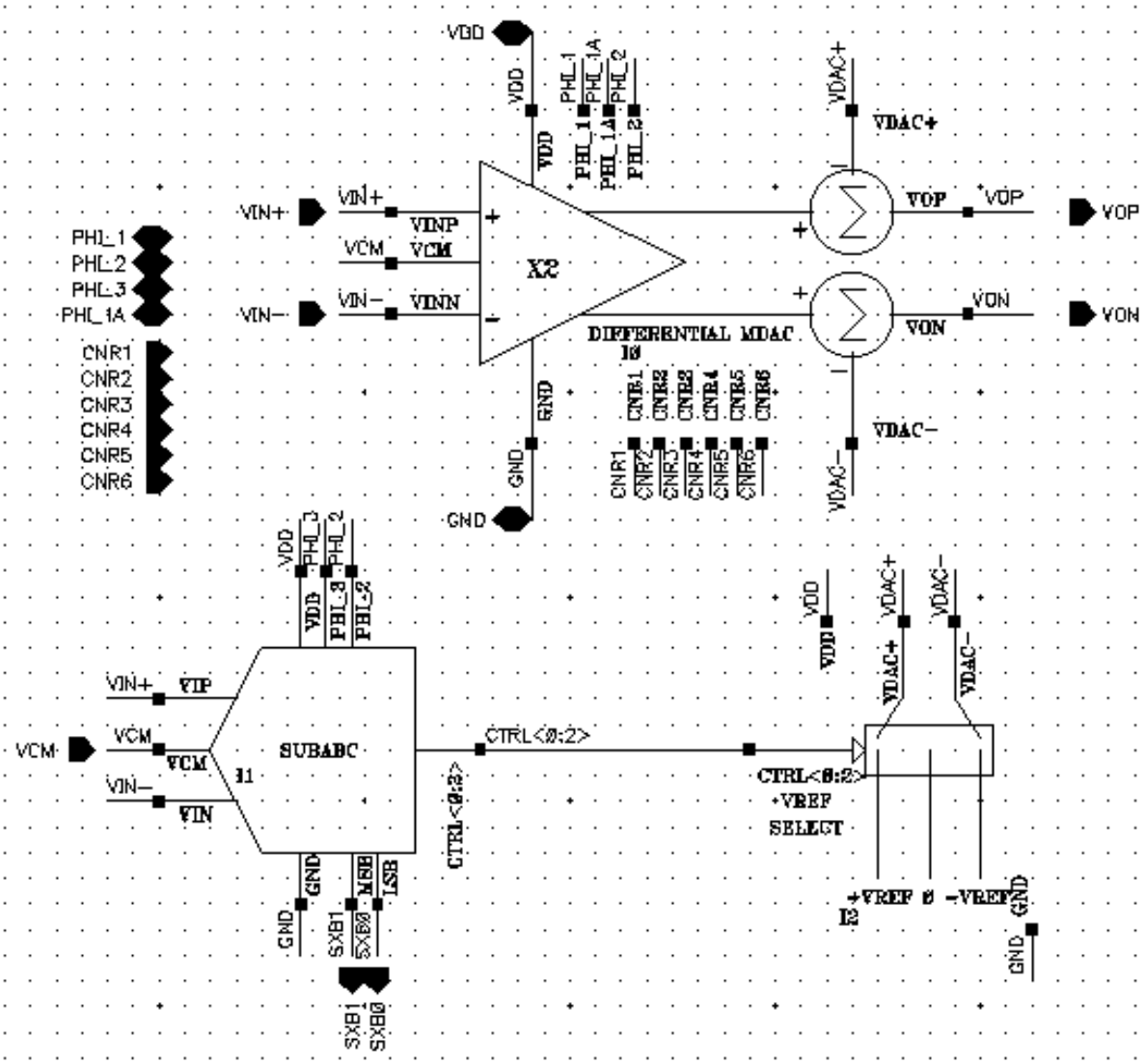


Figure A.7: Schematic of the Single Stage

Appendix B

Output of the pipeline ADC is shown in the Figure B.1 for the Ramp input at the nominal conditions

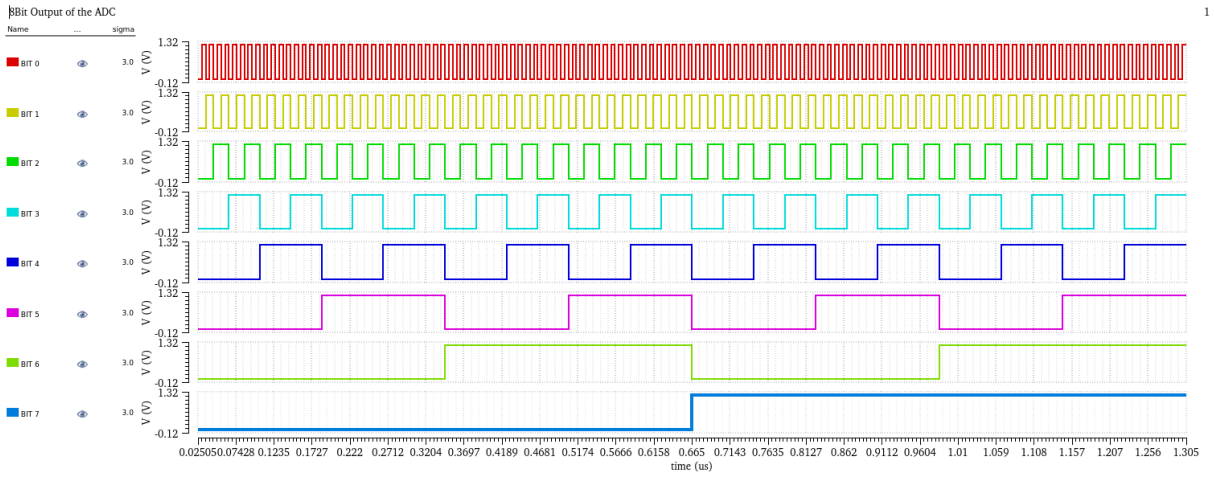


Figure B.1: Output bits of the Pipeline ADC for RAMP Input

Ramp input is applied to stage 1. In this stage, 1.5bit sub-ADC generates 2 bits comparing the ramp input with the threshold voltages. DAC produces the quantized signals to generate a residue amplifier. As shown in Figure B.2, over-ranging is avoided. Figures B.3 and B.4

illustrate how residue is generated in the cascaded stages.

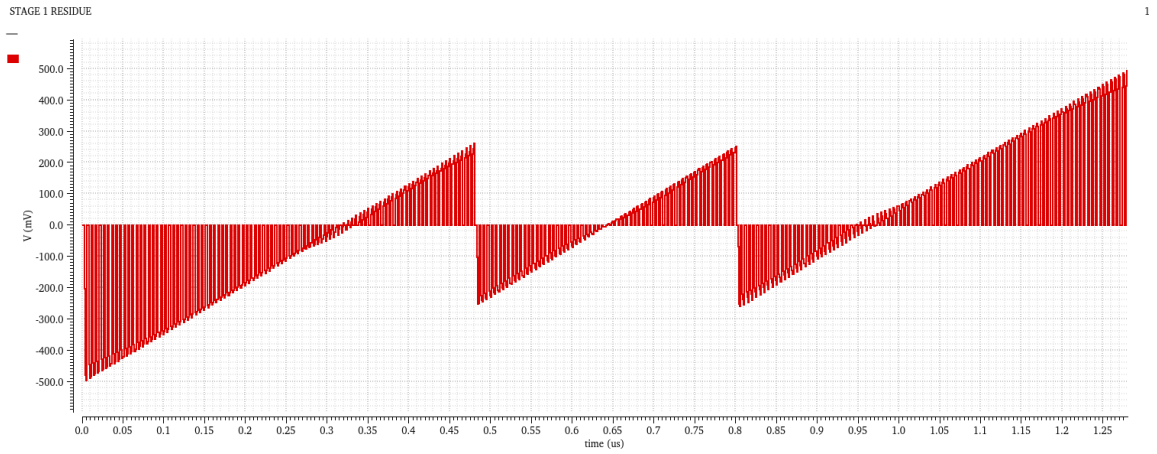


Figure B.2: Residue generated at the output of the first stage

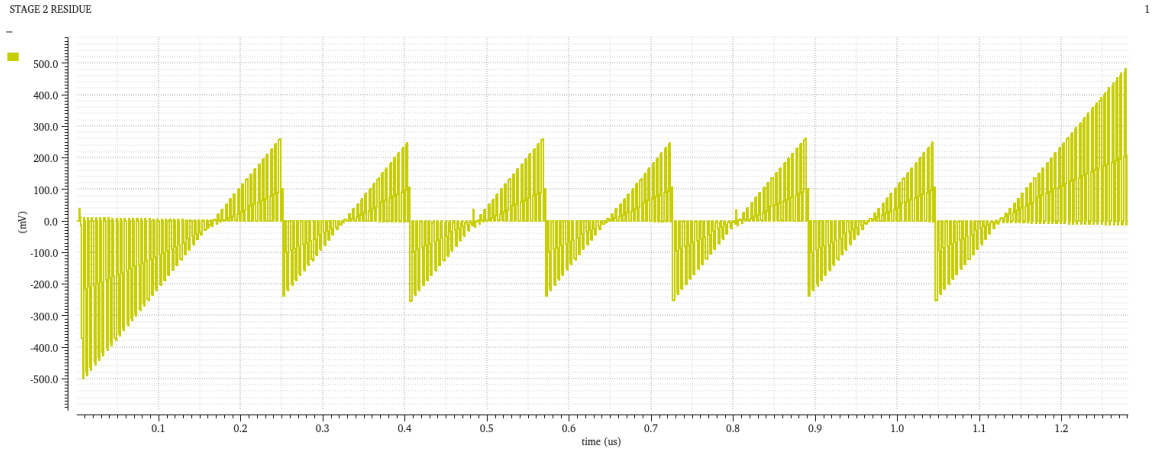


Figure B.3: Residue generated at the output of the second stage

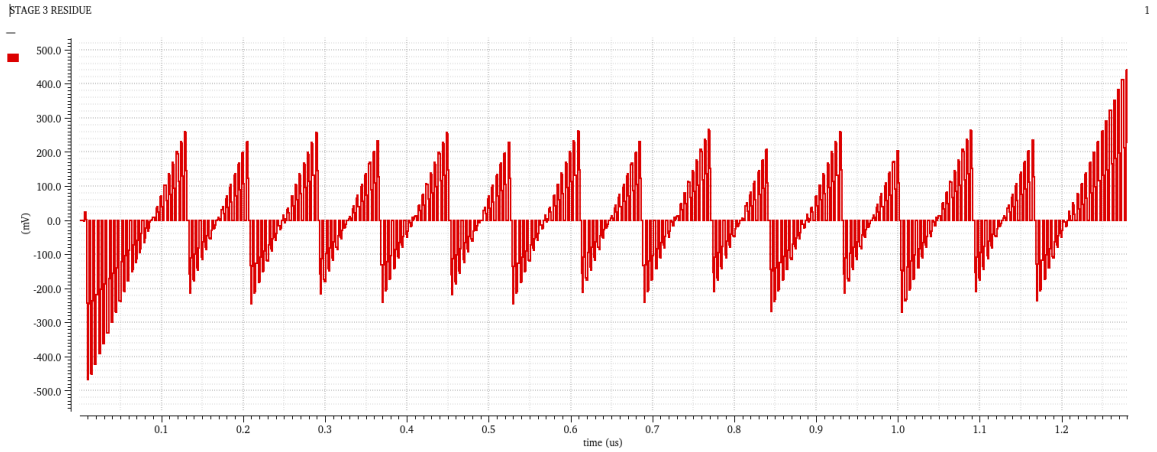


Figure B.4: Residue generated at the output of the Third stage

Following MATLAB code is used to determined the INL and DNL and distribution of list significant bit (LSB).

```
% Mtech Final Year Project 2022
% DNL and INL Calculation of 8 bit ADC
% Author: Sagar Zoting (203070064)
% June 24th, 2022
close all;
clc;
format longg;
% Number of bits
N = 8;
% Number of Digital Codes
M = 2^N-1;
%List of Decimal values representing Digital codes
CODES = [0:1:M]';
% Import the .csv data in the 'RAW_DATA' array.
RAW_DATA= readmatrix('MC_100_FINAL.csv');
[ROW_RAW_DATA,COL_RAW_DATA] = size(RAW_DATA);
%Time where output actual output starts
TIME_LATENCY = 25.05E-09;
SAMPLED_TRANSITIONS_POINTS = [];
SAMPLED_OUTPUT = [];
for i = 1:3:COL_RAW_DATA
    TRIMMED_INPUT = [];
    TRIMMED_DATA = [];
    index_to_trim = find(RAW_DATA(:,i) >= TIME_LATENCY,1);
    TRIMMED_DATA = RAW_DATA(index_to_trim:end,i+1);
    TRIMMED_INPUT = RAW_DATA(index_to_trim:end,i+2);
    V_FS = 1;
    IDEAL_VLSB = V_FS/(M+1);
    DESIRED_OUTPUT = 0:IDEAL_VLSB:V_FS-IDEAL_VLSB;
    transitions = [];
```

```
31      Output = [];
32      idx_Ad = 1;
33      for j =1:1:M
34          idx = find(TRIMMED_DATA==DESIRED_OUTPUT(j),1,'last');
35          if isempty(idx)
36              transitions = [transitions; TRIMMED_INPUT(idx_Ad)];
37              Output = [Output;TRIMMED_DATA(idx_Ad)];
38          else
39              transitions = [transitions; TRIMMED_INPUT(idx)];
40              Output = [Output;TRIMMED_DATA(idx)];
41              idx_Ad = idx;
42          end
43      end
44      SAMPLED_TRANSITIONS_POINTS = [SAMPLED_TRANSITIONS_POINTS
            transitions];
45      SAMPLED_OUTPUT = [SAMPLED_OUTPUT Output];
46  end
47  [S,D] = size(SAMPLED_TRANSITIONS_POINTS);
48  CODE_WIDTH = [];
49  OFFSET_ERROR = [];
50  FULL_SCALE_ERROR= [];
51  CORRECTED_LSB = [];
52  ACTUAL_V_FS = [];
53  RELATIVE_GAIN_ERROR = [];
54
55  for i=1:1:D
56      tmp1 = [];
57      for j=1:1:S-1
58          tmp = SAMPLED_TRANSITIONS_POINTS(j+1,i) -
                SAMPLED_TRANSITIONS_POINTS(j,i);
59          tmp1 = [tmp1;tmp];
60      end
```

```
61      CODE_WIDTH = [CODE_WIDTH tmp1];
62      tmp2 = SAMPLED_TRANSITIONS_POINTS(1,i)-DESIRED_OUTPUT(2);
63      OFFSET_ERROR = [OFFSET_ERROR ; tmp2];
64      tmp3 = SAMPLED_TRANSITIONS_POINTS(255,i)-DESIRED_OUTPUT
            (256);
65      FULL_SCALE_ERROR = [FULL_SCALE_ERROR; tmp3];
66      tmp4 = mean(CODE_WIDTH(:,i));
67      CORRECTED_LSB = [CORRECTED_LSB; tmp4];
68      ACTUAL_V_FS = [ACTUAL_V_FS;tmp4*256];
69      RELATIVE_GAIN_ERROR = [RELATIVE_GAIN_ERROR; IDEAL_VLSB/tmp4
            ];
70  end
71  MEAN_LSB = mean(CORRECTED_LSB);
72  STD_DEV = sqrt(var(CORRECTED_LSB));
73  DNL = [];
74  INL = [];
75  for i = 1:1:D
76      tmp5 = [];
77      tmp7 = [];
78      tmp8 = 0;
79      for j = 1:1:S-1
80          tmp6 = (CODE_WIDTH(j,i)-CORRECTED_LSB(i))/CORRECTED_LSB
                (i);
81          tmp5 = [tmp5; tmp6];
82          tmp8 = tmp8 + tmp6;
83          tmp7 = [tmp7; tmp8];
84      end
85      DNL = [DNL tmp5];
86      INL = [INL tmp7];
87  end
88  INL_RMS= [];
89  DNL_RMS = [];
```

```
for i = 1:1:M-1
    DNL_RMS = [DNL_RMS rms(DNL(i,:))];
    INL_RMS = [INL_RMS rms(INL(i,:))];
end
 figure, subplot(2,2,1)
 for j=1:D
   plot(INL(:,j)); hold on;
 end
 hold off;
title('INL of 8 bit ADC')
xlabel('DIGITAL OUTPUT CODES','FontSize', 12, 'FontWeight', '
    bold');
ylabel('INL(in LSB)','FontSize', 12, 'FontWeight', 'bold');
grid on;
subplot(2,2,2)
for i=1:D
    plot(DNL(:,i)); hold on;
end
 hold off;

title('DNL of 8 bit ADC')
xlabel('DIGITAL OUTPUT CODES','FontSize', 12, 'FontWeight', '
    bold');
ylabel('DNL(in LSB)','FontSize', 12, 'FontWeight', 'bold');
grid on;
 subplot(2,2,3)
 plot(INL_RMS);

title('INL(rms) of 8 bit ADC')
xlabel('DIGITAL OUTPUT CODES','FontSize', 12, 'FontWeight', '
    bold');
ylabel('INLrms(in LSB)','FontSize', 12, 'FontWeight', 'bold');
```

```
119 grid on;
120  subplot(2,2,4)
121  plot(DNL_RMS);
122 title('DNL(rms) of 8 bit ADC')
123 xlabel('DIGITAL OUTPUT CODES','FontSize', 12, 'FontWeight', '
      bold');
124 ylabel('DNLrms(in LSB)','FontSize', 12, 'FontWeight', 'bold');
125 grid on;
126 figure,
127 h = histfit(CORRECTED_LSB,4);
128 h(1).FaceColor = [0.8 0.8 1];
129 grid on;
130 hold on;
131 xl1 = xline(MEAN_LSB,'--r',{'mean','\mu'});
132 xl1.FontSize = 20;
133 xl1.LineWidth =3;
134 xl2 =xline(MEAN_LSB-STD_DEV,'--b',{'\mu - \sigma'});
135 xl2.FontSize = 20;
136 xl2.LineWidth =3;
137 xl3 = xline(MEAN_LSB+STD_DEV,'--b',{'\mu + \sigma'});
138 xl3.FontSize = 20;
139 xl3.LineWidth =3;
140 xl4 = xline(MEAN_LSB-2*STD_DEV,'--m',{'\mu - 2\sigma'});
141 xl4.FontSize = 20;
142 xl4.LineWidth =3;
143 xl5 = xline(MEAN_LSB+2*STD_DEV,'--m',{'\mu + 2\sigma'});
144 xl5.FontSize = 20;
145 xl5.LineWidth =3;
146 xl6 = xline(MEAN_LSB-3*STD_DEV,'-',{'\mu - 3\sigma'});
147 xl6.FontSize = 20;
148 xl6.LineWidth =3;
149 xl7 = xline(MEAN_LSB+3*STD_DEV,'-',{'\mu + 3\sigma'});
```

```
150 xl7.FontSize = 20;
151 xl7.LineWidth =3;
152 title('Distribution of LSB for 100 Point Monte-Carlo Simulation
    ')
153 xlabel('LSB (mV)','FontSize', 12, 'FontWeight', 'bold');
154 ylabel('Number of Samples','FontSize', 12, 'FontWeight', 'bold'
    );
155 hold off;
```

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