MTP Phase-II Presentation

Design of Pipeline ADC based on Ring Amplifier

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Outline

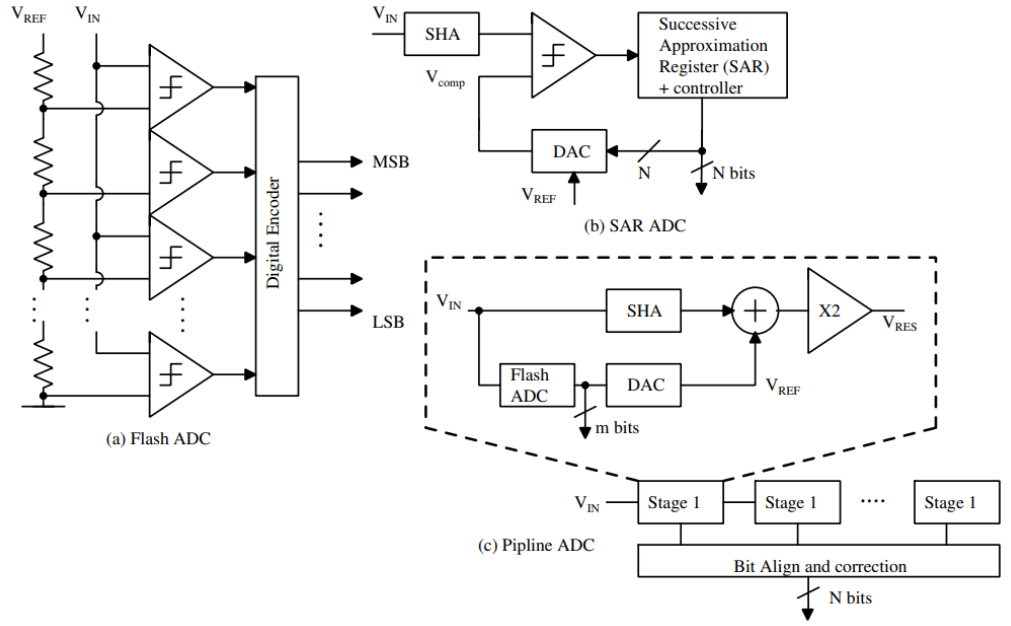
1. Introduction and Motivation
2. Pipeline ADC Architecture
3. Conventional Ring Amplifier
4. Self-Biased Ring Amplifier
5. Comparator
6. Complete Pipeline ADC
7. Simulations and Results
8. Conclusion
9. Future Work
10. References

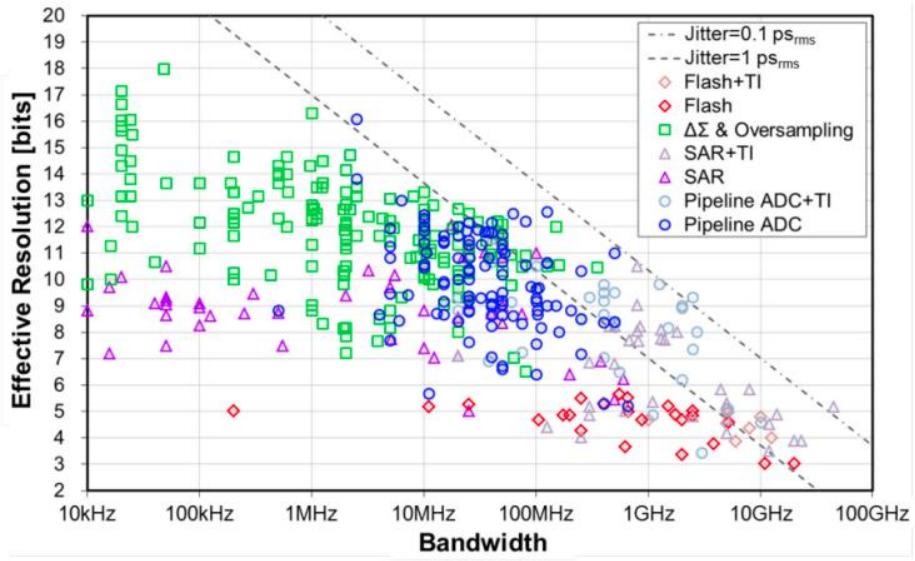
Motivation

- Walden Figure of Merit (FoM_W)

$$\mathbf{FoM_W = \frac{P}{f_s \times 2^{ENOB}}}$$

- Pipeline ADC:
  - Moderate to High Conversion Rate (**MHz to GHz**)
  - High Resolution (**6b to 16b**)
- Limitation:
  - **Adverse effect** on the Residue Amplifier due to **Technology Scaling**

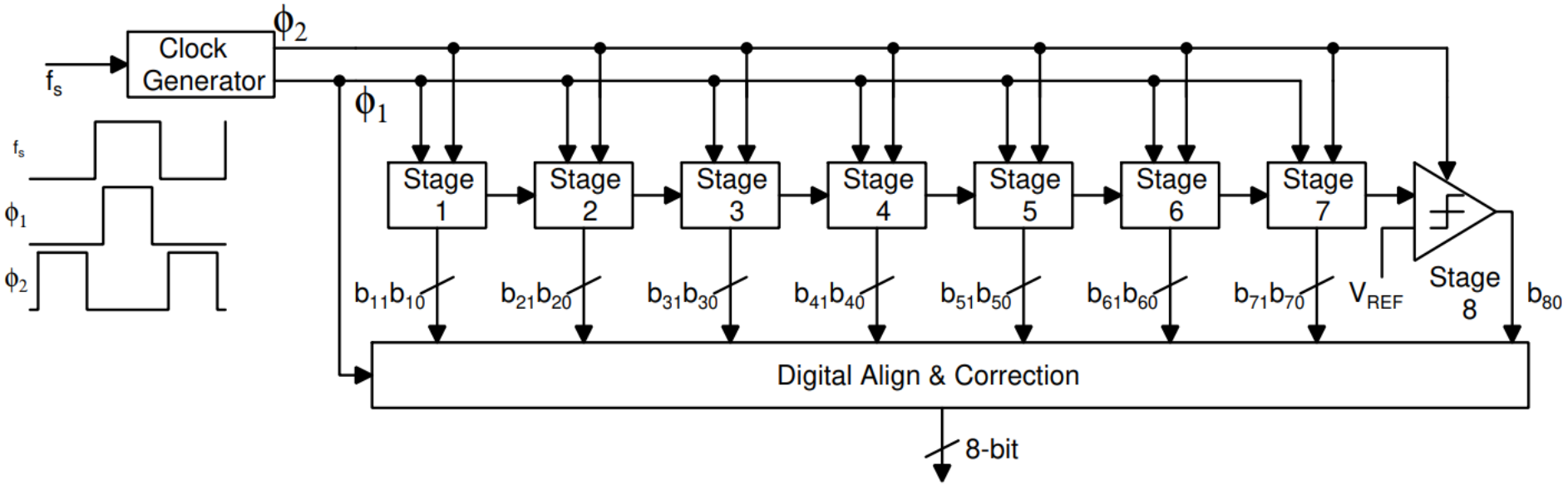




Ref: R. H. Walden, "Analog-to-digital converter survey and analysis," in *IEEE Journal on Selected Areas in Communications*, vol. 17, no. 4, pp. 539-550, April 1999, doi: 10.1109/49.761034.

B. Murmann, "The Race for the Extra Decibel: A Brief Review of Current ADC Performance Trajectories," in IEEE Solid-State Circuits Magazine, vol. 7, no. 3, pp. 58-66, Summer 2015, doi: 10.1109/MSSC.2015.2442393.

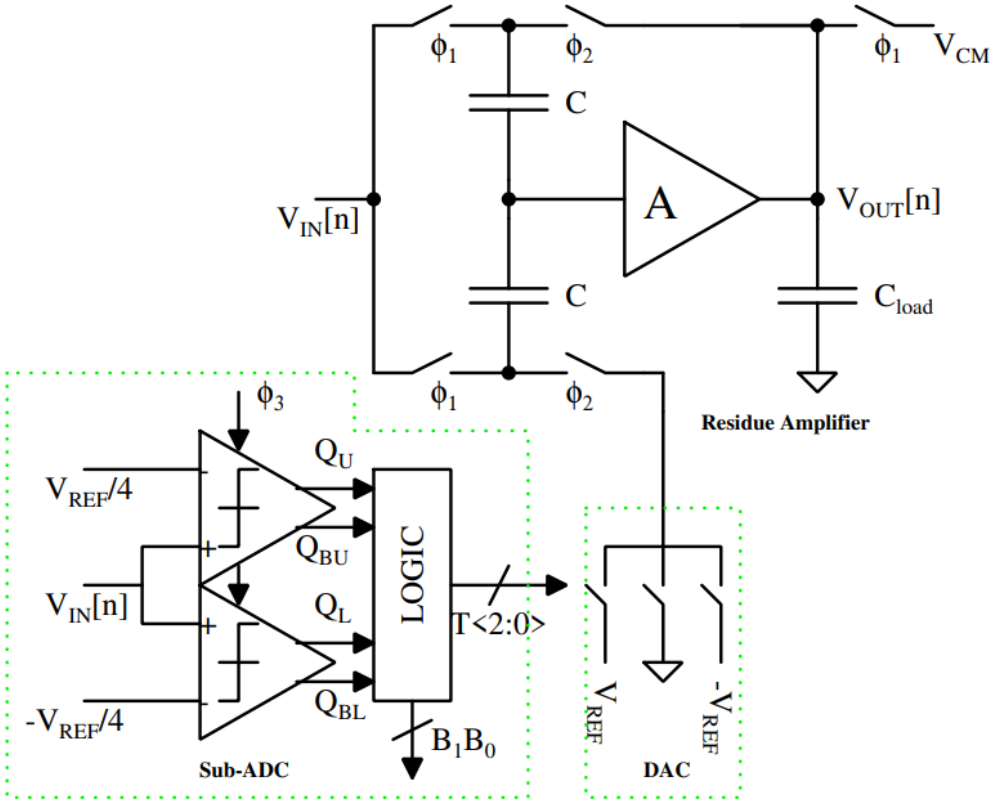
Pipeline ADC Architecture



- Clock Phases: Non-Overlapping
- Pipeline Stage Consist of Residue Amplifier, Sub-ADC and DAC
- Bits are stored and synchronized
- Corrected using Adders

Pipeline ADC Architecture

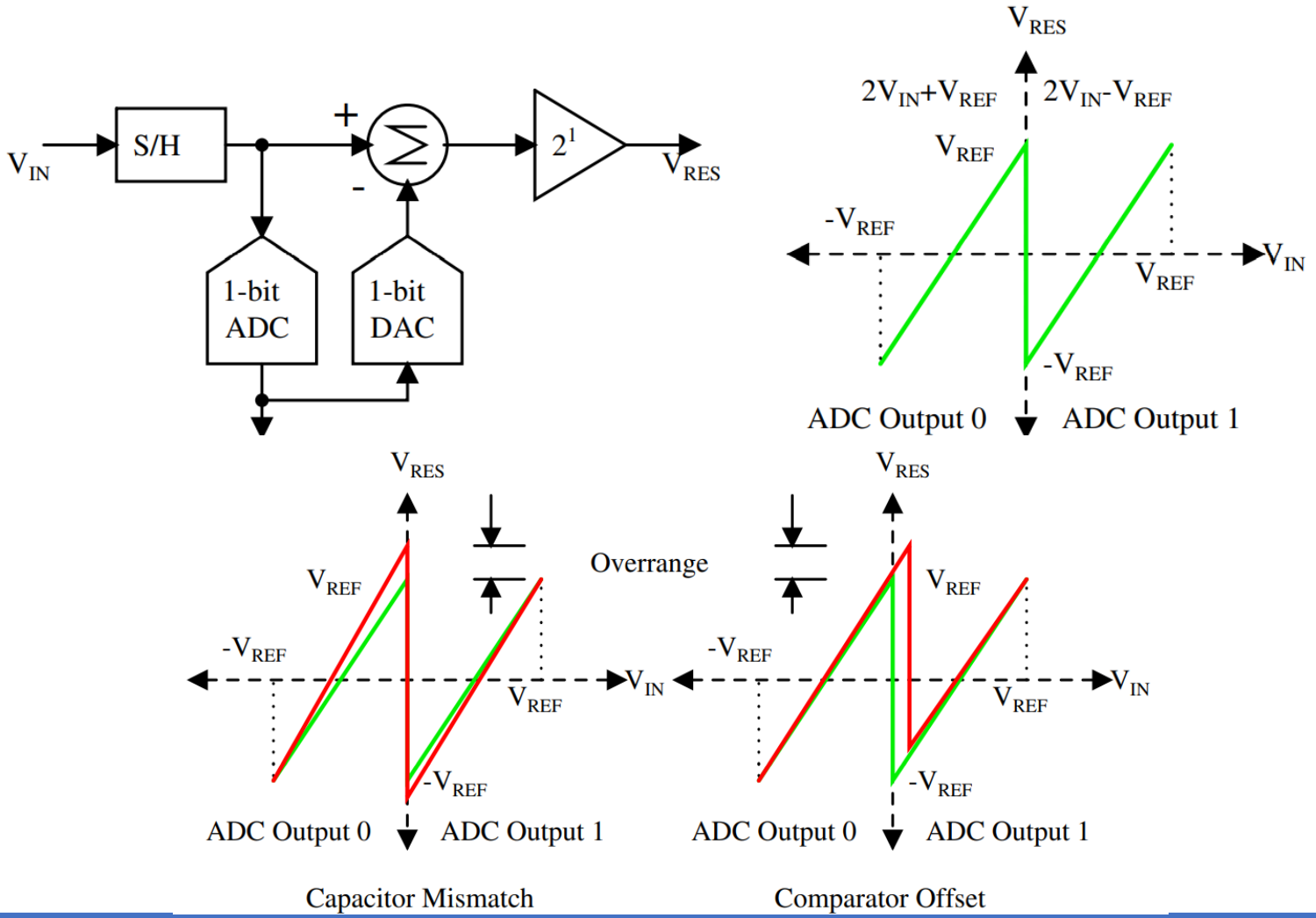
- Single Stage of Pipeline ADC



- ϕ_3 is High, during Non-overlapping period
- $C_{Load} = C_L + C_{sampling,i+1}$

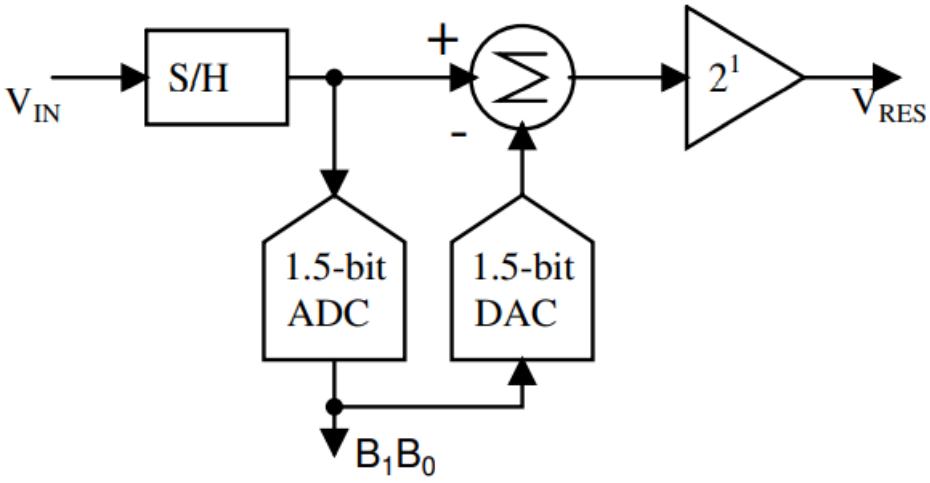
Pipeline ADC Architecture

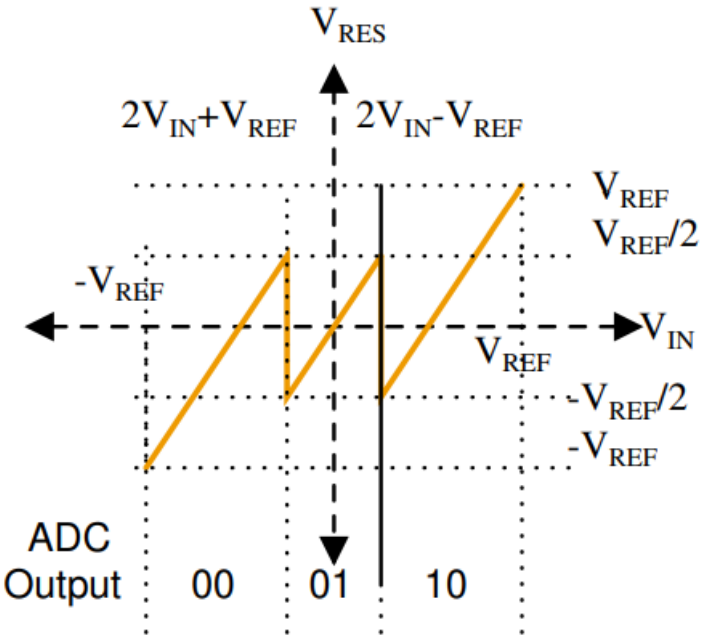
- Necessity of the Redundant Bit



Pipeline ADC Architecture

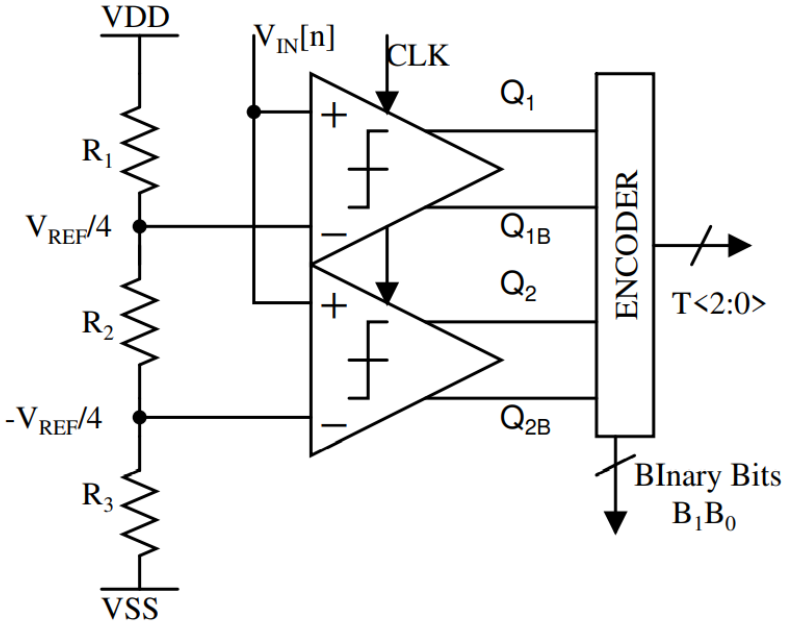
- 1.5 bits/stage block diagram and Transfer Function





Pipeline ADC Architecture

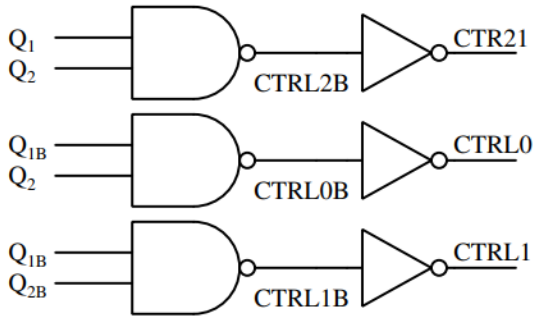
- 1.5 bit Sub-ADC

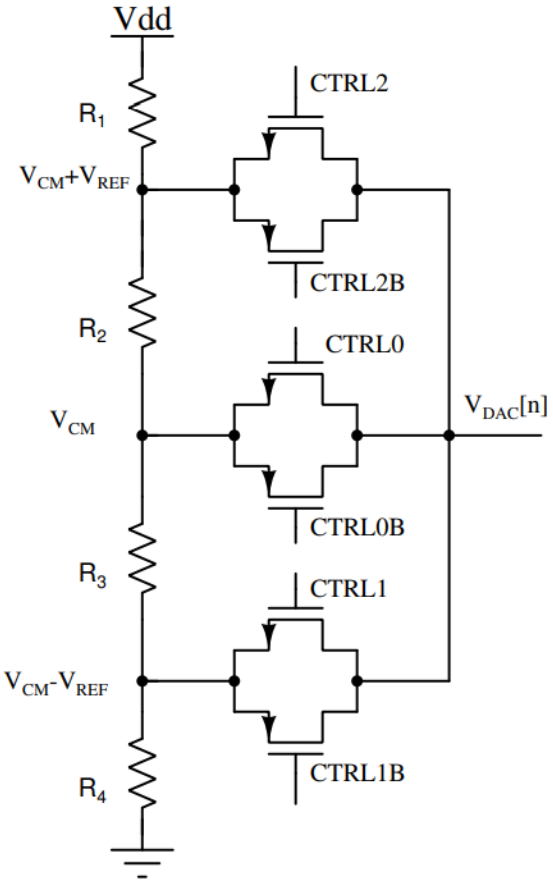


Sub-ADC Input(V_{IN})	Q_1	Q_2	Q_{1B}	Q_{2B}	B_1	B_0
$V_{IN} \leq -V_{REF}/4$	0	0	1	1	0	0
$-V_{REF}/4 \leq IN \leq V_{REF}/4$	0	1	1	0	0	1
$V_{IN} \geq V_{REF}/4$	1	1	0	0	1	0

Pipeline ADC Architecture

- 1.5-bit DAC

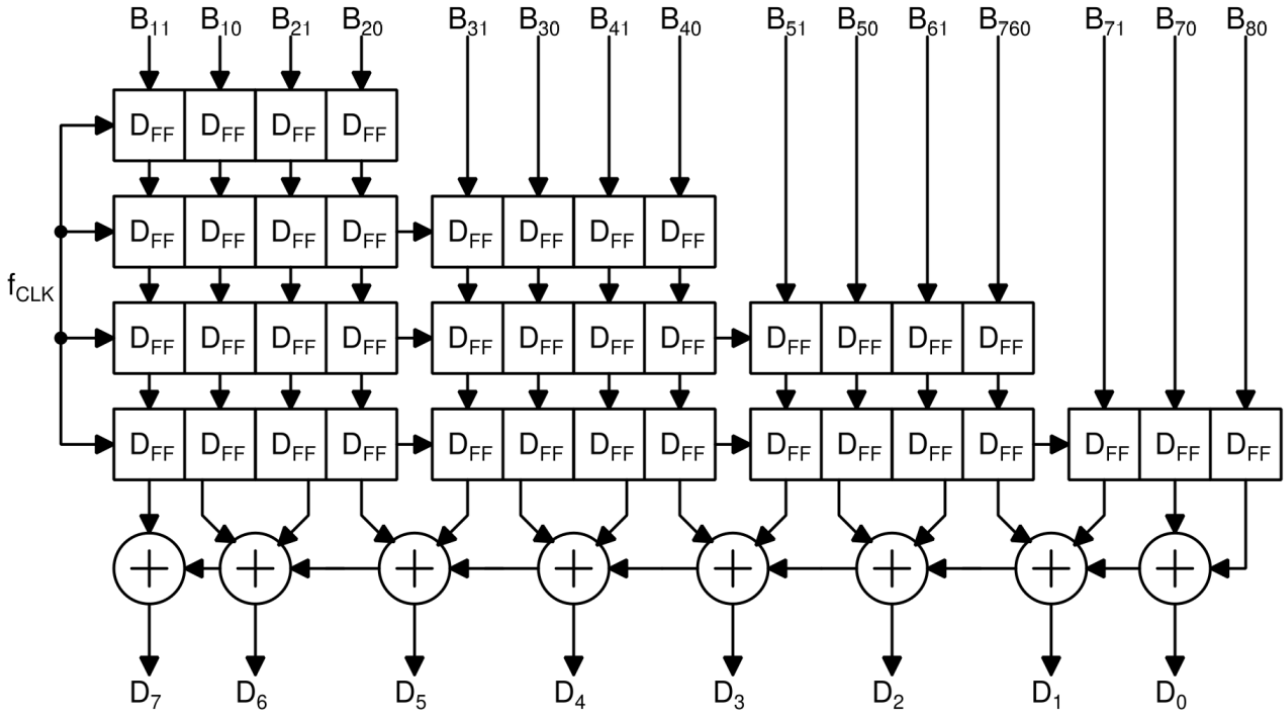




Q_1	Q_2	Q_{1B}	Q_{2B}	CTRL1	CTRL0	CTRL2	V_{DAC}
0	0	1	1	1	0	0	V_{CM} -V_{REF}
0	1	1	0	0	1	0	V_{CM}
1	1	0	0	0	0	1	V_{CM}+V_{REF}

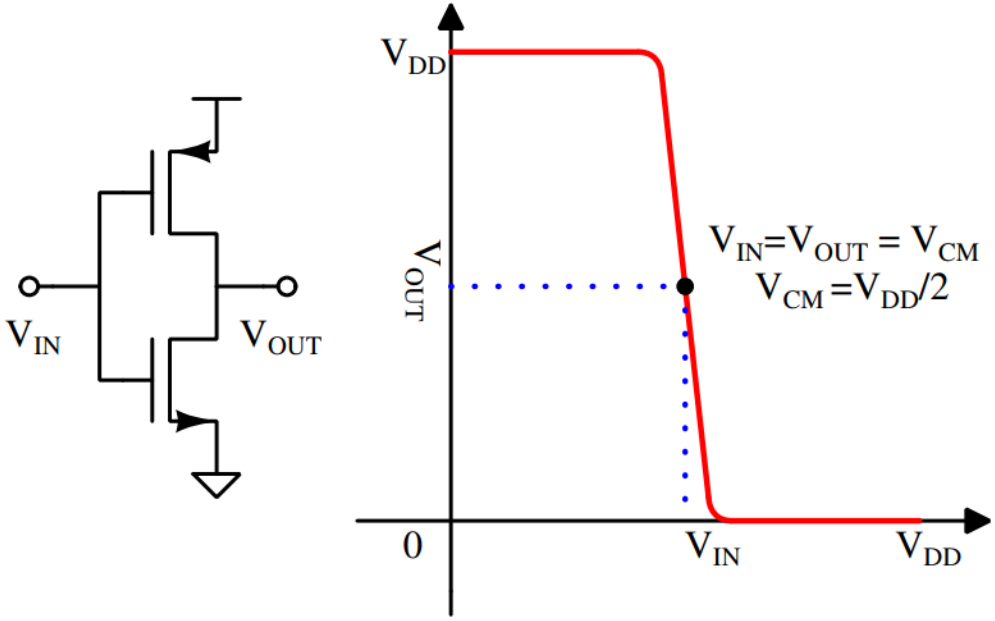
Pipeline ADC Architecture

- Digital Bit Alignment and Correction



Conventional Ring Amplifier

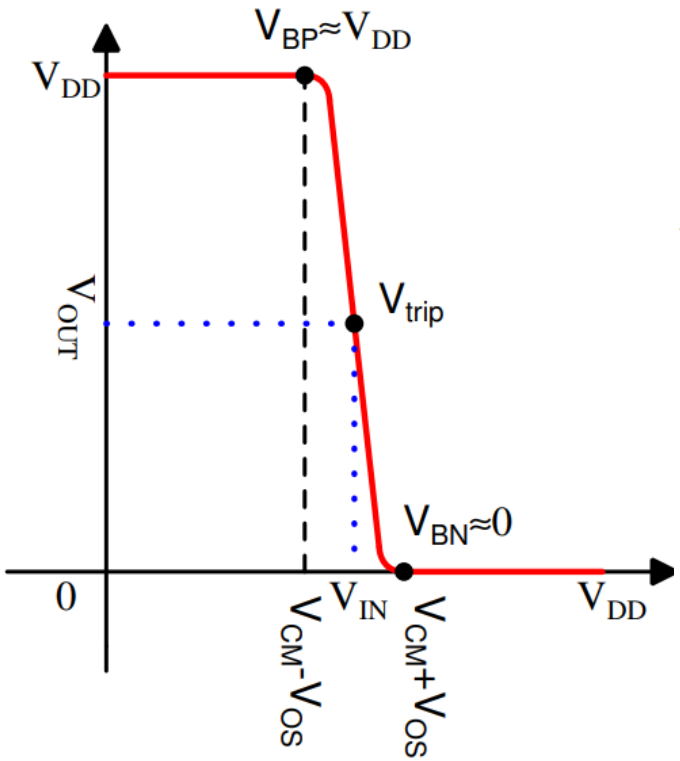
- Inverter Characteristics
  - High gain, High Bandwidth
  - Balanced at the trip point
    ($V_{IN} = V_{OUT} = V_{CM}$)

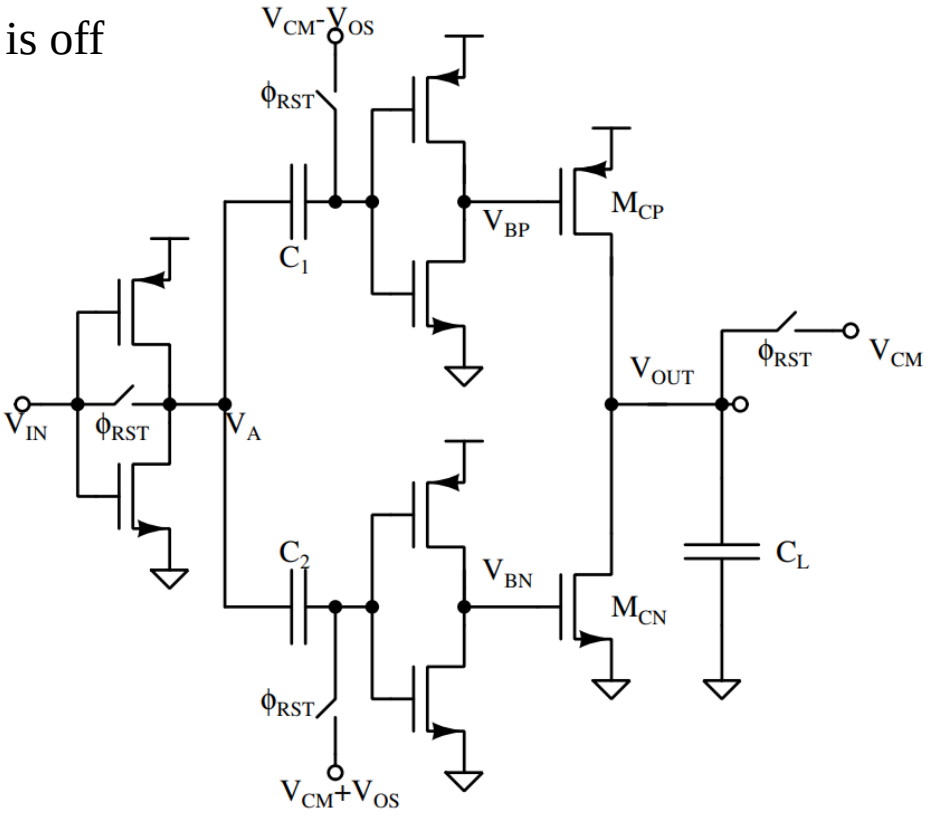


Conventional Ring Amplifier

- Operation of the Ring Amplifier
  - ϕ_{rst} is High: Ring Amplifier is off

$\therefore V_{IN} = V_A = V_{CM}$





$$\mathbf{V_{BP} > V_{DD} - |V_{thp}|,\ V_{BN} < V_{thn}}$$

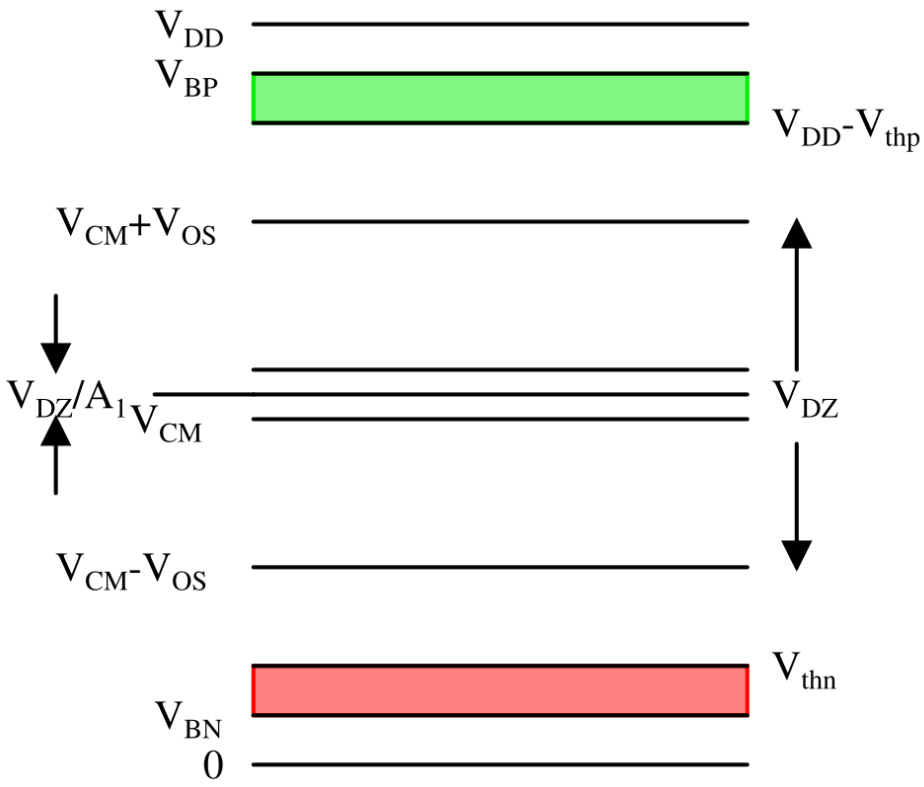
B. Hershberg, S. Weaver, K. Sobue, S. Takeuchi, K. Hamashita and U. Moon, "Ring Amplifiers for Switched Capacitor Circuits," in IEEE Journal of Solid-State Circuits, vol. 47, no. 12, pp. 2928-2942, Dec. 2012, doi: 10.1109/JSSC.2012.2217865.

Conventional Ring Amplifier

- Dead zone
  - A_1 is gain of the First stage inverter
  - $\frac{V_{DZ}}{A_1}$ is input referred dead zone
  - Range of input V_{IN} for which

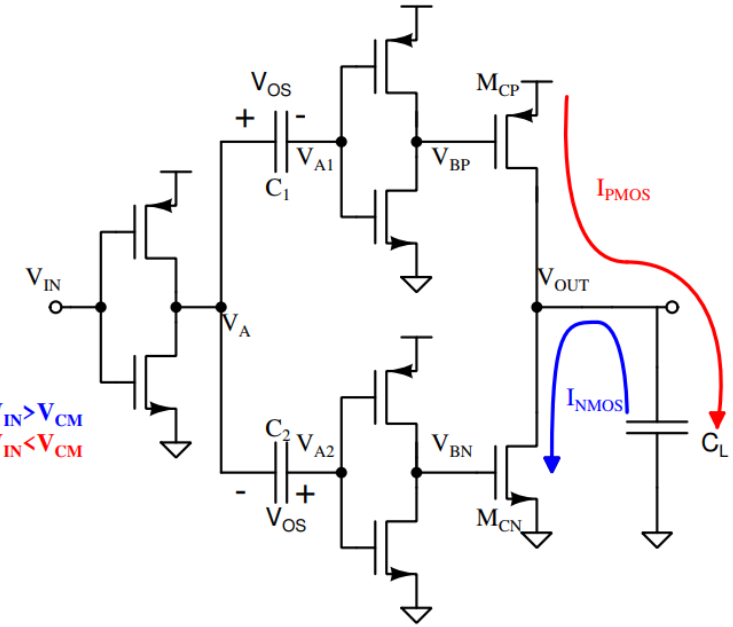
$V_{BP} > V_{DD} - V_{thp}$ and

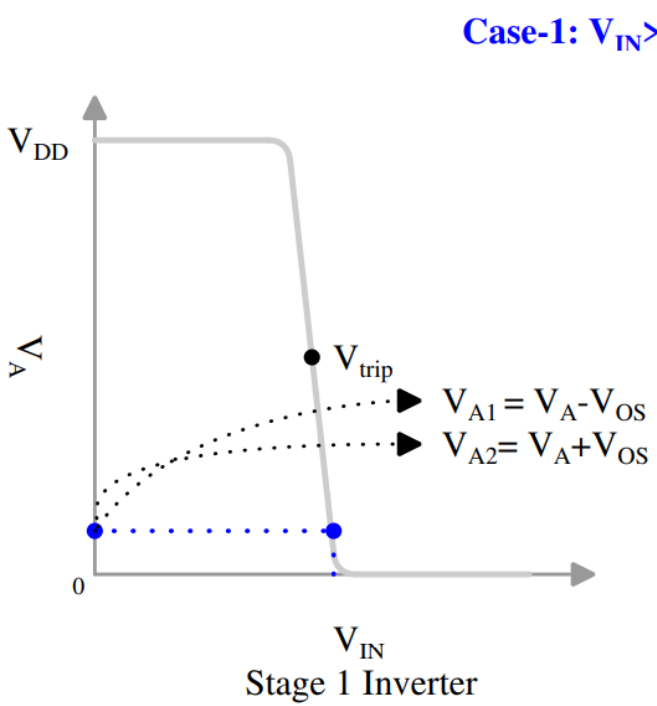
$V_{BN} < V_{thn}$ is called dead zone.

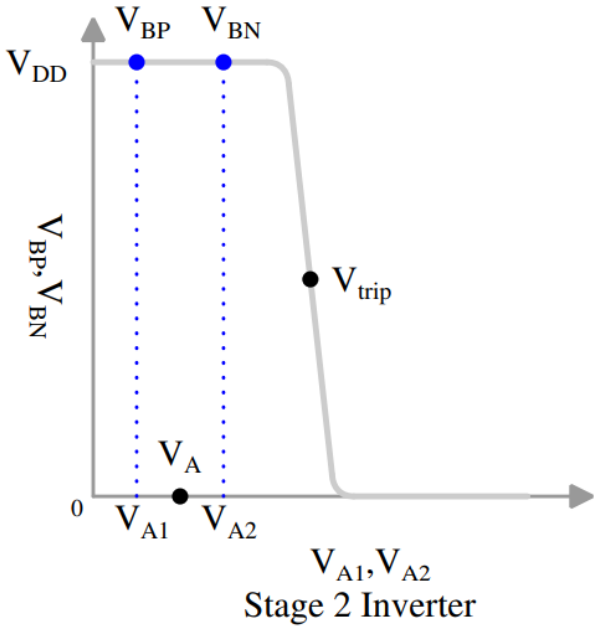


Conventional Ring Amplifier

- Case -1: $V_{IN} > V_{CM}$
  - $V_{BP} > V_{DD} - |V_{thp}|$
  - Minimum $V_{OUT} = 0$

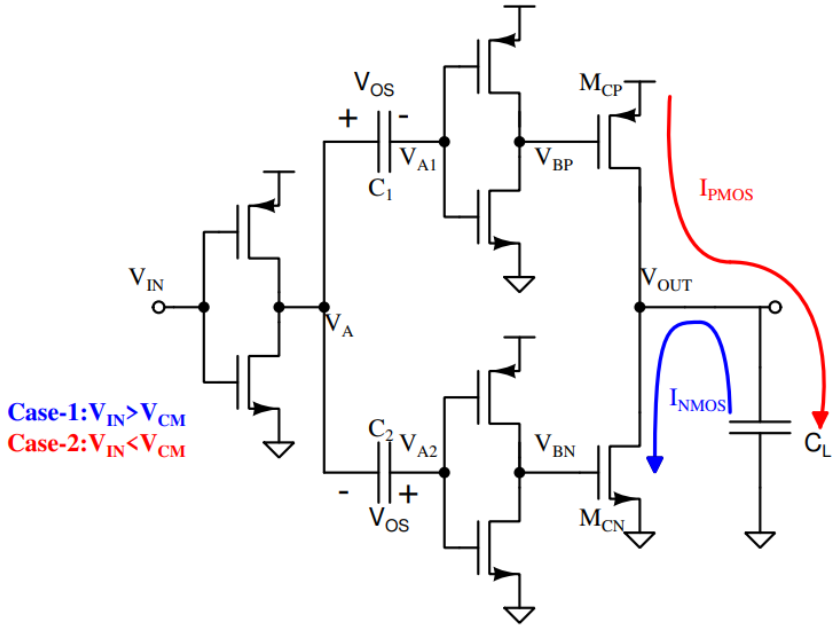


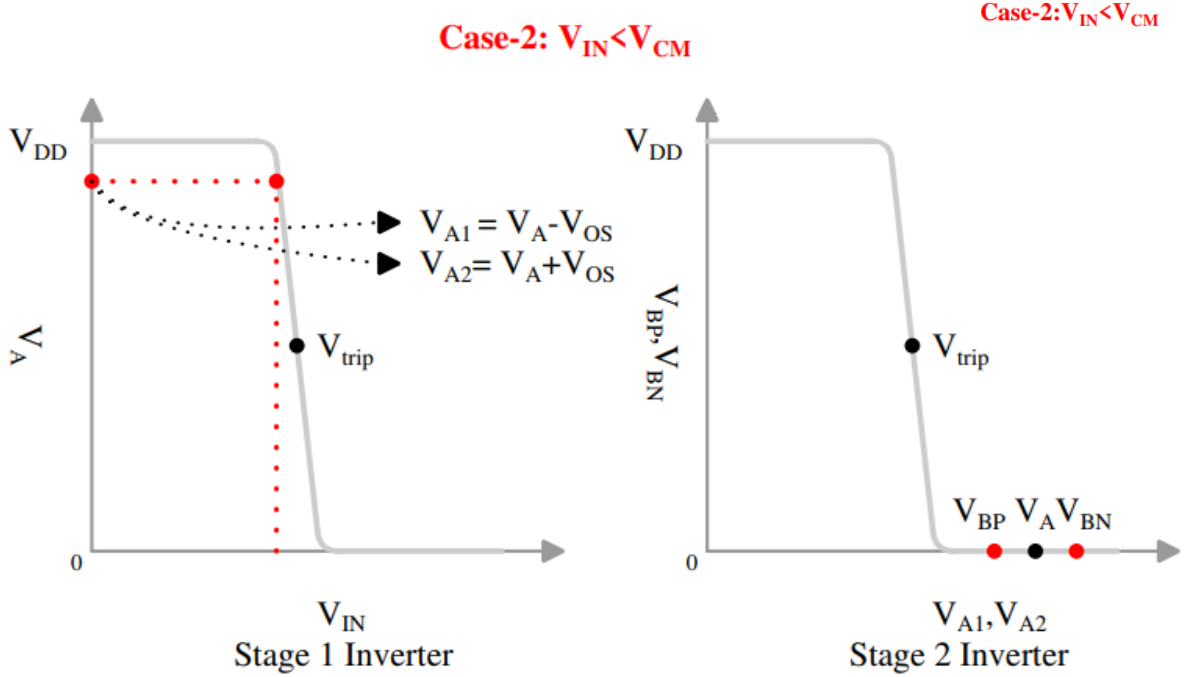




Conventional Ring Amplifier

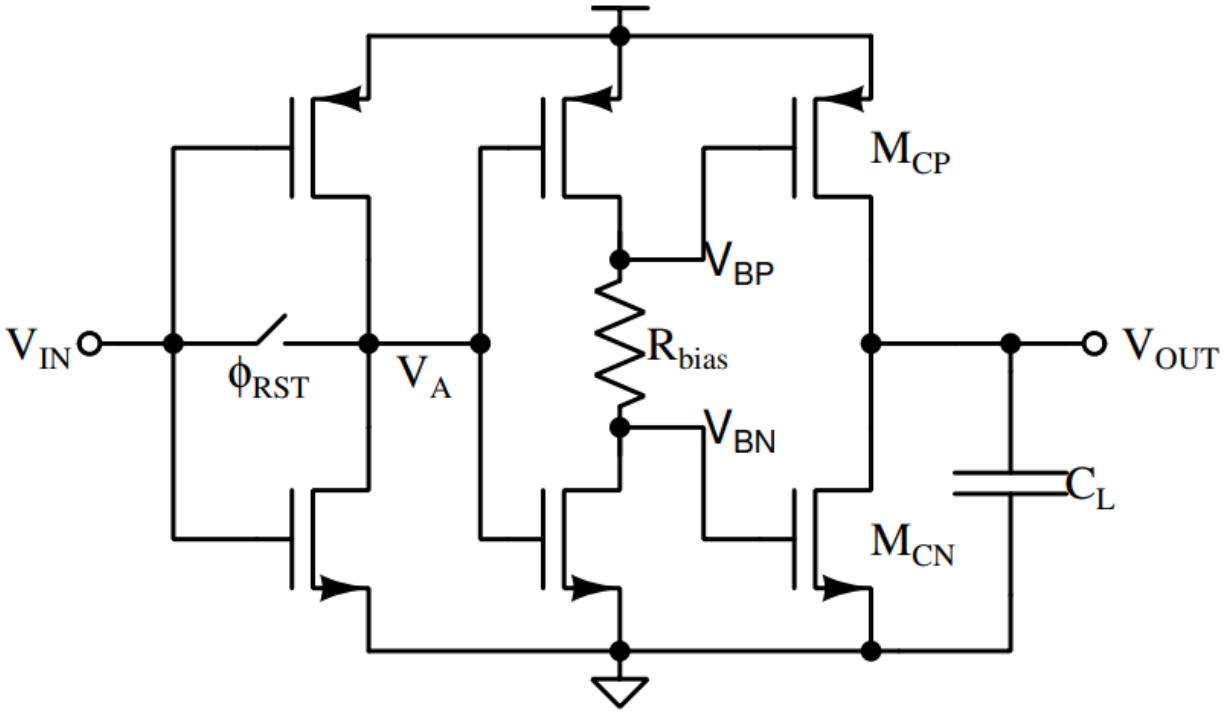
- Case -2: $V_{IN} < V_{CM}$
  - $V_{BN} < V_{thn}$
  - Maximum $V_{OUT} = VDD$





Self-Biased Ring Amplifier

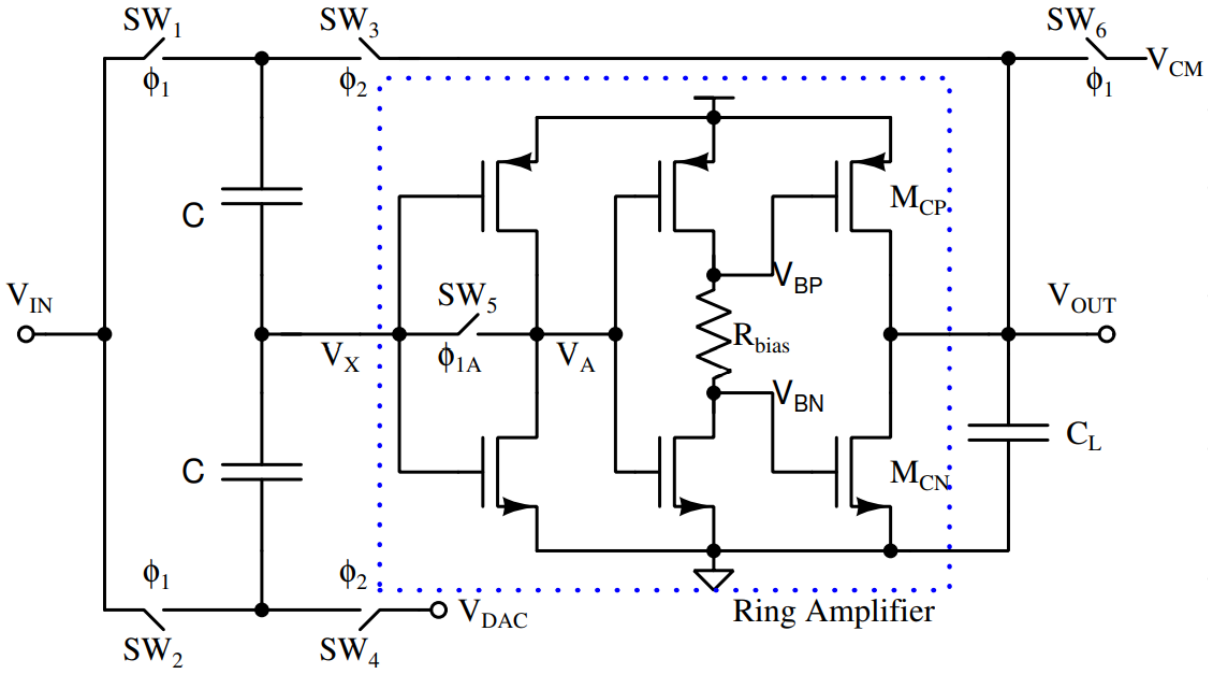
- Limitations of the Conventional Ring Amplifier
  - Floating Capacitors
  - Sensitive to PVT Variation
  - Dead zone independent of V_{DD}



Y. Lim and M. P. Flynn, "A 100 MS/s, 10.5 Bit, 2.46 mW Comparator-Less Pipeline ADC Using Self-Biased Ring Amplifiers," in IEEE Journal of Solid-State Circuits, vol. 50, no. 10, pp. 2331-2341, Oct. 2015, doi: 10.1109/JSSC.2015.2453332.

Self-Biased Ring Amplifier

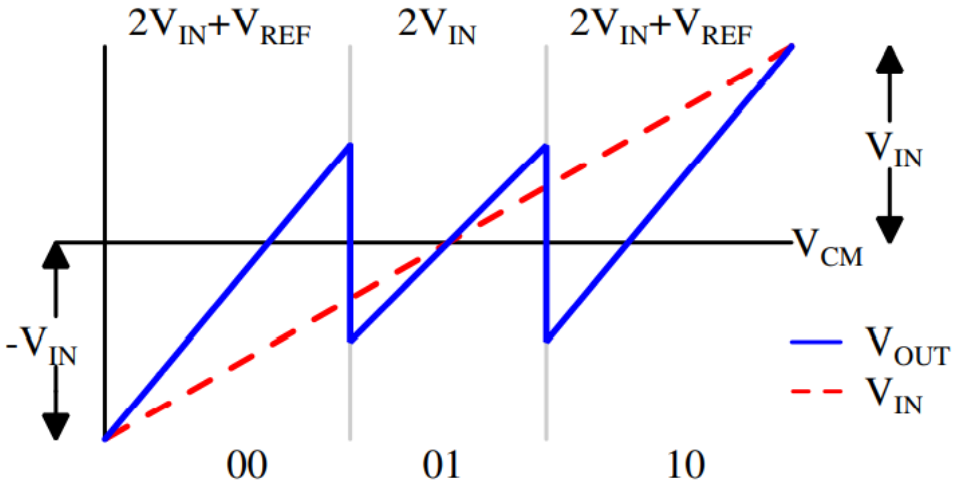
- MDAC using Self-Biased Ring Amplifier



- ϕ_1 : Sampling phase
- ϕ_2 : Amplification Phase
- V_X moves from V_{CM} to $V_{CM} - V_{in} + \frac{V_{dac}}{2} + \frac{V_{out}}{2}$
- Amplification Phase starts
- C_{Load} charges until $V_{OUT} = 2V_{in} - V_{dac}$

Self-Biased Ring Amplifier

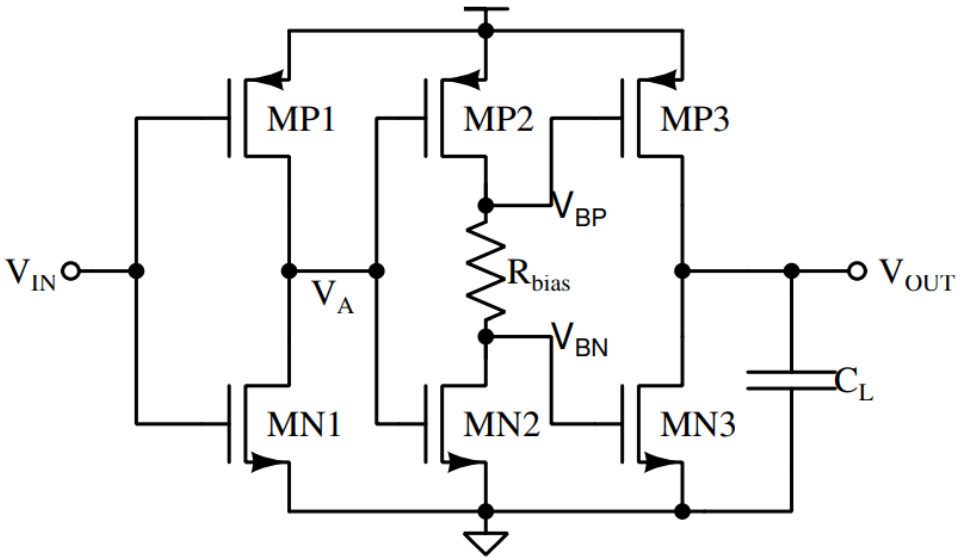
- MDAC Output



Output of Sub-ADC	Output of DAC	Output of MDAC
00	$-V_{REF}$	$2V_{IN}+V_{REF}$
01	0	$2V_{IN}$
10	V_{REF}	$2V_{IN}-V_{REF}$

Self-Biased Ring Amplifier

- Design

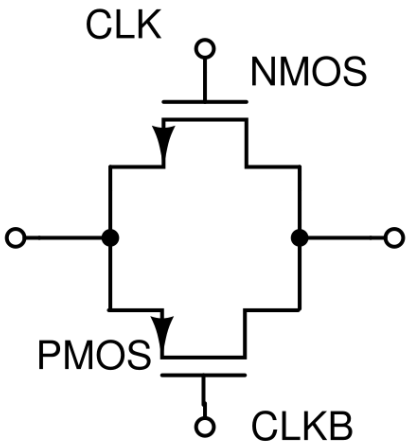


Transistor	MP1	MN1	MP2	MN2	MP3	MN3
Width (µm)	2.805	1.11	2.805	1.11	0.3	0.135
Length(nm)	90	90	90	90	60	60
Multiplier	12	12	2	2	2	2
R_{bias}(kΩ)	8		**Capacitor(fF)**		300	-

Self-Biased Ring Amplifier

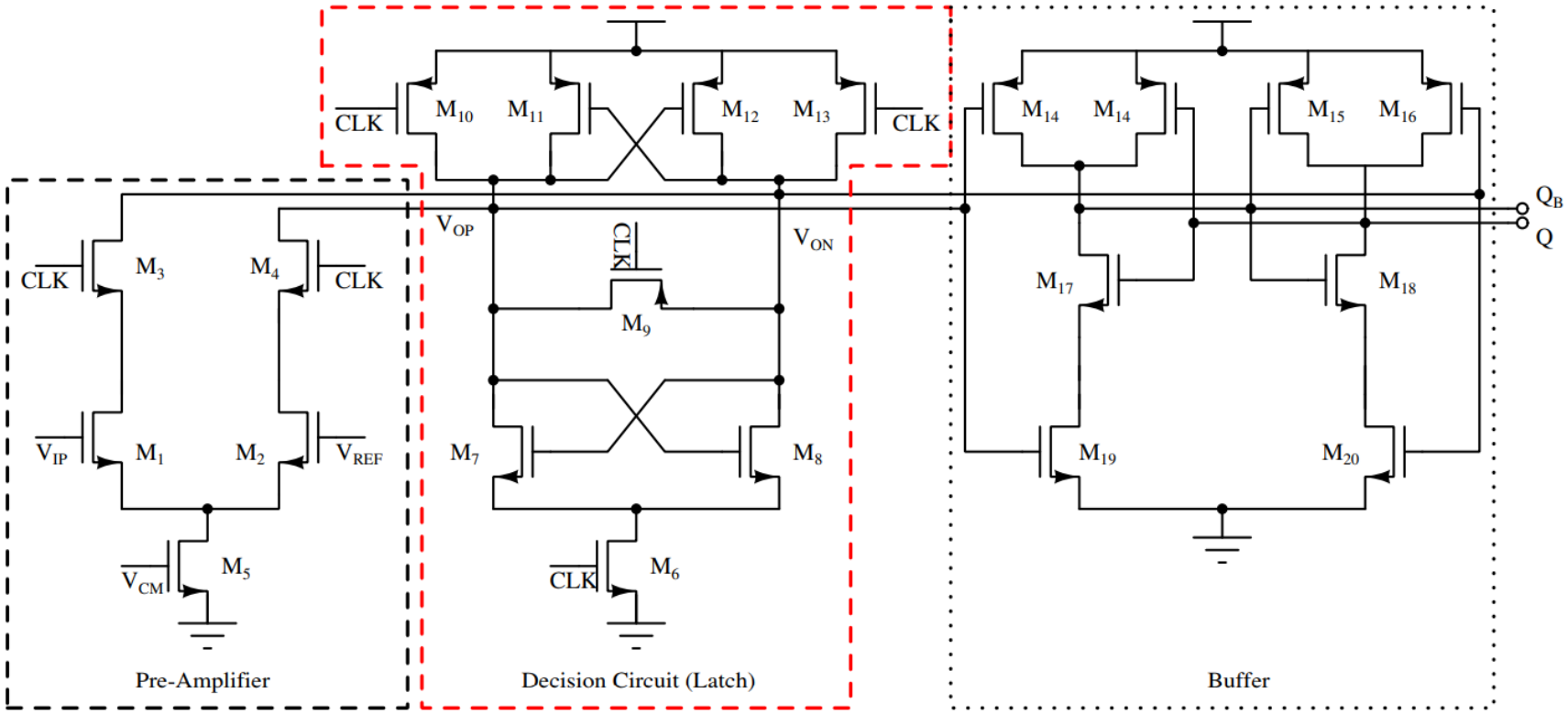
- Switch Design

Switch	W_{PMOS} (µm)	W_{NMOS} (µm)	L(nm)
Sampling Switch SW1, SW2	5	5	60
Reset Switch SW5	1.8	1.8	60
Output Switch SW6	5	5	60
Amplification Switch SW3, SW4	2.05	2.05	60



Comparator

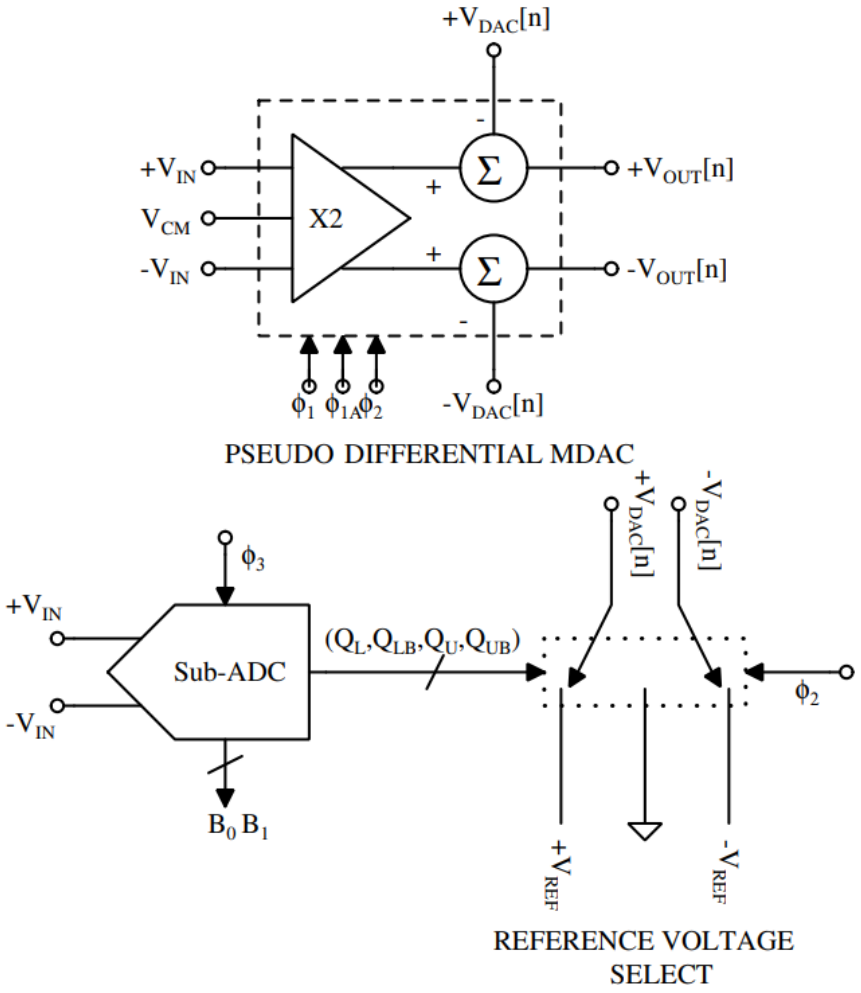
- Preamplifier Based Dynamic Comparator

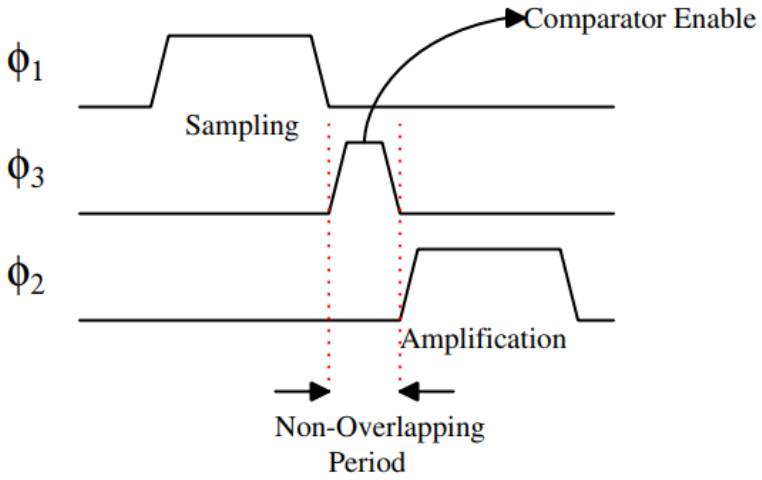


Jipeng Li and Un-Ku Moon, "A 1.8-V 67mW 10-bit 100MSPS pipelined ADC using time-shifted CDS technique," Proceedings of the IEEE 2003 Custom Integrated Circuits Conference, 2003., 2003, pp. 413-416, doi: 10.1109/CICC.2003.1249430.

Complete Pipeline ADC

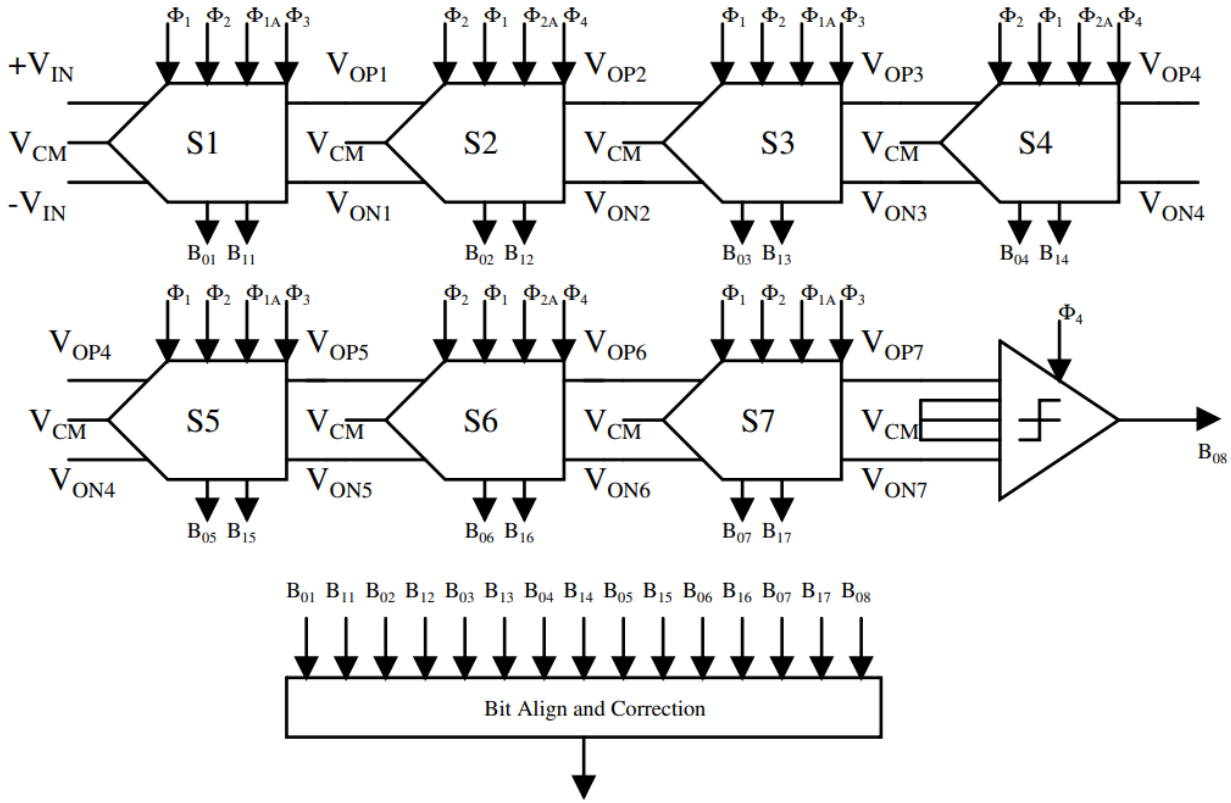
- Single Stage of Pipeline ADC





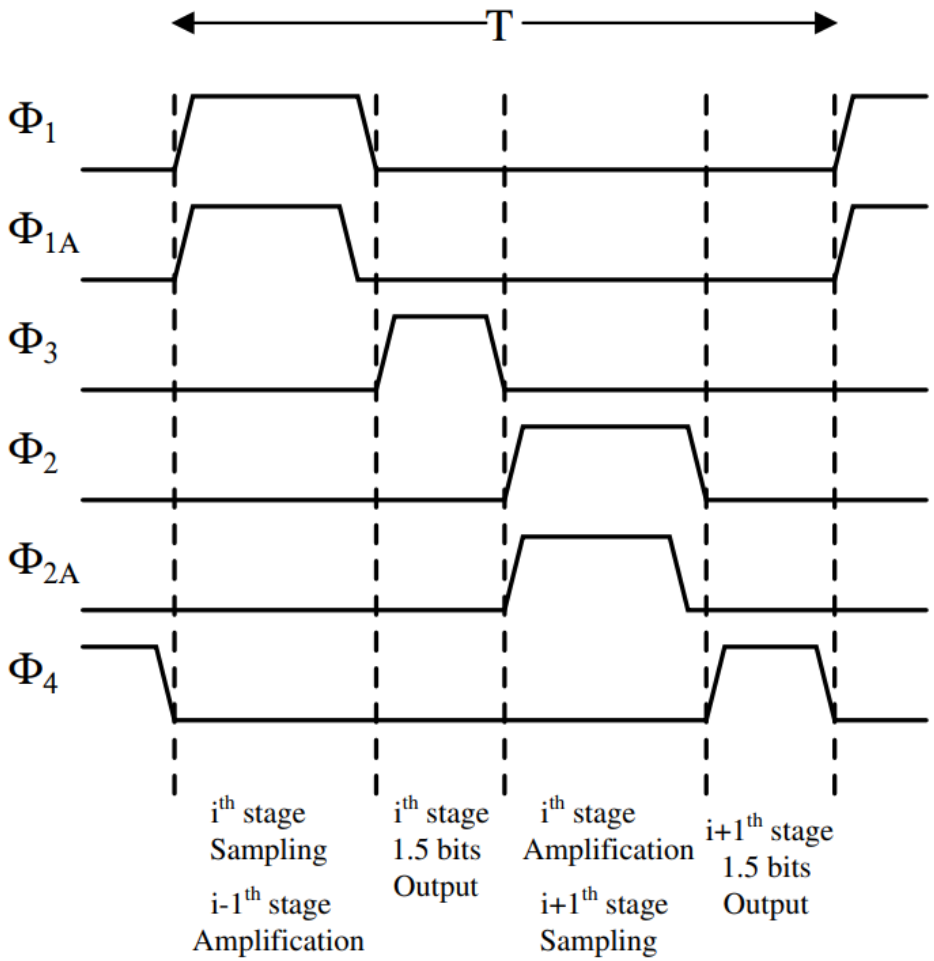
Complete Pipeline ADC

- Block Diagram of the Pipeline ADC



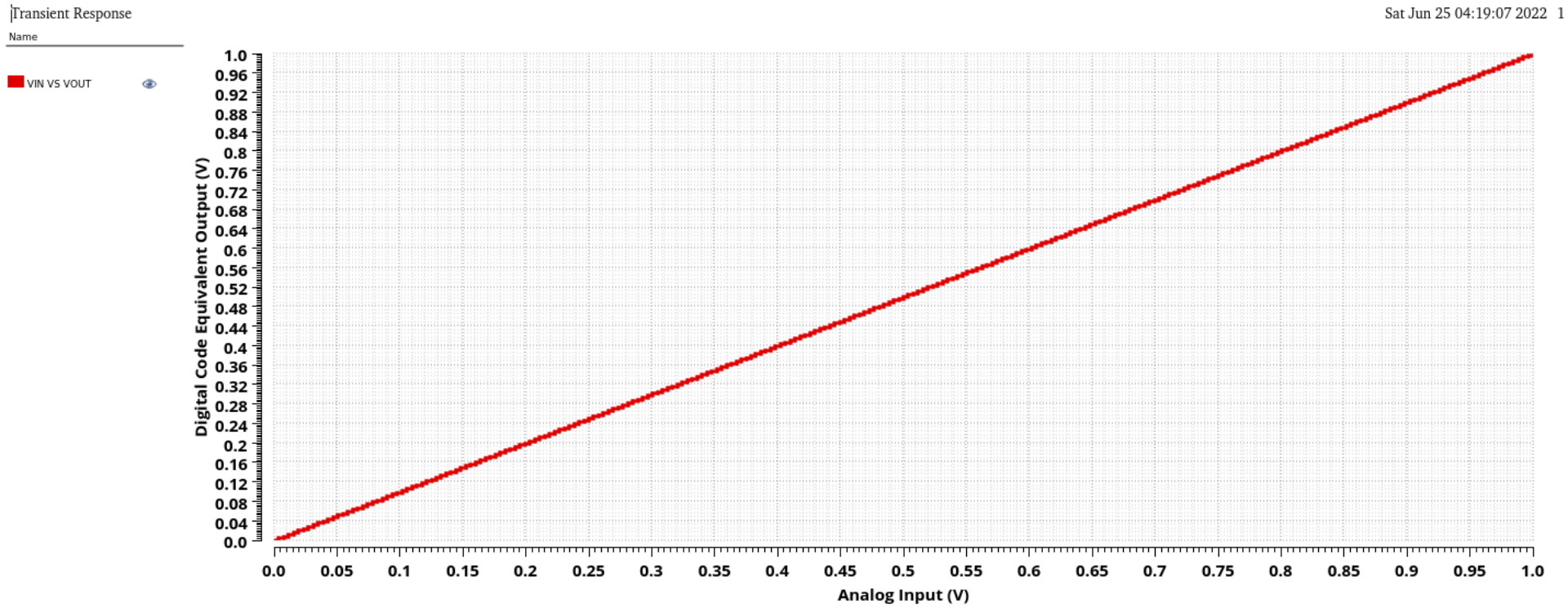
Complete Pipeline ADC

- Clock Scheme Used in the Pipeline ADC



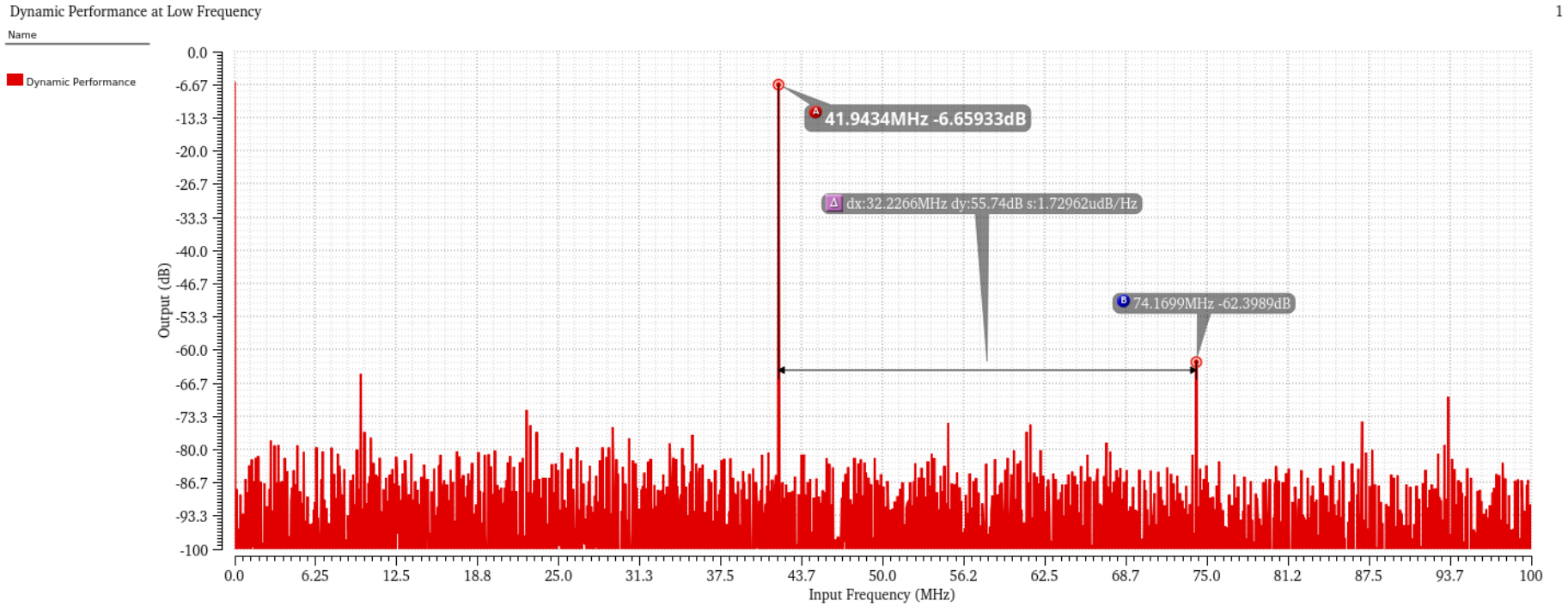
Simulations and Results

- Transient Simulation of the ADC
  - $V_{OUT} = \frac{D_7}{2} + \frac{D_6}{4} + \frac{D_5}{8} + \frac{D_4}{16} + \frac{D_3}{32} + \frac{D_2}{64} + \frac{D_1}{128} + \frac{D_0}{256}$



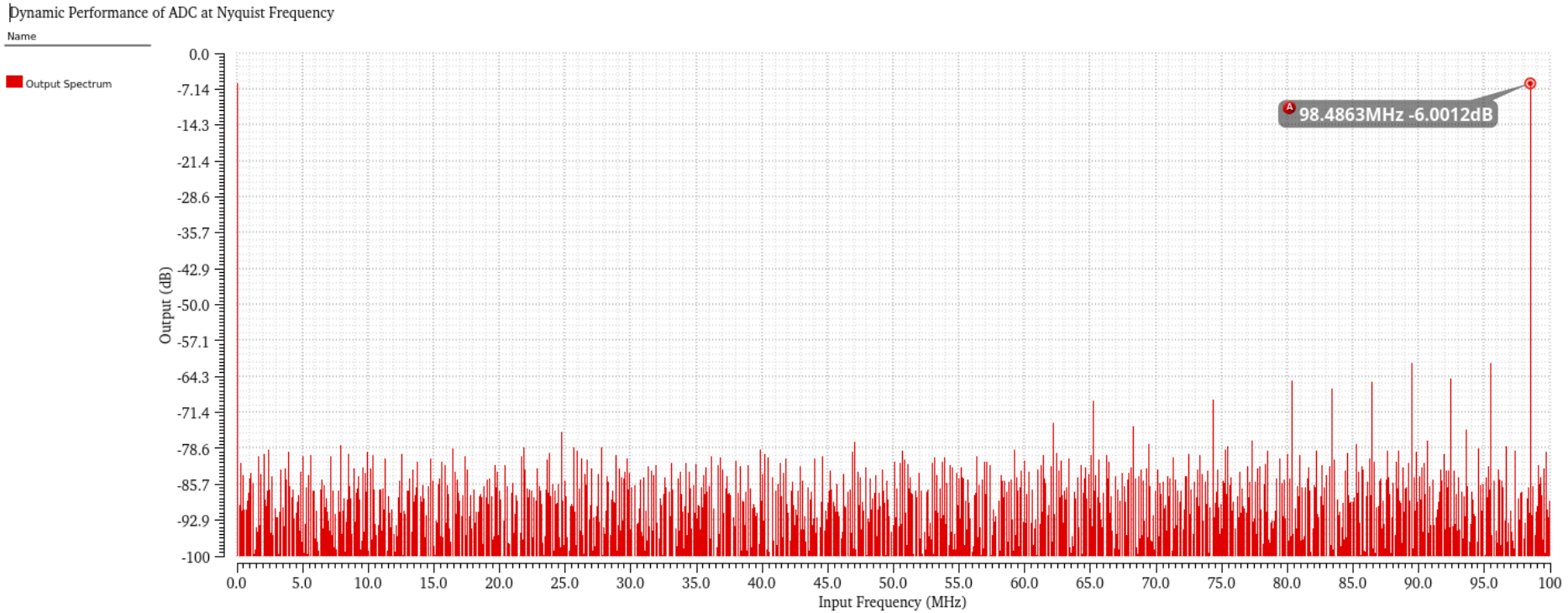
Simulations and Results

- Dynamic Performance of the ADC
  - N = 4096 for FFT plot, $f_{sample} = 200MHz$
  - For Low frequency, M = 859 → $f_{in} \approx 42MHz$
  - ENOB = 7.73b, SNDR = 48.3dB, SFDR = 55.73 dBc



Simulations and Results

- Dynamic Performance of the ADC
  - N = 4096 for FFT plot, $f_{sample} = 200MHz$
  - For Nyquist frequency, M = 2017 → $f_{in} \approx 98MHz$
  - ENOB = 7.62b, SNDR = 47.68dB, SFDR = 54.3 dBc

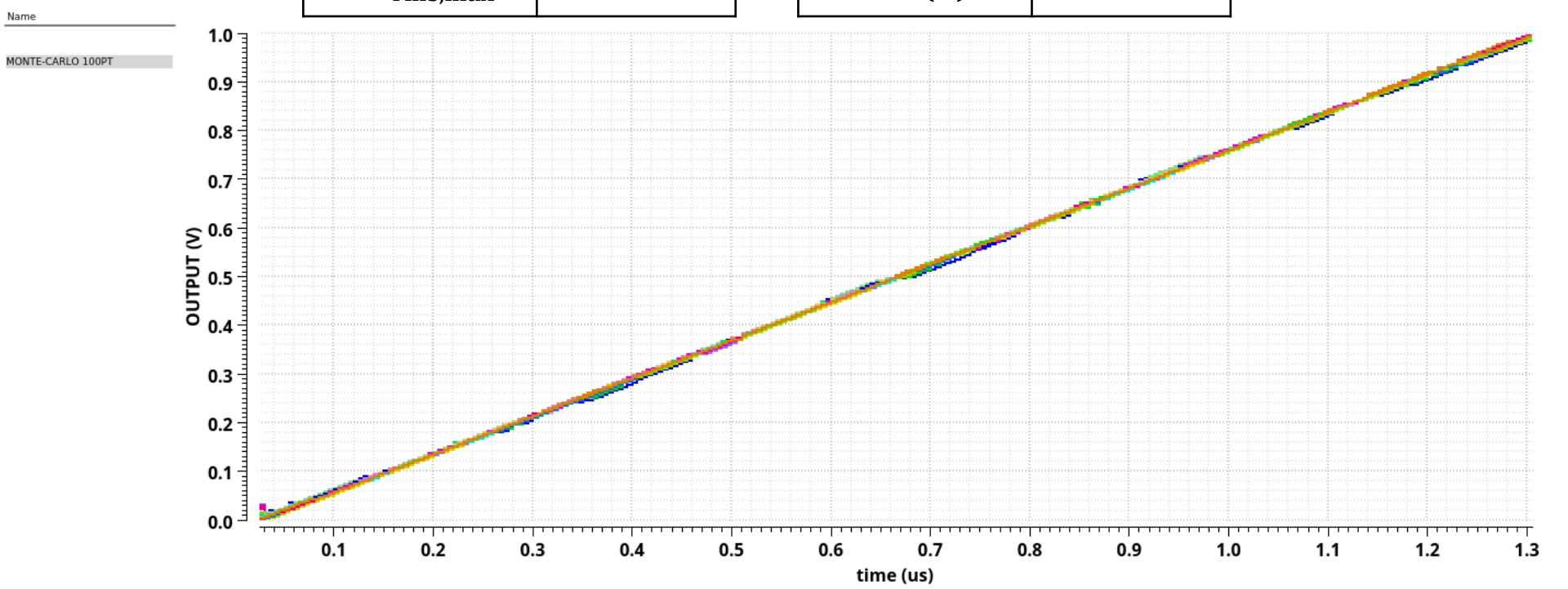


Simulations and Results

- Static Performance of ADC
  - 100 point Monte-Carlo simulation performed: Ideal LSB =3.90625mV

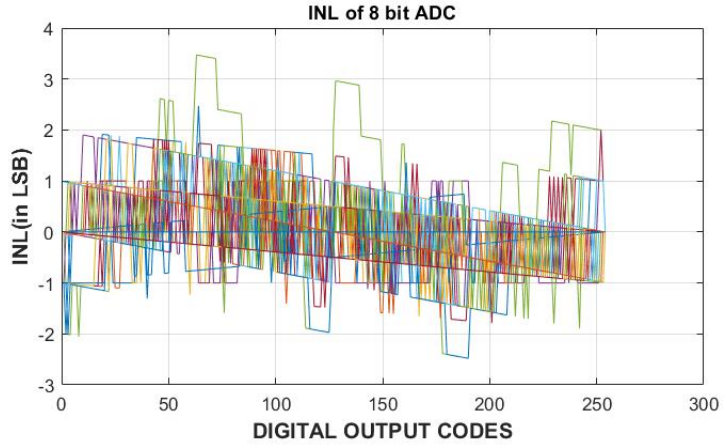
	LSB
$\mathbf{DNL_{rms,max}}$	0.65
$\mathbf{INL_{rms,max}}$	0.91

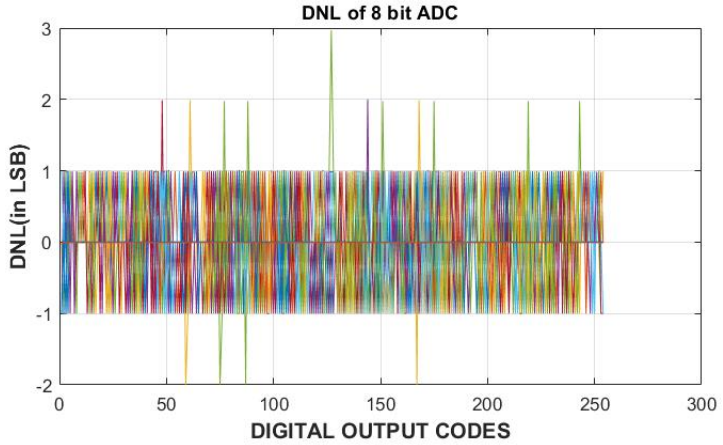
	mV
$\mathbf{Mean}(\boldsymbol{\mu})$	3.92
$\mathbf{S.D.}(\boldsymbol{\sigma})$	0.012

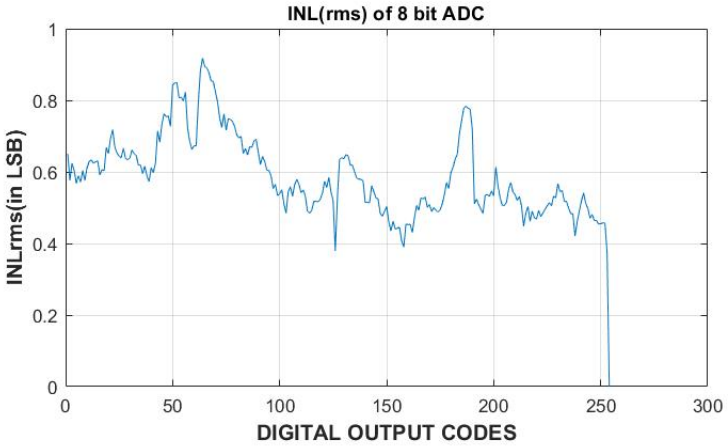


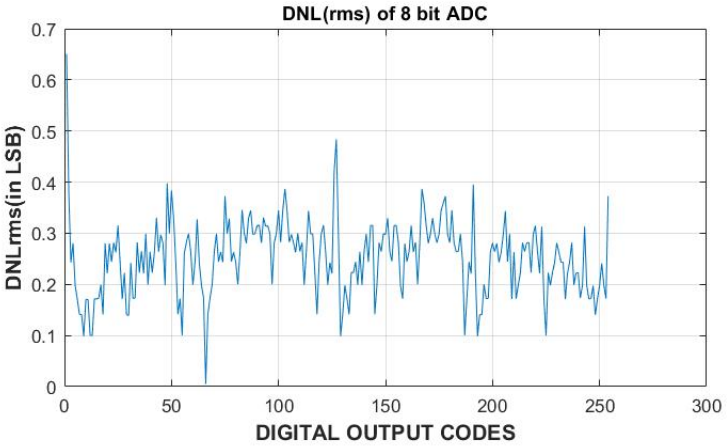
Simulations and Results

- Static Performance of ADC



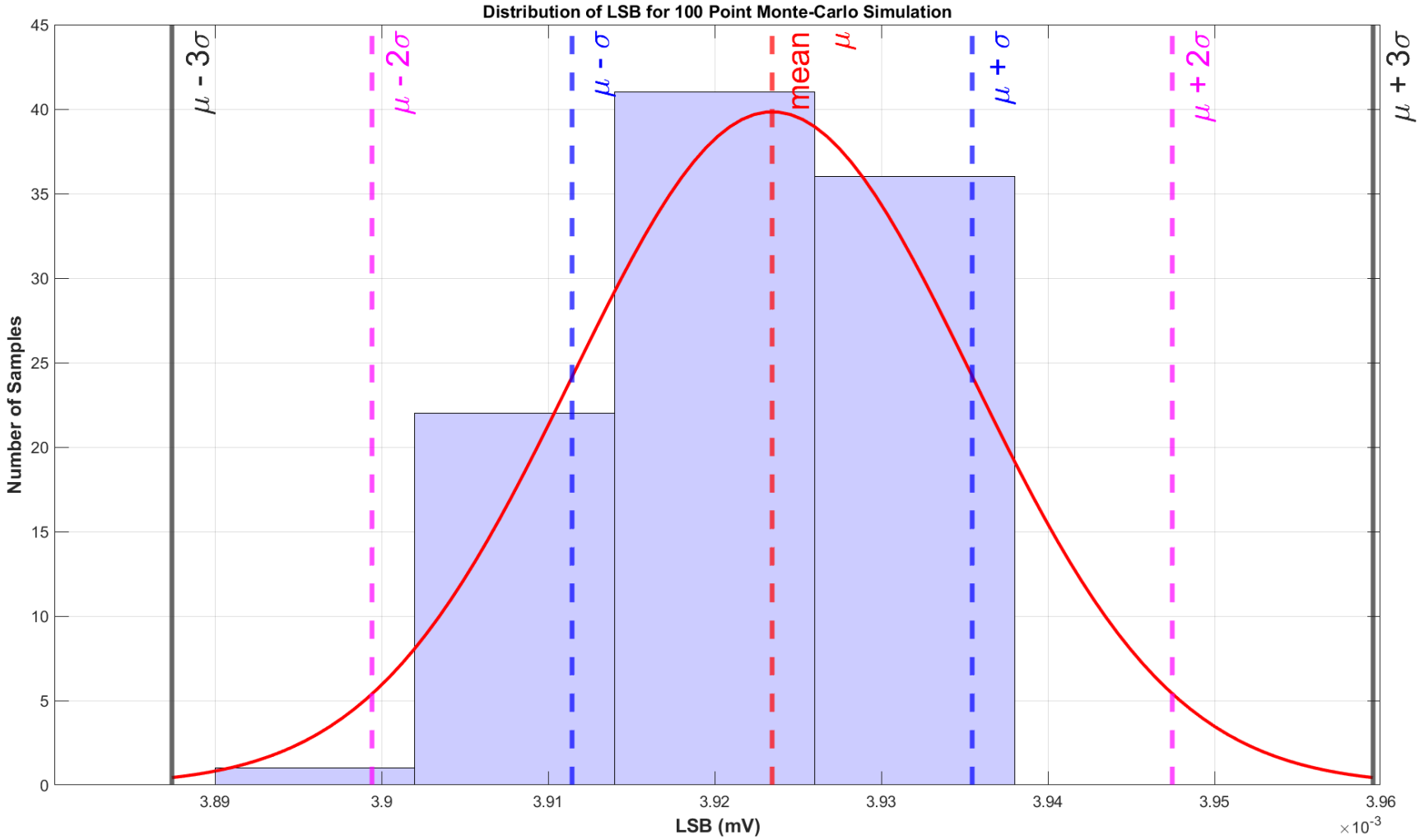






Simulations and Results

- Static Performance of ADC



Simulations and Results

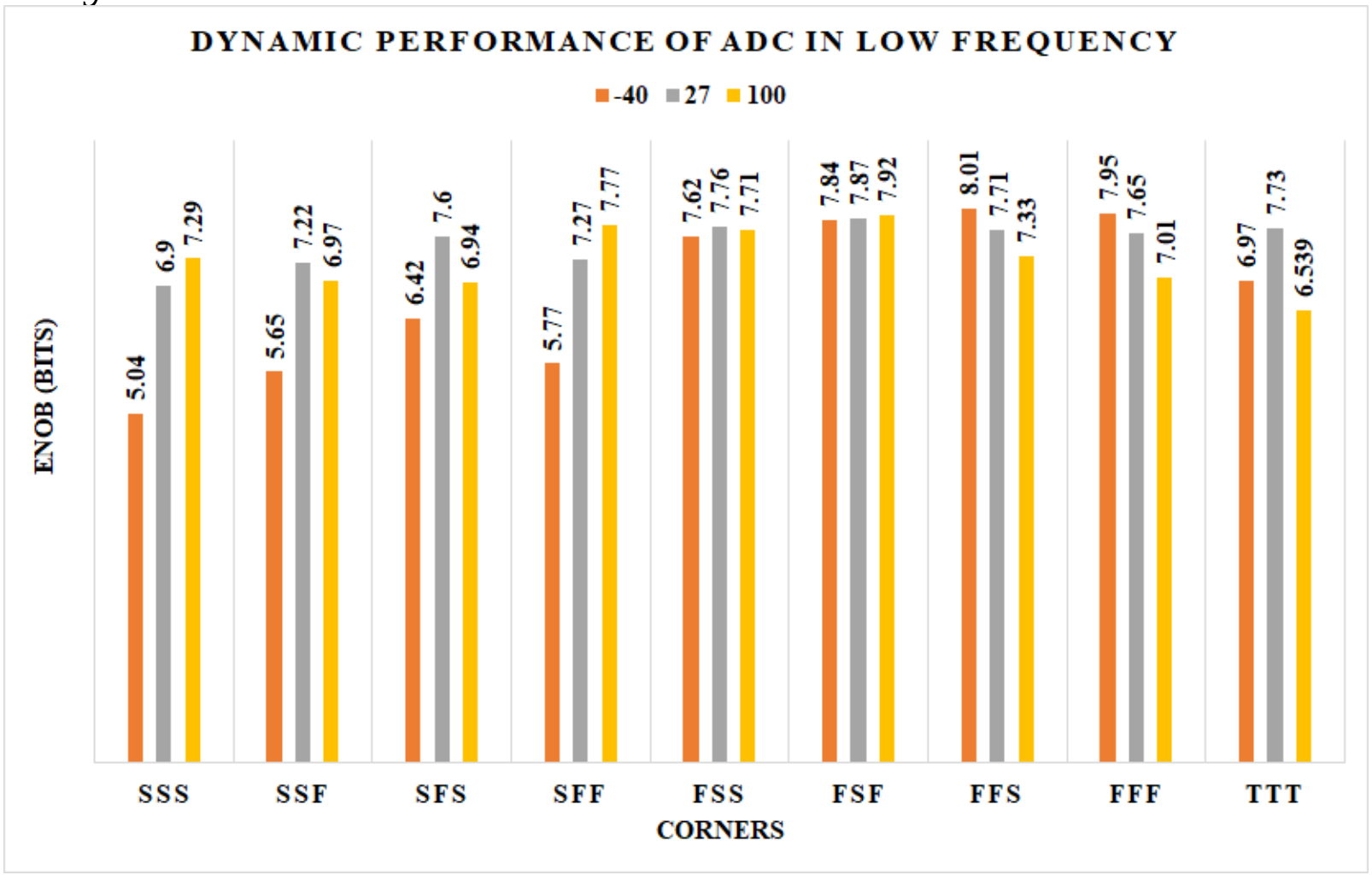
- Dynamic Performance [ENOB] in Different Corners
- Corner :[Transistor Resistor Capacitor] ex. SSS = [Slow Slow Slow]

Low Frequency (M = 859)			
	Temperature		
Corner	-40	27	100
SSS	5.04	6.9	7.29
SSF	5.65	7.22	6.97
SFS	6.42	7.6	6.94
SFF	5.77	7.27	7.77
FSS	7.62	7.76	7.71
FSF	7.84	7.87	7.92
FFS	8.0	7.71	7.33
FFF	7.95	7.65	7.0
TTT	6.97	7.73	6.54

High Frequency (M = 2017)			
	Temperature		
Corner	-40	27	100
SSS	3.86	6.63	6.5
SSF	4.96	7.09	6.59
SFS	5.97	6.76	7.14
SFF	5.18	6.38	7.08
FSS	7.53	7.66	7.7
FSF	7.6	7.57	7.79
FFS	7.89	7.58	6.69
FFF	7.83	6.93	6.84
TTT	6.38	7.44	6.25

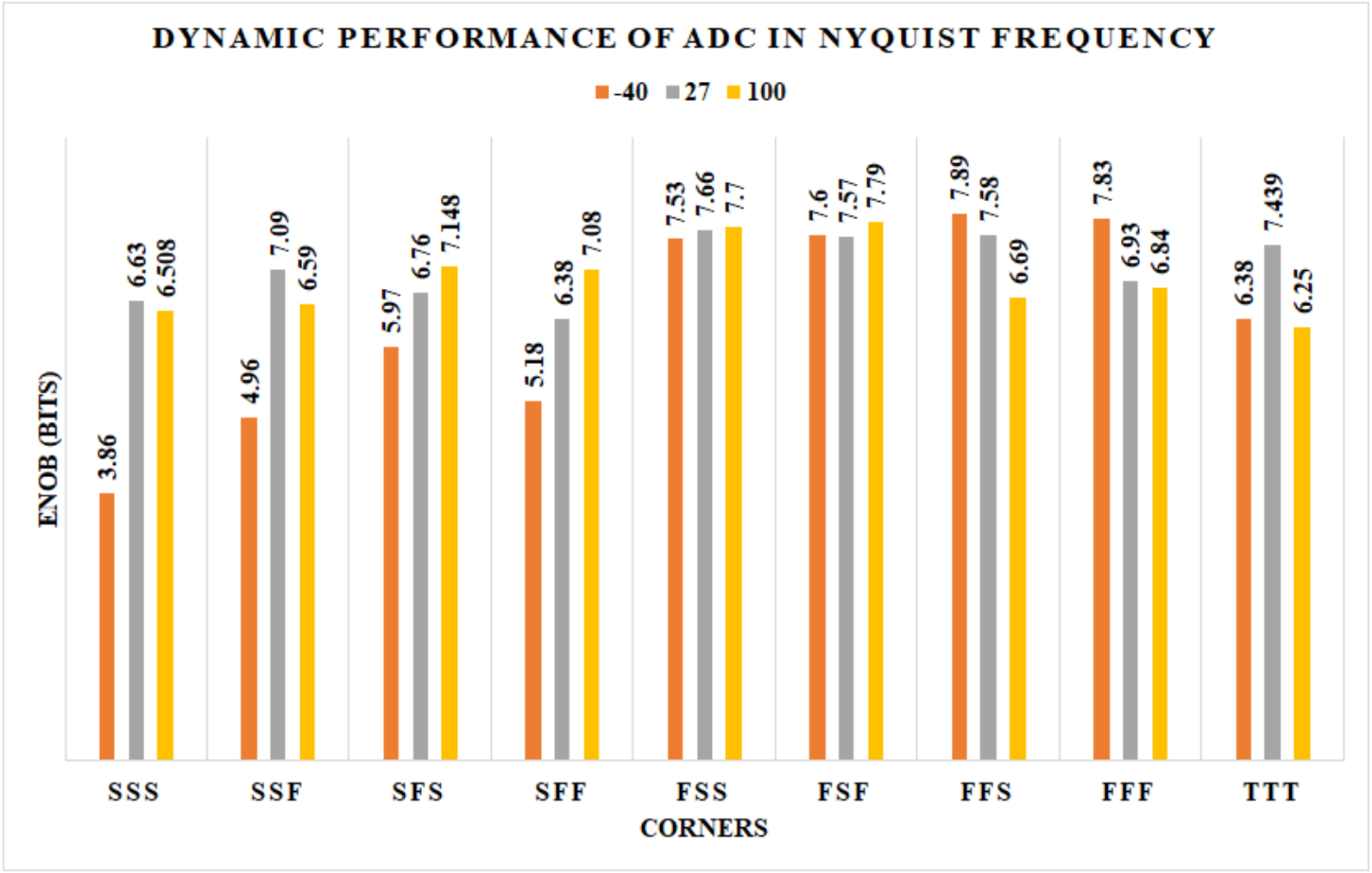
Simulations and Results

- Dynamic Performance in Different Corners



Simulations and Results

- Dynamic Performance in Different Corners



Conclusion

- Ring Amplifier designed for interstage residue amplification.
- 8 bit Pipeline ADC is constructed using Sub-ADC(1.5 bit) and MDAC.
- Operating frequency is 200Msps. Total latency of the pipeline ADC is 5 clock cycle:
  - 4 Clock cycles for bit alignment
  - 1 clock cycle for bit correction
- For proposed pipeline ADC, ENOB, SNDR and SFDR are 7.44, 47.68 and 54.3 achieved for the $f_{in} \approx 98MHz$(Nyquist frequency)
- $DNL_{rms,max}$ and $INL_{rms,max}$ are less than LSB

Future Work

- Ring Amplifier structure can be explored more low power consumption and to improve the performance in the corners
- Comparators needs to be optimized for minimum power consumption and accuracy
- Clock generator circuit using logic gates
- Transistor level implementation of the digital components like D flip-flop and adders
- Layout of the complete pipeline ADC

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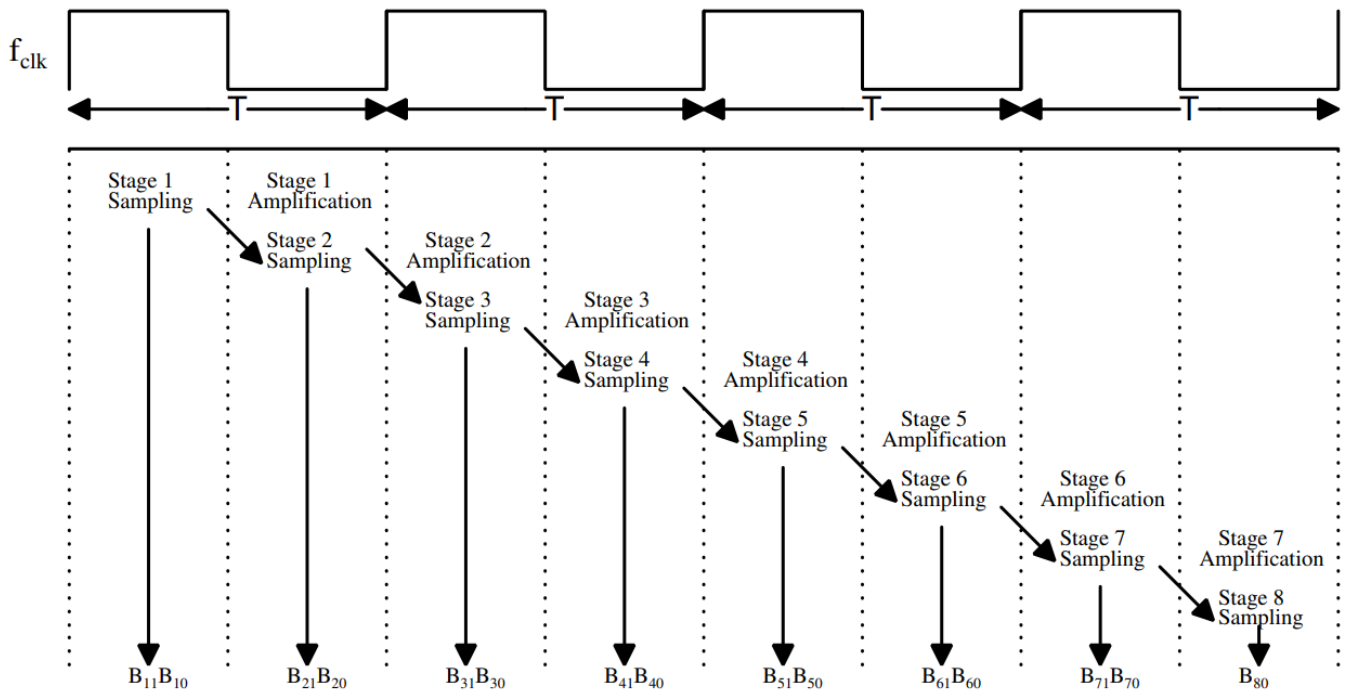
THANK YOU

Pipeline ADC Architecture

- Pipeline ADC Operations

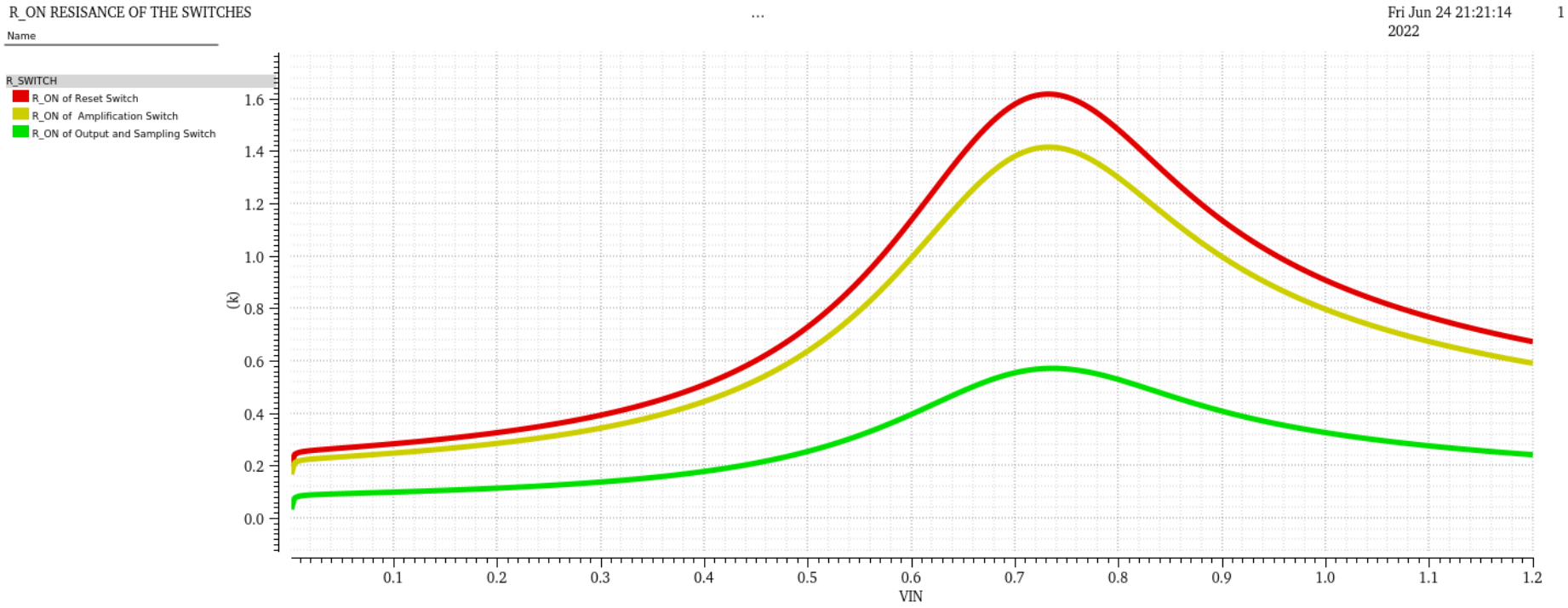


Comparison

Comparison of Proposed ADC with Published Work					
	JSSC 2012[4]	**JSSC 2015[5]**	**ICEIC 2020[12]**	**ISCAS 2015[13]**	**This Work**
f_{sample}(MHz)	30	100	100	70	200
Resolution(bits)	10.5	10.5	11	10	8
ENOB(bits)	9.9	9.33	10.8	8.36	7.44
SNDR(dB)	61.9	57.9	66.8	52	47.68
SFDR(dBc)	74.2	71.9	76.03	-	54.3
Power(mW)	2.6	2.46	18.6	3.64	22
FoM(fJ/C-step)	90	38.4	104	159.2	460
Technology	180	65	65	90	65

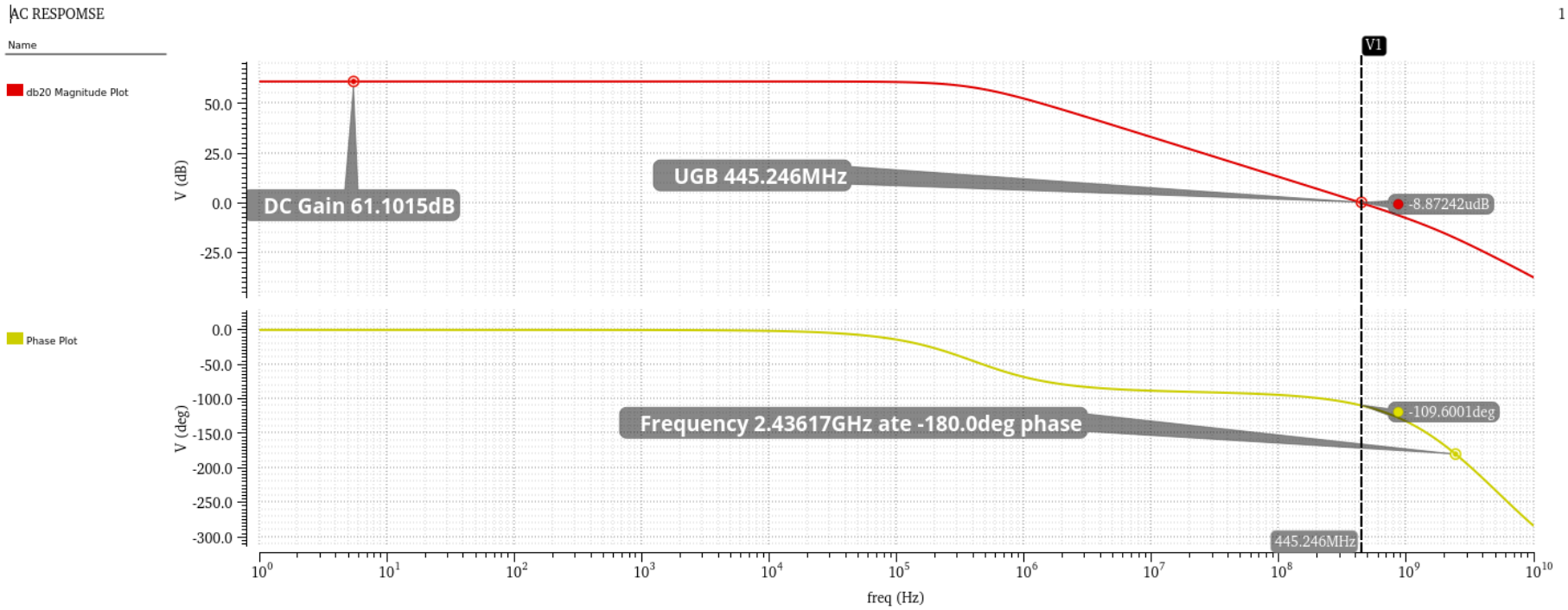
Simulation and Results

- On Resistance of the Switch
- $R_{on} \ll \frac{1}{C.N.f_{sample} 2 \ln 2}$; C = 300f ∴ R ≪ 4.5kΩ



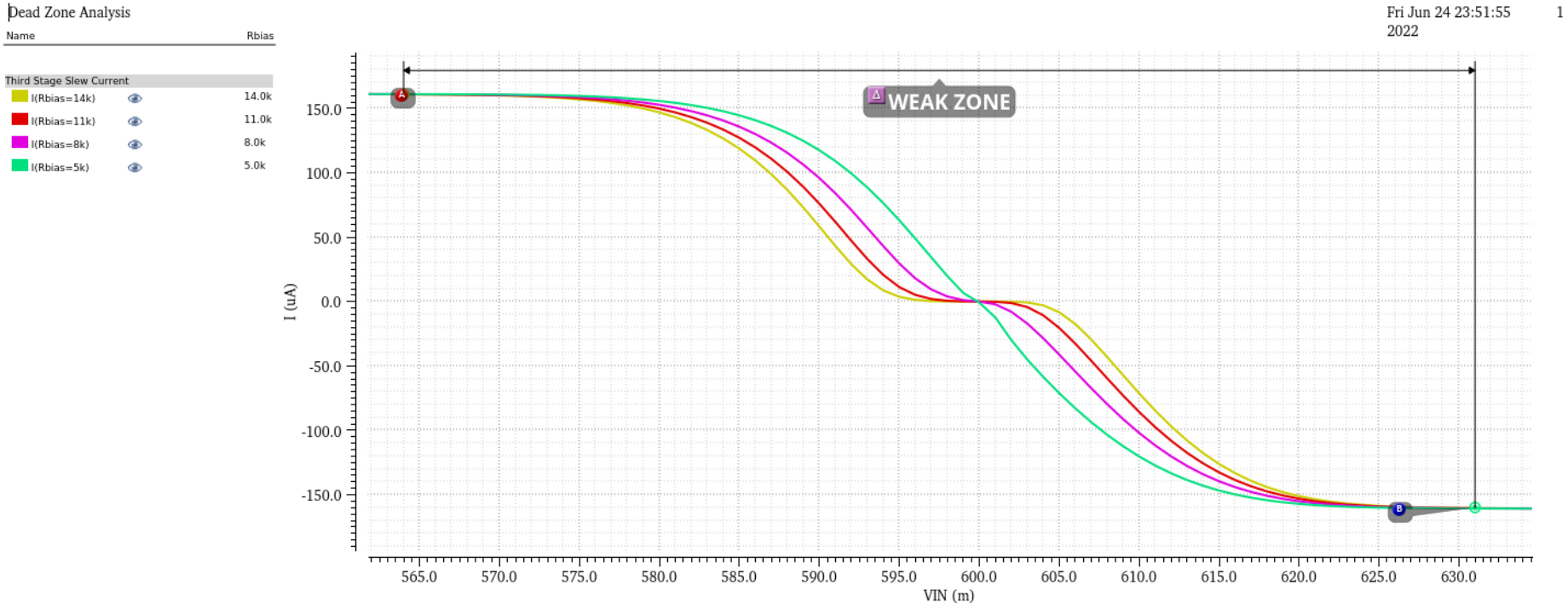
Simulation and Results

- Open Loop Gain of the Ring Amplifier



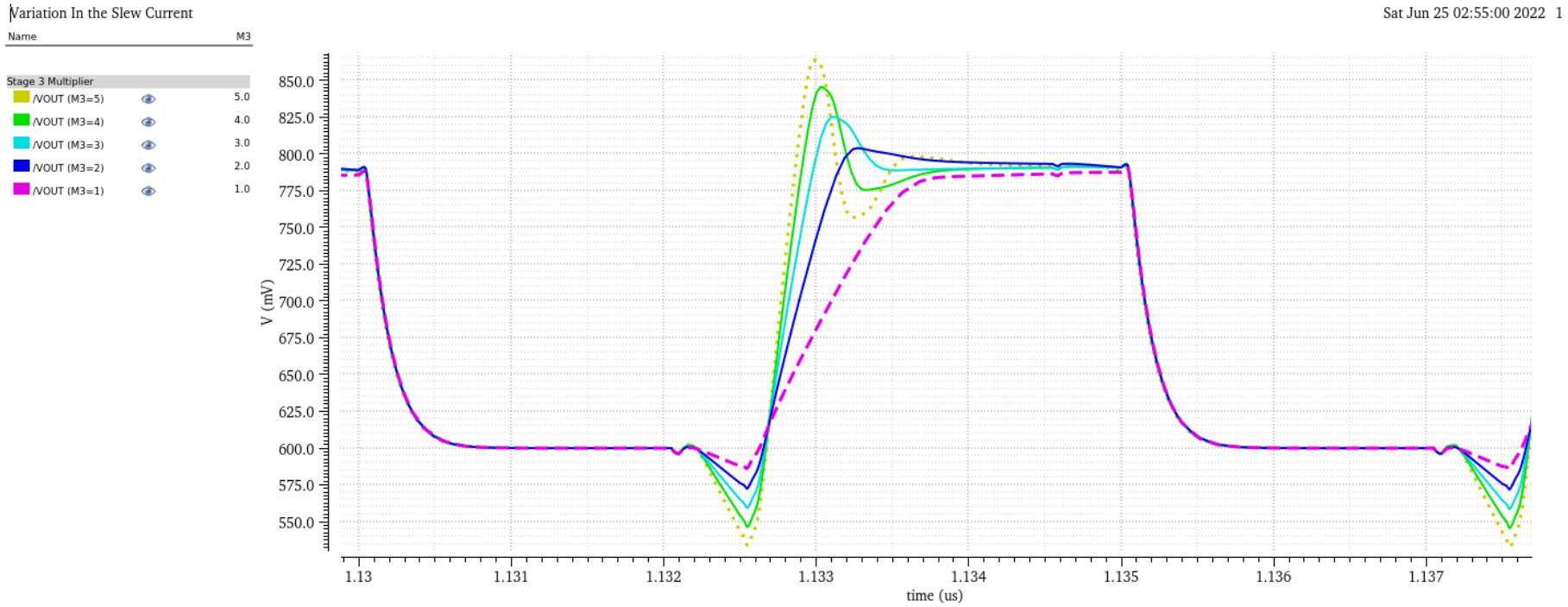
Simulation and Results

- Variation in Dead Zone due to R_{bias} in the Ring Amplifier
  - $R_{bias} = 5k, 8k, 11k, 14k$
  - $V_{DZ} = V_{BP} - V_{BN} = I \times R_{bias}$



Simulations and Results

- Variation in Transient Behavior due to Slew Current
  - $SR = \frac{I_{I3}}{C_L} = \frac{\mu C_{ox} W_3 (V_{GS} - V_{th})^2}{2 C_L L_3}$
  - Variation in Width of output inverter: W, 2W, 3W, 4W, 5W
  - For W = 80μA



Simulations and Results

- Variation in Transient Behavior due to R_{bias}
  - $V_{overshoot} = I_{I3}.\frac{T_{delay}}{C_{load}}$
  - Variation in R_{bias}: 5k, 8k, 11k, 14k