



Digital-to-Analog Converter Design

EE719 Course Project

IIT Bombay

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Problem Statement:

Design an 8-bit Binary Current Steering DAC to meet the specification listed in Table 1. The block level architecture of the DAC is shown in Fig. 1.

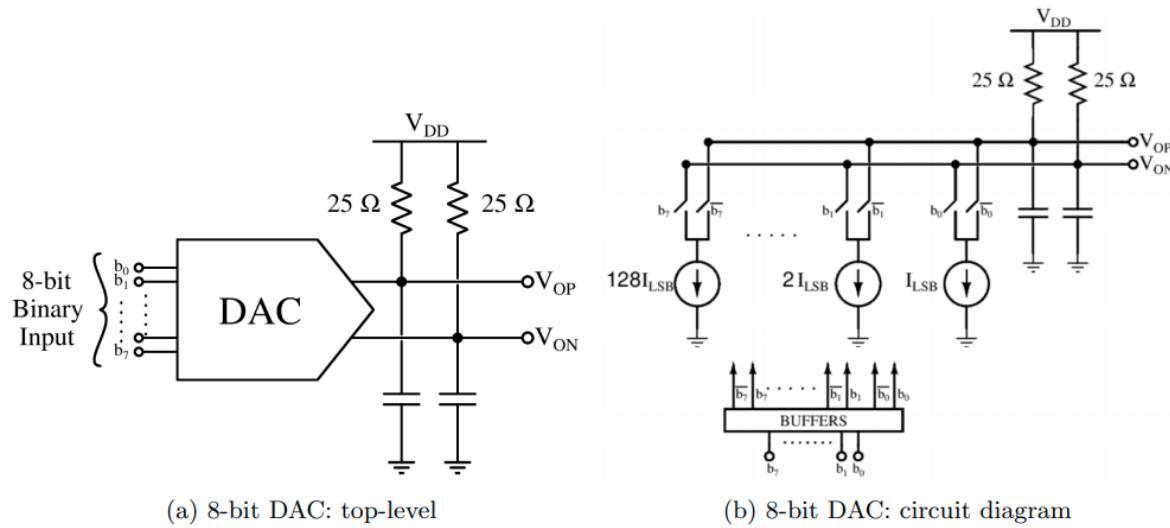


Figure 1: Overview of DAC Architecture

Parameter	Value
Number of bits	8
Analog Supply Voltage (V_{DD})	1.2 / 1.8V
Digital Supply Voltage (V_{DD})	1.2V
Output Voltage Swing (Differential Peak-Peak), V_{FS}	>0.8V
INL	< 0.5LSB
DNL	< 1LSB
SFDR (Nyquist Bandwidth)	>50dB
Sampling Frequency	1GSps

Table 1: 8-bit DAC Specification

References

1. [DAC Design](#): B. Razavi, "The Current-Steering DAC [A Circuit for All Seasons]"
2. [Buffer Design](#): Ivan. E Sutherland, "Logical Effort: Design for speed on the back of an envelope"
3. [Cascode Design](#): EE204 Lecture 24

PART 1

Design of unit cell of the 8-bit Binary DAC

Part (a). Write the detailed design procedure for a unit cell of an 8-bit Binary DAC as shown in Fig. 2. Use these values for your hand calculations: $\mu_n C_{ox} = 210 \mu\text{A}/\text{V}^2$ and $\mu_p C_{ox} = 140 \mu\text{A}/\text{V}^2$, $A_\beta = 2\% \mu\text{m}$, $A_{V_{TH}} = 2.3\text{mV. } \mu\text{m}$. If you choose to use $V_{DD} = 1.8\text{V}$, state your reasons.

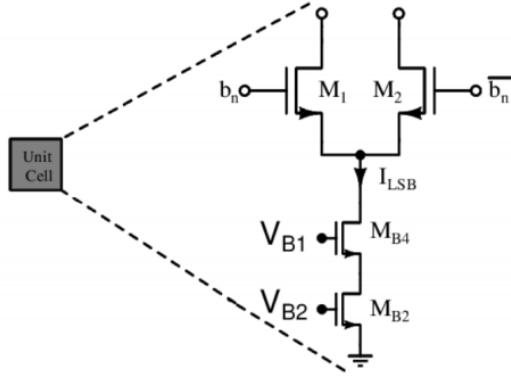


Figure 2: DAC unit cell

Design Procedure:

$$\text{Step 1} \quad \text{INL}_{\max} = \frac{\sigma_I}{2I_u} \sqrt{2^N} \text{ LSB}$$

Number of bits (N) := 8

$$\text{INL} < 0.5 \text{ LSB} \quad 4 \cdot \text{INL}_{\max} = 0.5 \text{ LSB}$$

$$\therefore \frac{\sigma_I}{2I_u} \sqrt{2^N} = 0.5 \rightarrow \frac{\sigma_I}{I_u} = \frac{1}{16}$$

$$\text{Step 2} \quad \left(\frac{\sigma_I}{I_u}\right)^2 = \left(\frac{(2\sigma_{V_{TH}})}{V_{GS} - V_{TH}}\right)^2 + \left(\frac{A_\beta}{\sqrt{WL}}\right)^2 \quad \text{and} \quad \sigma_{V_{TH}} = \frac{A_{V_{TH}}}{\sqrt{WL}}$$

Given $A_{V_{TH}} = 2.3\text{mV. } \mu\text{m}$ and $A_\beta = 0.02\mu\text{m}$

$$\left(\frac{1}{16}\right)^2 = \frac{\left(\frac{(2 \times 2.3 \times 10^{-9}\text{V.m})^2}{(V_{GS} - V_{TH})^2} + (0.02 \times 10^{-6}\text{m})^2\right)}{WL}$$

$$WL = 256 \times \left(\frac{(2.116 \times 10^{-17}\text{V}^2\text{m}^2)}{(V_{GS} - V_{TH})^2} + (4 \times 10^{-16}\text{m}^2) \right) \dots (1)$$

$$\text{Step 3} \quad V_{FS} = V_{OP} - V_{ON} = 1.02\text{V}$$

$$V_{OP(\max)} = 0.51\text{V}$$

$$I_{out(\max)} \times R_L = 0.51\text{V} \text{ when } D = 255 \therefore I_{out} = 255 \times I_u$$

$$\therefore I_u = I_{LSB} = \frac{0.51}{255 \times 25} = 80 \times 10^{-6} A$$

Step 4 If $INL_{max} = \frac{2^N R_L}{4r_o} > 0.5$ LSB then cascode device atop. In our design given, cascoding therefore assuming equal $\therefore \frac{2^N R_L}{4r_o} = 0.5 \times I_{LSB}$

$$\therefore r_o = \frac{256 \times 25}{4 \times 0.5 \times 80 \times 10^{-6}} = 40 \times 10^6 \Omega$$

Step 5 $I_{LSB} = \frac{\mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_{TH})^2}{2} \rightarrow \therefore I_{LSB} \times \frac{2}{\mu_n \times C_{ox}} = \left(\frac{W}{L}\right) (V_{GS} - V_{TH})^2$
 $\therefore \frac{80 \times 10^{-6} \times 2 A}{210 \times \frac{10^{-6} A}{V^2}} = \left(\frac{W}{L}\right) (V_{GS} - V_{TH})^2 \rightarrow \therefore 0.76190 = \left(\frac{W}{L}\right) \times (V_{GS} - V_{TH})^2$

Assume for M_{B2} and M_{B4} $(V_{GS} - V_{TH}) = 0.231V$

$$\therefore \left(\frac{W}{L}\right)_{M_{B2}, M_{B4}} = \frac{0.76190}{0.231^2} = 14.278$$

From equation (1) $\therefore WL = 256 \times \left(\frac{(2.116 \times 10^{-17} V^2 m^2)}{(0.231)^2} + (4 \times 10^{-16} m^2) \right)$

$$WL = 2.0391 \times 10^{-13} m^2 \rightarrow \therefore 14.278 \times L^2 = 2.0391 \times 10^{-13} m^2$$

$$L = \sqrt{2.0391 \times \frac{10^{-13}}{14.278}} = 1.1950 \times 10^{-7} m$$

$$\therefore W = 2.0391 \times \frac{10^{-13} m^2}{1.1950} \times 10^{-7} m$$

Assume $W = 1.7063 \times 10^{-6} m \approx 1.715 \mu m$ and $L \approx 120nm$.

Step 6 for M_1 and $M_2 := V_{GS} - V_{TH} = 0.1V$ and $I_u = I_{LSB} = 80 \times 10^{-6} A$

$$I_{LSB} = \frac{\mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_{TH})^2}{2} \rightarrow \therefore 160 \times \frac{10^{-6}}{210 \times 10^{-6} \times 0.1^2} = \left(\frac{W}{L}\right)_{1,2}$$

$$\therefore \left(\frac{W}{L}\right)_{1,2} = 76.19$$

Assume $L = 90 nm$ (for even number of buffers in logical effort)
 $W = 6857.1 nm \approx 6.857 \mu m$

Parameters	M_{B2}	M_{B4}	M_1	M_2	$V_{FS} (V_{op} - V_{on})$	I_{LSB}
Width	$1.715 \mu m$	$1.715 \mu m$	$6.857 \mu m$	$6.857 \mu m$	$1.02V$	$80 \mu A$
Length	$120nm$	$120nm$	$90nm$	$90nm$	-	-

Table 2: Parameter Values

Part (b). Design the cascode current source biasing for the unit cell as shown in Fig. 3 and tabulate the mentioned parameters.

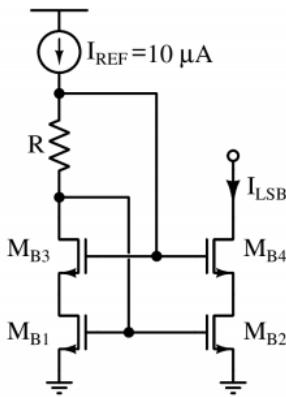


Figure 3: Cascode current source bias

$$V_{DS_{B1}} = V_{DS_{B2}} = V_{DSAT} = 0.231V$$

$$V_{G3,4} = V_{GS3} + V_{DSAT} = V_T + 2V_{DSAT} = V_T + 0.462V$$

$$V_{o,min} = V_{DSAT4} + V_{DSAT2} = 0.462V \quad 4. I_{REF} \times R = V_{G3,4} - V_{GS1}$$

$$\therefore I_{REF} \times R = V_{DSAT1-4} \quad \therefore R = \frac{0.231}{10 \times 10^{-6}} = 23.100k\Omega$$

Current through M_{B1} and M_{B3} is $10 \mu A$

$$\therefore I_d = \frac{1}{2} \times \mu_n C_{ox} \times \left(\frac{W}{L}\right) \times (V_{GS} - V_{TH})^2 \rightarrow \therefore \frac{20\mu A}{210\mu A/V^2} = \left(\frac{W}{L}\right) \times (V_{GS} - V_{TH})^2$$

$$0.09524V^2 = \left(\frac{W}{L}\right) \times (V_{GS} - V_{TH})^2 \rightarrow \therefore \left(\frac{W}{L}\right) = \frac{0.09524}{0.231^2} = 1.78$$

$$W_{B3} \approx 120nm; L_{B3} \approx 65nm$$

$$W_{B4} \approx 120nm; L_{B4} \approx 65 nm$$

$$R = 23.100 k\Omega$$

Part (c). The binary input has to drive the current switches M_1 and M_2 of the unit DAC cell. Say, the capacitance to be driven is C_u , calculate the required number of stages in the buffer. Use C_{in} of minimum sized inverter from the cadence practice assignment. Also, use a chain of even number of inverters with stage ratio of $e=2.72$

Given 1. Stage ratio (e) = 2.72, 2. Load capacitance = C_u , 3. C_{in} of minimum sized inverter

g = logical effort

$$h = \text{electrical effort} = \frac{C_{out}}{C_{in}} = \frac{C_u}{C_{in}}$$

C_u = Capacitance that loads the logic gate

C_{in} = capacitance presented by logic gate at one of its input

$$d = b \times g \times h + p$$

p and g independent of size of transistors

We are using buffers that is minimum sized inverters logical effort will be '1'.

τ is the delay of an inverter with no parasitic delay that drives another identical inverter.

$$P_{inv} + \rho(1 - \ln \rho) = 0 \therefore \rho = e = 2.718 \text{ is given} \therefore P_{inv} = 0$$

$$\frac{1}{\ln F} = \frac{1}{N} \therefore \ln F = N \rightarrow \ln H = N$$

$$\ln \left(\frac{C_{out}}{C_{in}} \right) = N \rightarrow N = \ln \left(\frac{C_u}{C_{in}} \right)$$

Transistor	W(nm)	L(nm)	C_{gg} when $V_{in} = 1.2V$	C_{gg} when $V_{in} = 0V$
PMOS (min. inverter)	215	45	98.9344E-18 F	210.318 E-18 F
NMOS (min. inverter)	130	45	117.77 E-18 F	50.2701 E-18 F
Total (C_{in})			216.704 E-18F	260.5881 E-18 F
NMOS M1	6855	90	7.9564 E-15 F	3.1486 E-15 F

Table 3: C_{gg} of transistors

$$\therefore N = \ln \left(\frac{C_u}{216.704 \times 10^{-18} F} \right) \text{ when input logical high}$$

$$\therefore N = \ln \left(\frac{C_u}{260.558 \times 10^{-18} F} \right) \text{ when input logical low}$$

From 1st hand calculation-based simulation $C_u = 7.9564\text{fF}$ when high input and $C_u = 3.1486\text{ fF}$ when low input $\therefore N = 3.6031 \approx 4$ and $N = 2.4918 \approx 2$

PART 2

Circuit Implementation of DAC Unit cell on cadence

Fig. 4 shows the DAC unit cell with the digital driving circuitry. Using the calculations in Part 1, implement the circuit as per the following instructions. You may need to re-iterate your design as required to meet the specifications.

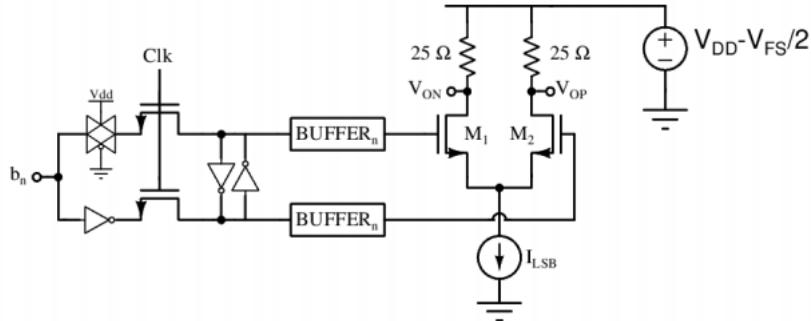


Figure 4: DAC unit cell with resistive load

Part (a). Implement the circuit of the unit cell in Fig. 2 along with the current source biasing circuit. Perform the DC analysis. Report the schematics with component sizing. Report the DC operating points annotated in the schematic (I_d , region) for $b_n = 1$ and $b_n = 0$

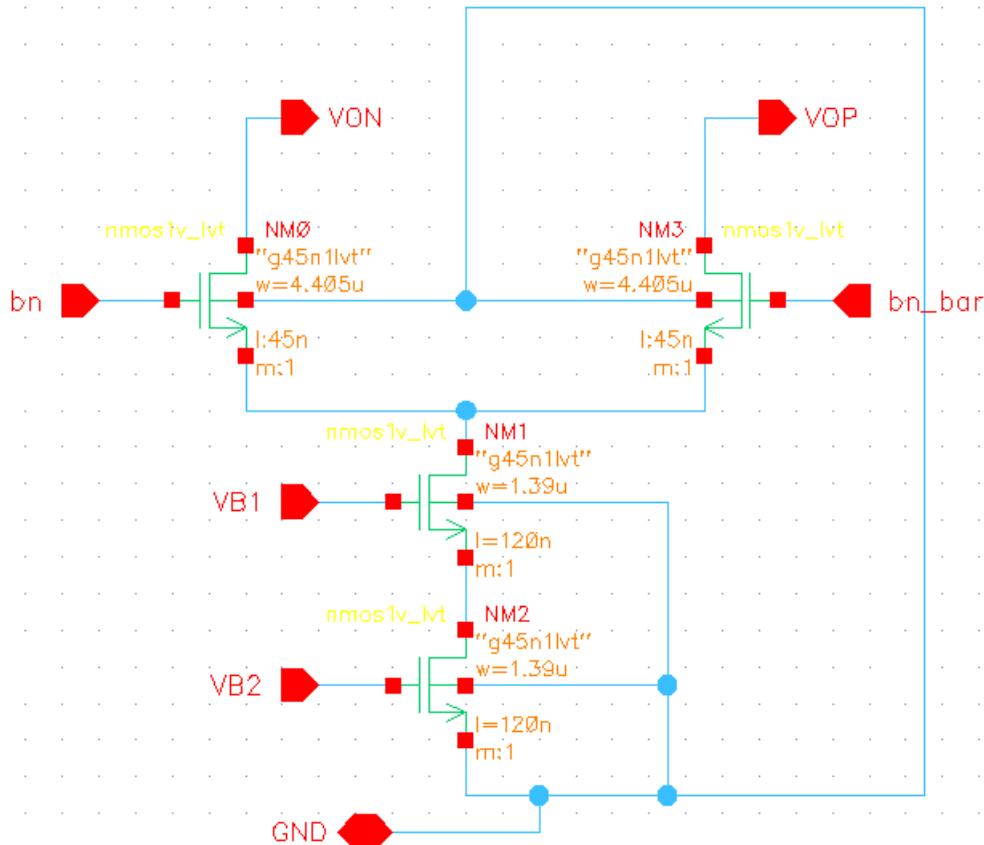


Figure 1: Unit Cell

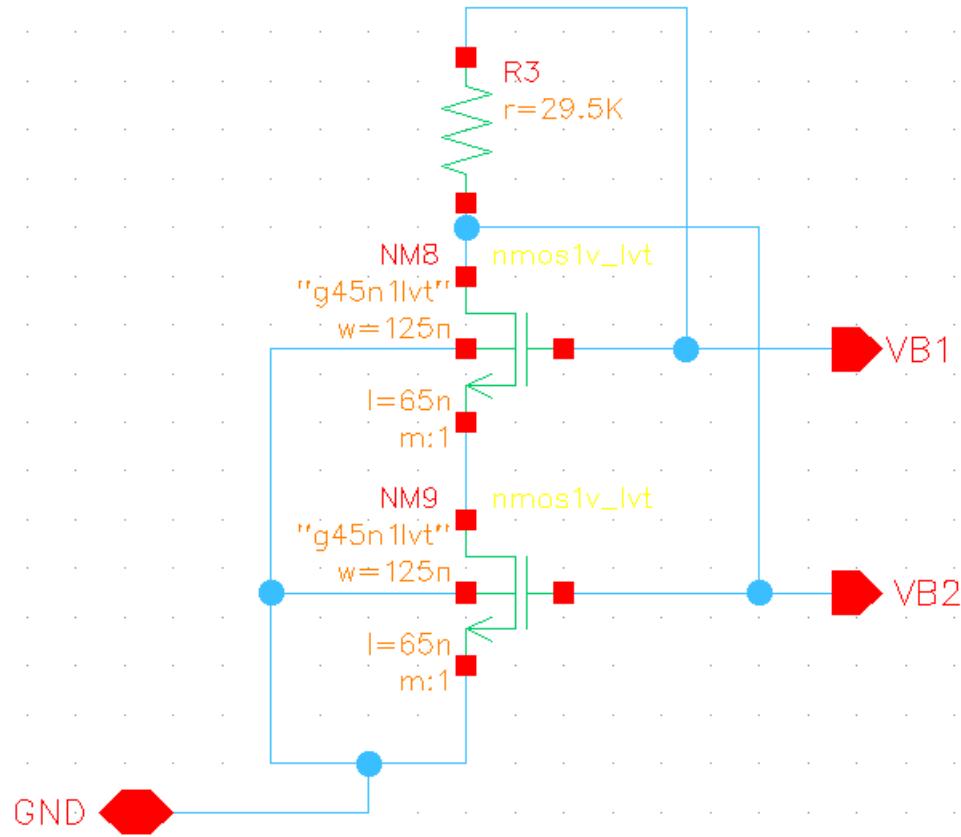


Figure 2: Current Source

Component Sizes:

Operating regions => 0 = cutoff ; 1 = triode ; 2 = saturation ; 3 = subthreshold

Component	Width w (nm)	Length l (nm)	$\frac{W}{l}$	When $b_n = 1$ Biasing condition	When $b_n = 0$ Biasing condition
NM0 => M1	4405	45	97.88	$80.0475\mu A, 2$	$80.72pA, 0$
NM3 => M2	4405	45	97.88	$80.72pA, 0$	$80.0475\mu A, 2$
NM1 => MB2	1390	120	11.58	$80.0475\mu A, 2$	$80.0475\mu A, 2$
NM2 => MB4	1390	120	11.58	$80.0475\mu A, 2$	$80.0475\mu A, 2$
NM4=> MB1	125	65	1.92	$10.25\mu A, 2$	$10.25\mu A, 2$
NM5=> MB3	125	65	1.92	$10.25\mu A, 2$	$10.25\mu A, 2$

Table 4: Buffer Design

Resistor Values: $R = 29.5K\Omega$; $R_L = 25 \Omega$

Supply Voltages: $DV_{DD} = 1.2V$; $AV_{dd} = 1.2V$; $b_n = 1.2V$; (non – ideal) $I_{ref} = 10.25 \mu A$

NOTE:

In the calculation, haven't consider the second order effects. Therefore, Simulation results with calculated parameters not matching. So, width and length of MOSFETs are changed to some extends to get current $80\mu A$ and all the transistors in saturation region

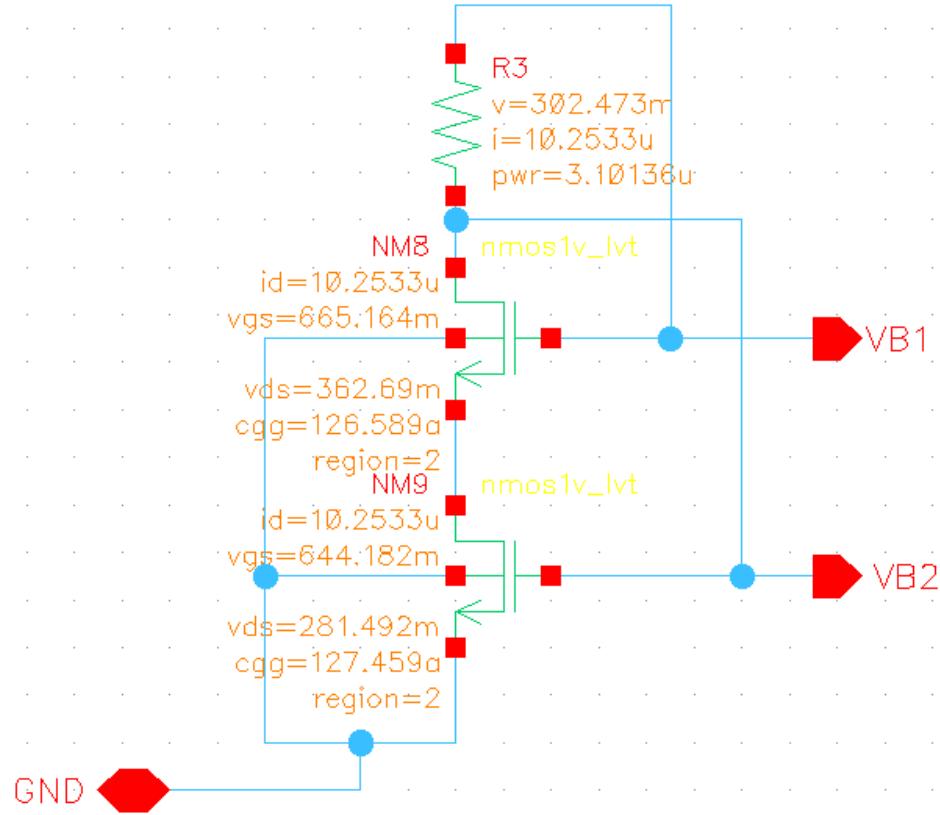
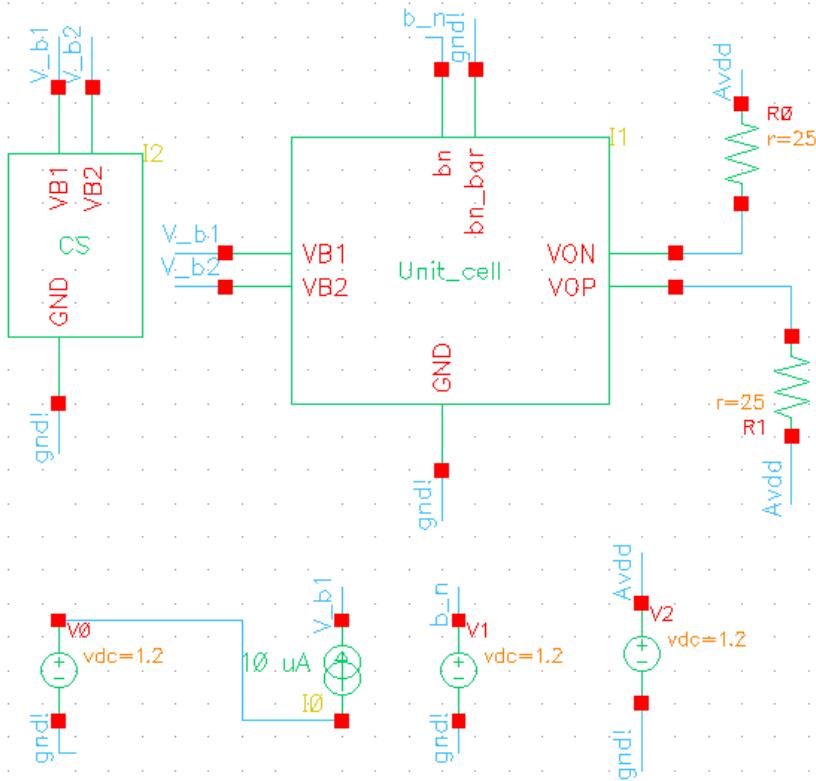


Figure 3: Simulation of Current Source

DC analysis:

When $b_n = 1$ Figure 4: Schematic of unit cell simulation when $b_n = '1'$

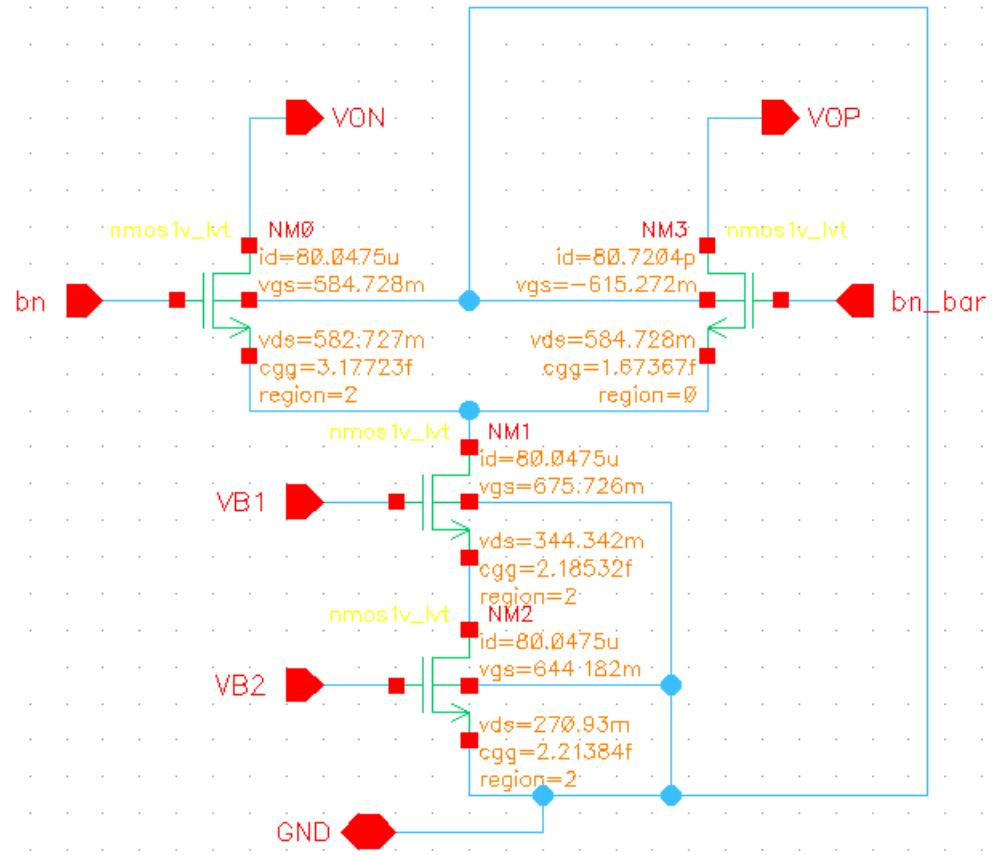


Figure 5: Simulation when $b_n = '1'$

When $b_n = 0$

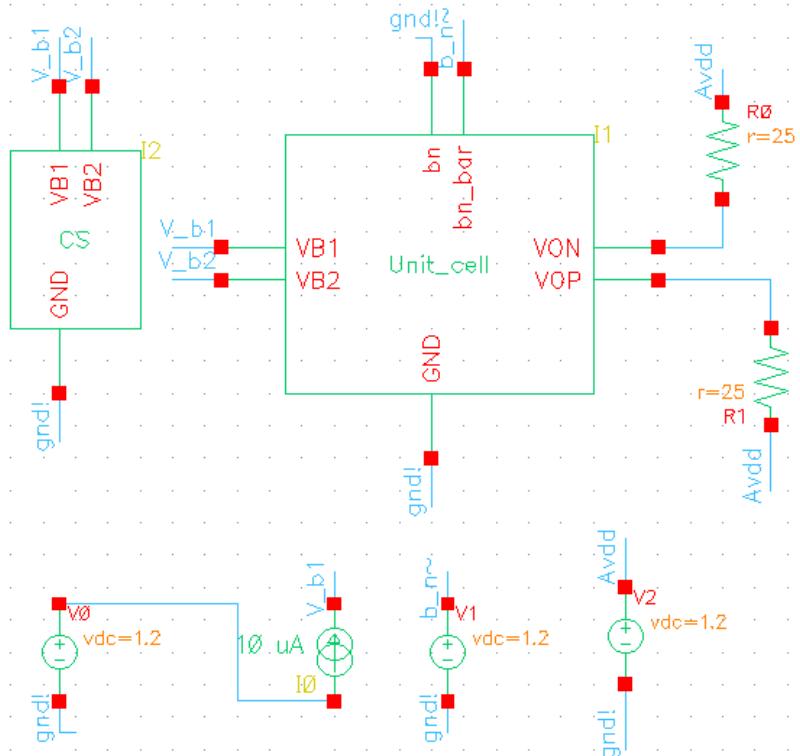


Figure 6: Simulation of schematic when $b_n = '0'$

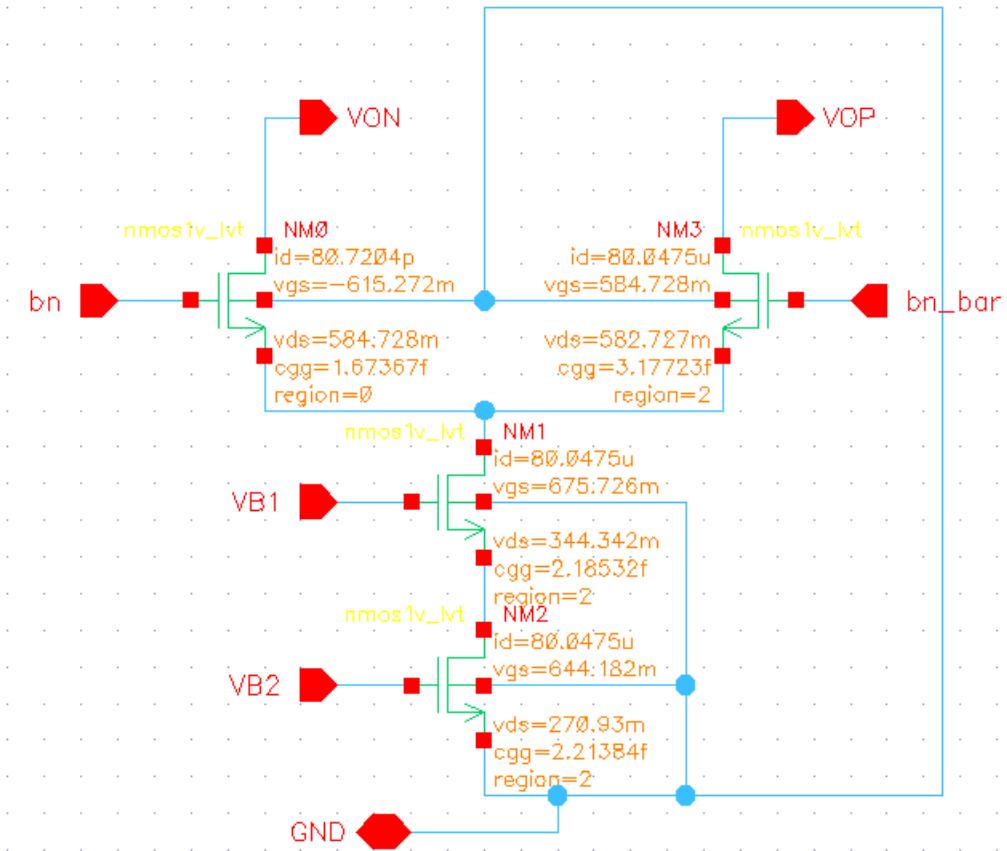


Figure 7: simulation when $b_n = '0'$

Part (b). To equalize delay in driving circuitry, design a pass-transistor as shown in Fig. 5. Adjust size of the transistors to get delay same as your minimum sized inverter. Report the size of the transistors used in the pass-transistor circuit. Plot and annotate the delay of your inverter and the pass-transistor.

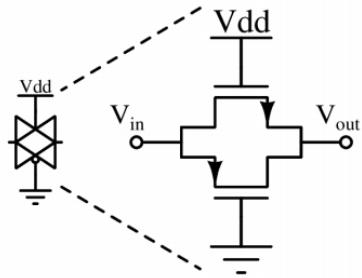


Figure 5: Pass transistor

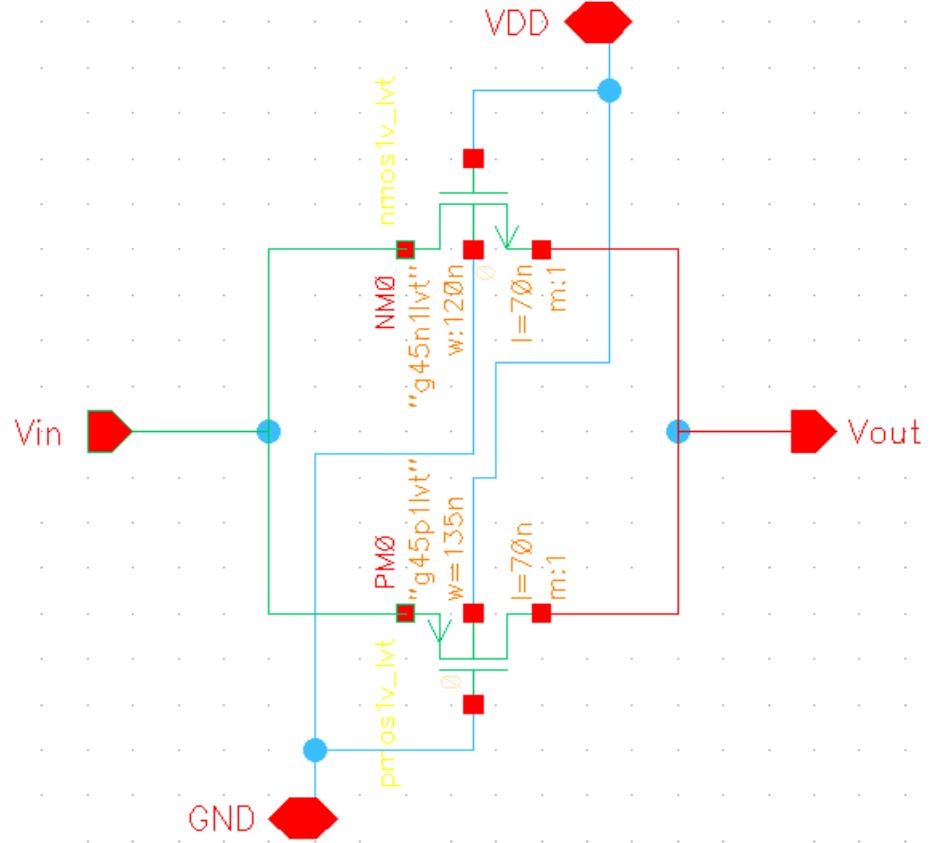


Figure 8: Circuit of Pass-Transistor gate

Size of NMOS and PMOS in transmission gate:

	NMOS	PMOS
W(nm)	120	135
L(nm)	70	70

Table 5: Transmission gate parameter

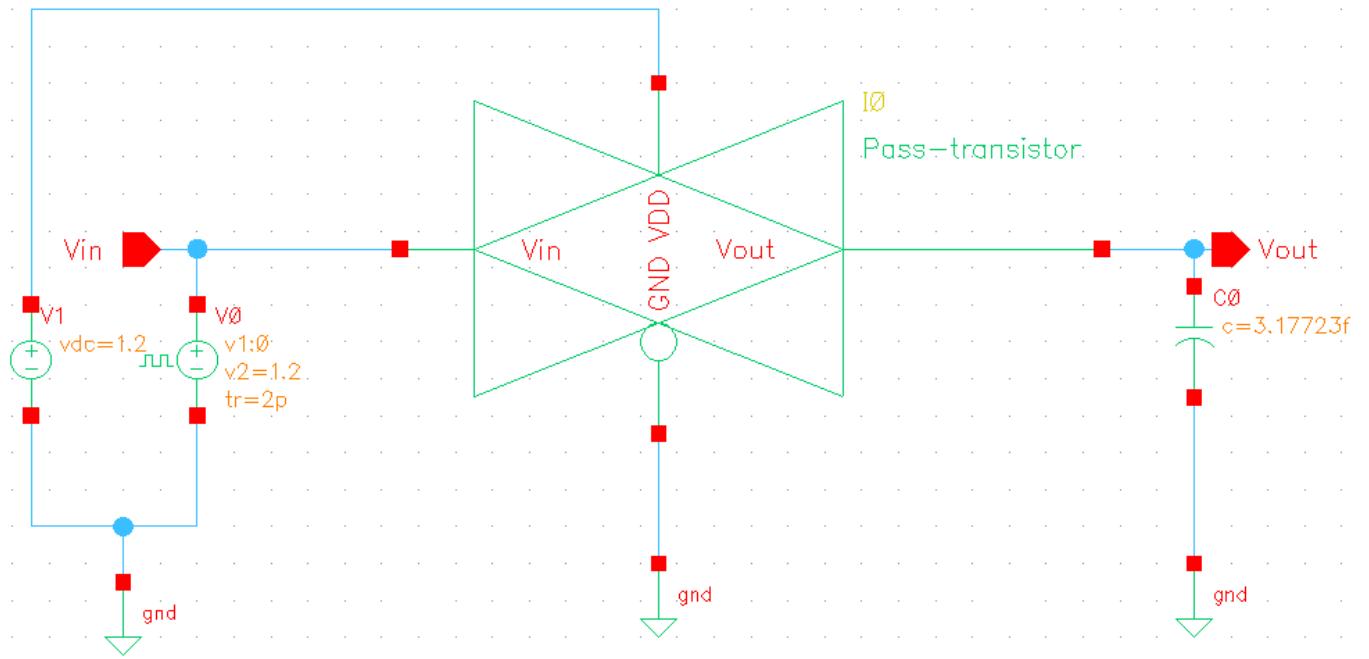


Figure 9: Schematic of Pass-Transistor gate

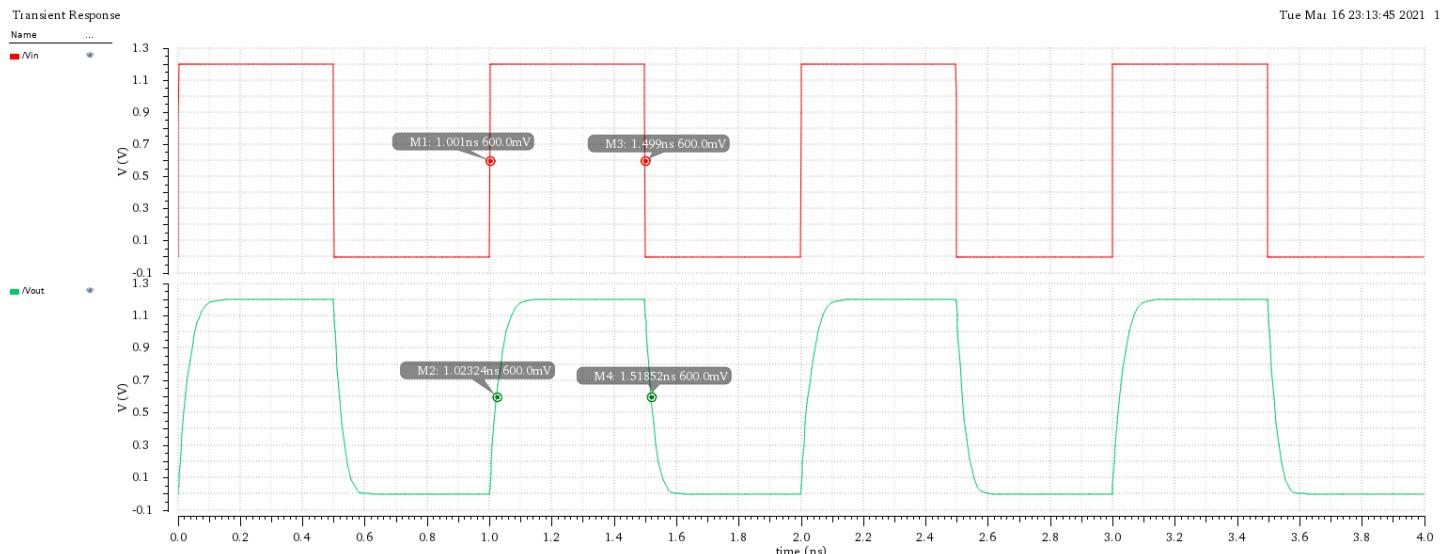


Figure 10: Simulation result for delay determination

Delay from 50% input to 50% output:

$V_{out}(V)$	$t_{out}(\text{ns})$	$V_{in}(V)$	$t_{in}(\text{ns})$	Rising edge delay
0.6	1.02324	0.6	1.001	0.02224
$V_{out}(V)$	$t_{out}(\text{ns})$	$V_{in}(V)$	$t_{in}(\text{ns})$	Falling edge delay
0.6	1.51852	0.6	1.499	0.01952

Table 6: Delay Timings of Transmission gate

Transmission gate delay is tried to match with minimum inverter. Rising edge is match but falling edge is different value.

Minimum Inverter:

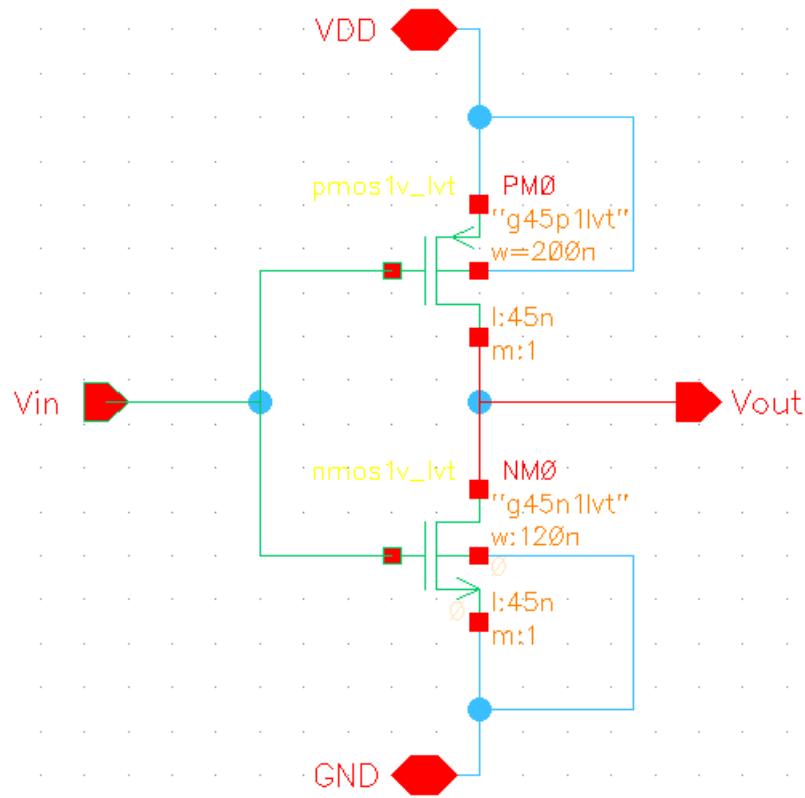


Figure 11: Circuit of Minimum Inverter

Size of PMOS and NMOS in minimum inverter:

	NMOS	PMOS
W(nm)	120	200
L(nm)	45	45

Table 7: Inverter Parameter

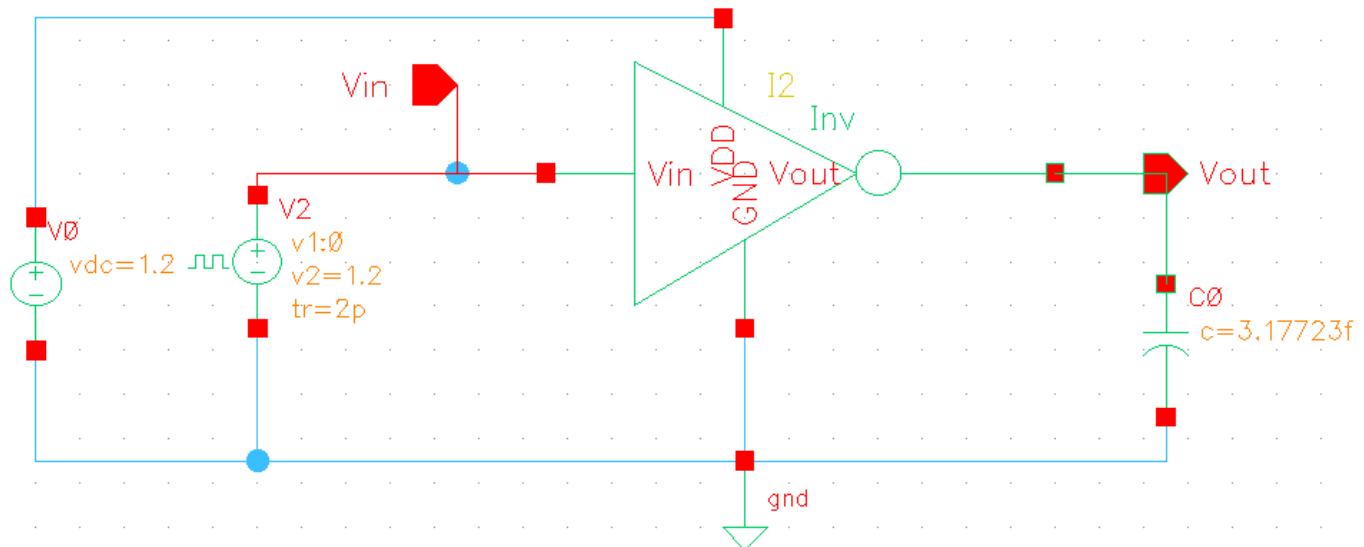


Figure 12: Schematic of minimum inverter simulation

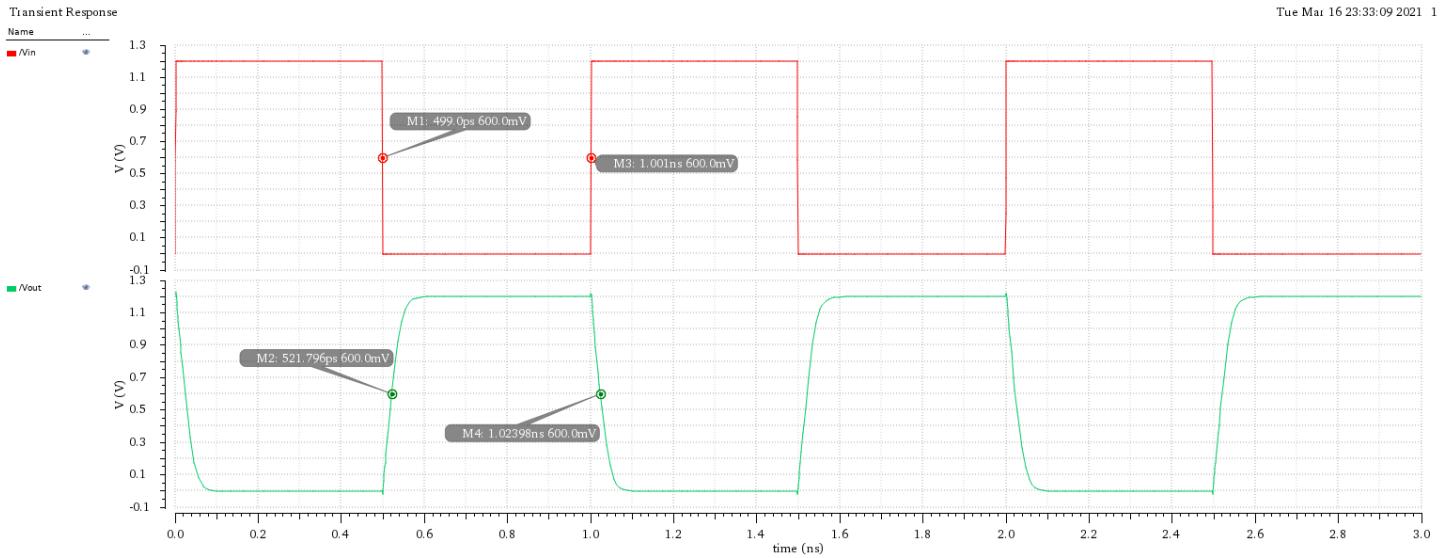


Figure 13: Simulation waveform for Minimum Inverter

Delay from 50% input to 50% output:

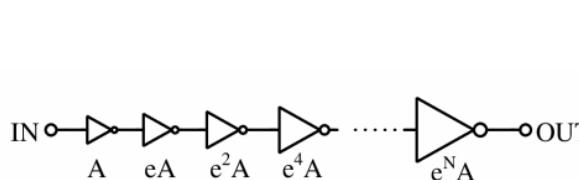
$V_{out}(V)$	$t_{out}(\text{ns})$	$V_{in}(V)$	$t_{in}(\text{ns})$	Rising edge delay
0.6	1.02398	0.6	1.001	0.02298 ns
$V_{out}(V)$	$t_{out}(\text{ns})$	$V_{in}(V)$	$t_{in}(\text{ns})$	Falling edge delay
0.6	0.521796	0.6	0.499	0.02279 ns

Table 8: Delay Timings pf Inverter

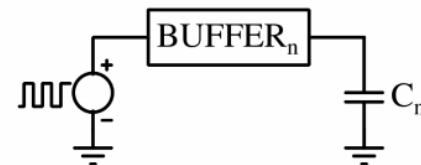
	Minimum Inverter	Pass Transistor gate
Rising edge delay (ps)	22.98	22.24
Falling edge delay (ps)	22.79	19.52

Table 9: Comparison Table of Inverter and Transmission gate

Part (c). Implement the driving buffer for the binary input for the number of stages calculated in Part 1-Part(c) for the line (b_0). Report the sizes of the transistors in the buffer chain.



(a) Digital buffer chain



(b) Buffer test setup

Figure 6: Digital Buffer

From simulation of minimum inverter and unit cell, C_{gg} is determined as follows:

$$C_{gg_inv} = 46.3986 \times 10^{-18} \text{ F} \dots \dots \dots \text{(minimum Inverter)}$$

$$C_{gg_cell} = 3.17723 \times 10^{-15} \text{ F} \dots \dots \dots \text{(Unit Cell)}$$

From Part 1 number of inverters in buffer is $N = \ln\left(\frac{3.17723 \times 10^{-15}}{46.3986 \times 10^{-18}}\right) = 4.2264$

$$\therefore N \approx 4$$

i	W_p (nm)	L_p (nm)	W_n (nm)	L_n (nm)
1	200	45	120	45
2	545	45	325	45
3	1480	45	885	45
4	4025	45	2405	45

Table 10: Buffer Design

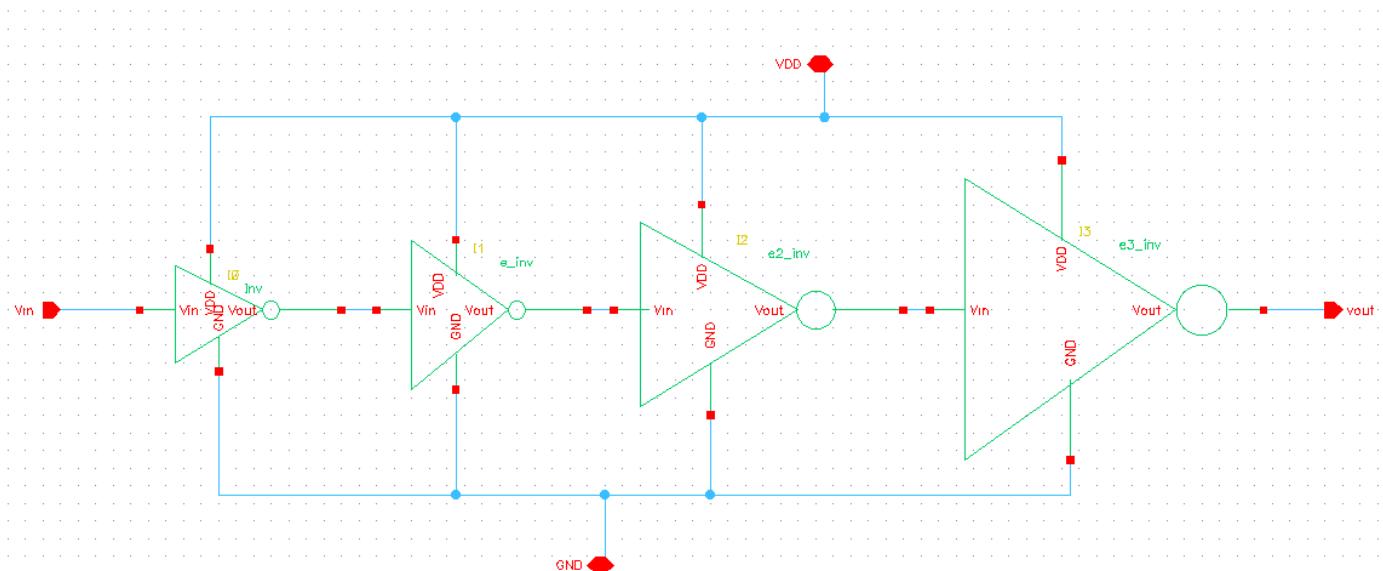


Figure 14: Circuit diagram of Buffer with 4 inverters

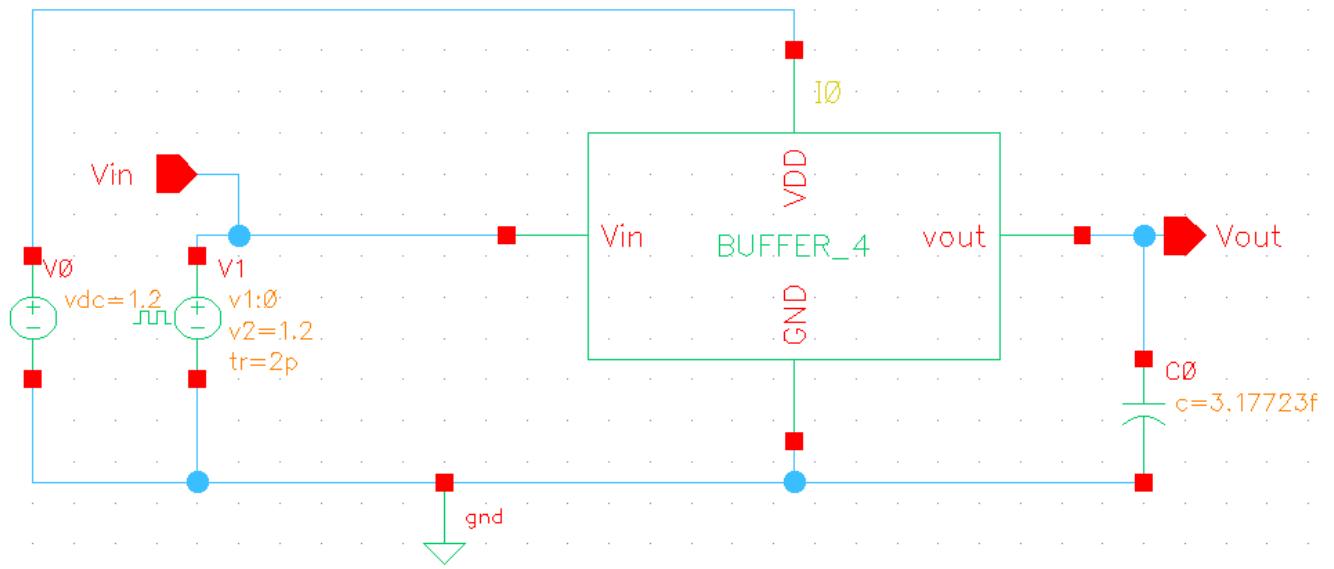


Figure 15: Simulation of Buffer Schematic

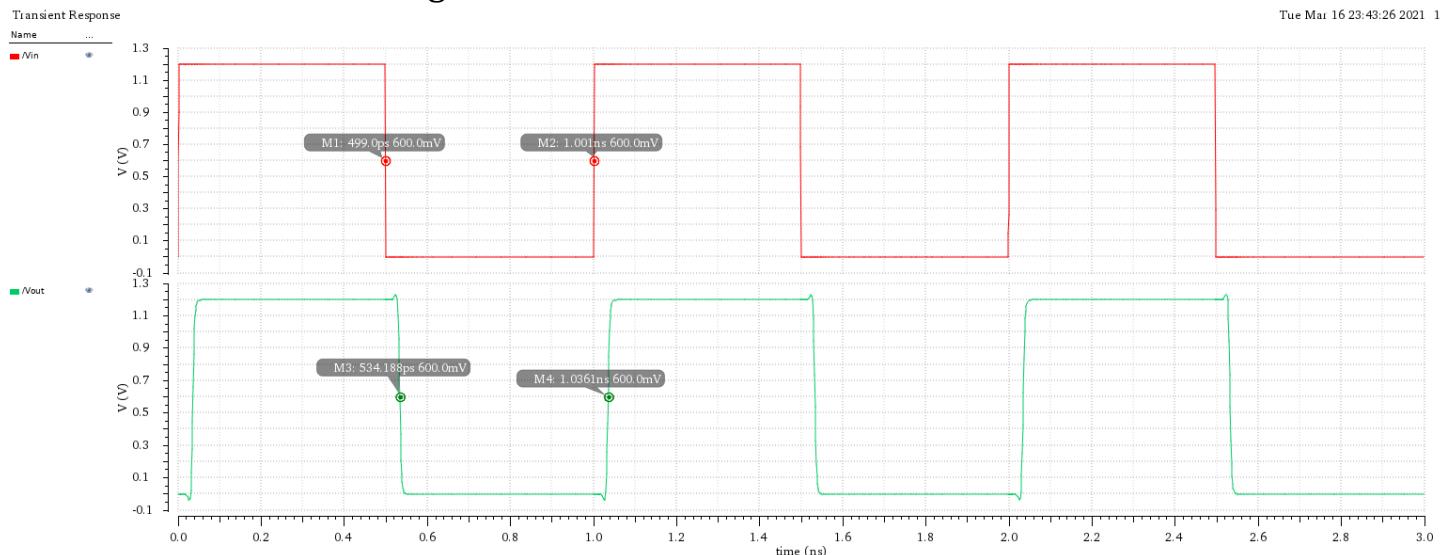


Figure 16: Waveform of Buffer delay

Rising delay (50% input to 50% output of Low to High) = 35.18ps

Falling delay (50% input to 50% output of High to Low) = 35.10ps

Part (d). Implement the circuit and report the schematic in Fig. 4. Perform a transient analysis for $b_n: 0 \rightarrow 1$ and $1 \rightarrow 0$ with a voltage source of value $(V_{DD} - V_{FS}/2)$. Report the plot of region of operation of the current source and current switch transistors. Report the plots of the driving signals and V_{on} and V_{op} . Does the cross-point of the input signals have an impact on the circuit performance? Reason your answer.

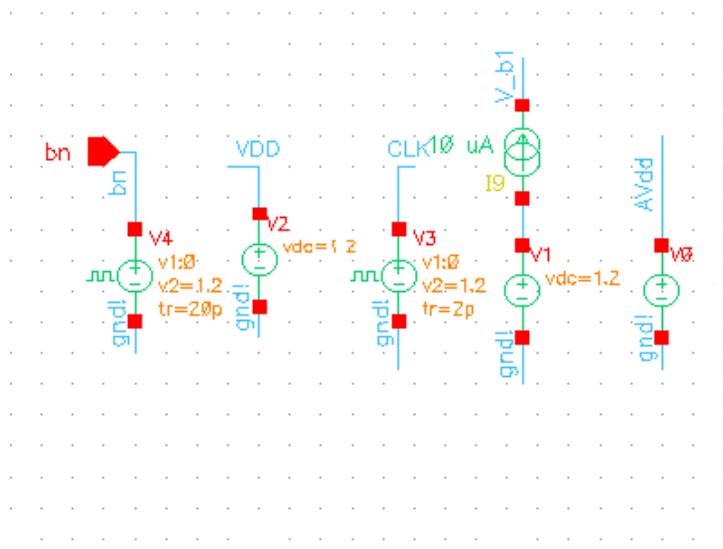


Figure 17: Voltage Source and non-ideal current source

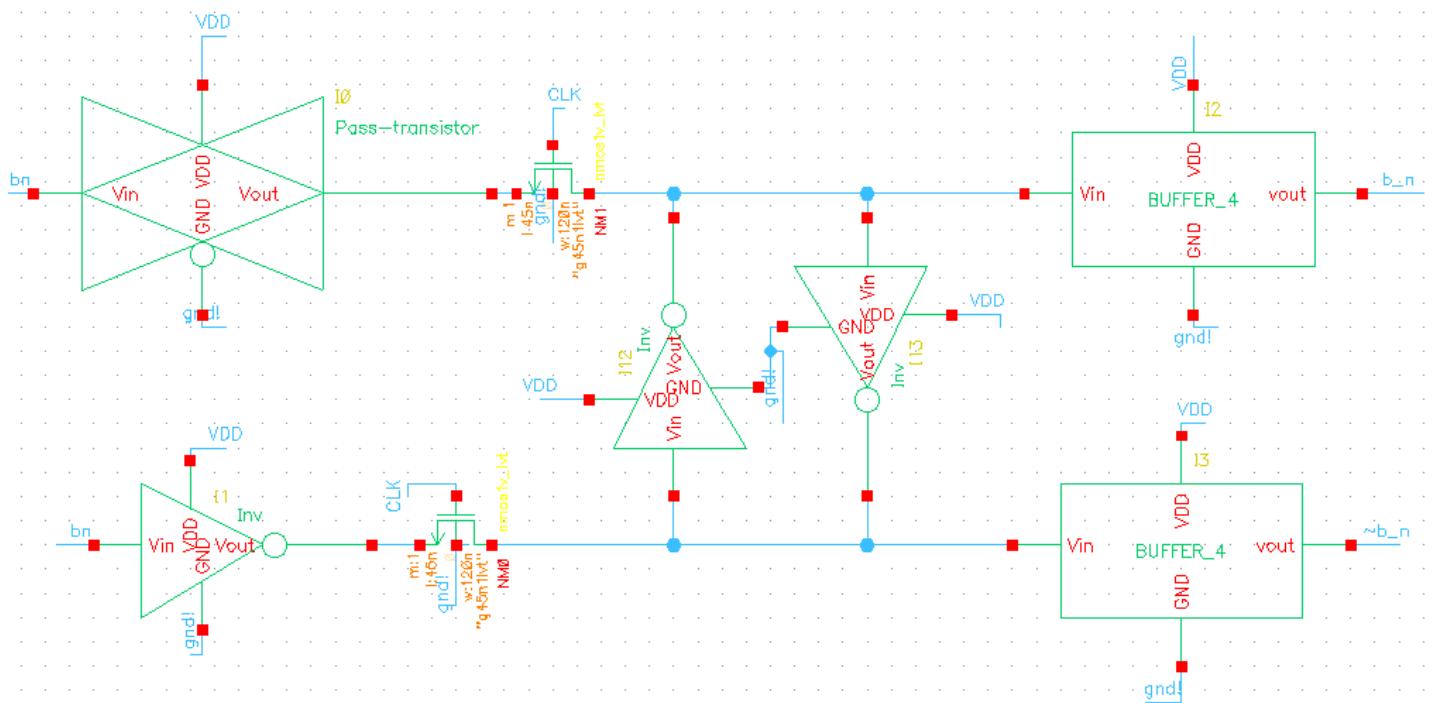


Figure 18: Schematic of derivation of driving signals for switching transistors

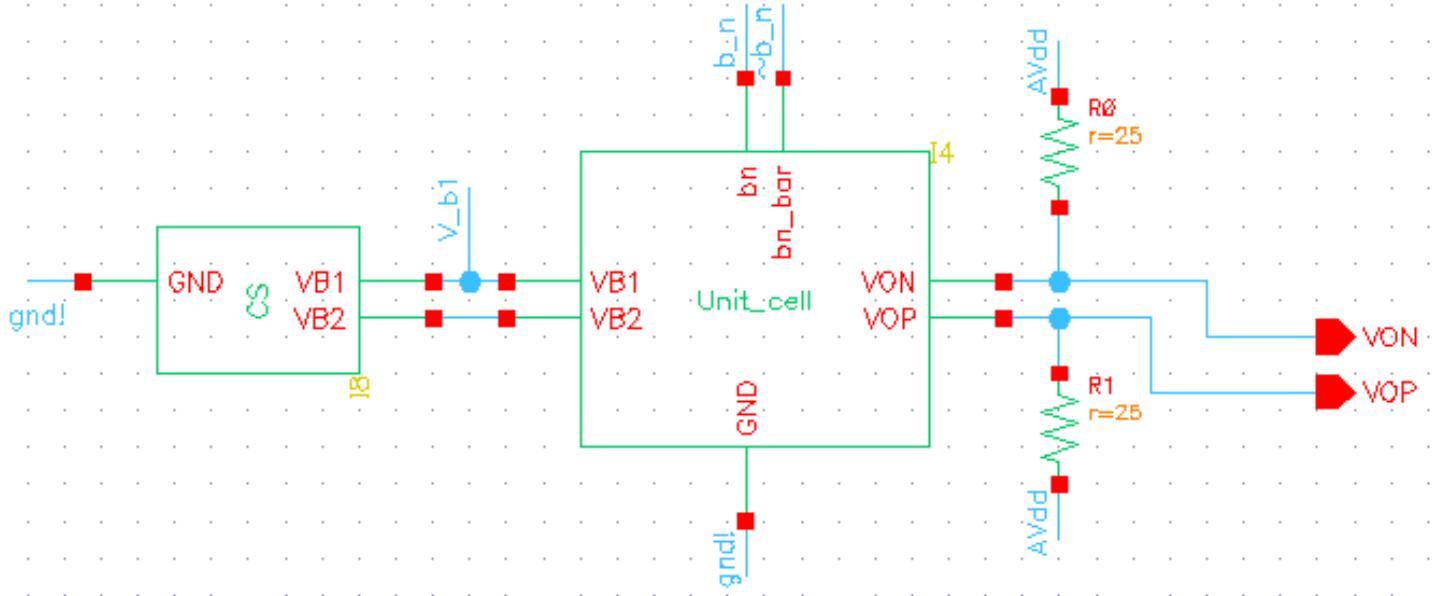


Figure 19: schematic of unit cell driven by switching signals

When the input transient from high to low or low to high. Current source transistor changes its region of operation momentarily to linear. Which makes switching transistor go in subthreshold region. It causes small spikes at output. If the frequency of input increases, we will see this glitch regularly, which will cause error, power dissipation. It may affect INL, DNL of DAC.

Transient analysis of DAC unit cell:

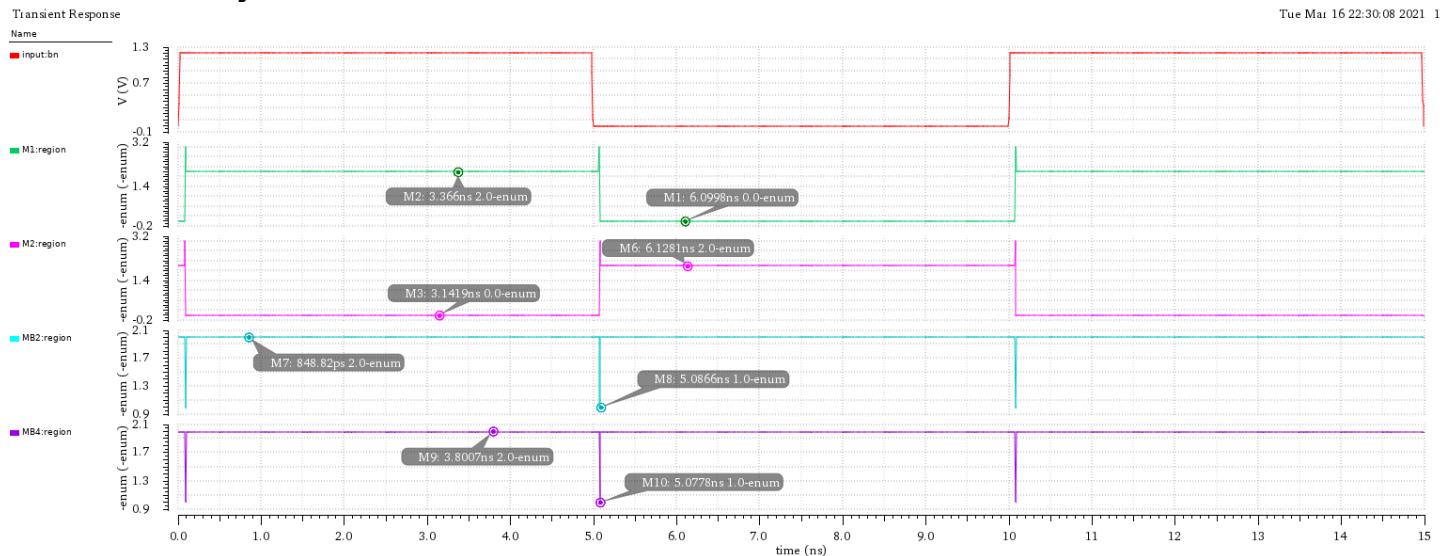


Figure 20: Waveform for region of operation

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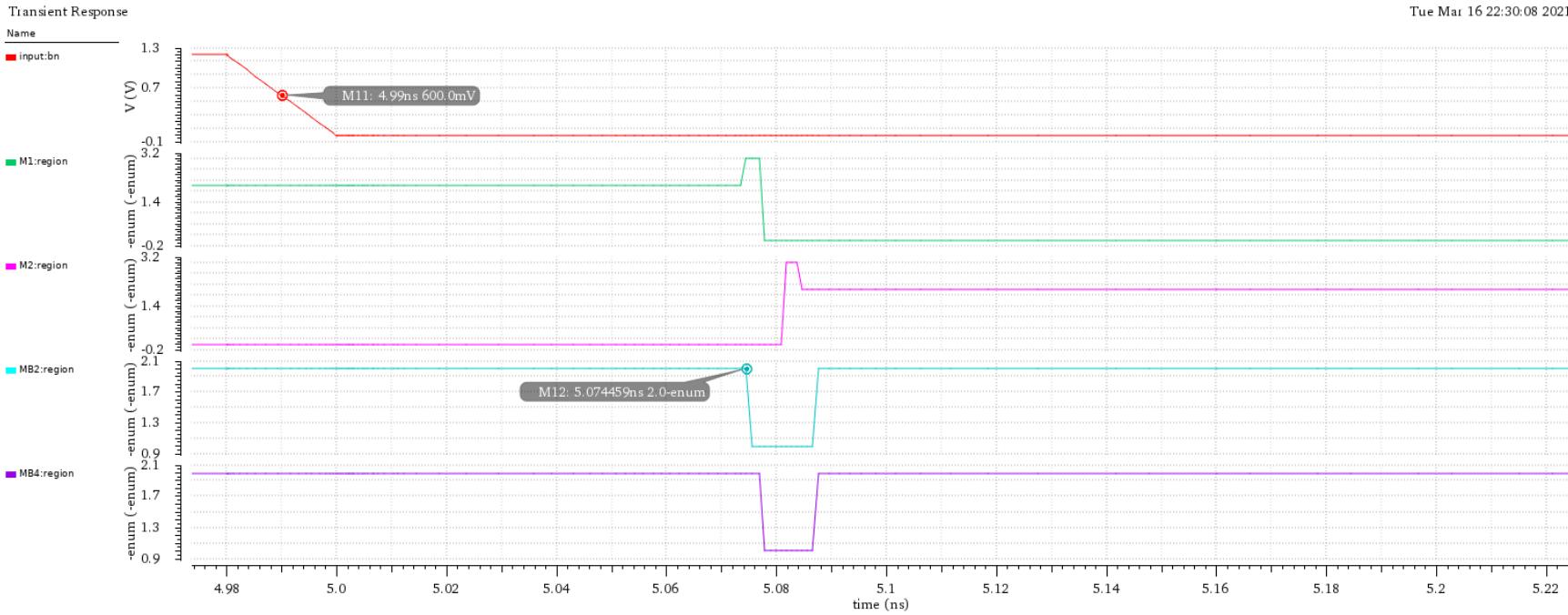


Figure 21: Waveform of falling edge transient

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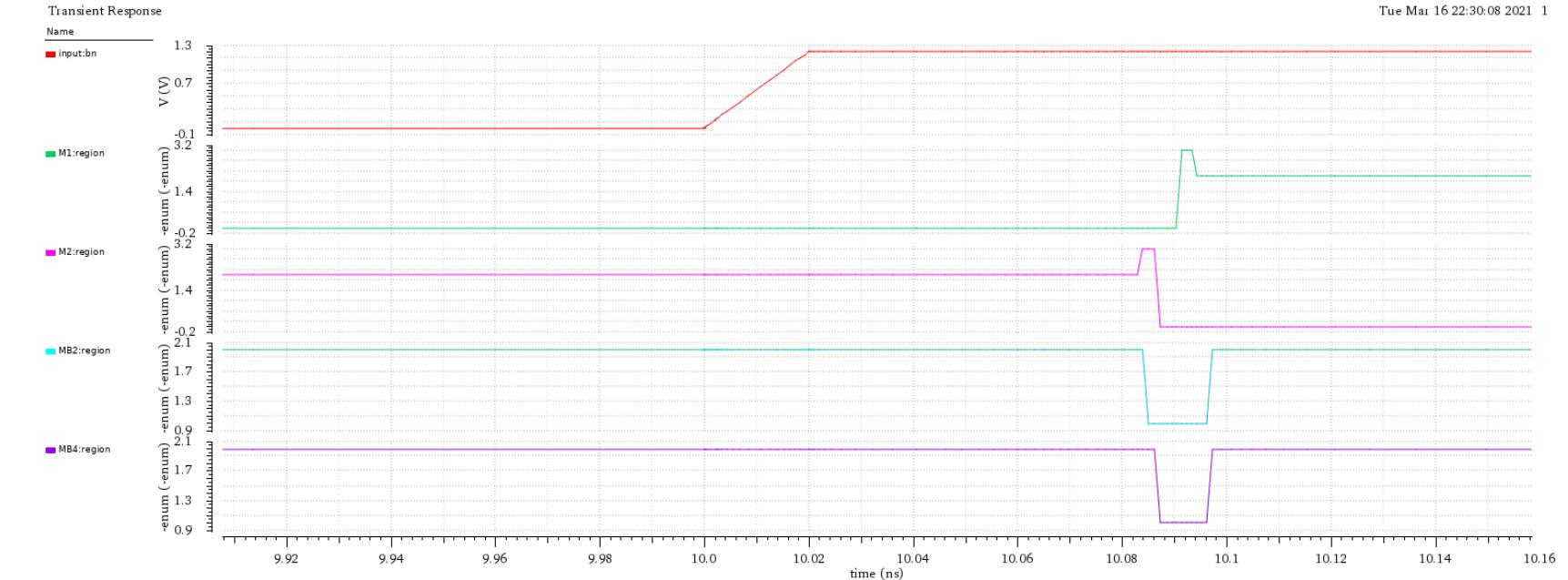


Figure 22: Waveform of rising edge transient

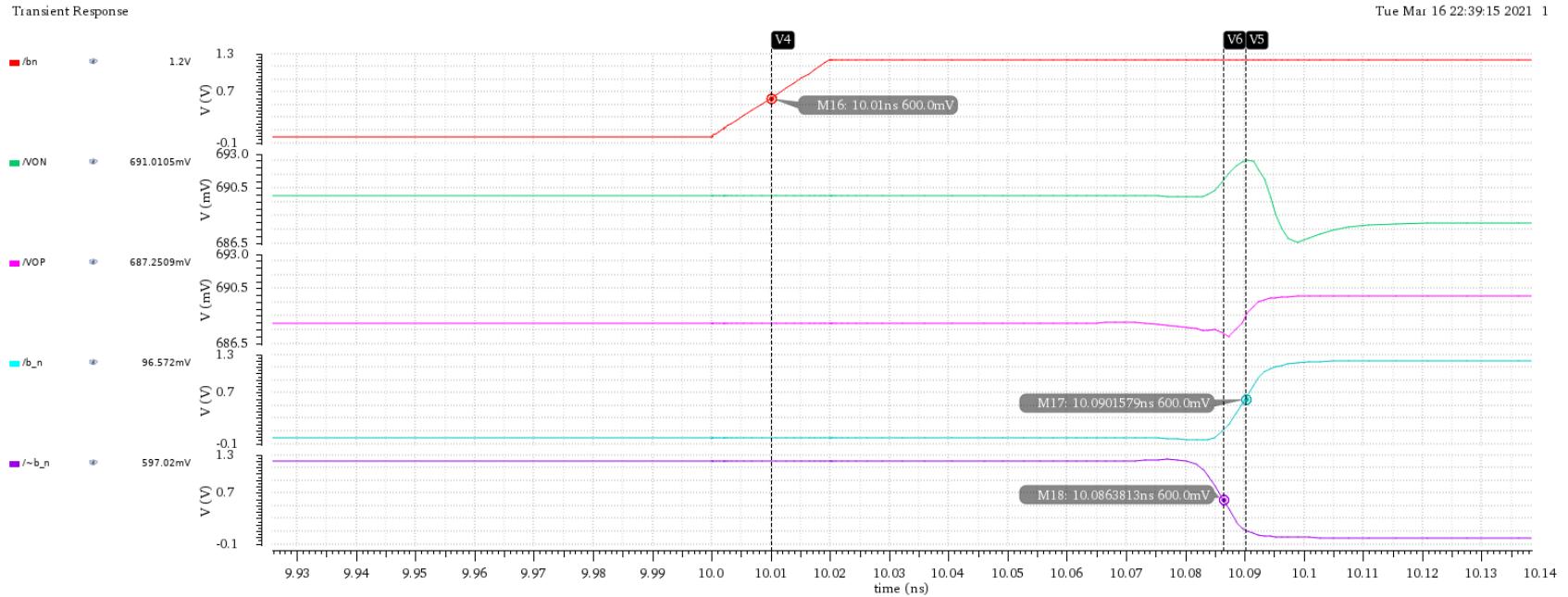


Figure 23: Waveform for Rising edge transient of Output and driving signals

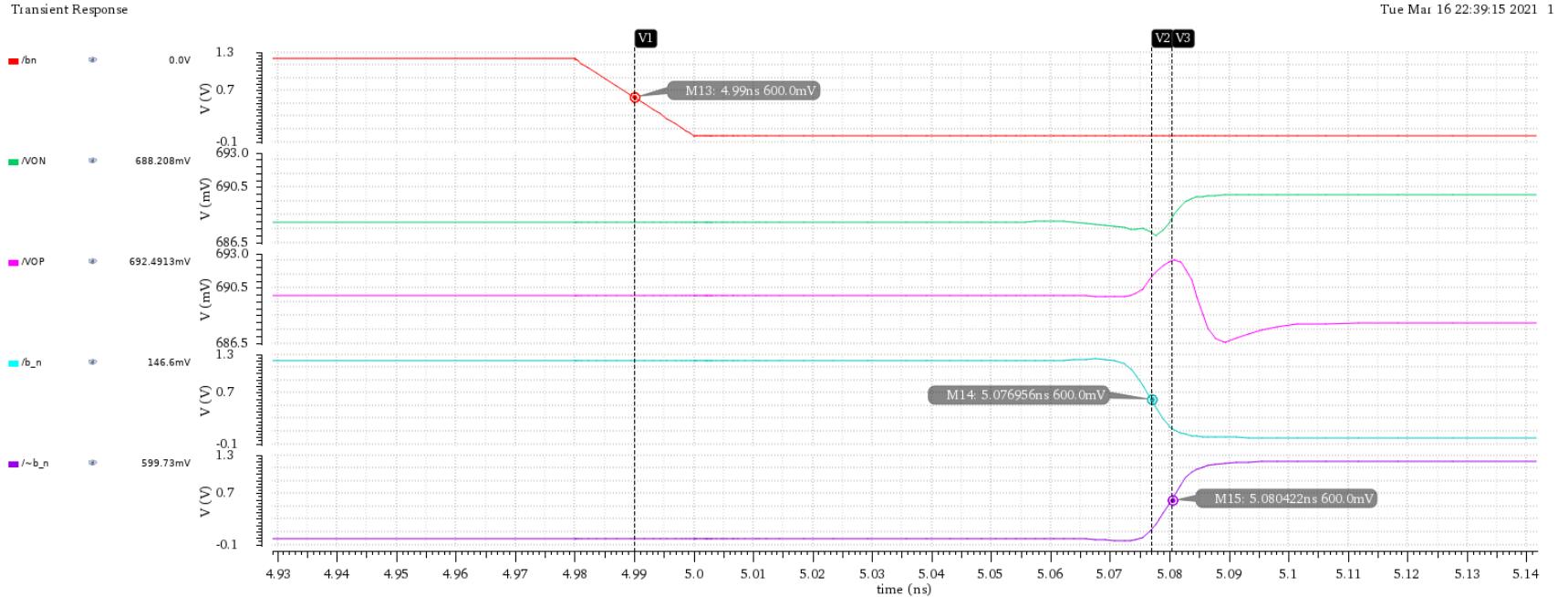


Figure 24: Waveform for Falling edge transient of output and driving signals

PART 3

8-bit DAC Implementation and Characterization

Part (a). Scale the unit element of DAC in Part 2 by 2x to generate current sources until 128 I_{LSB} . Generate the symbol for your DAC. Replace the Device under test (DUT) with your 8-bit CS DAC and setup the test bench shown in Fig. 7

ANS:

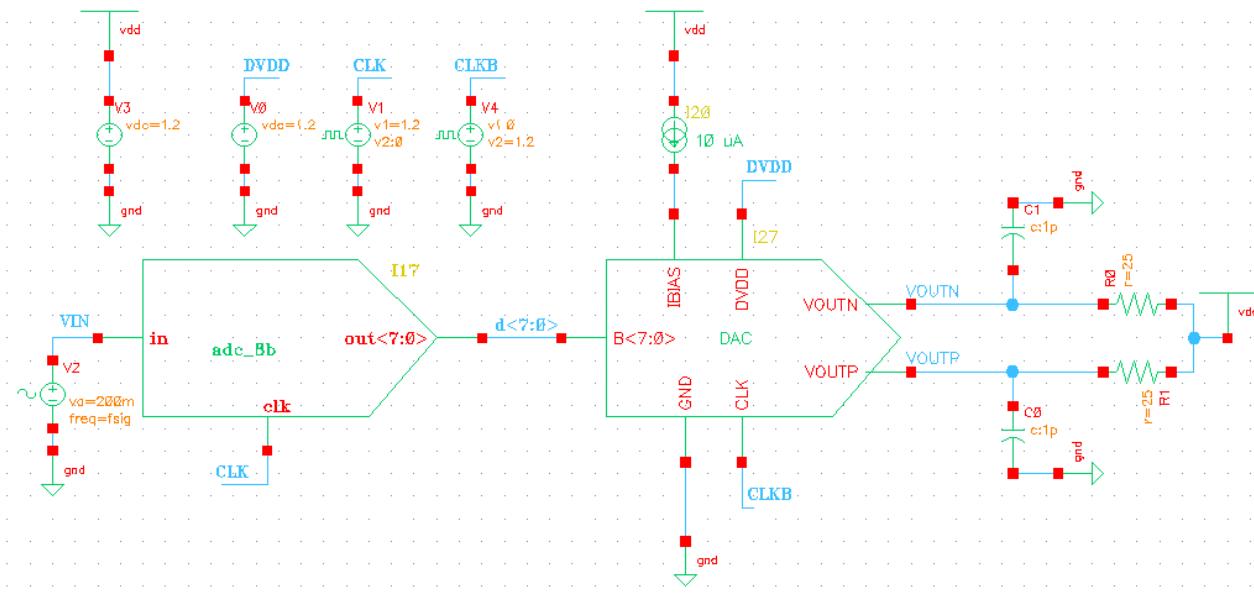


Figure 25: DAC is under test

Important Note:

As we go from bit 0 to bit 7 the load capacitance on buffer output was increasing. Therefore, there was need of scaling and increasing number of inverters in buffers. When first time DAC device was under test it showed that all the buffer are designed for different minimum delays respect to number of unit cell connected to them. So, tried to optimize the delay for bit 7 and that same buffer is used for all the bits. The digital inputs were reaching at same time but the slope of transition was different therefore there is still little spikes. Slope was different because loads are different on pair of buffers. So that the digital inputs will reach switching transistors at same time. This was adaptation in design from part 2. Because of minimum inverter used in part 2 delay was greater than 0.5ns and clock time period is 1ns.

Width and Length of transmission gate is set to 120nm and 45nm for PMOS and NMOS. In part 2 it was 120nm and 70 nm respectively. Change in length reduced the spikes because clock NMOS connected to output of transmission gate. Possible reason will be clock feed through and charge injection.

Part (b). Perform the transient analysis for a ramp binary input and report the differential output annotated with maximum and minimum voltage. Also, report a zoomed-in image of the output around 0V output annotating the unit step size. Write your observations.

ANS:

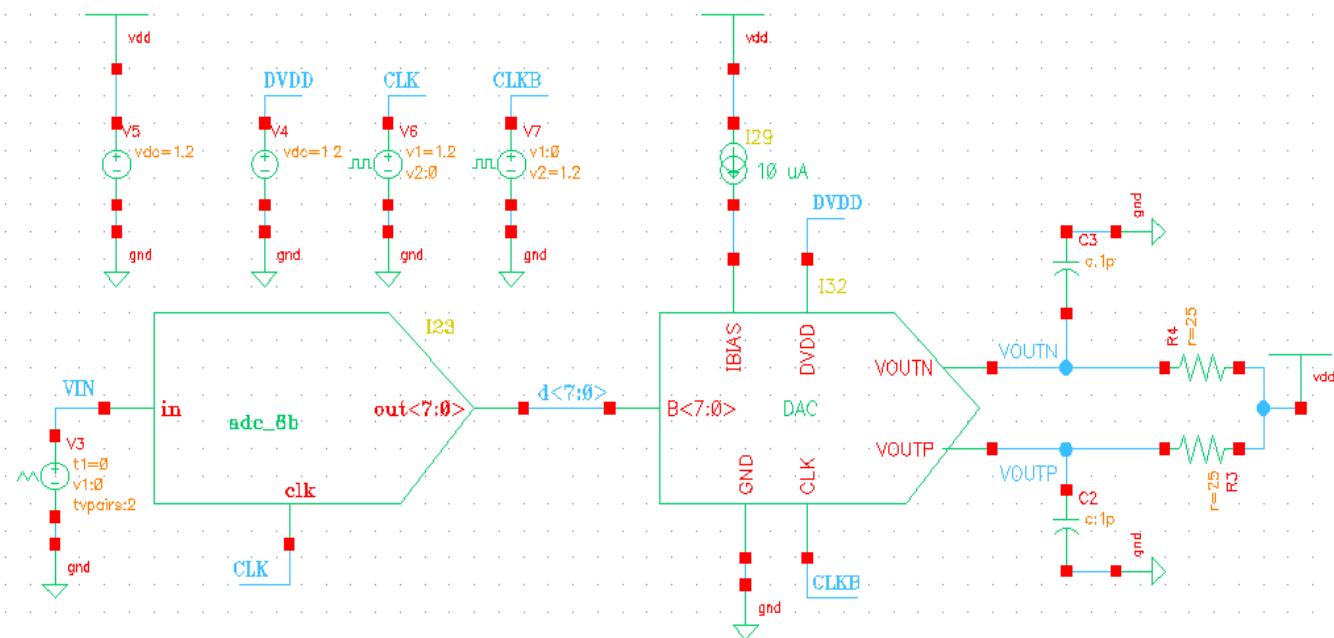


Figure 26: Ramp Input given to DAC

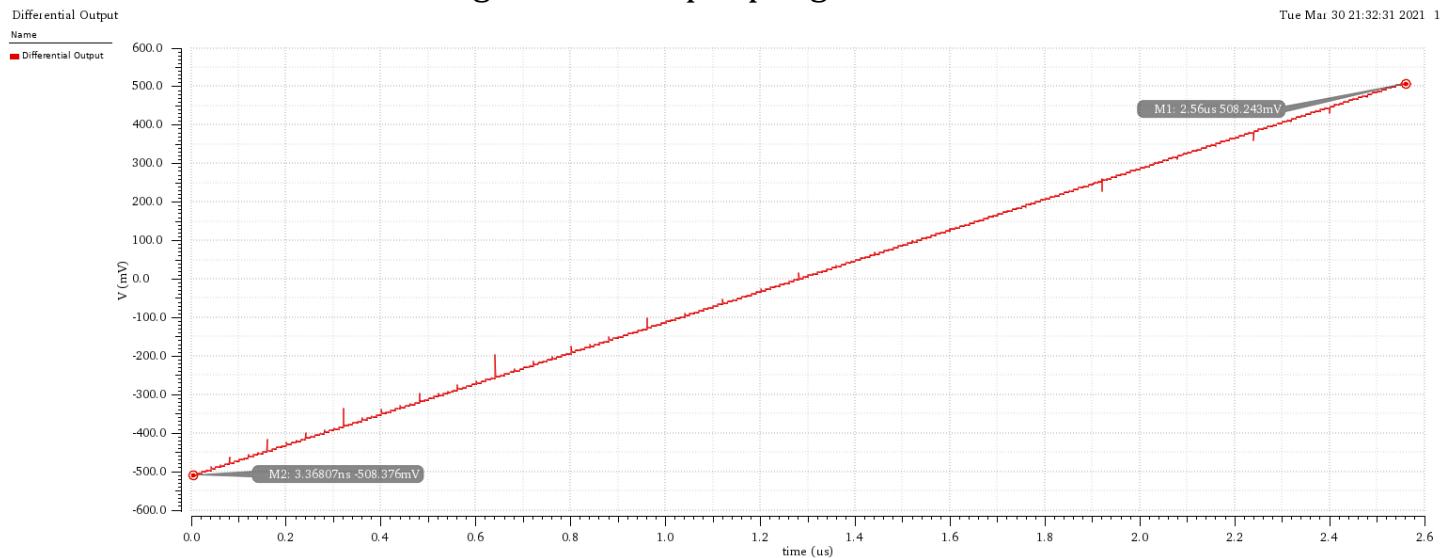


Figure 27: DAC with Maximum and Minimum Output

Observation: There is small spikes in waveform because of the small delay in switching transistor which is recorded in pico-seconds. When there is transition in MSB transistors but LSB transistors are not off yet which causes a spike.

$$0111 \rightarrow 1111(\text{momentarily}) \rightarrow 1000$$

8bit gives total 255 transition and V_{FS} taken as 1.02V therefore ideal step size is 4mV. In below plot we can see step size is $\approx 4\text{mV}$

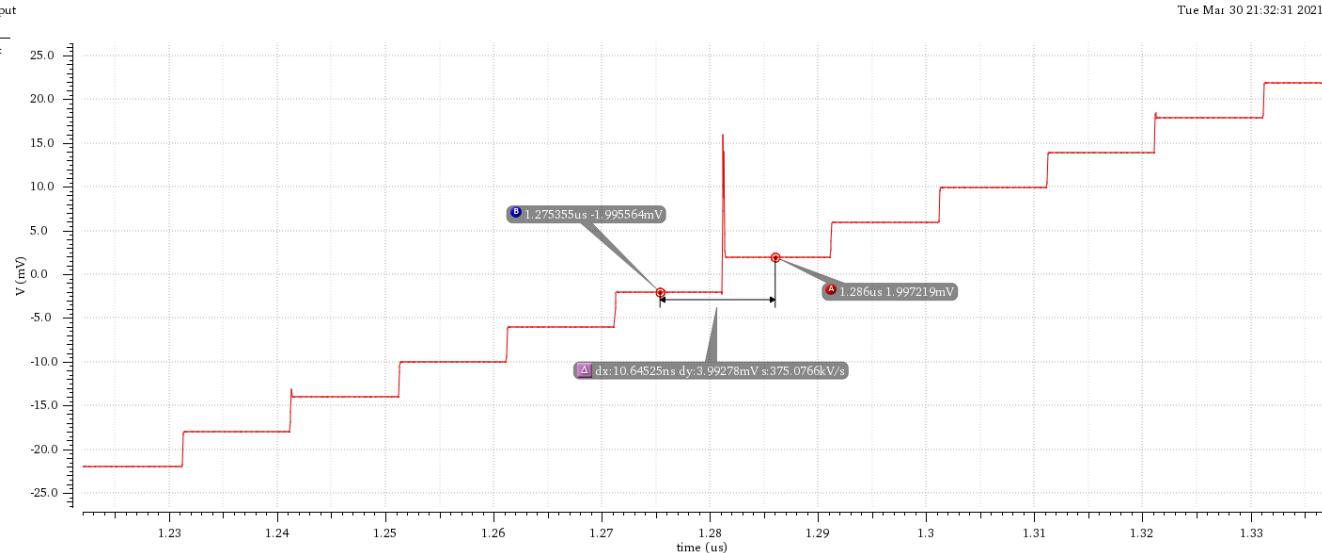


Figure 28: Zoomed Portion near 0V and step size

This result is recorded with input ramp from 0 to 400mV in $2.56\mu\text{s}$. Therefore, it has enough time to settle. So, we can see clear staircases, less noisy. But for Monte-Carlo simulation $2.56\mu\text{s}$ is large taking lots of memory and simulation time. So, ramp input is changed to 256 ns. But now settling time is very low so noise increased. Which affects INL, DNL, ENOB and SFDR of the design. After running Monte-Carlo and frequency response simulation, it showed that dynamic performance matching with specifications but static performance not matching when the input ramp is 0 to 400mV in 0 to 256ns.

Part (c). Tabulate the offset, full scale error, gain error and plot the DNL and INL for the output obtained in Part(b) above.

ANS:

As explained above when input is for $2.56 \mu\text{s}$ the INL and DNL is matching as per specifications. Due to change in input to 256ns INL is not matching as per requirement. Ideal parameters

$$V_{o(\min)} = -0.51V \text{ and } V_{o(\max)} = 0.51V$$

OFFSET Error	0.0016V	0.4LSB
FULL SCALE Error	-0.0018V	-0.45LSB
GAIN Error	1.003	-

Table 11: Static characteristics binary DAC

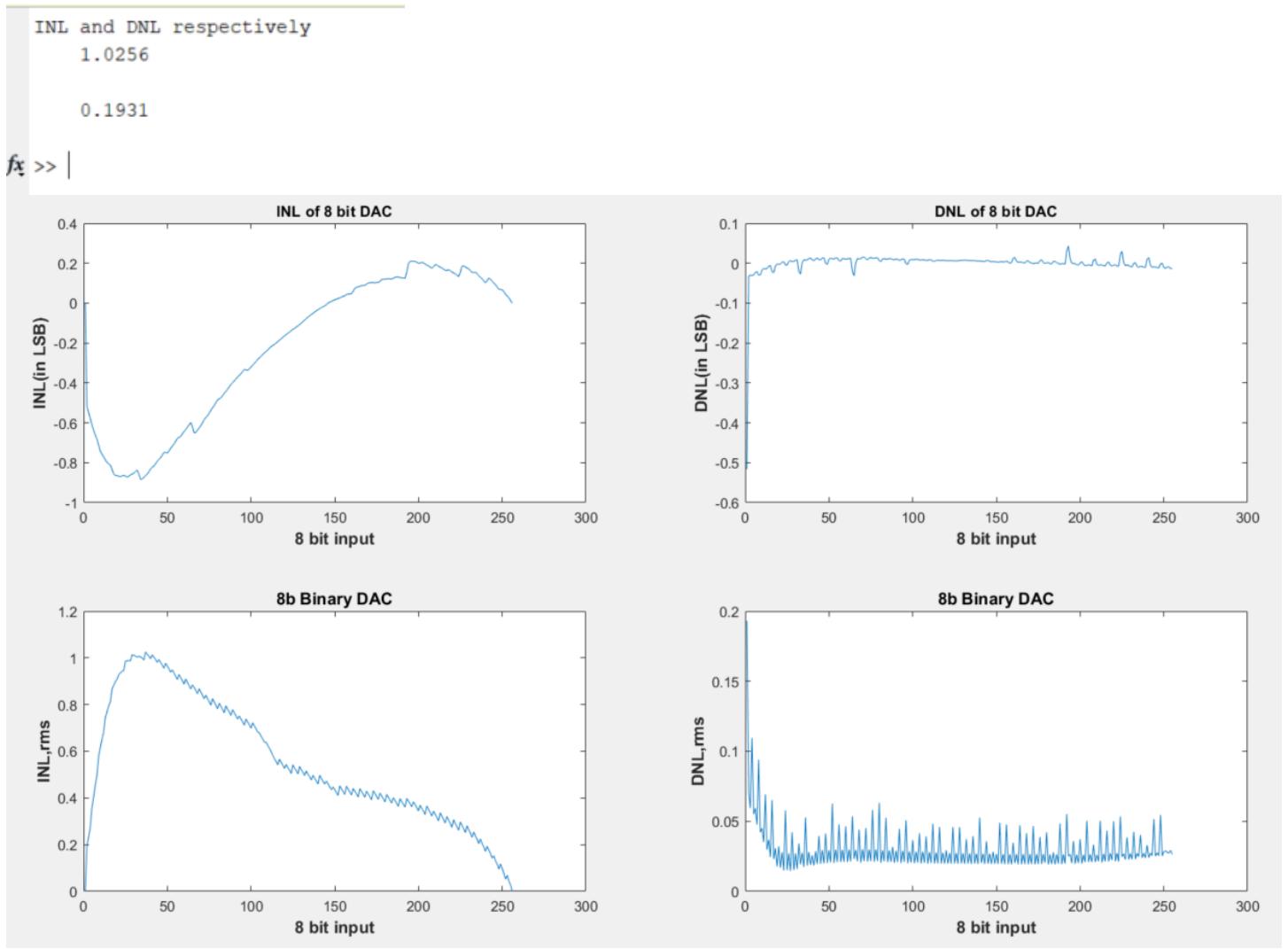


Figure 29: INL and DNL of RAMP input

Part (d). Perform 100 Monte-Carlo simulations. Report the mean and standard deviation of unit current I_{LSB} . Plot the aggregate root-mean square(rms) DNL and INL values. Report the maximum INL_{rms} and DNL_{rms} . Calculate the theoretical expected INL_{rms} and DNL_{rms} . Explain your observations.

ANS:

Performed Monte-varlo for 8 jobs.

Mean of unit current $I_{LSB} = 79.37\mu A$; Standard deviation (σ) = $8.797\mu A$

INL_{rms} and DNL_{rms} determined using MATLAB code.

Maximum $INL_{rms} = 1.8274$ LSB

Maximum $DNL_{rms} = 0.6142$ LSB

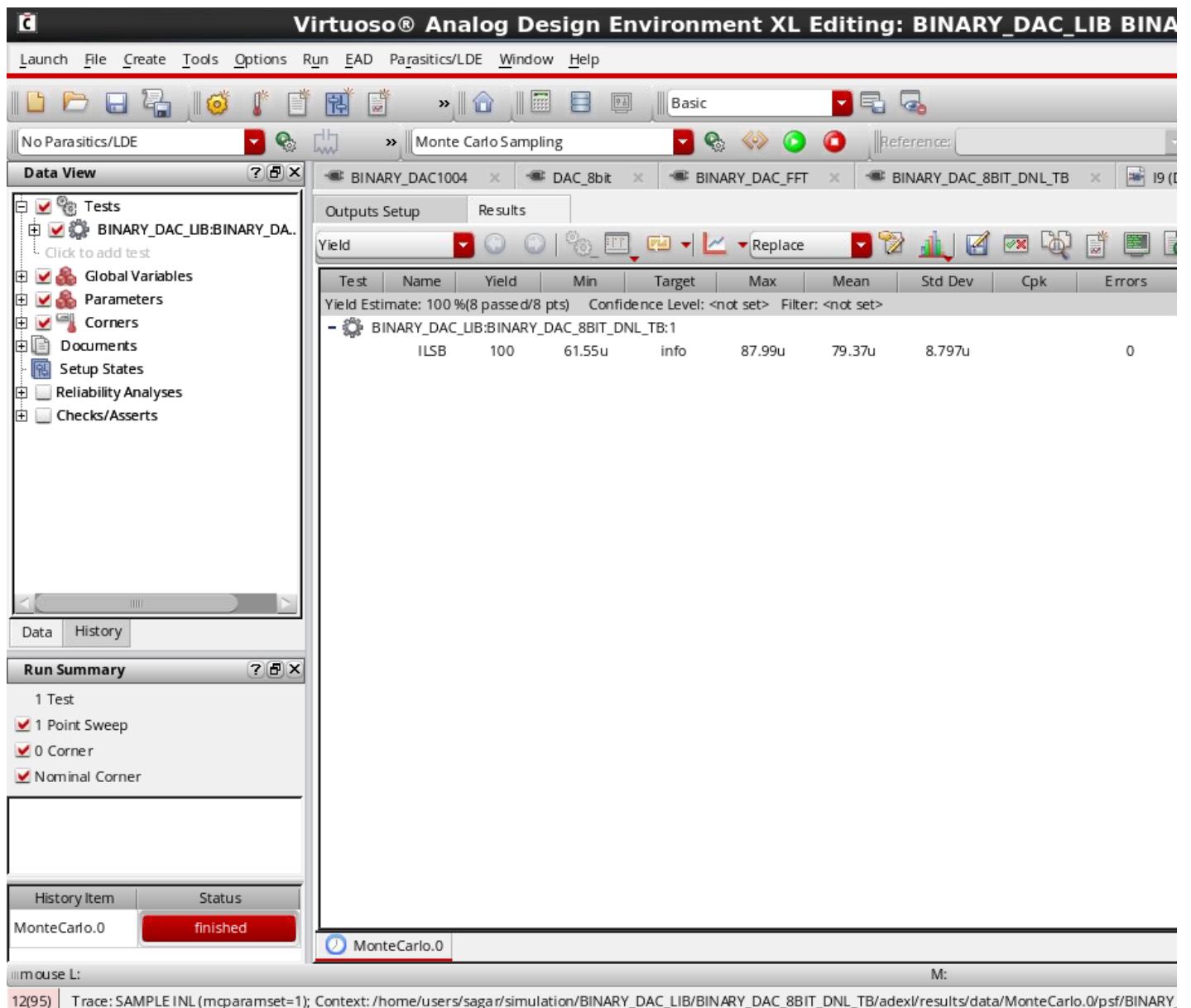


Figure 30: Monte-Carlo Simulation

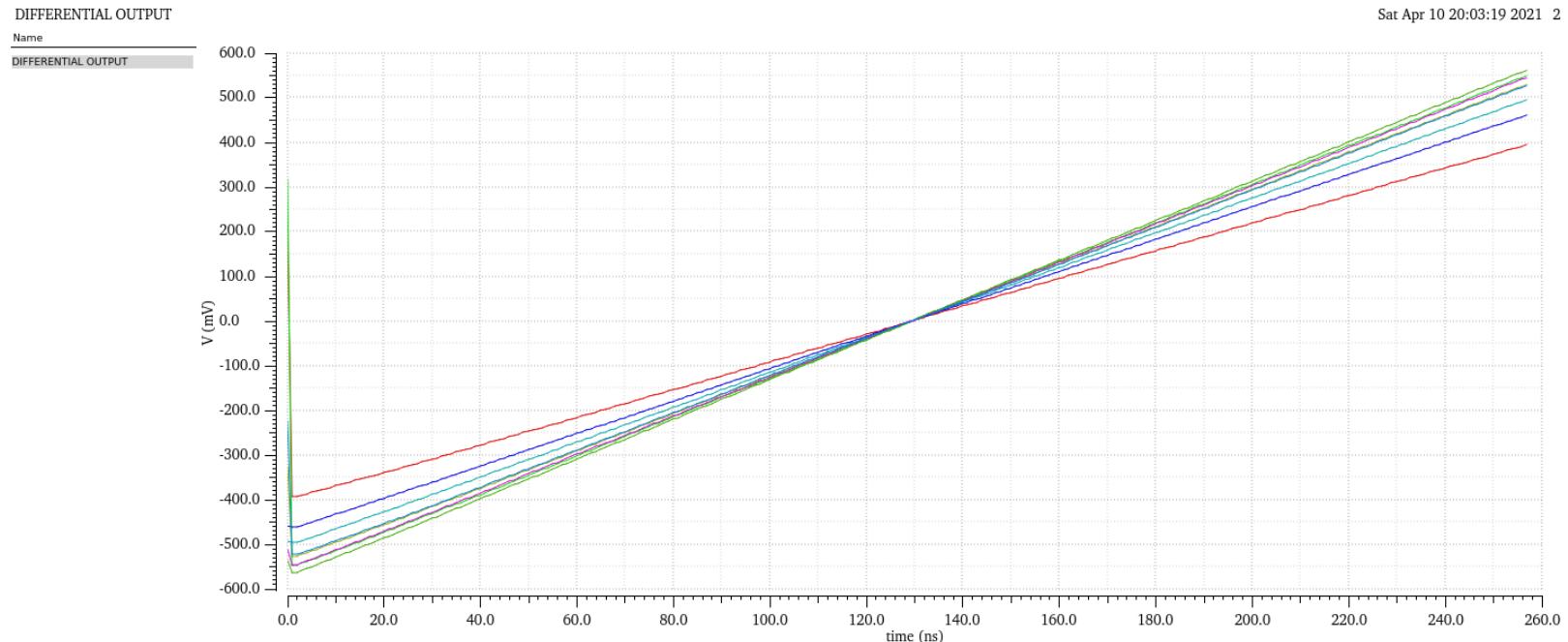


Figure 31: Differential Output from MC Simulation

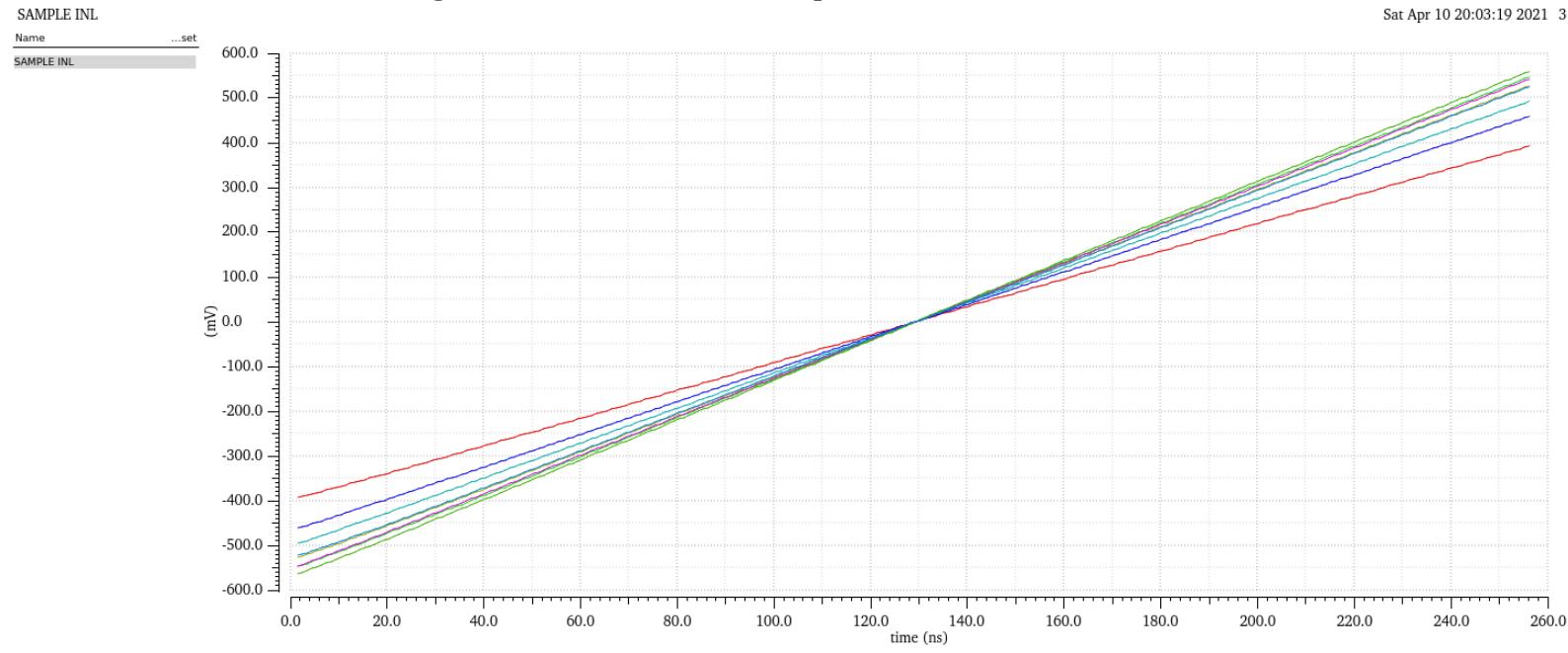


Figure 32: SAMPLE INL results from MC Simulation

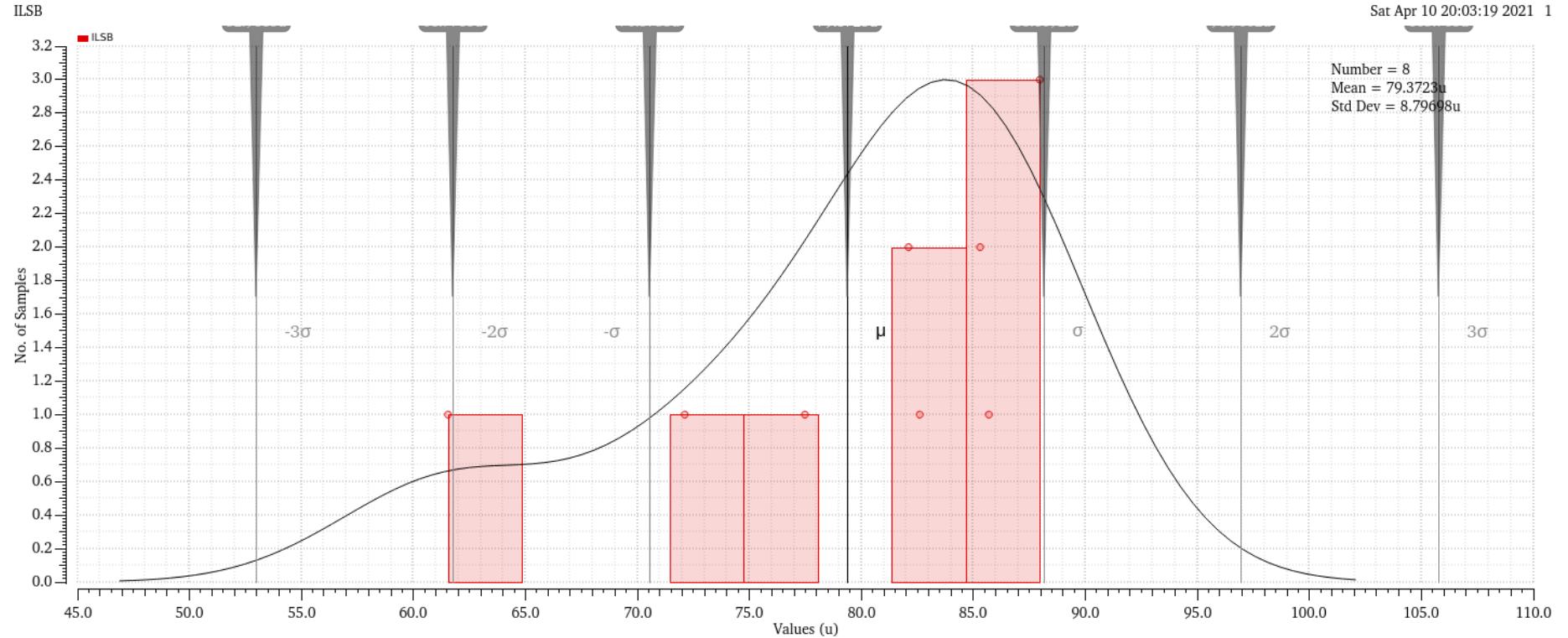


Figure 33: I_{LSB} Distribution for 8 jobs in MC Simulation

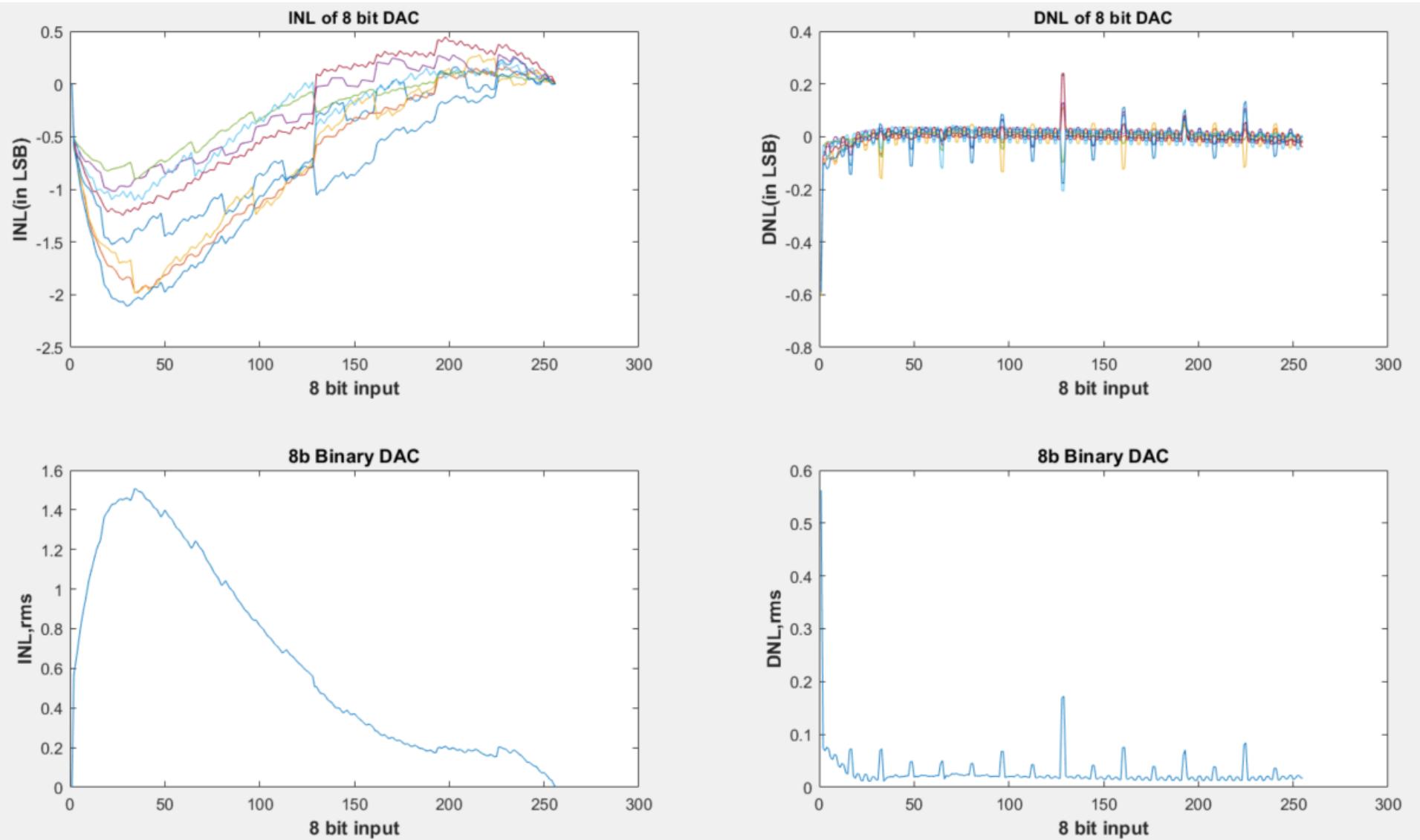


Figure 34: MATLAB simulation for INL_{rms} and DNL_{rms} on INL data determined by MC simulation

Part (e). Provide a sinusoidal input of frequency $< 100\text{MHz}$ and plot 2048-point FFT Spectrum. Mark the fundamental and the subsequent harmonic frequency peaks in the spectrum. Explain the observations and possible reason behind the harmonic frequencies.

ANS:

Input frequency is $79.5898 \text{ MHz} < 100 \text{ MHz}$

Due to circuit mismatches, there is noise in circuit. This noise appears near the harmonic frequencies. One of the possible reasons will be correlation of the input and noise.

2^{nd} harmonic frequency shown in the plot that is 159.18MHz .

Code dependent glitches also causes the harmonic distortion.

Mid-code transitions like $00000111 \rightarrow 00001000$ or MSB transitions $01111111 \rightarrow 10000000$

Are not synchronize. Their delay is different. There are glitches due to derivation of digital input and its inverted signal on different time. E.g., for bit 4 there are digital input B_4 which is fed to transmission gate and inverter b_4 and $\sim b_4$ which is then given to buffer block. b_4 and $\sim b_4$ not reaching same time causing glitches.

Other than this parasitic capacitance present between switching transistors gate and cascode current transistors. At high frequency which starts to interfere with switching signal.

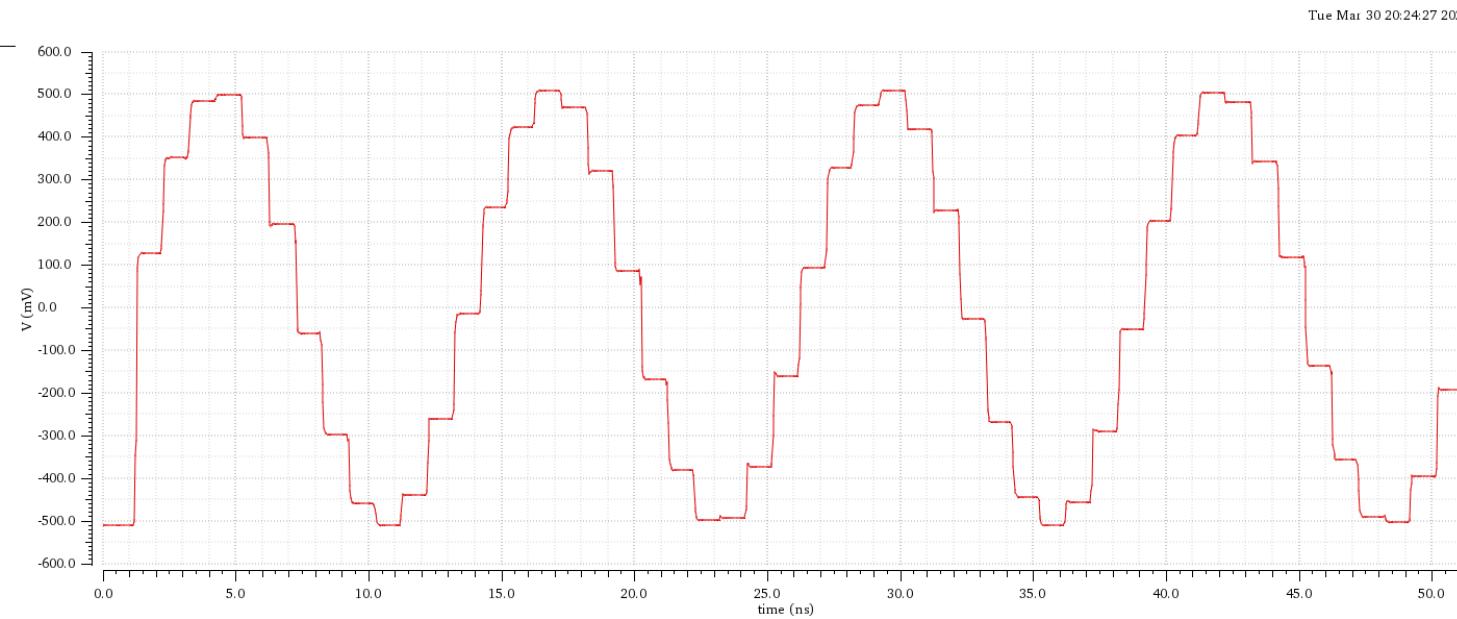


Figure 35: DAC output for 79.58MHz sinusoidal input

```
db20(dft((v("/VOUTP" ?result "tran") - v("/VOUTN" ?result "tran")) 1u 3.048u 131072 "Rectangular" 0 0 1))
```

1

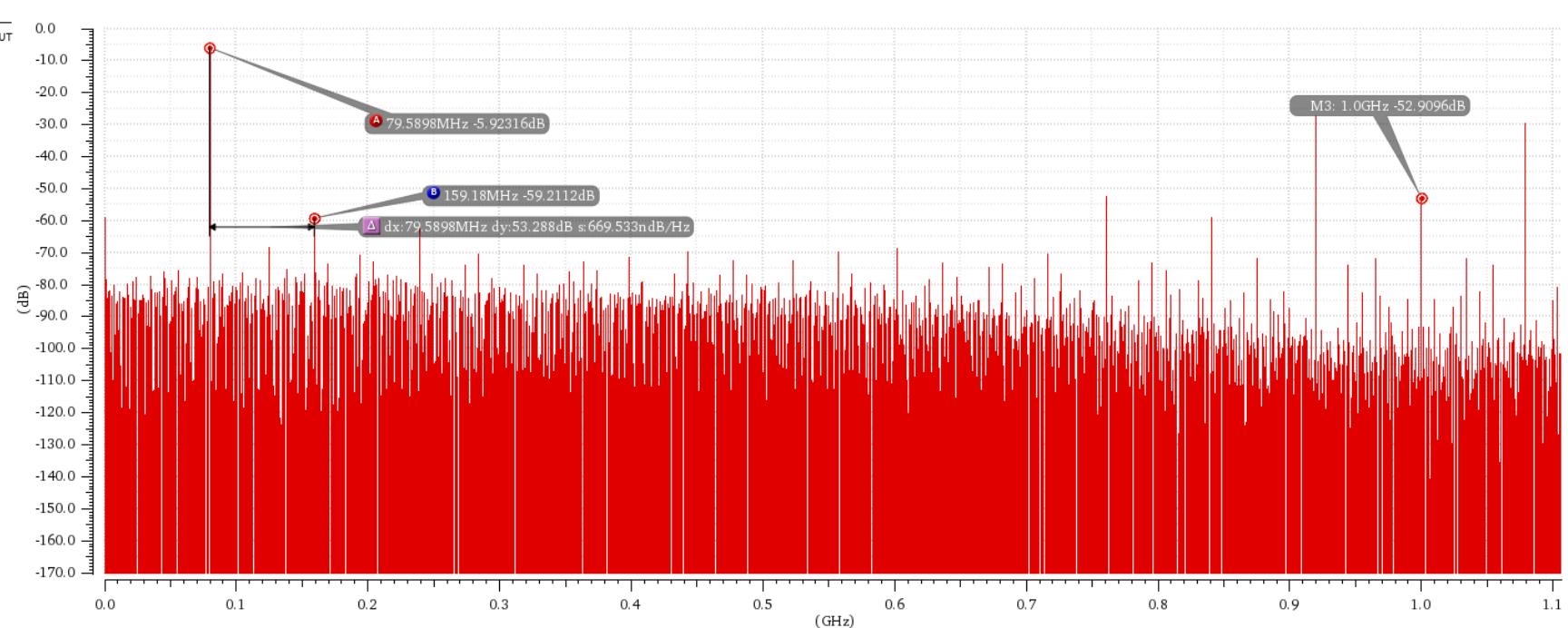


Figure 36: DAC frequency spectrum for 79.58MHz Sinusoidal Input

Part (f). Provide a sinusoidal input of frequency $> 400\text{MHz}$ and plot 2048-point FFT Spectrum. Mark the fundamental and the subsequent harmonic frequency peaks in the spectrum. Explain the observations and possible reason behind the harmonic frequencies.

ANS:

Input frequency $401.855\text{MHz} > 400\text{MHz}$

For this input frequency time period is 2.488ns and clock time period is 1ns .

Input is very fast. DAC couldn't detect intermediate values of input. Therefore, high distortion is seen at output. As distortion is high, more harmonic frequency will be present.

As above mentioned in above question glitches present. Parasitic capacitance present which causes harmonic distortions at high frequency.

Below signal doesn't look like sinusoidal because its time period is approximate 2 ns and clock is 1ns . Due to these 1 or 2 samples is reached to output.

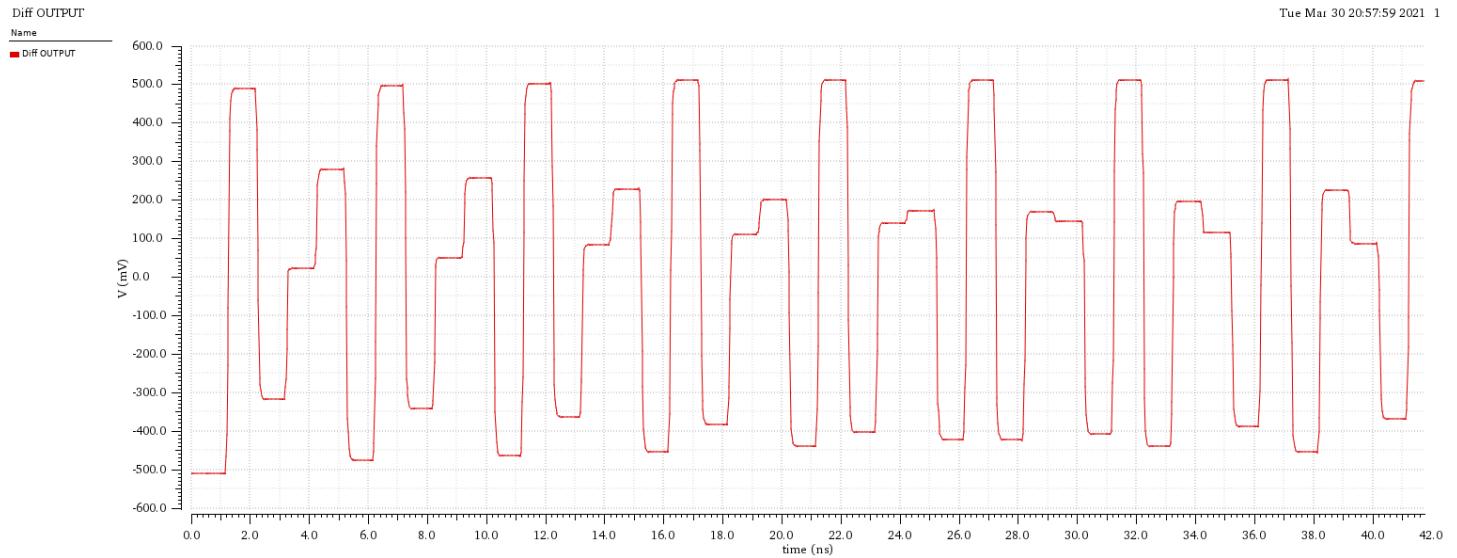


Figure 37: DAC output for 401.855MHz Sinusoidal input

`db20(dft((v("/VOUTP") ?result "tran") - v("/VOUTN") ?result "tran")) 1u 3.048u 131072 "Rectangular" 0 0 1)`

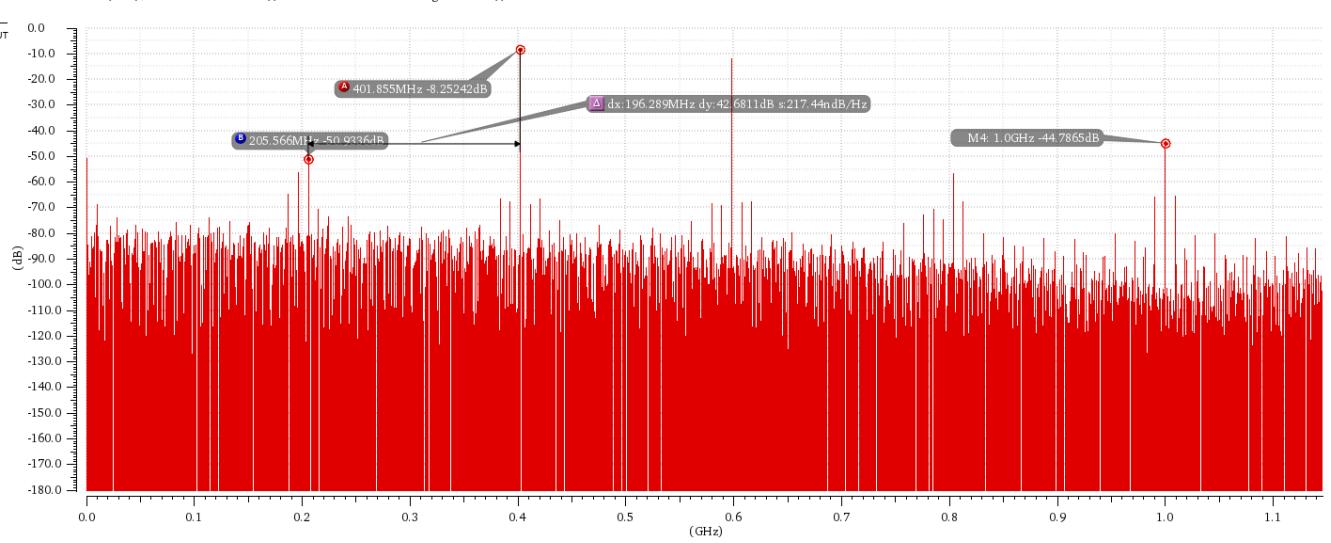


Figure 38: DAC frequency Spectrum for 401.855MHz Sinusoidal input

Part (g). Tabulate the simulated dynamic performance characteristics (SNDR, SFDR, ENOB) of your DAC in Part€ and Part(f).

	Input Frequency 79.58MHz	Input Frequency 401.855MHz
SNDR (dB)	46.912123	40.165276
SFDR (dBc)	53.288024	42.681141
ENOB (bits)	7.4998544	6.3791156

Table 12; Dynamic Performance Binary DAC

Following Images for the dynamic characteristics:

1. Input frequency 401.855MHz

2. Input frequency 79.58Mhz

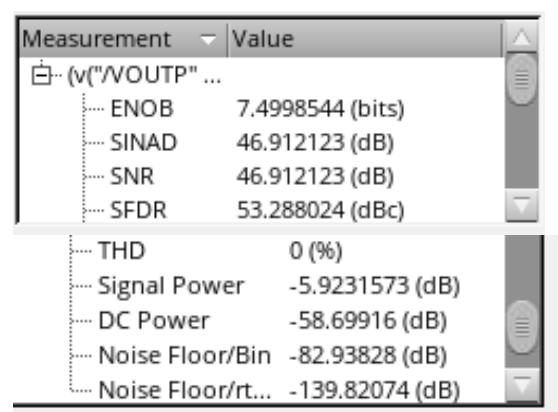
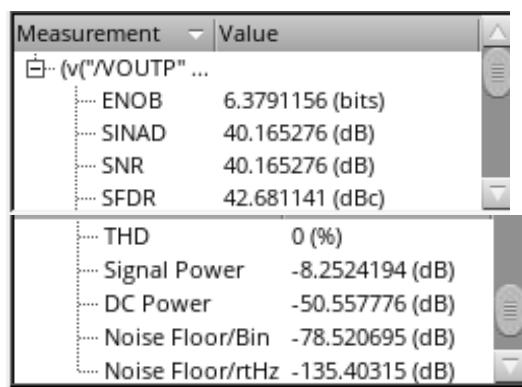


Figure 39: Snapshots of SFDR,ENOB and SNR

Part (h). Report the total power consumption (digital + analog) of your 8-bit DAC.

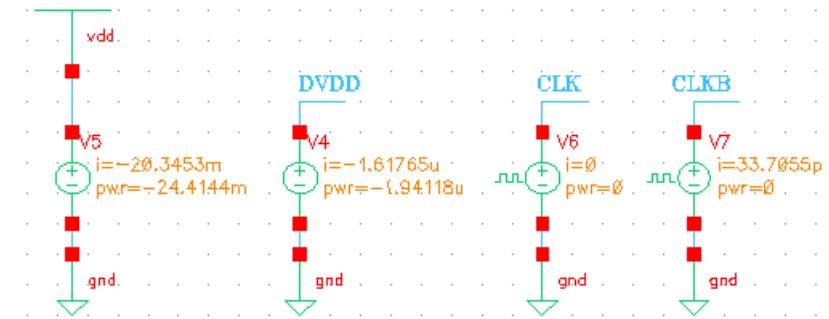


Figure 40: Power Consumption

Figure 16: Power consumption

Total Power consumption will be 24.4124mW

Part (i). Report the total area (digital + analog) of your 8-bit DAC.

CURRENT SOURCE (nm)			
MOS	W	L	AREA
M1	4405	45	198225
M2	4405	45	198225
TOTAL AREA E-18			16250
CLOCK MOS			
NMOS	W	L	AREA
1	120	45	5400

TRANSMISSION GATE (nm)			
MOS	W	L	AREA
NMOS	120	45	5400
PMOS	120	45	5400
TOTAL AREA E-18			10800

INVERTER(nm)			
MOS	W	L	AREA
NMOS	120	45	5400
PMOS	200	45	9000
TOTAL AREA E-18			14400

BUFFER				BUFFER bar			
PMOS	W	L	AREA	PMOS	W	L	AREA
1	200	45	9000	1	200	45	9000
2	544	45	24480	2	544	45	24480
3	1479.68	45	66585.6	3	1479.68	45	66585.6
4	4024.73	45	181112.9	4	4024.73	45	181112.9
5	10947.264	45	492626.9	5	10947.264	45	492626.9
6	29776.56	45	1339945	6	29776.56	45	1339945
7	80992.24	45	3644651	7	80992.24	45	3644651
8	220298.8	45	9913446	8	220298.8	45	9913446
NMOS	W	L	AREA	NMOS	W	L	AREA
1	120	45	5400	1	120	45	5400
2	326.4	45	14688	2	326.4	45	14688
3	887.808	45	39951.36	3	887.808	45	39951.36
4	2414.838	45	108667.7	4	2414.838	45	108667.7
5	6568.3584	45	295576.1	5	6568.3584	45	295576.1
6	17865.936	45	803967.1	6	17865.936	45	803967.1
7	48595.344	45	2186790	7	48595.344	45	2186790
8	132179.28	45	5948068	8	132179.28	45	5948068
TOTAL AREA E-18		2.5E+07		TOTAL AREA E-18		2.5E+07	

AREA OF DAC			
COMPONENT	AREA	TIMES	TOTAL AREA
UNIT CELL	730050	255	186162750
CURRENT AOURCE	16250	1	16250
BUFFER	25074956	8	200599645.8
BUFFERBAR	25074956	8	200599645.8
INVERTER	14400	24	345600
TRANSMISSION GATE	10800	8	86400
CLOCK NMOS	5400	16	86400
TOTAL DAC AREA E-18			587896691.6
AREA IN UM²			587.8966916

Figure 41: Area of Original design

Part (j). Explain how you can possibly improve the static and dynamic performance of your DAC.

As we saw above results:

$$\text{INL} = 1.8\text{LSB}$$

$$\text{DNL} = 0.612\text{LSB}$$

$$\text{SFDR} = 53\text{dB}$$

$$\text{ENOB} = 7.499$$

Other than INL, static and dynamic characteristics matches required parameters. As explain before INL for ramp input $2.56\mu\text{s}$ was satisfying the requirement. But as time period is decreased the INL degraded. To improve INL following process followed.

1. reference from "A 10-b, 500-MSample/s CMOS DAC in 0.6 mm" by Chi-Hung Lin and Klaas Bult
 - a. in this reference $\sigma^2 \propto \frac{1}{\text{Area}}$ relationship of σ and Area is explained. So as area increased the INL will improved.
 - b. Therefore, increased the area by 4 times to make INL near 0.9LSB and 16 times to make INL $< 0.5\text{LSB}$.
 - c. As area increased static performance improved but dynamic performance degraded. There are spikes in staircases when the sinusoidal input is applied.
 - d. When the area of tailing current and cascode transistor (M_{B2} and M_{B4}) increased. The parasitic capacitance between gate of switching transistor and drain of tail current transistor causes spike in output. Probable reason will be clock feedthrough and charge injection.
 - e. To lower this effect, WL of switching transistor is increased. So, buffer can take a load of switching transistors their sizes increased. So, the inverters and buffers sizes also increased.

Comparison 1: Ramp Input is applied to the DAC designed
Ideal parameters are $V_{o(min)} = -0.51V$ and $V_{o(max)} = 0.51V$

OFFSET Error	0.6268mV	0.1567LSB
FULL SCALE Error	2.818mV	0.7045LSB
GAIN Error	1.0021	-

Table 13: Static Performance of Final Binary DAC

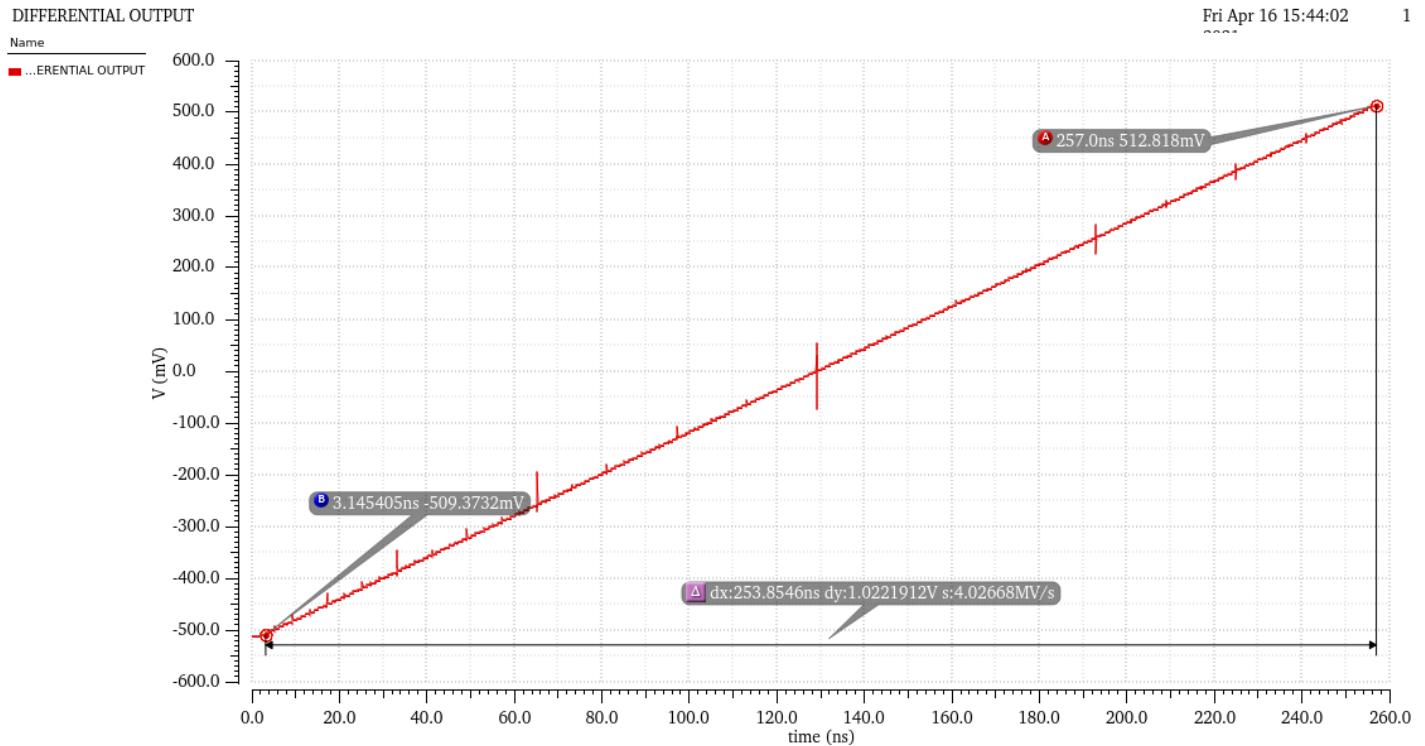


Figure 42: Output result of RAMP input to scaled design to improve INL

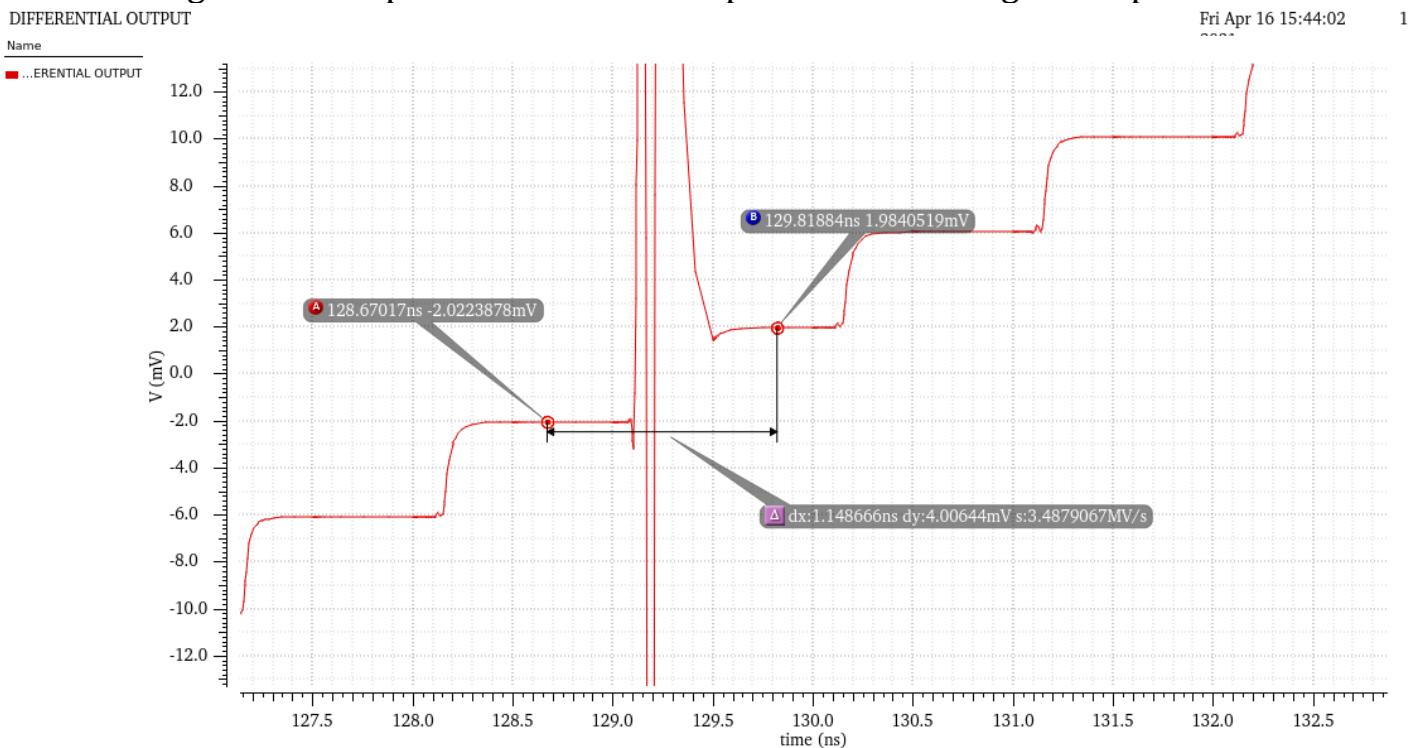
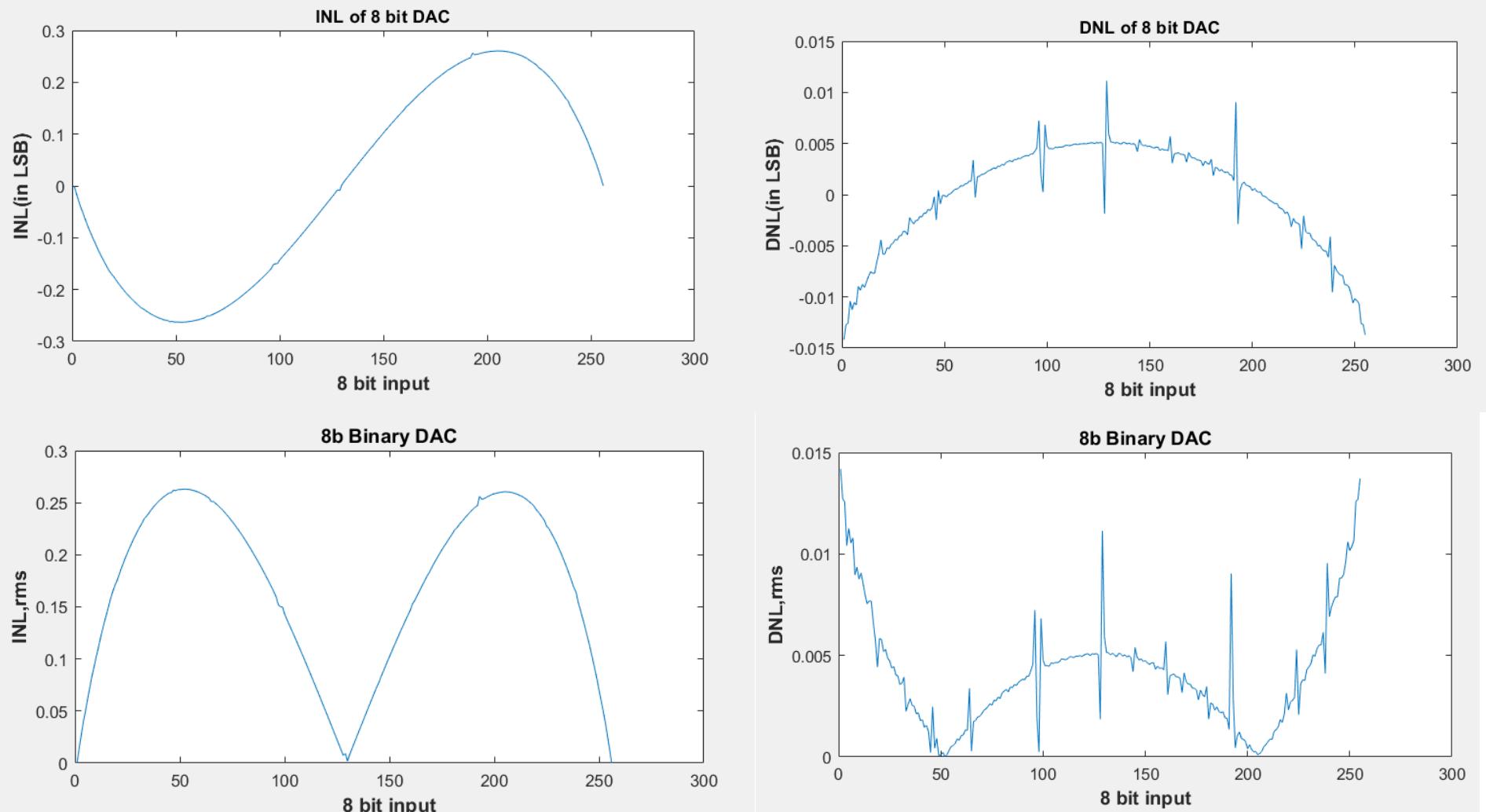


Figure 43: Zero crossing of output

Comparison 2: INL and DNL



```
>> EE719_INL_DNL
INL and DNL respectively
0.2630

0.0142
```

Figure 44: INL and DNL analysis on single ramp input to scaled design

Comparison 3: Monte-Carlo Simulation



Figure 45: Monte-Carlo Simulation on updated unit cell

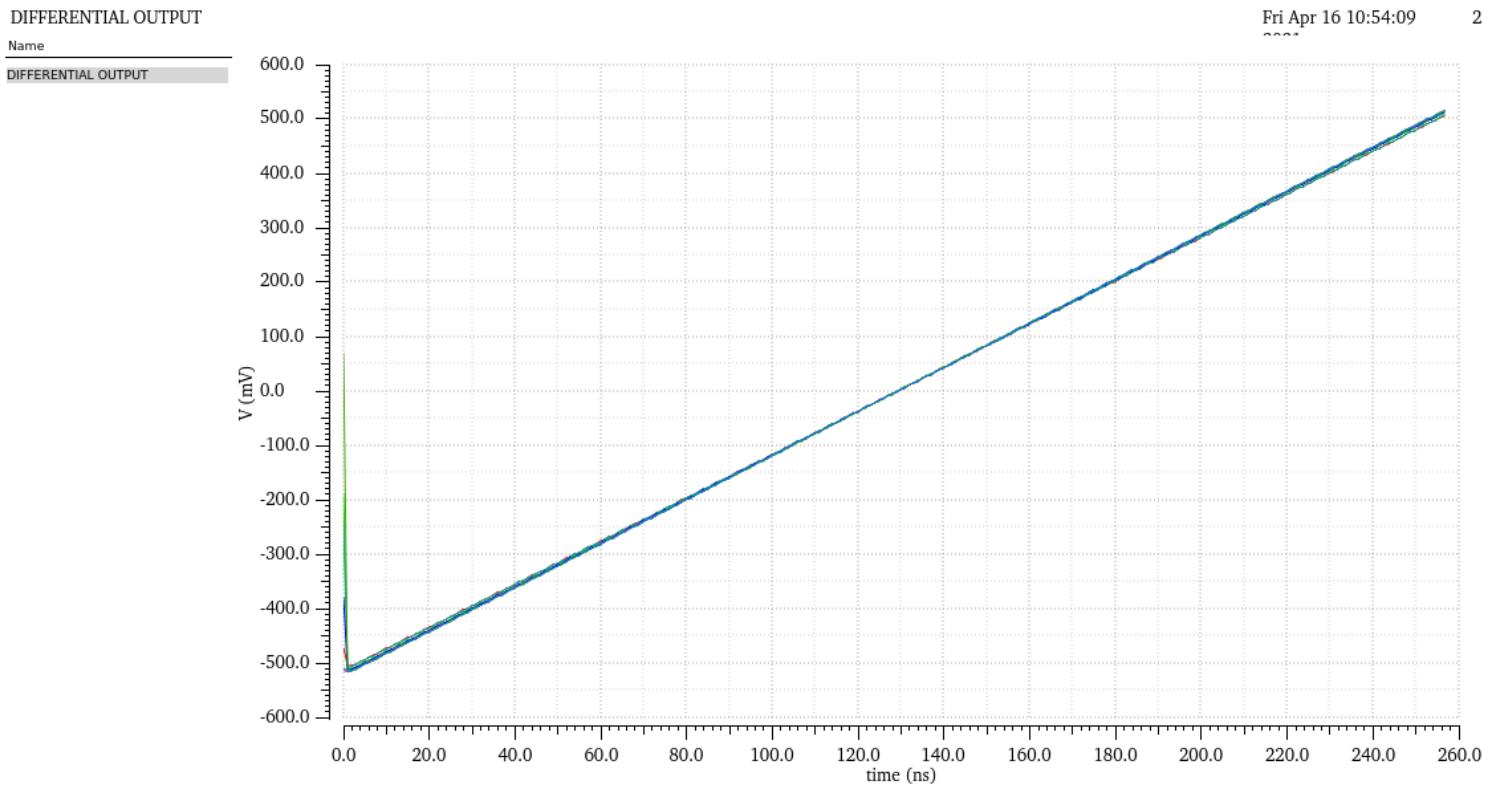


Figure 46: differential output results after MC simulation

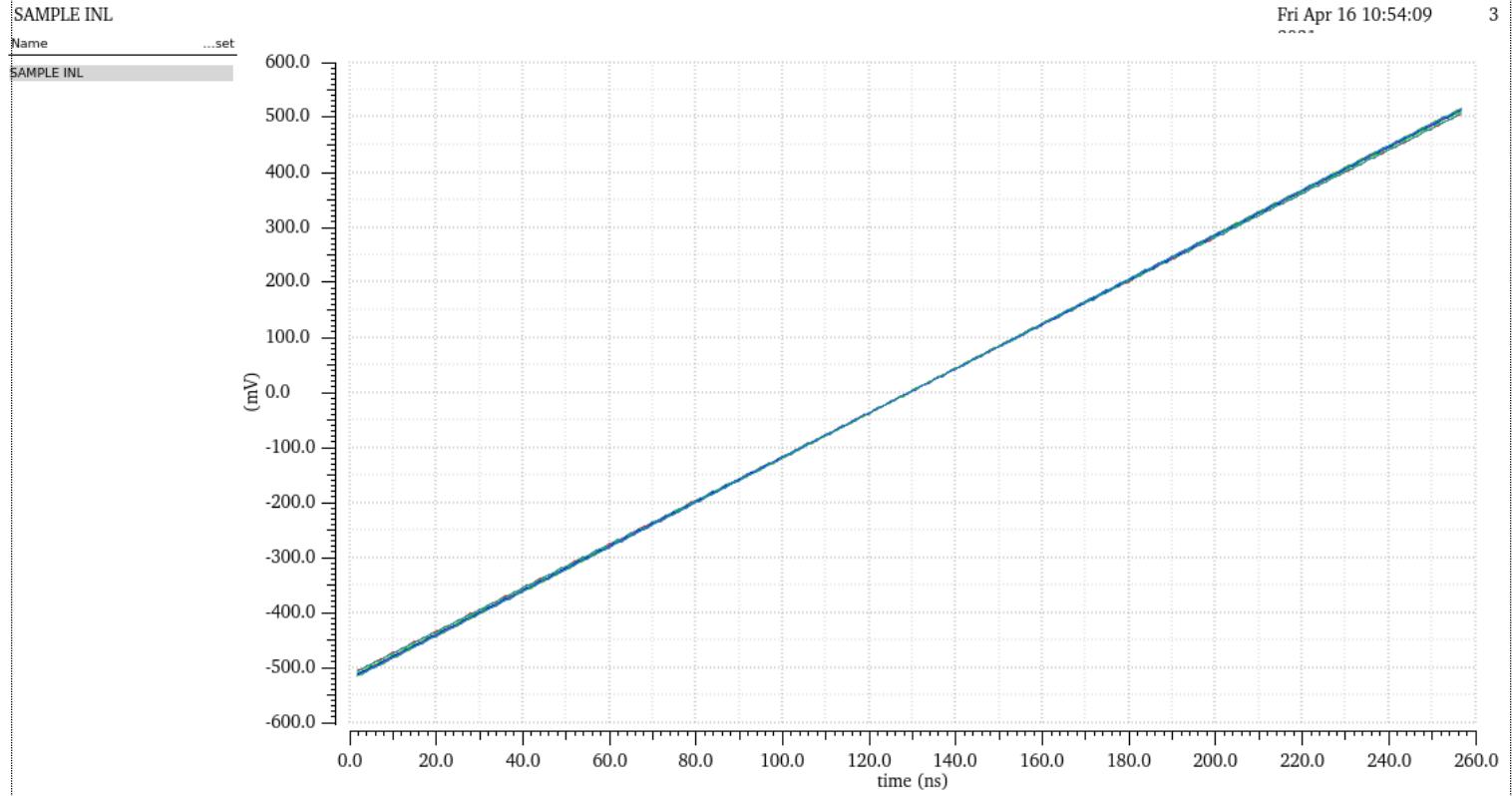


Figure 47: INL results after MC simulation

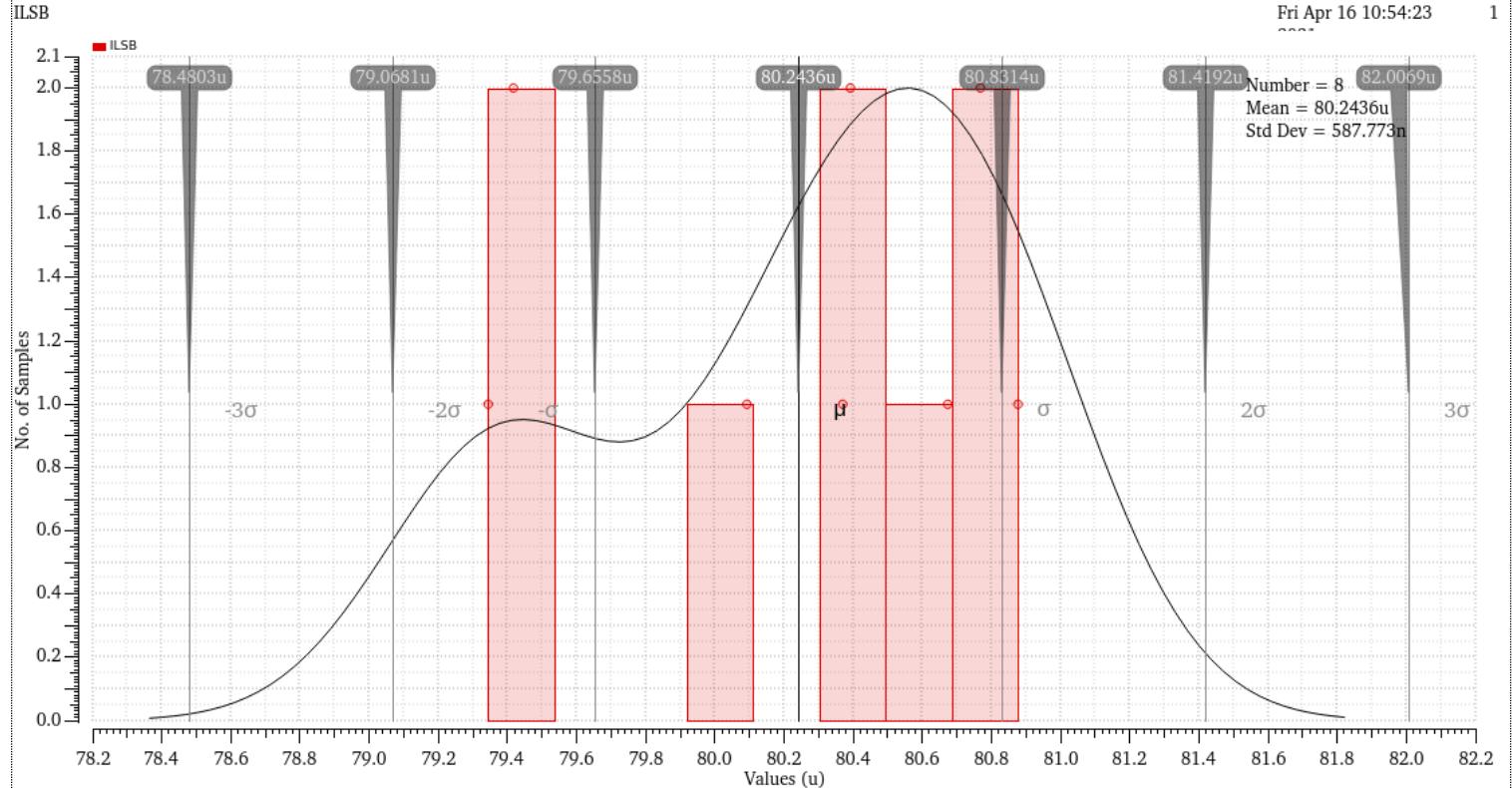
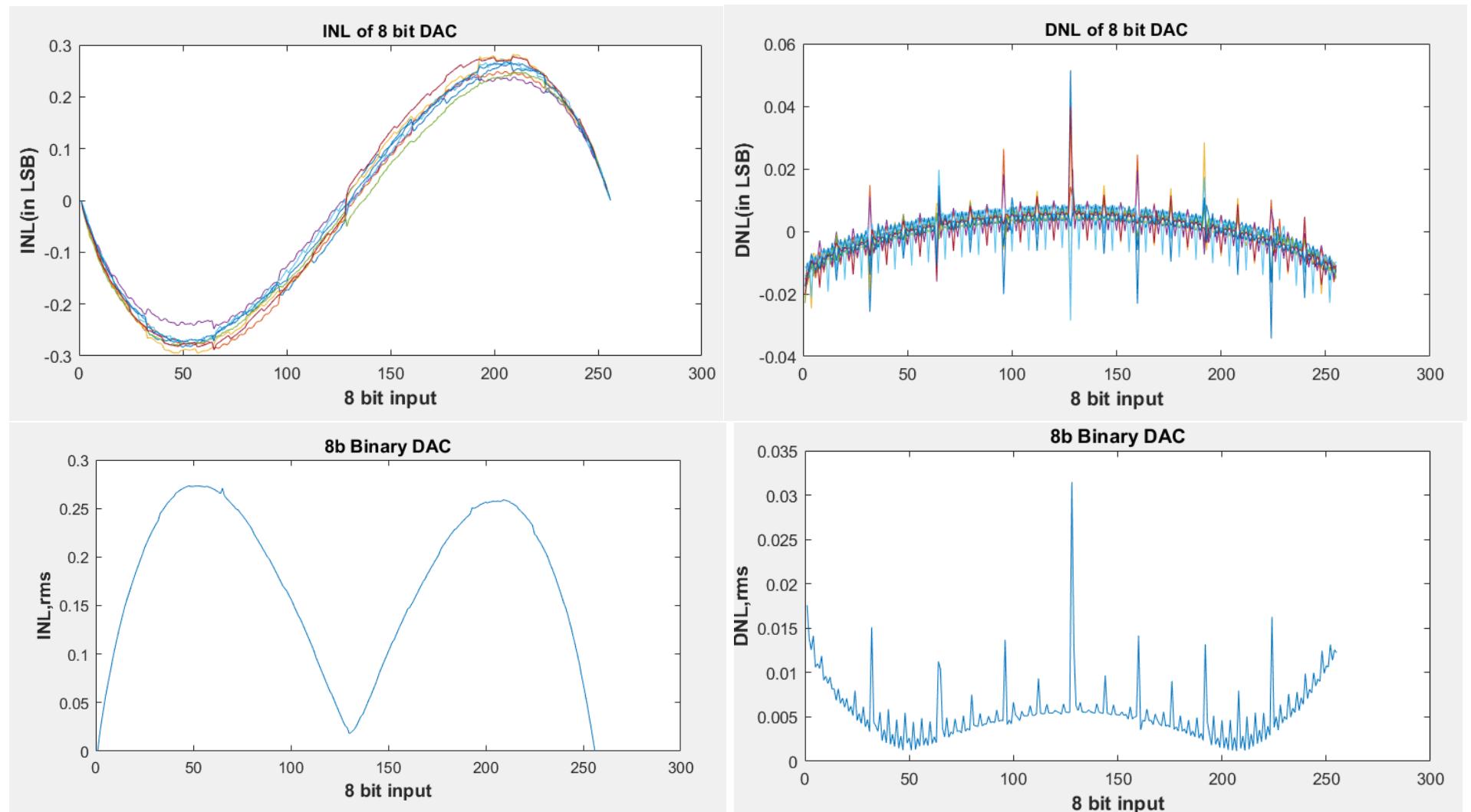


Figure 48: I_{lsb} results after MC simulation



```
>> EE719_INL_DNL
INL and DNL respectively
0.2732
0.0315
```

Figure 49: Improved INL and DNL after scaling the area

Comparison 4: Frequency Response

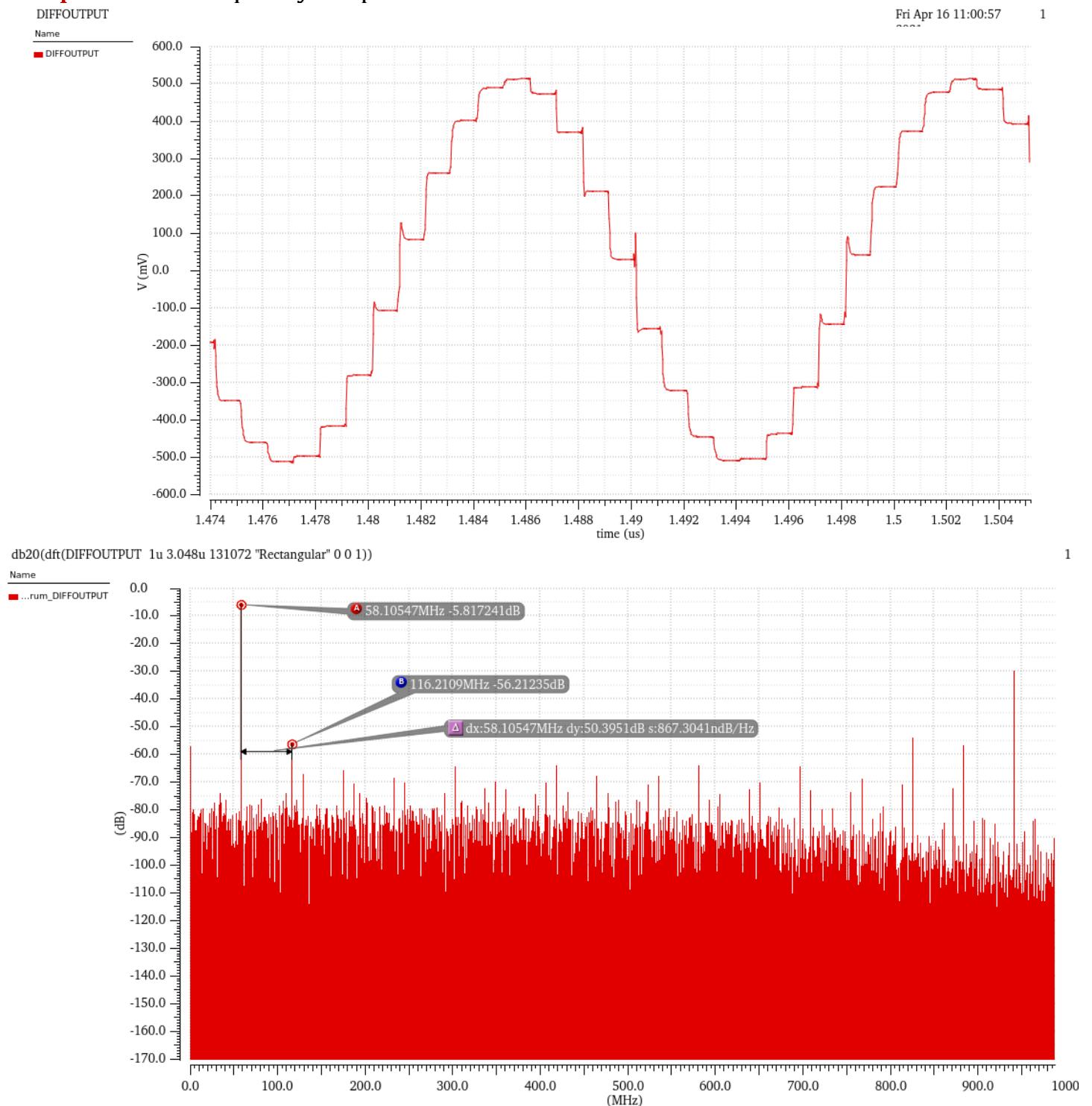


Figure 50: Frequency response of the output with sinusoidal input ($f < 100\text{MHz}$)

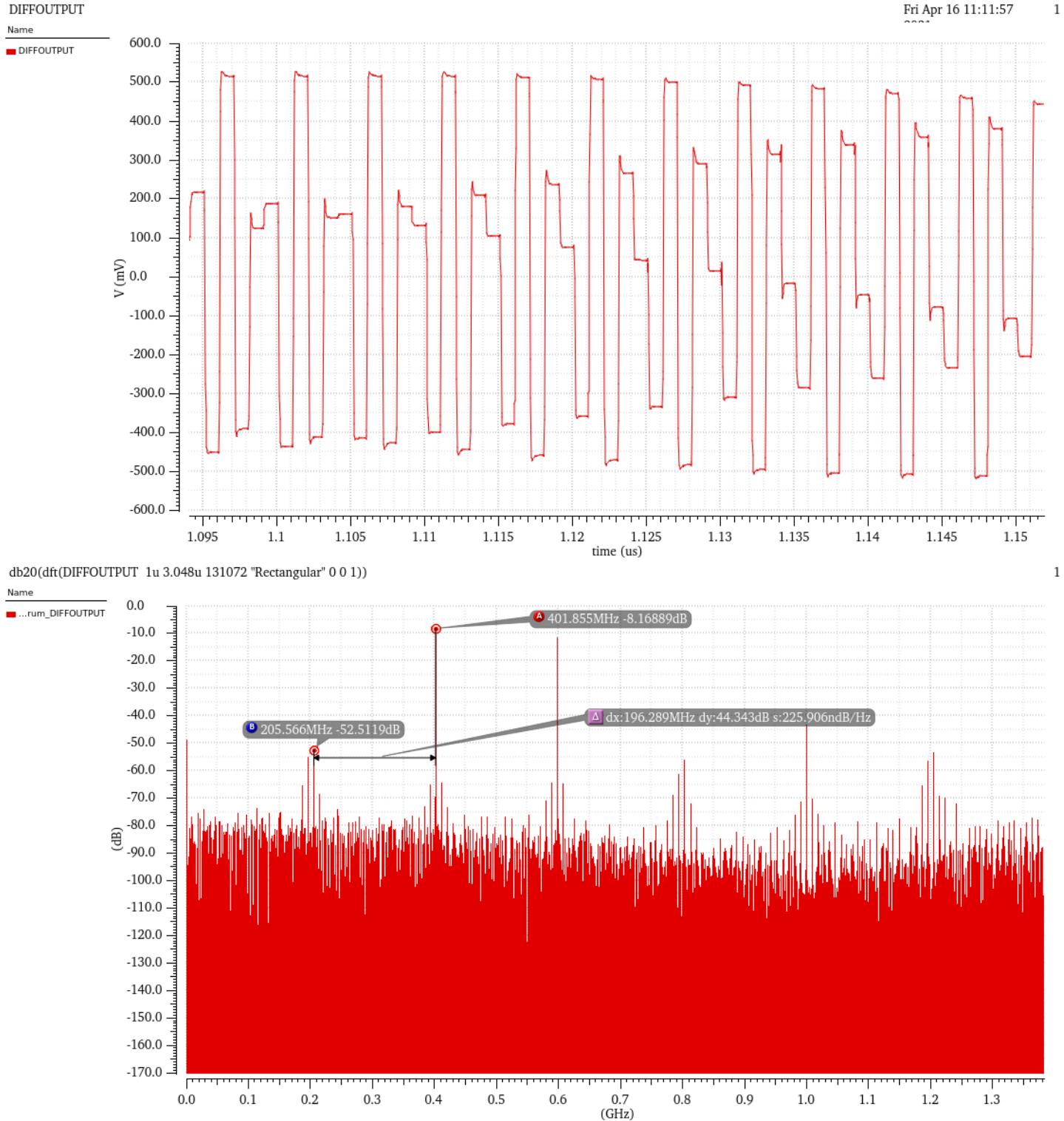


Figure 51: Frequency response of the output with sinusoidal input ($f > 400\text{MHz}$)

Frequency <100MHz

Measurement	Value
DIFFOUTPUT	
ENOB	7.3063466 (bits)
SINAD	45.747207 (dB)
SNR	45.747207 (dB)
SFDR	50.395111 (dBc)
THD	
Signal P...	-5.8172409 (dB)
DC Power	-56.948208 (dB)
Noise Fl...	-81.667447 (dB)
Noise Fl...	-138.5499 (dB)

Frequency >400MHz

Measurement	Value
DIFFOUTPUT	
ENOB	6.4716957 (bits)
SINAD	40.722608 (dB)
SNR	40.722608 (dB)
SFDR	44.342968 (dBc)
THD	
Signal P...	-8.1688893 (dB)
DC Power	-48.776582 (dB)
Noise Fl...	-78.994497 (dB)
Noise Fl...	-135.87695 (dB)

Figure 52: Dynamic Parameters

	Input Frequency 58.10MHz	Input Frequency 401.855MHz
SNDR (dB)	45.74	40.20
SFDR (dBc)	50.3951	44.3429
ENOB (bits)	7.3063	6.471

Table 14: Dynamic Performance of Final Binary DAC

Table 13:

Comparison 5: power consumption

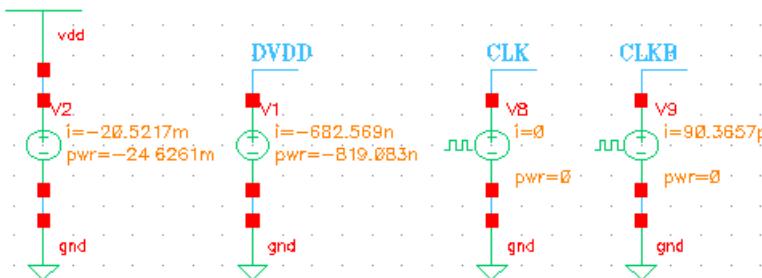


Figure 53: Power Consumption

Comparison 6: Area of the scaled design is:

CURRENT SOURCE (nm)			
MOS	W	L	AREA
M1	8000	45	360000
M2	8000	45	360000
MB2	21300	1920	40896000
MB4	21300	1920	40896000
TOTAL AREA E-18		82512000	
TRANSMISSION GATE (nm)			
MOS	W	L	AREA
NMOS	210	45	9450
PMOS	210	45	9450
TOTAL AREA E-18		18900	
INVERTER(nm)			
MOS	W	L	AREA
NMOS	315	45	14175
PMOS	430	45	19350
TOTAL AREA E-18		33525	

BUFFER				BUFFER bar			
PMOS	W	L	AREA	PMOS	W	L	AREA
1	500	45	22500	1	500	45	22500
2	1360	45	61200	2	1360	45	61200
3	3700	45	166500	3	3700	45	166500
4	10060	45	452700	4	10060	45	452700
5	27370	45	1231650	5	27370	45	1231650
6	74440	45	3349800	6	65010	45	2925450
NMOS	W	L	AREA	NMOS	W	L	AREA
1	315	45	14175	1	315	45	14175
2	855	45	38475	2	855	45	38475
3	2330	45	104850	3	2330	45	104850
4	6340	45	285300	4	6340	45	285300
5	17240	45	775800	5	17240	45	775800
6	46900	45	2110500	6	46900	45	2110500
TOTAL AREA E-18		8613450	TOTAL AREA E-18		8189100		
AREA OF DAC							
COMPONENT	AREA	TIMES	TOTAL AREA				
UNIT CELL	82512000	255	210405600000				
CURRENT AOURCE	3785600	1	3785600				
BUFFER	8613450	8	68907600				
BUFFERBAR	8189100	8	65512800				
INVERTER	33525	24	804600				
TRANSMISSION GATE	18900	8	151200				
CLOCK NMOS	14175	16	226800				
TOTAL DAC AREA E-18			21179948600				
AREA IN UM^2			21179.9486				

Figure 54. Area of Updated DAC

Summary of the comparison of original design and final design

Parameters	Original Design	Final Design
Offset error	0.4LSB	0.1567LSB
Full scale error	-0.45LSB	0.7045LSB
Gain error	1.003	1.0021
INL (transient analysis)	1.00256LSB	0.2630LSB
DNL (transient analysis)	0.1931LSB	0.0142LSB
INL (rms) (MC simulation)	1.8274LSB	0.2732LSB
DNL (rms) (MC simulation)	0.6142LSB	0.0315LSB
Frequency <100MHz (SFDR, SNDR and ENOB) f = 79.58 MHz ,58.1054MHz	53.288024 dBc 46.912123 dB 7.49985 bits	50.3951dBc 45.74dB 7.3063 bits
Frequency >400MHz (SFDR, SNDR and ENOB) f = 401.855MHz	42.681141 dBc 40.165276 dB 6.3791156 bits	44.3429 dBc 40.20 dB 6.471 bits
Power consumption	24.4124mV	24.6226mV
Area	587.89669μm ²	21179.9486 μm ²

Table 15: Original Design v/s Final Design of Binary DAC

PART 4

BONUS

Choose any one of the following reference papers and implement the idea on your DAC. You may choose to refer any other research paper on DAC published in JSSC with prior approval from your TA.

1. [Klass Bult Paper](#) : Klass Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6 mm² "
2. [Calibration Technique](#) : Groeneveld, "A Self-Calibration Technique for Monolithic High-Resolution"
3. [OIC concept](#) : Tai-Haur Kuo, "A 0.07- mm² 162-mW DAC Achieving >65 dBc SFDR and < 70 dBc IM3 at 10 GS/s With Output Impedance Compensation and Concentric Parallelogram Routing"
4. [DEM](#) : Richard Carley, "A Noise-Shaping Coder Topology for 15+ Bit Converters"

CRITERIA FOR EVALUATION

Part (a). Explain in detail the key problem addressed in the research paper and the proposed solution by the authors.

Reference paper used

1. Klass Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6 mm² "
2. Mr. Ganesa H.S. "A 8-Bit Hybrid Architecture Current-Steering DAC"

In the above papers, Current Steering DAC is described with optimized performance for frequency domain applications. For understanding the problem with binary DAC take our 8-bit Binary DAC for explanation. Binary DAC is simple, no decoding logic required. But Drawbacks are like major bit transitions e.g. (0111111 → 10000000) current sources of MSB need to match with rest LSB current sources within 0.5 LSB. This is difficult compensate. From Part 3 report Figure 4 you can see spike of greater than 0.5 LSB. Likewise, there are other similar spike when (XXXX0111 → XXXX1000) sub-mid transitions. This mismatching is never good when we are designing for lots of DAC ICs. There is statistical spread of such parameters. It also affects monotonic characteristics of DAC. This problem is severe as we move from LSB to MSB. Resulting Differential Non-linearity (DNL). Other than this problem there is charge injection and clock-feedthrough problem in switching transistors. Which results in glitches in output.

In the binary DAC switching errors are depends on weight of the digital input. For example, if input changes from 00000001 to 11000000 there is switching of 191 current elements. In the segmented DAC switching of maximum 9-to-10-unit cell. Causes lowers the errors because of switching. In Part 3 of project, we calculated the area requirement of Binary 8-bit DAC 845 μm². Solution proposed by the paper is elegant. We divide the digital bits into two parts. As we know DNL is depends on the weightage of the bits we tried to develop code with equal weightage. In this paper goal is improve the static and dynamic performance while using effective switching network so we are using thermometer code.

001	0000001	101	0011111
010	0000011	110	0111111
011	0000111	111	1111111
100	0001111		

Table 16: Binary to thermometer code conversion

It is simple but effective method all the thermometer code has equal weightage. Switching error significantly lowered. In our case we divide the input 2 section. Lower bits b_0 and b_1 to the binary DAC. Higher bits from b_2 to b_7 to binary to thermal code converter. Only error present when switching happens from binary DAC to thermal DAC. Because of delay is not matched. Area is less than binary DAC. DNL and INL is improved. SFDR and ENOB is improved.

Decoding logic and conversion is complex because delay matching is important task in the thermometer DAC.

Part (b). Implement the proposed idea using MOSFETs or Verilog-A blocks. (Note: Verilog-A implementation would be awarded 0.5X Marks)

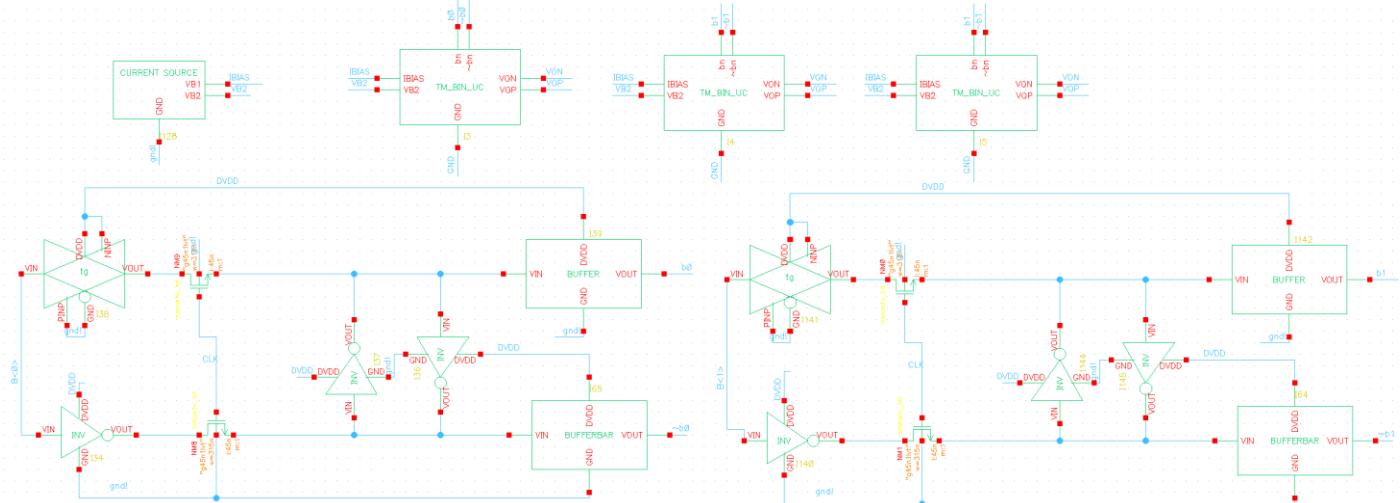
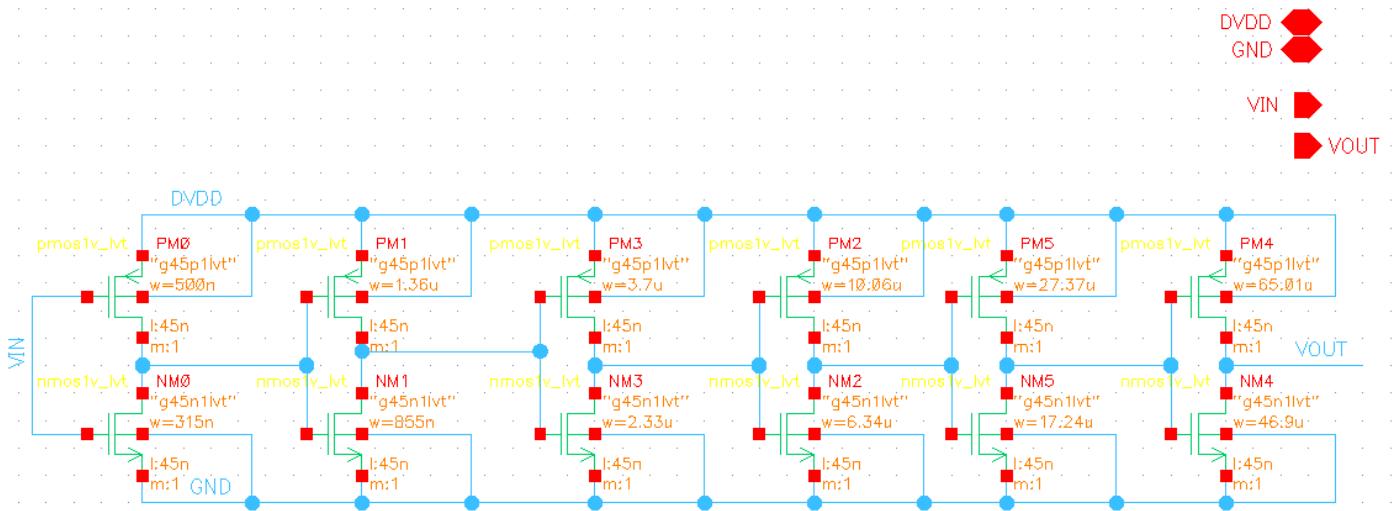


Figure 55: 2-bit BINARY part of segmented DAC



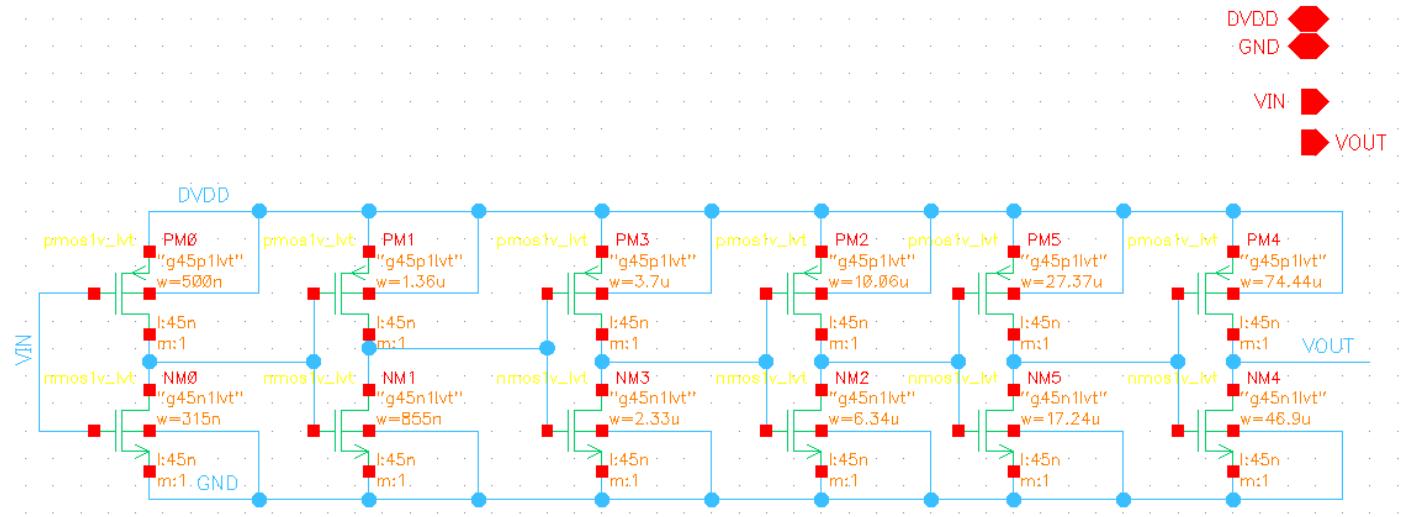


Figure 56: Buffers to derive signals \bar{b}_n and b_n

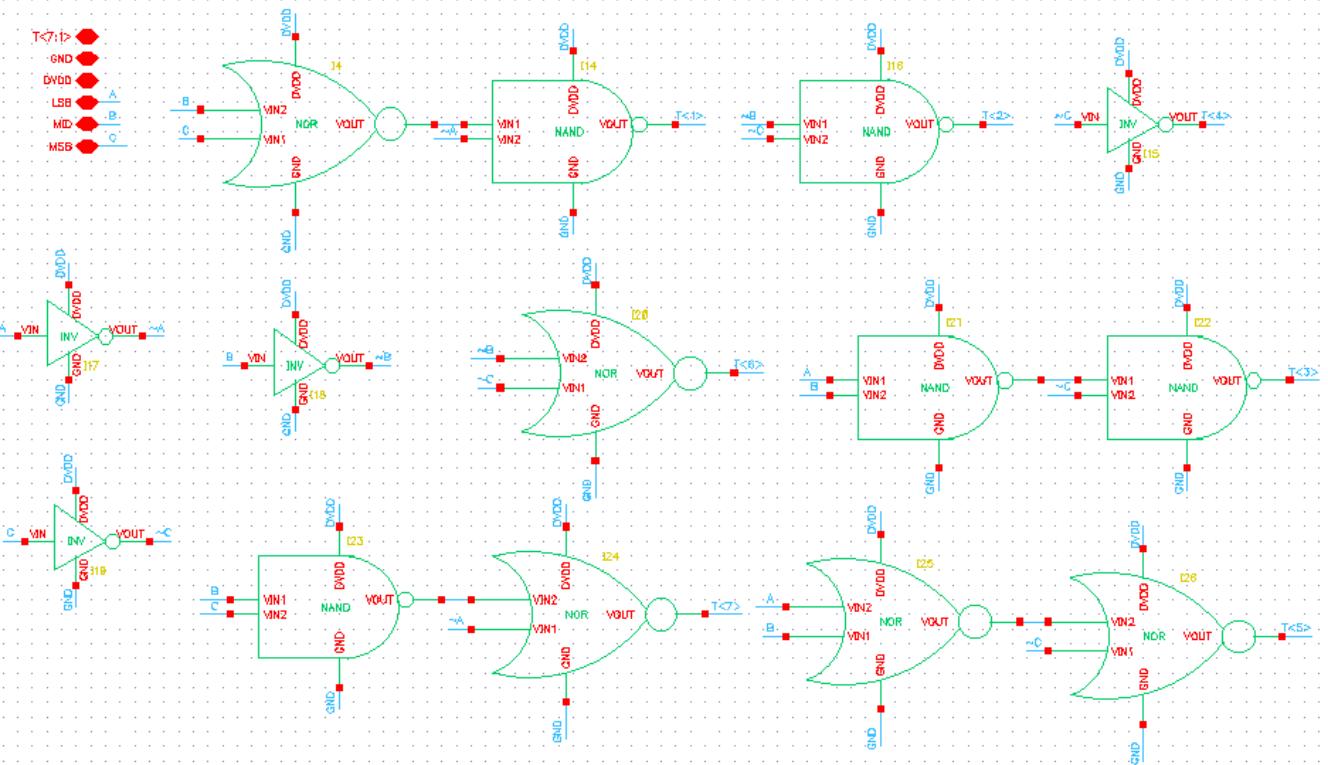


Figure 57: Binary to thermometer code converter:

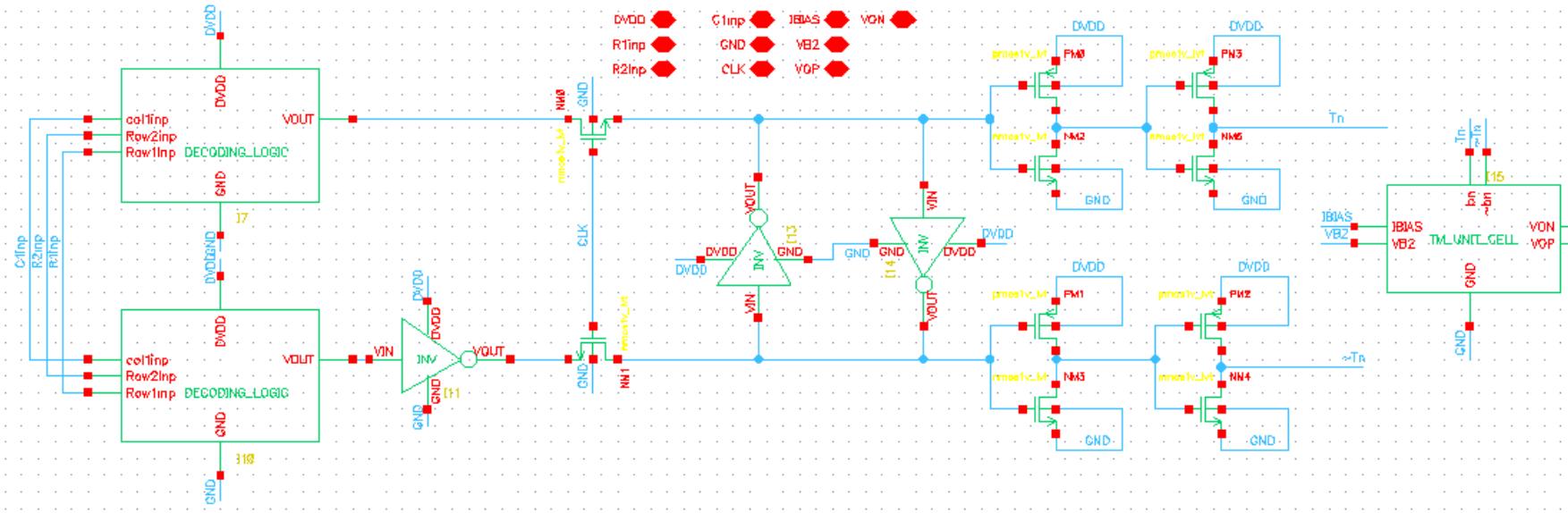


Figure 58: Unit cell of Thermometer DAC

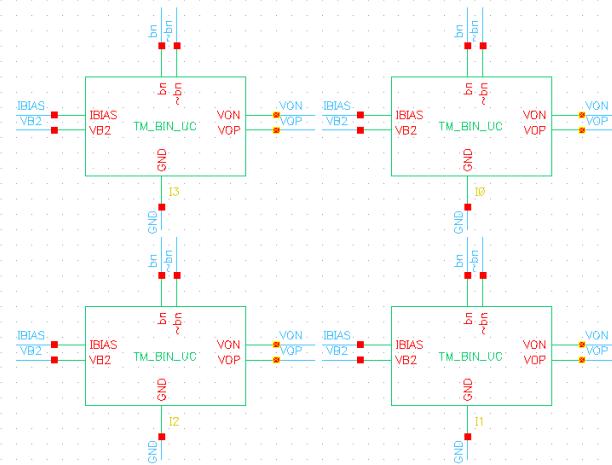


Figure 59: Thermo current cell

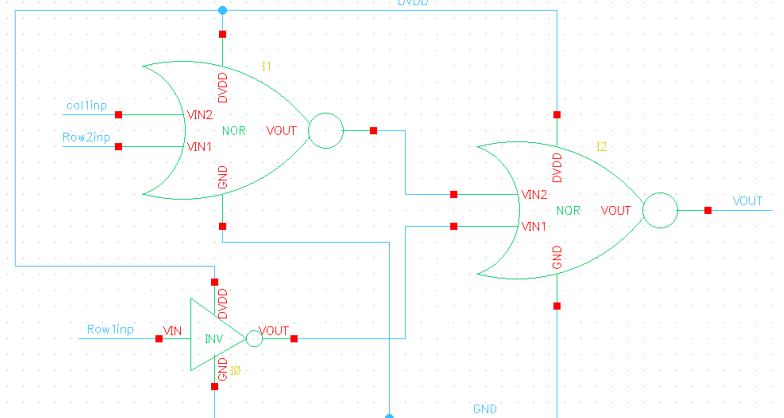


Figure 60: Decoding Logic

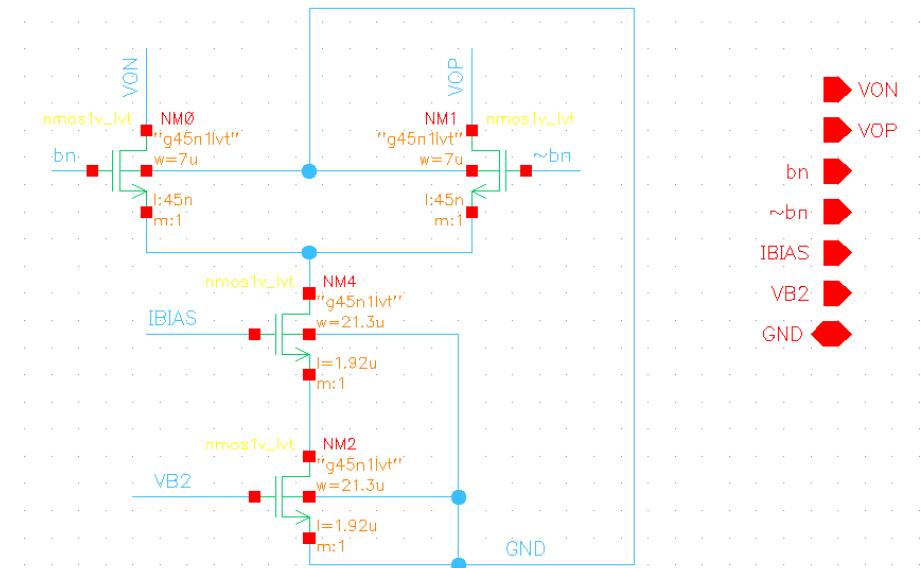


Figure 61: Binary Unit cell

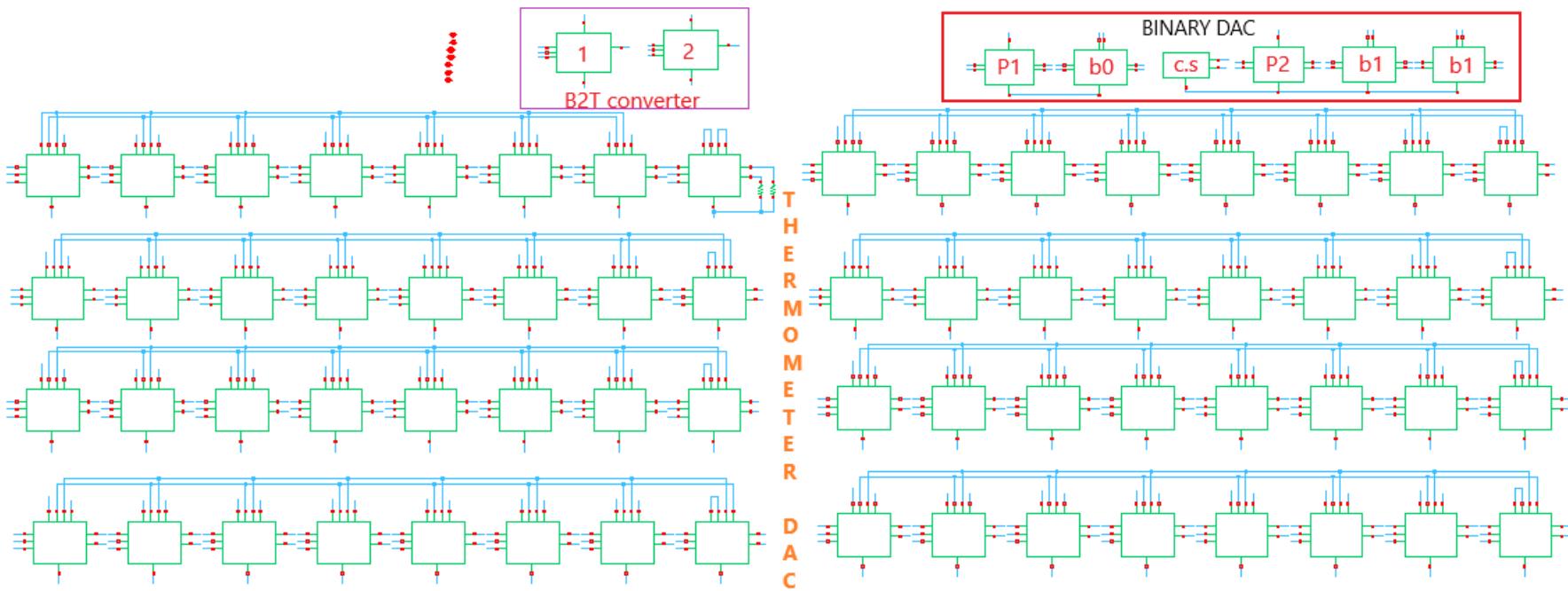


Figure 62: Final Schematic of DAC

Part (c). Show improvement in results static (INL/DNL) and(or) dynamic performance (SFDR) metrics as compared to the results reported in Part 3.

Perform the transient analysis for a ramp binary input and report the differential output annotated with maximum and minimum voltage. Also, report a zoomed-in image of the output around 0V output annotating the unit step size. Write your observations.

ANS:

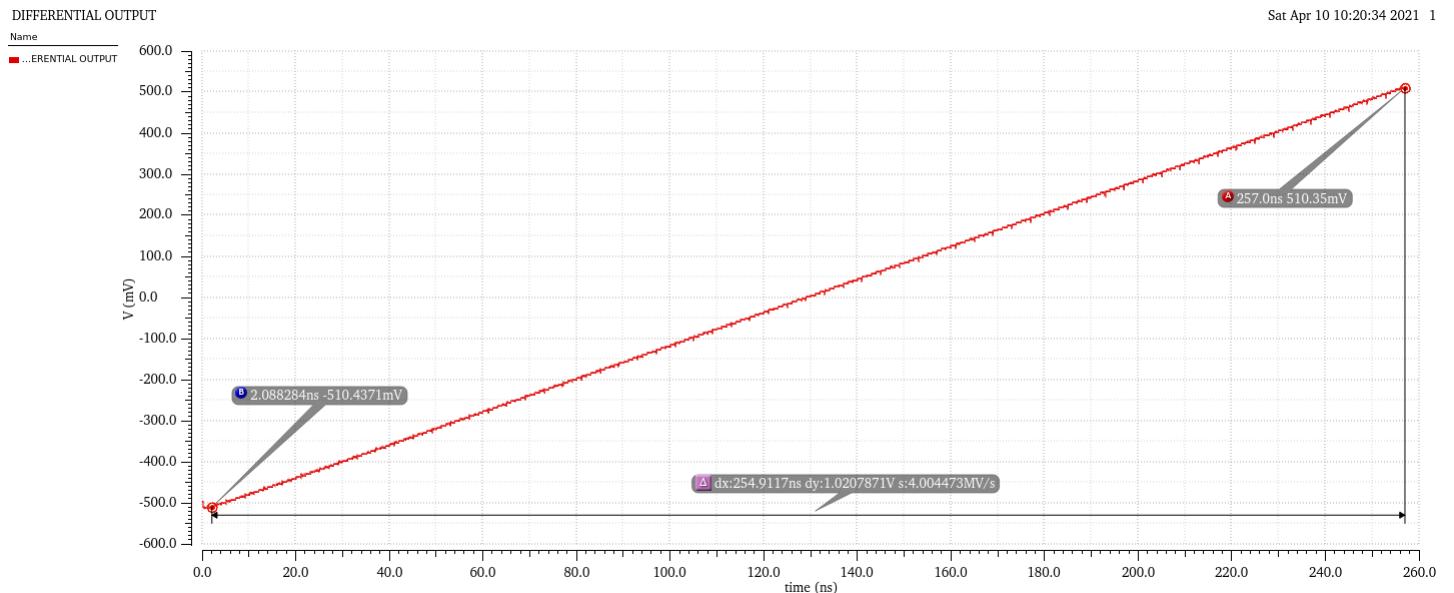


Figure 63: DAC with Maximum and Minimum Output

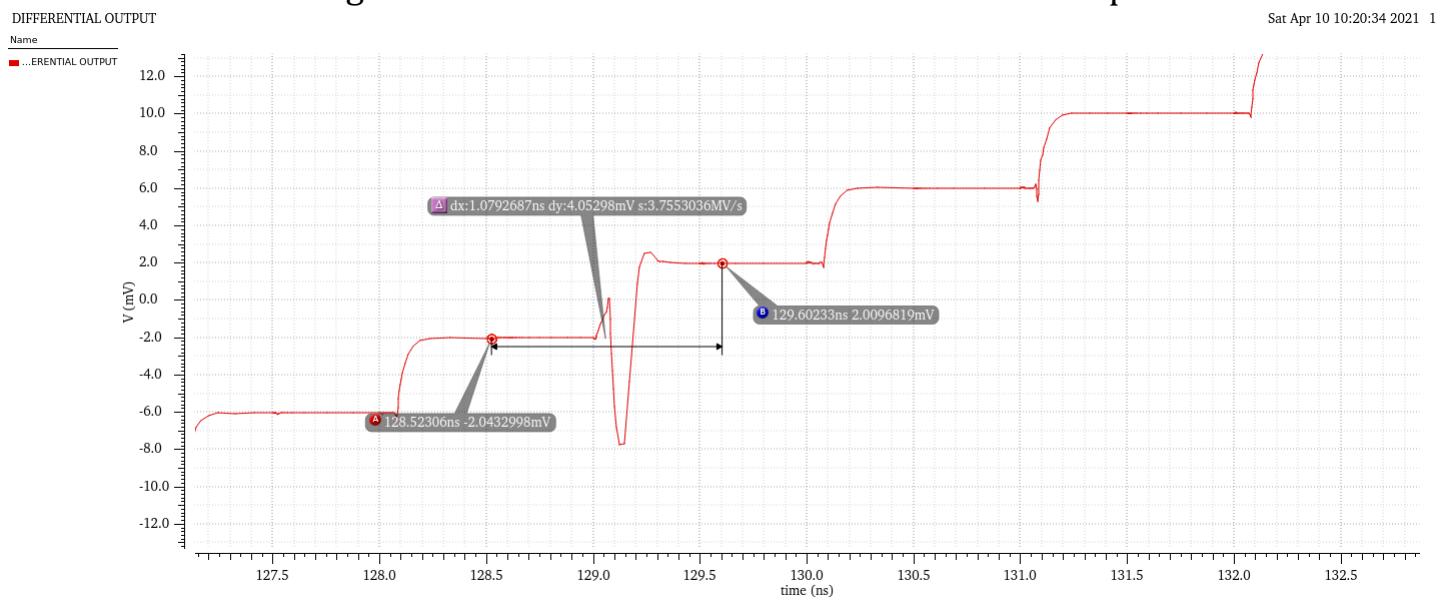


Figure 64: Zoomed Portion near 0V and step size

Observation: negative spikes are seen when there is transition from Binary count to Thermometer count $000\ 000\ 11 \rightarrow 000\ 001\ 00$ (thermometer code $0000000\ 0000001\ 00$)

Tabulate the offset, full scale error, gain error and plot the DNL and INL for the output obtained in Part(b) above.

ANS:

Ideal DAC output is determined using cadence calculator.

Offset, Full scale, gain error is determined using MATLAB code and data exported from cadence.

OFFSET Error	-0.4371mV	-0.109LSB
FULL SCALE Error	0.2462mV	0.08LSB
GAIN Error	1.0007	-

Table 17: Static Performance of Segmented DAC

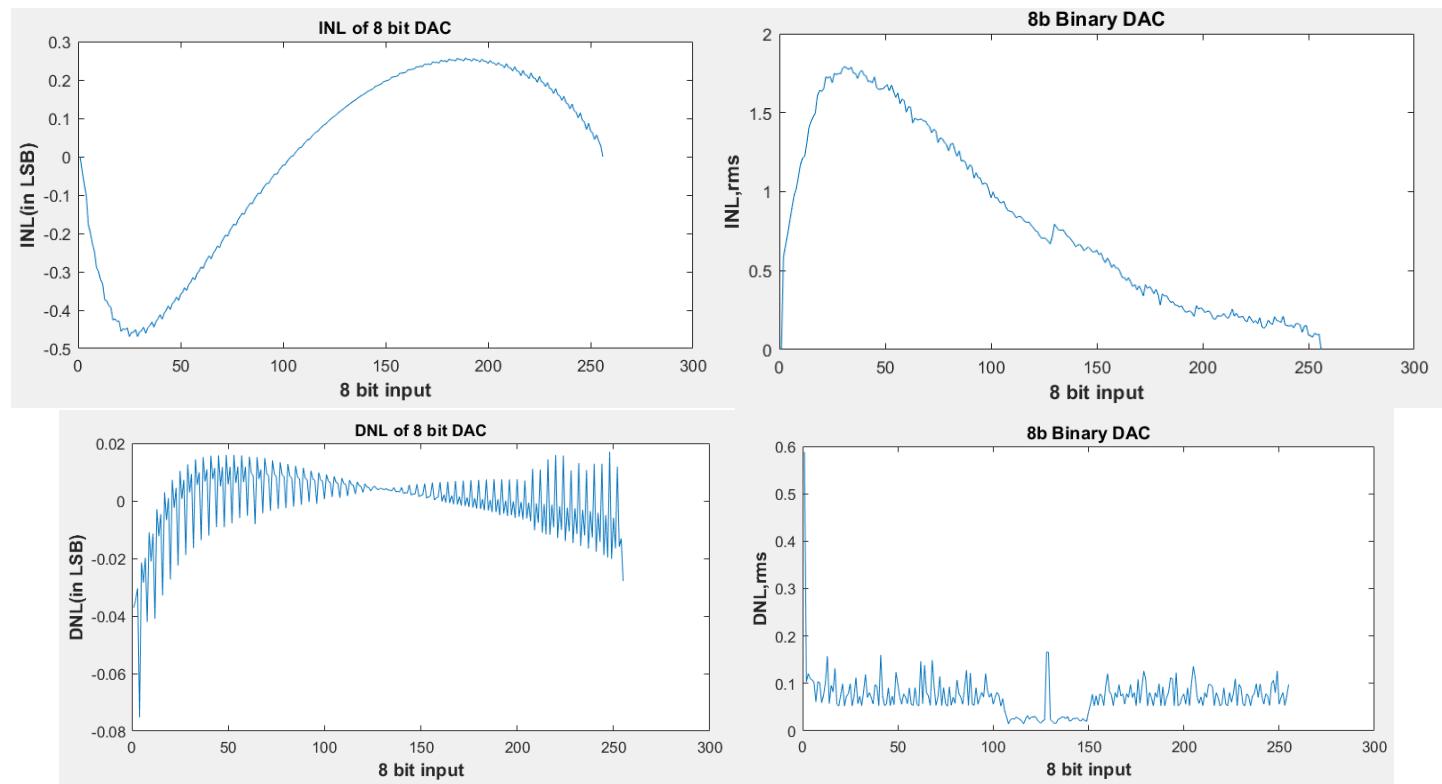


Figure 65: INL and DNL for Ramp input to DAC

Perform 100 Monte-Carlo simulations. Report the mean and standard deviation of unit current I_{LSB} . Plot the aggregate root-mean square(rms) DNL and INL values. Report the maximum INL_{rms} and DNL_{rms} . Calculate the theoretical expected INL_{rms} and DNL_{rms} . Explain your observations.

ANS:

For unknown reasons couldn't perform Monte-Carlo simulation for 8 jobs.

Performed Monte-Carlo for 8 jobs.

Mean of unit current $I_{LSB} = 78.62\mu A$; Standard deviation (σ) = $9.327\mu A$

INL_{rms} and DNL_{rms} determined using MATLAB code.

Maximum $INL_{rms} = 1.0290LSB$

Maximum $DNL_{rms} = 0.1185LSB$

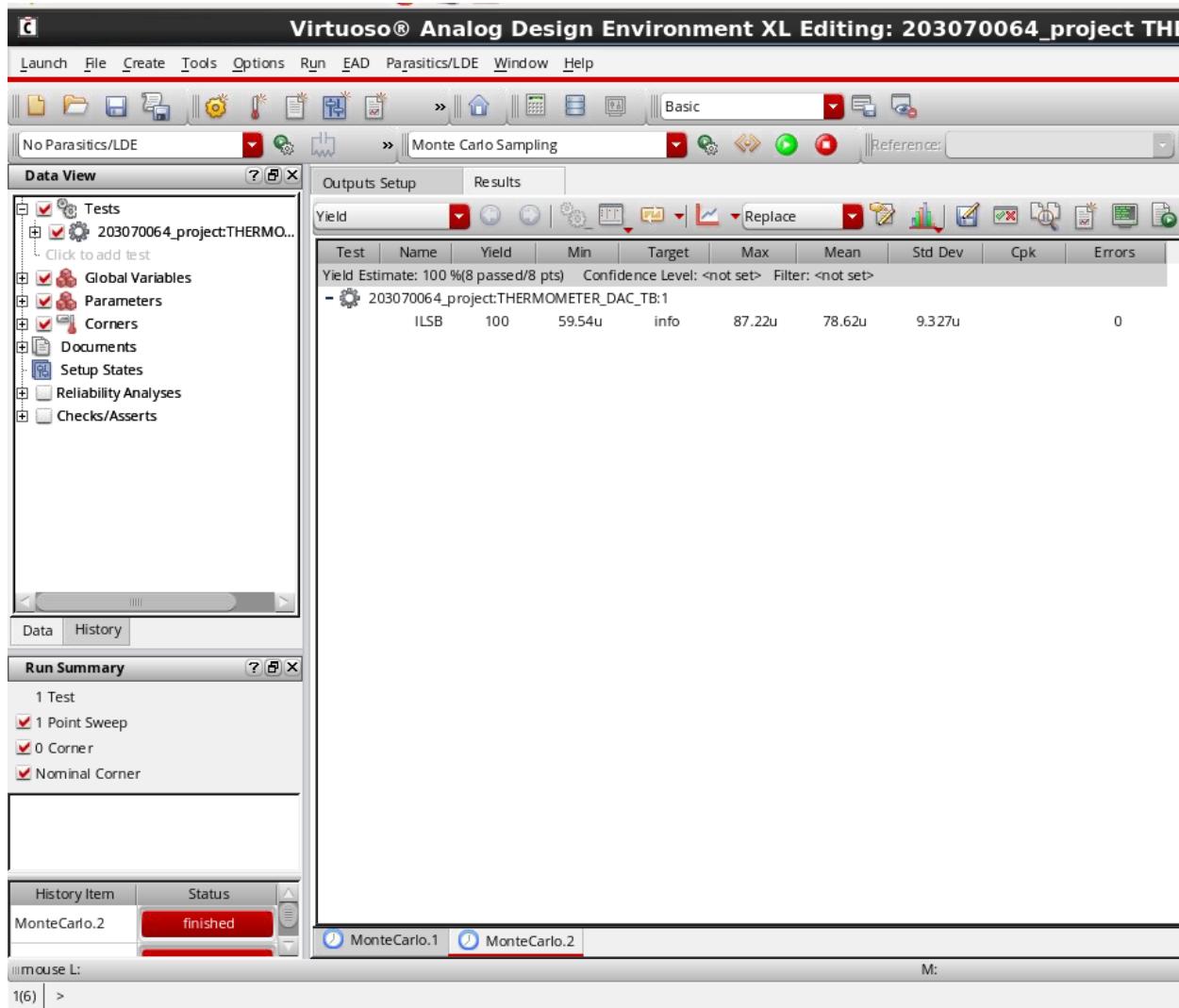


Figure 66: Monte-Carlo Simulation

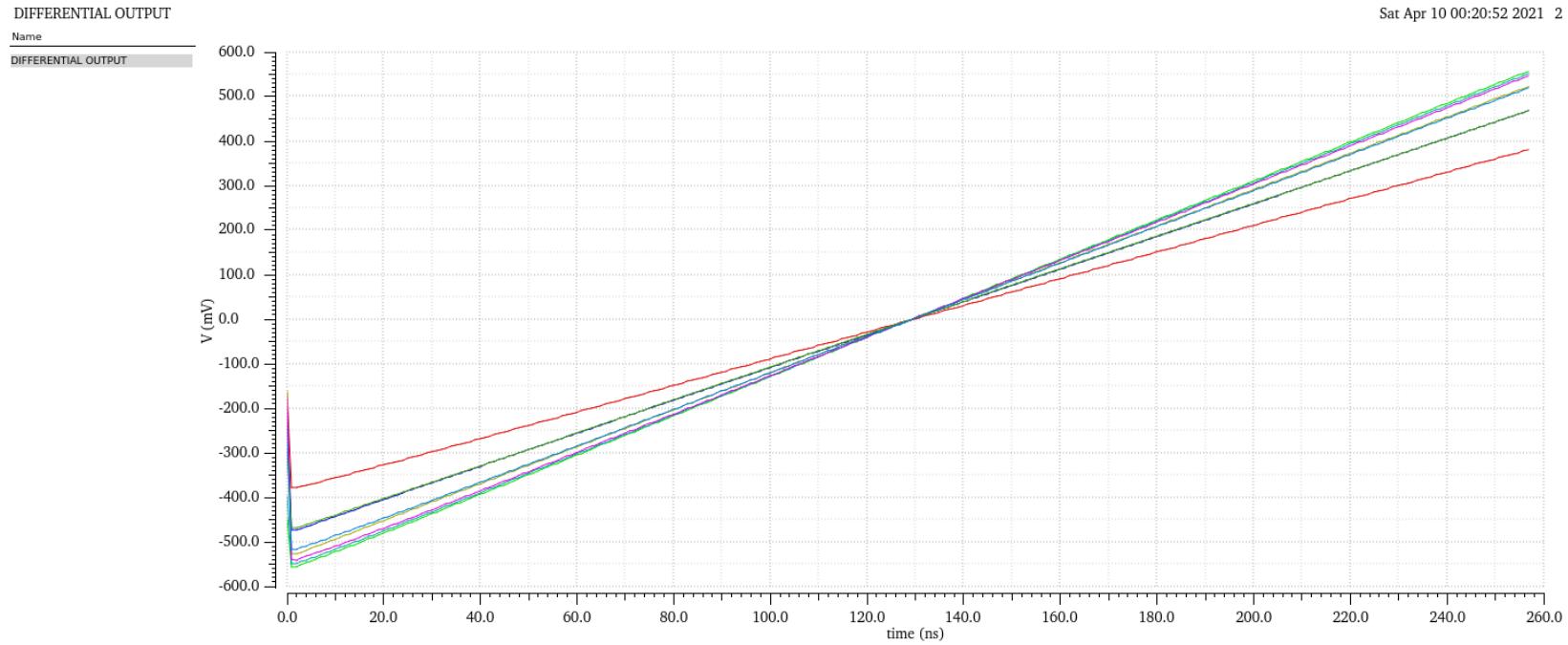


Figure 67: Differential Output from MC Simulation

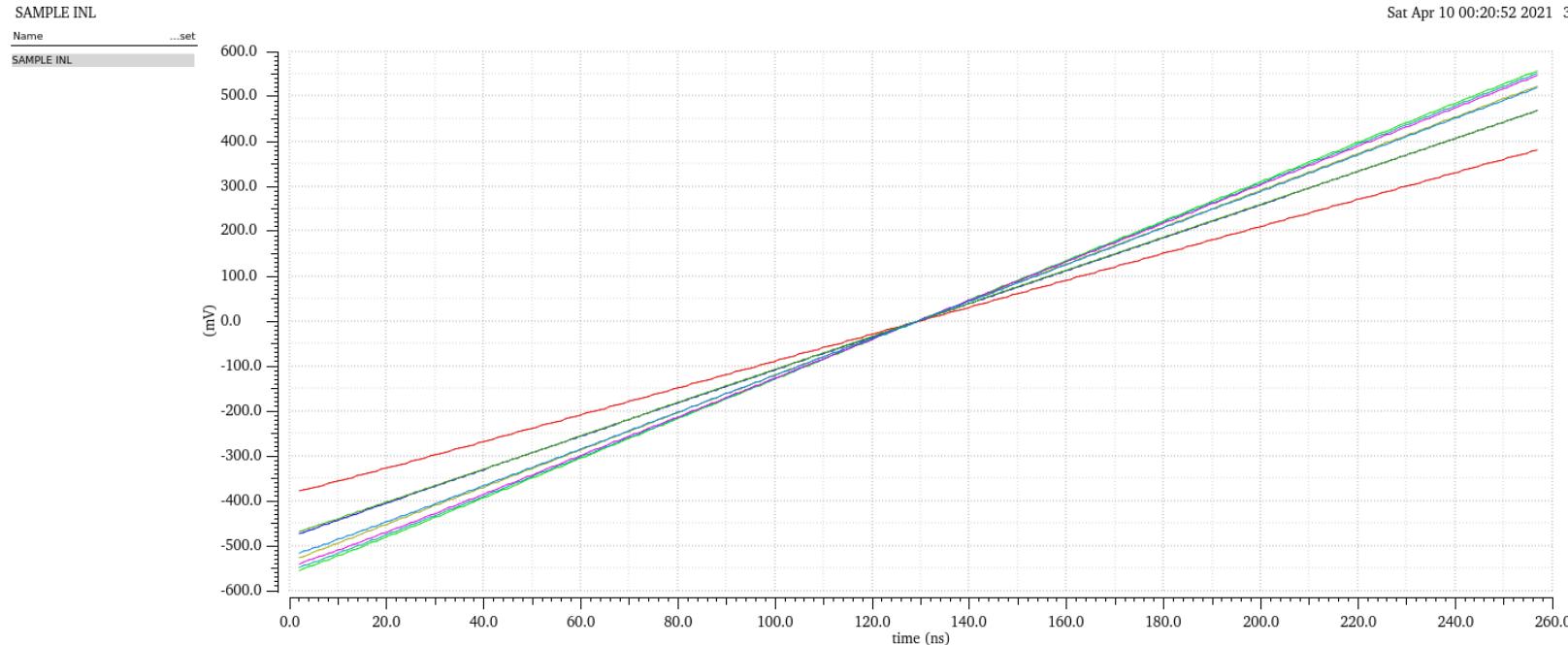


Figure 68: SAMPLE INL results from MC Simulation

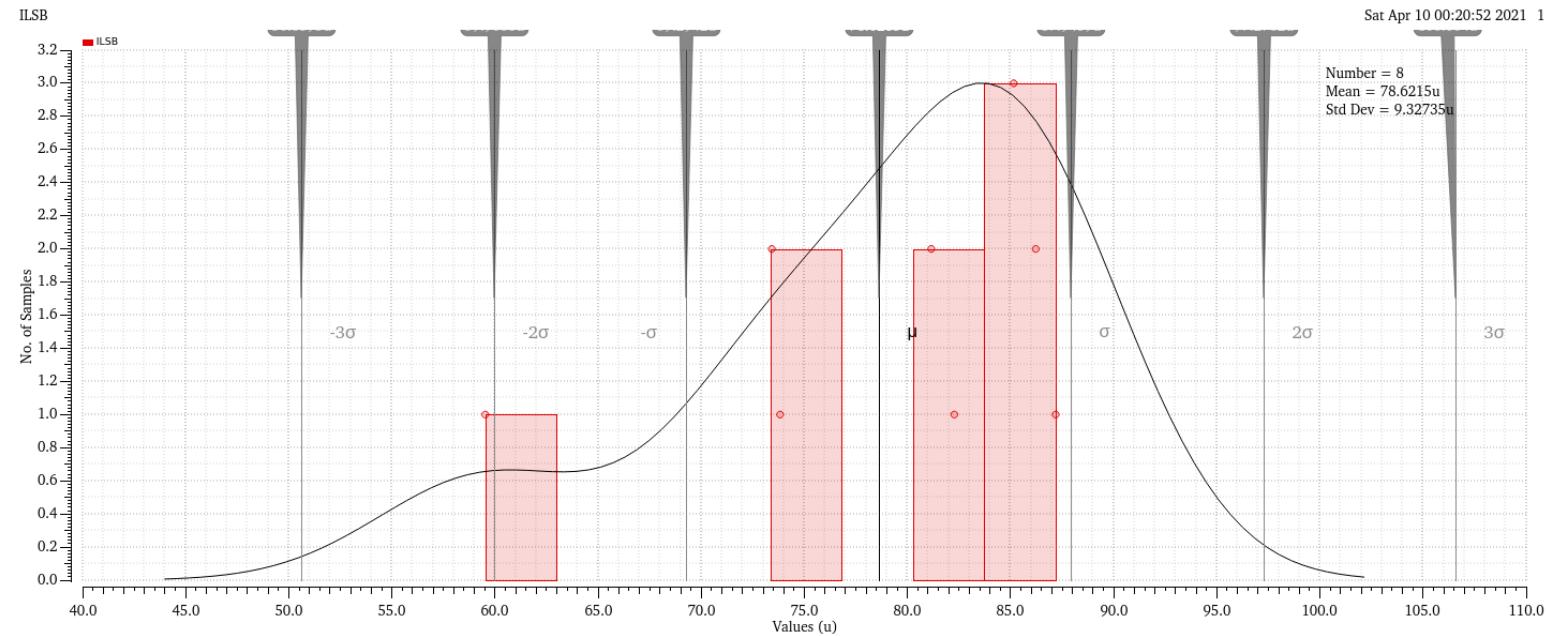


Figure 69: I_{LSB} Distribution for 8 jobs in MC Simulation

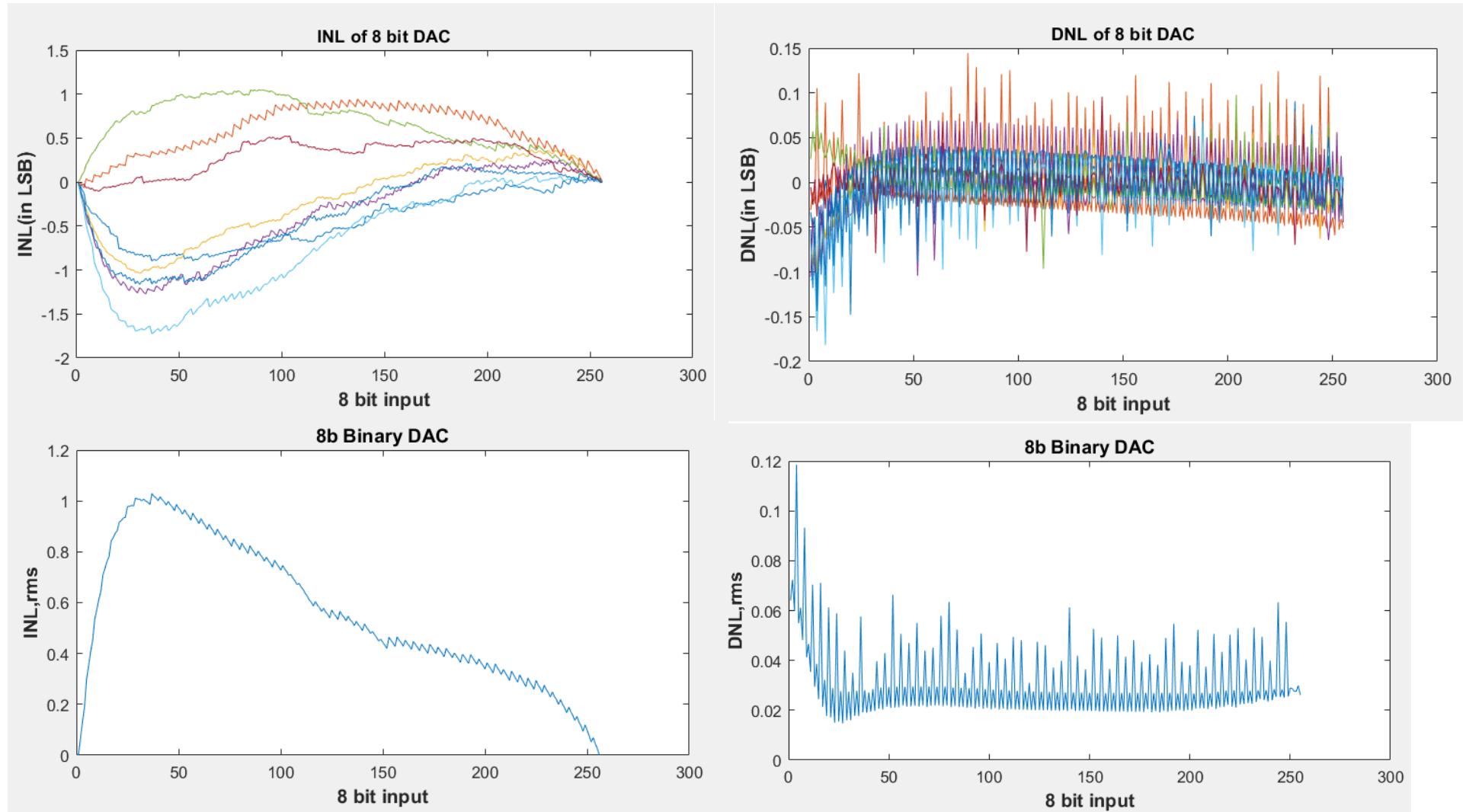


Figure 70: MATLAB simulation for INL_{rms} and DNL_{rms}

Provide a sinusoidal input of frequency < 100MHz and plot 2048-point FFT Spectrum. Mark the fundamental and the subsequent harmonic frequency peaks in the spectrum. Explain the observations and possible reason behind the harmonic frequencies.

ANS:

Input frequency is 73.73 MHz < 100 MHz

Due to circuit mismatches, there is noise in circuit. This noise appears near the harmonic frequencies. One of the possible reasons will be correlation of the input and noise.

Code dependent glitches also causes the harmonic distortion.

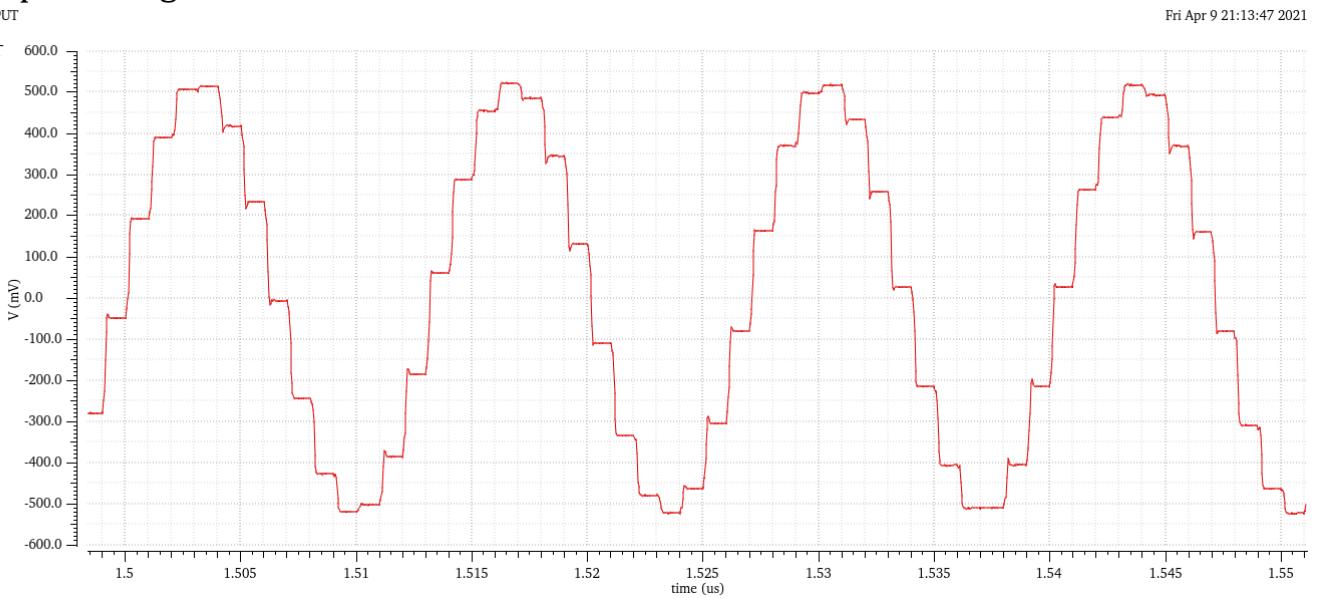


Figure 71: DAC output for 73.73MHz sinusoidal input

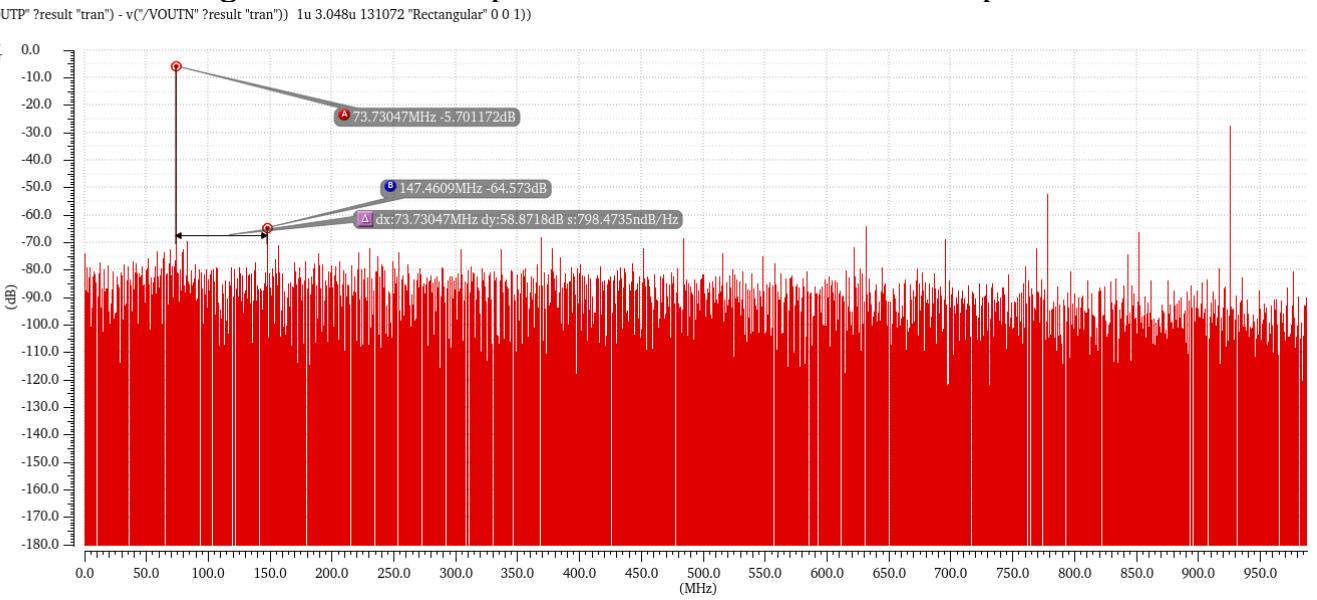


Figure 72: DAC frequency spectrum for 73.73MHz Sinusoidal Input

Provide a sinusoidal input of frequency > 400MHz and plot 2048-point FFT Spectrum. Mark the fundamental and the subsequent harmonic frequency peaks in the spectrum. Explain the observations and possible reason behind the harmonic frequencies.

ANS:

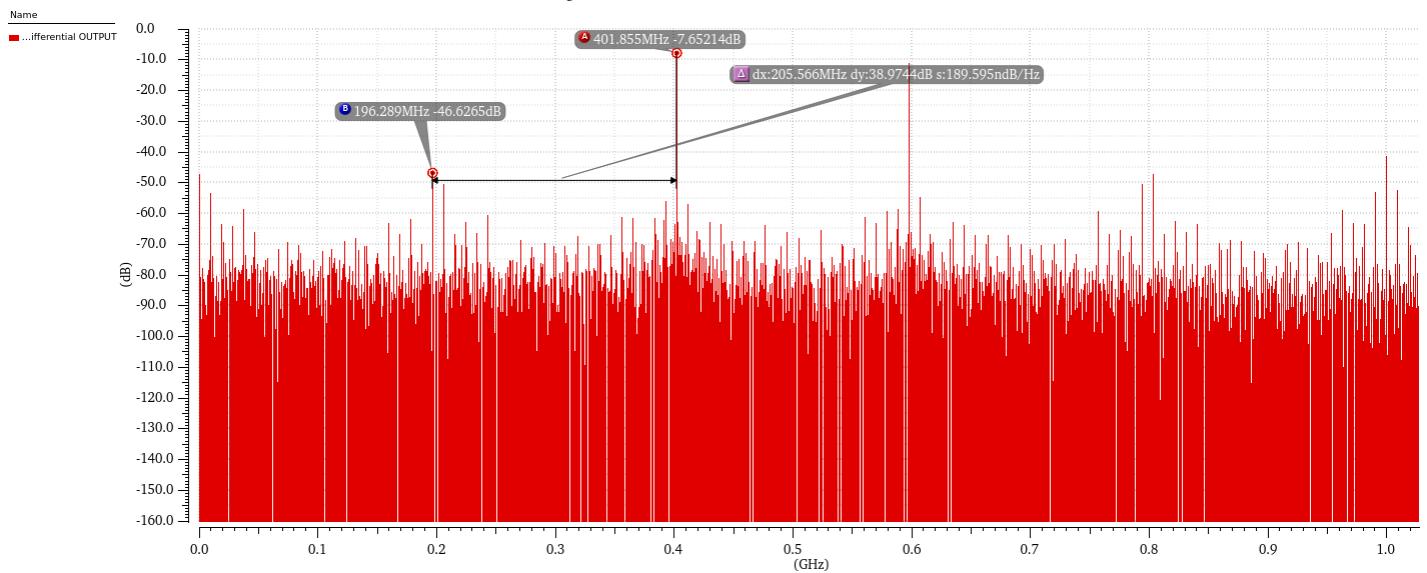
Input frequency 401.855MHz > 400MHz

For this input frequency time period is 2.488ns and clock time period is 1ns.

Input is very fast. DAC couldn't detect intermediate values of input. Therefore, high distortion is seen at output. As distortion is high, more harmonic frequency will be present.

db20(dft((v("VOUTP") ?result "tran") - v("VOUTN") ?result "tran")) 1u 3.048u 131072 "Rectangular" 0 0 1)

1



Sat Apr 10 18:15:29 2021 1

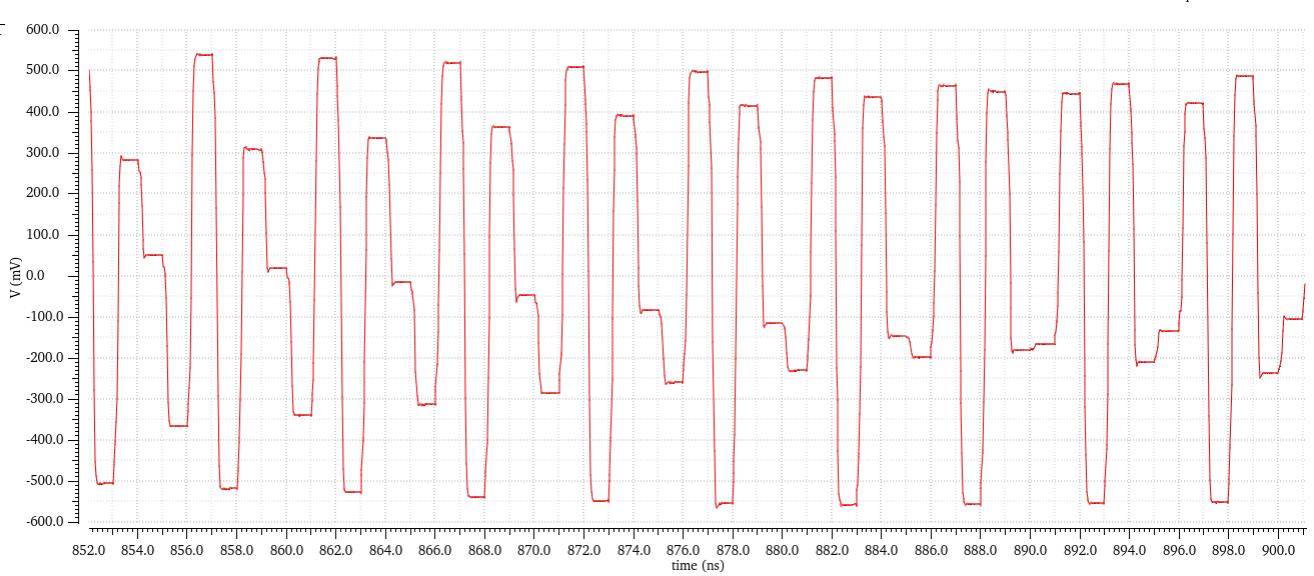
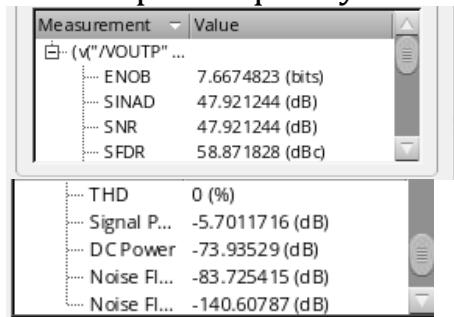


Figure 73: DAC output for 401.855MHz Sinusoidal input

Following Images for the dynamic characteristics:

1. Input frequency 79.58MHz



2. Input frequency 401.855MHz

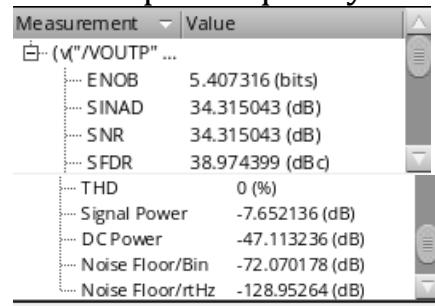


Figure 74: snapshots of ENOB, SFDR and SND

Tabulate the simulated dynamic performance characteristics (SNDR, SFDR, ENOB) of your DAC in Part(e) and Part(f).

	Input Frequency 79.58MHz	Input Frequency 401.855MHz
SNDR (dB)	47.92	40.165276
SFDR (dBc)	58.87	42.681141
ENOB (bits)	7.66748	6.3791156

Table 18: Dynamic Performance of Segmented DAC

Report the total power consumption (digital + analog) of your 8-bit DAC.

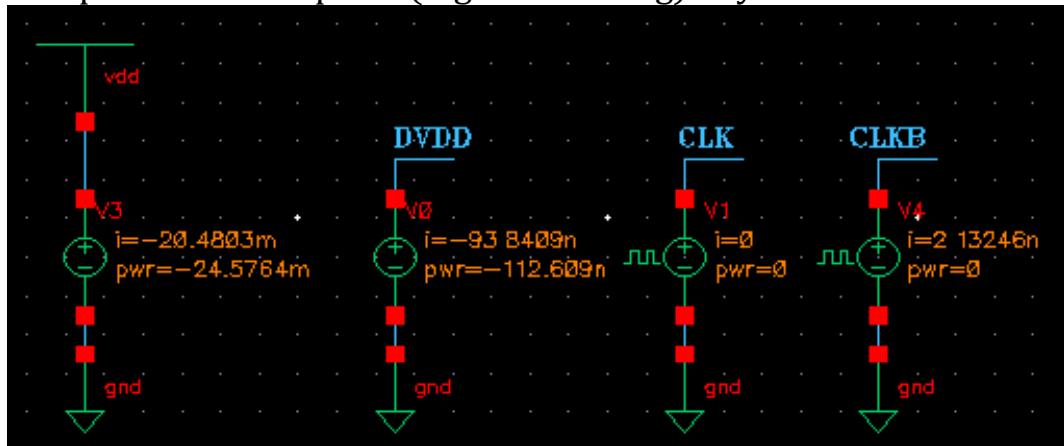


Figure 75: Power consumption

Total Power consumption will be 24.576mW

Report the total area (digital + analog) of your 8-bit DAC.

BINARY UNIT CELL			
MOS	W	L	AREA
M1	4405	45	198225
M2	4405	45	198225
MB2	1400	120	168000
MB4	1400	120	168000
TOTAL AREA E-18		732450	

CURRENT SOURCE			
MOS	W	L	AREA
MB1	125	65	8125
MB3	125	65	8125
TOTAL AREA E-18		16250	

INVERTER			
MOS	W	L	AREA
MP	200	45	9000
MN	120	45	5400
TOTAL AREA		14400	

TRANSMISSION GATE (nm)			
MOS	W	L	AREA
NMOS	120	45	5400
PMOS	120	45	5400
TOTAL AREA E-18		10800	

DECODING LOGIC			
COMPONENT	TIMES	AREA	TOTAL
NOR	2	46800	93600
INVERTER	1	14400	14400
TOTAL AREA E-18		108000	

BINARY TO THERMO CONVERTER			
COMPONENT	TIMES	AREA	TOTAL AREA
INVERTER	4	14400	57600
NOR	5	46800	234000
NAND	5	39600	198000
TOTAL AREA E-18		489600	

BUFFER			
PMOS	W	L	AREA
1	200	45	9000
2	544	45	24480
3	1479.68	45	66585.6
4	4024.73	45	181112.85
5	0	0	0
6	0	0	0
NMOS	W	L	AREA
1	120	45	5400
2	326.4	45	14688
3	887.808	45	39951.36
4	2414.838	45	108667.71
5	0	0	0
6	0	0	0
TOTAL AREA E-18		449885.5	

BUFFER bar			
PMOS	W	L	AREA
1	200	45	9000
2	544	45	24480
3	1479.68	45	66585.6
4	4024.73	45	181112.85
5	0	0	0
6	0	0	0
NMOS	W	L	AREA
1	120	45	5400
2	326.4	45	14688
3	887.808	45	39951.36
4	2414.838	45	108667.71
5	0	0	0
6	0	0	0
TOTAL AREA E-18		449885.5	

NOR GATE			
MOS	W	L	AREA
MP1	400	45	18000
MP2	400	45	18000
MN1	120	45	5400
MN2	120	45	5400
TOTAL AREA E-18		46800	

THERMO CURRENT CELL				THERMO UNIT CELL				
BINARY UNIT CELL		4	732450	2929800	COMPONENT	TIMES	AREA	TOTAL
NAND GATE					DECODING LOGIC	2	108000	216000
MOS	W	L	AREA		INVERTER	4	14400	57600
MP1	200	45	9000		TRANSMISSION GATE	2	10800	21600
MP2	200	45	9000		CURRENT CELL	1	2929800	2929800
MN1	240	45	10800		MP1	0	19350	0
MN2	240	45	10800		MN1	0	14175	0
TOTAL AREA E-18		39600			MP2	0	166500	0
					MN2	0	104850	0
				TOTAL AREA E-18				3225000

THERMO DAC AREA				
COMPONENT		TIMES	AREA	TOTAL
BINARY UNIT CELL		3	732450	2197350
BUFFER		2	449885.52	899771.04
BUFFEER BAR		2	449885.52	899771.04
INVERTER		6	14400	86400
CLOCK MOS		4	5400	21600
TRANSMISSION GATE		2	10800	21600
CURRENT SOURCE		1	16250	16250
BIN2 THERMP CONV		2	489600	979200
THERMO UNIT CELL		64	3225000	206400000
TOTAL AREA		E-18	211521942.1	
IN UM^2		E-12	211.521942	

Figure 76: Area of the THERMOMETER DAC

How to improve static characteristics and dynamic performance of DAC

As done in early part we can increase area of the tailing current transistor and cascode transistors. It will improve the static performance. But it affects the dynamic performance. For that we need to increase the switching transistors areas. So ultimately need to increase the inverter and transmission gate area. There is major change in segmented DAC than previous one is that we added two stage buffers so that delay is matched between the switching signals. Buffer designed was 4 stage but to match the delay with binary 2bit DAC removed the middle 2 stages of inverter. Therefore, buffer with two stages of inverter.

Which increases area.

Comparison 1: Ramp Input to Segmented DAC

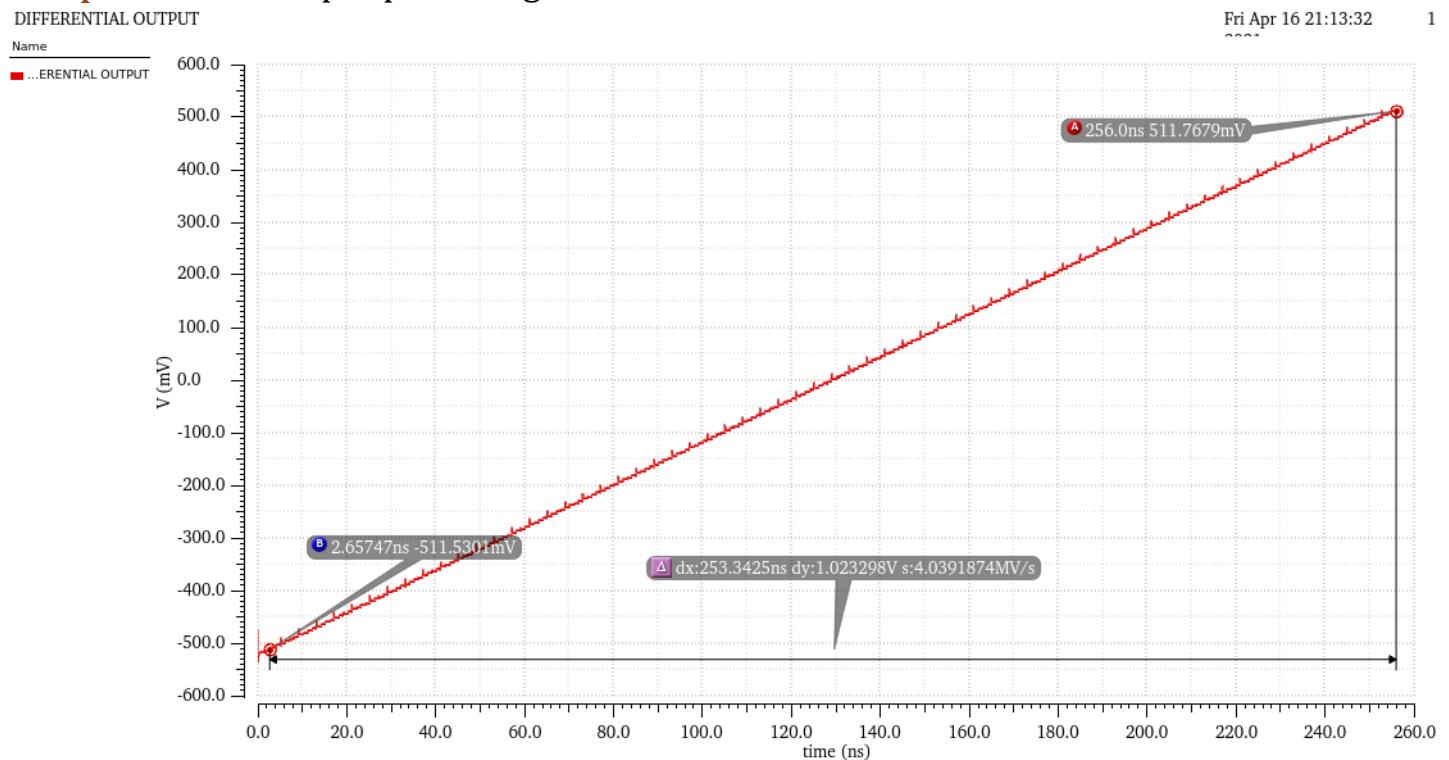


Figure 77: Output result of RAMP input to scaled design to improve INL

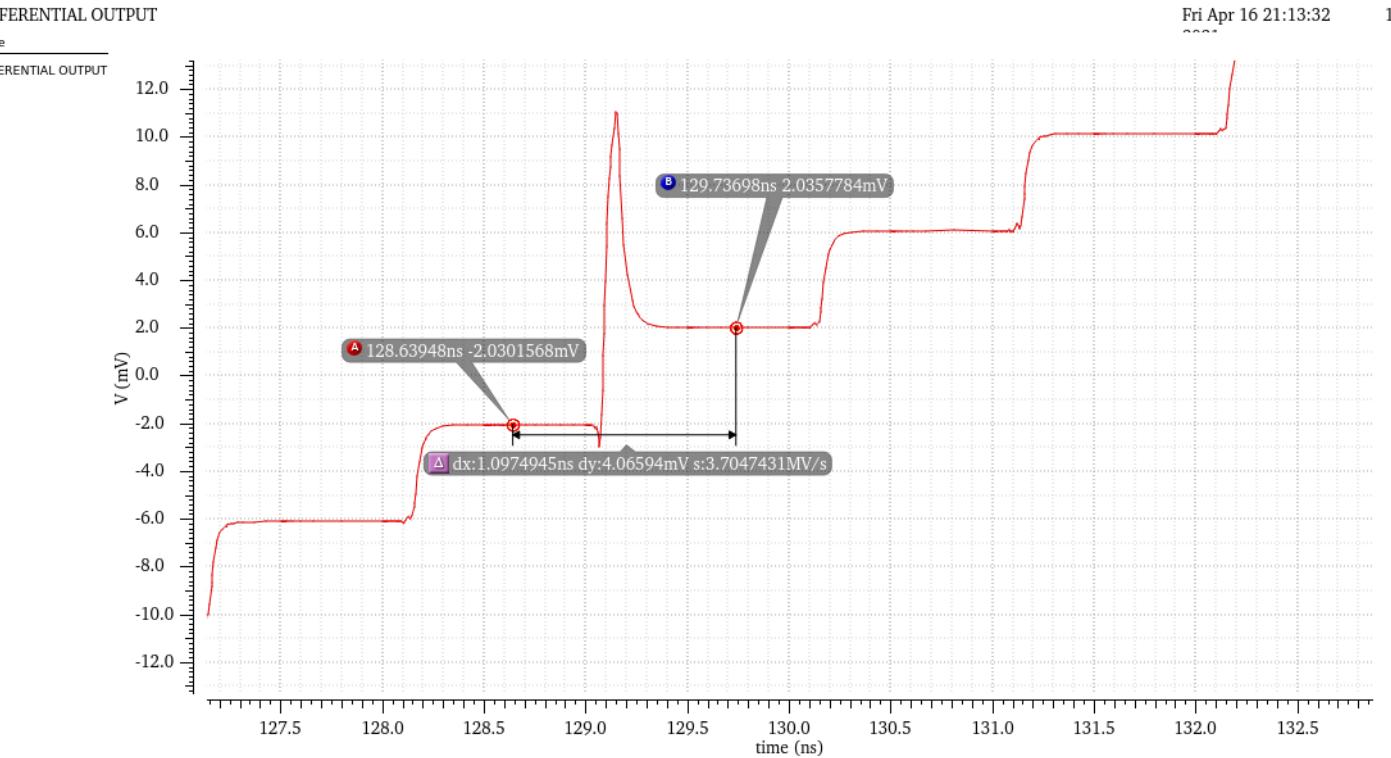
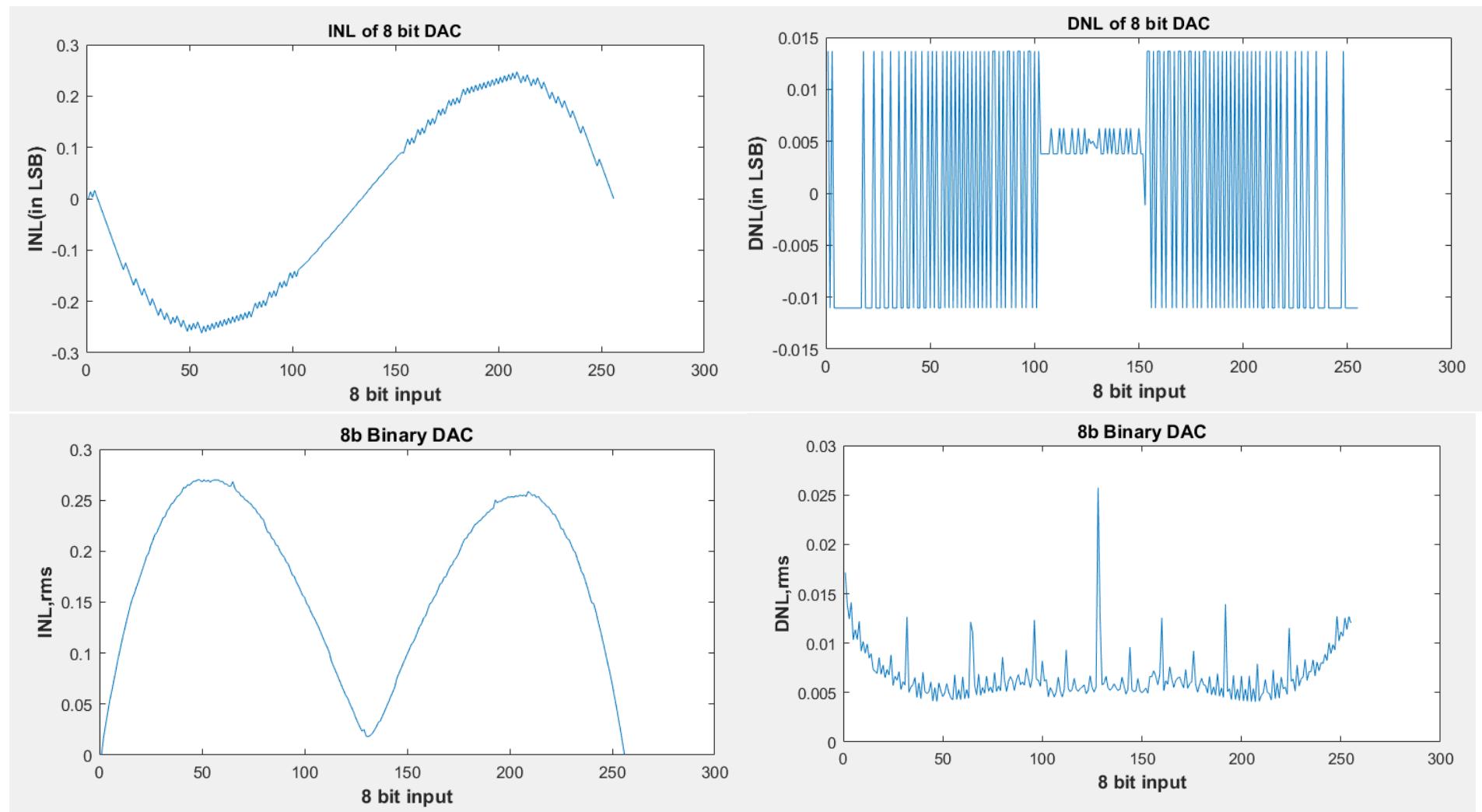


Figure 78: Zero crossing of output

OFFSET Error	-1.53	-0.3825LSB
FULL SCALE Error	1.7679mV	0.4419LSB
GAIN Error	1.0032	-

Table 19: Static performance of Final Segmented DAC



```
>> EE719_INL_DNL
INL and DNL respectively
0.2702
0.0257
```

Figure 79: INL and DNL analysis on single ramp input to scaled design

Comparison 2: Monte-Carlo Simulation



Figure 80: Monte-Carlo Simulation on updated unit cell

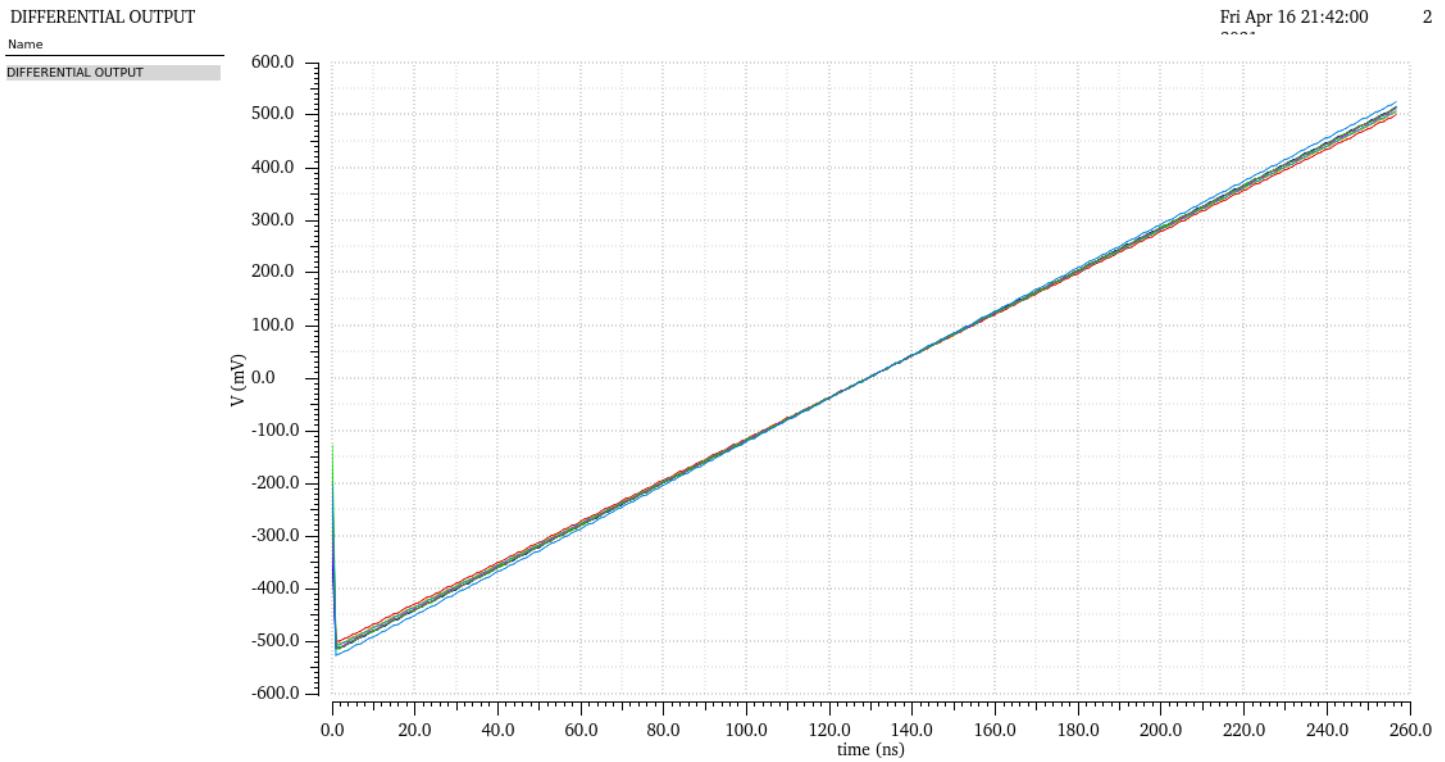


Figure 81: differential output results after MC simulation

SAMPLE INL

Name ...set
SAMPLE INL

Fri Apr 16 21:42:00

3

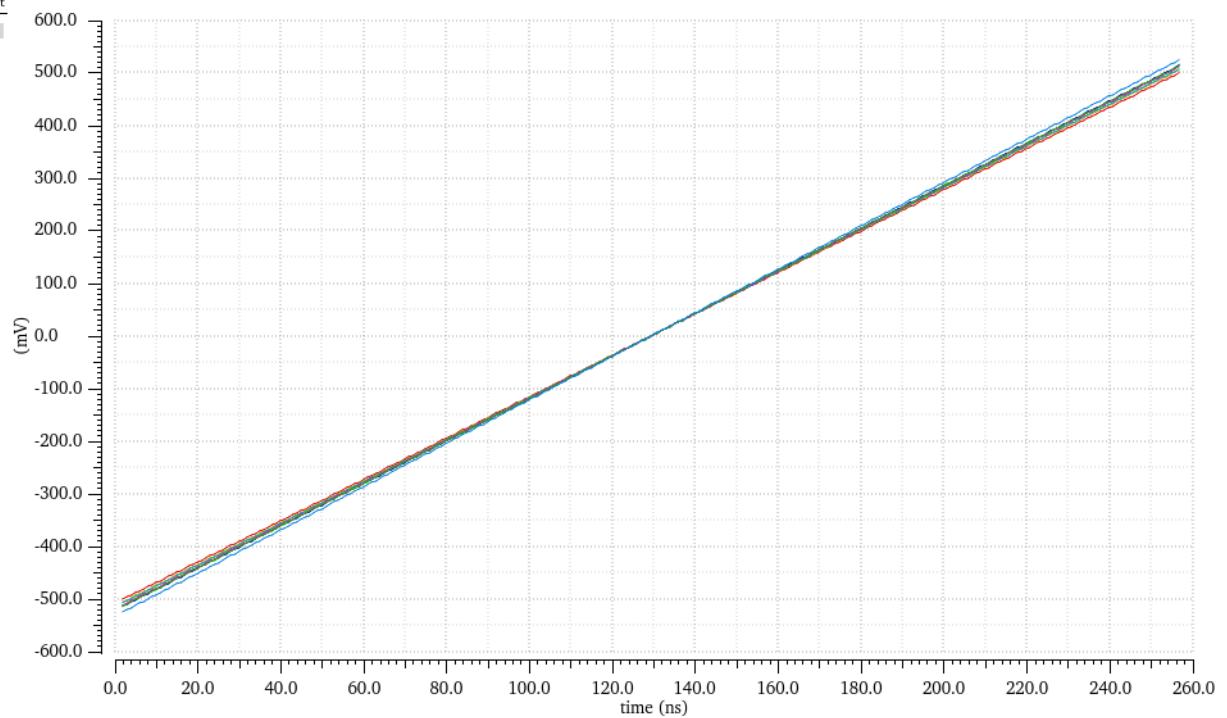
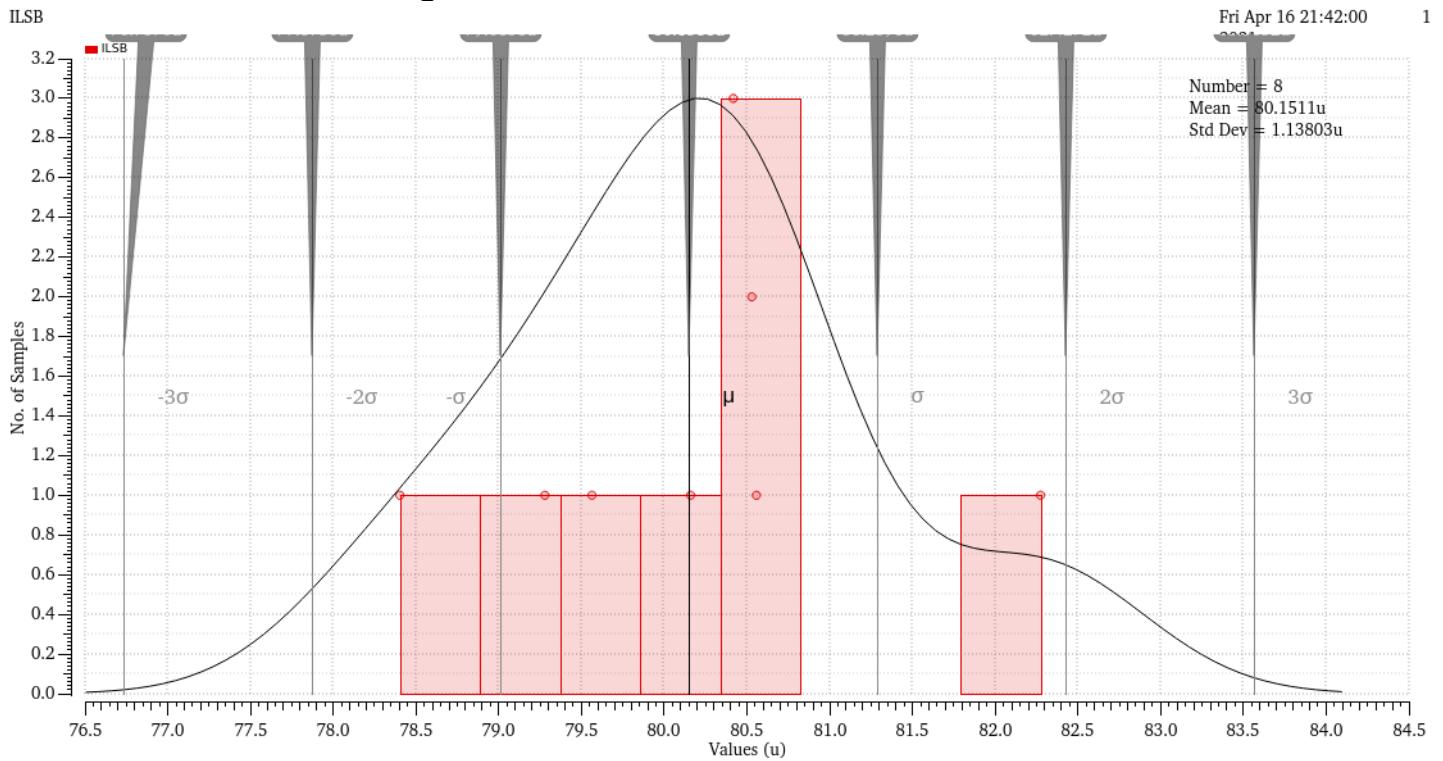
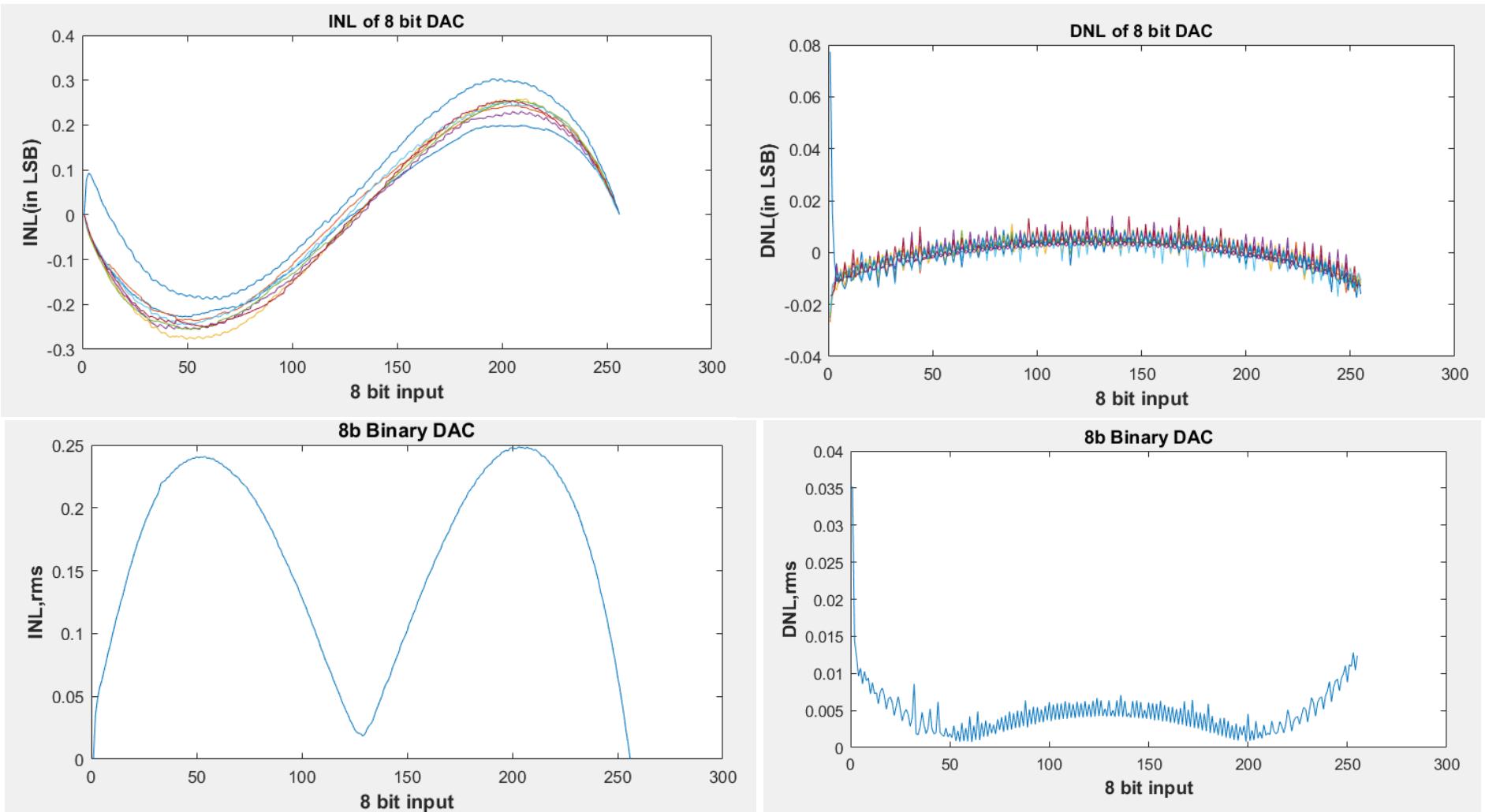


Figure 82: INL results after MC simulation

ILSB

Figure 83: I_{LSB} results after MC simulation



```
>> EE719_INL_DNL
INL and DNL respectively
0.2486
0.0352
```

Figure 84: Improved INL and DNL after scaling the area

Comparison 3: Dynamic Performance

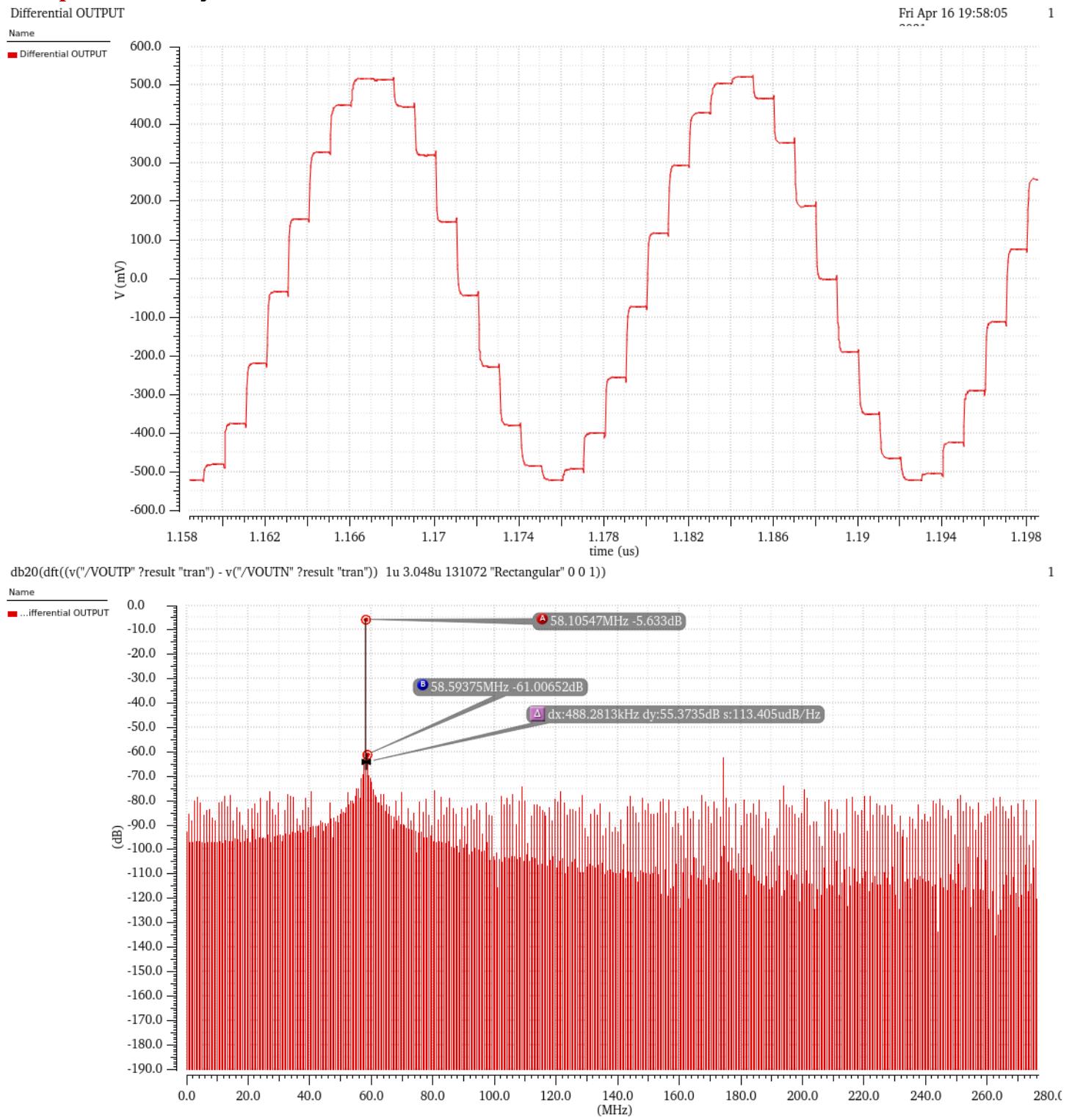
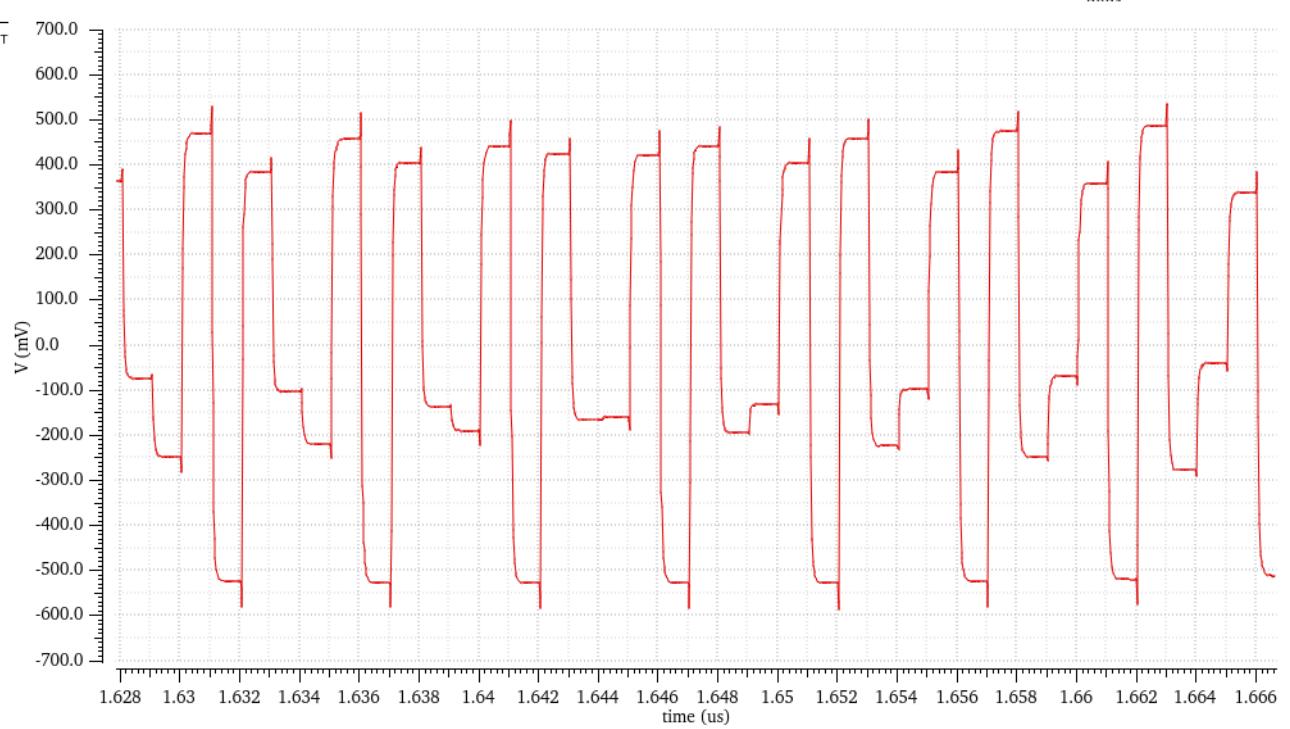


Figure 85: Frequency response of the output with sinusoidal input ($f < 100\text{MHz}$)

Differential OUTPUT

Fri Apr 16 21:01:57

1



db20(dft((v"/VOUTP" ?result "tran") - v("/VOUTN" ?result "tran")) 1u 3.048u 131072 "Rectangular" 0 0 1)

1

Name

Differential OUTPUT

Figure 86: Frequency response of the output with sinusoidal input ($f > 400\text{MHz}$)

Frequency 58.10MHz		Frequency 401.855MHz	
Measurement	Value	Measurement	Value
ENOB	7.4858615 (bits)	ENOB	6.3453191 (bits)
SINAD	46.827886 (dB)	SINAD	39.961821 (dB)
SNR	46.827886 (dB)	SNR	39.961821 (dB)
S FDR	55.29574 (dBc)	S FDR	42.458708 (dBc)
THD	0 (%)	THD	0 (%)
Signal P...	-5.6329997 (dB)	Signal P...	-8.018054 (dB)
DC Power	-92.705448 (dB)	DC Power	-60.711669 (dB)
Noise Fl...	-82.563886 (dB)	Noise Fl...	-78.082874 (dB)
Noise Fl...	-139.44634 (dB)	Noise Fl...	-134.96533 (dB)

Figure 87: Dynamic Parameters

Tabulate the simulated dynamic performance characteristics (SNDR, SFDR, ENOB) of your DAC in Part(e) and Part(f).

	Input Frequency 58.10MHz	Input Frequency 401.855MHz
SNDR (dB)	46.82	39.96
SFDR (dBc)	55.2954	42.458
ENOB (bits)	7.485	6.345

Table 20: Dynamic Performance of Final Segmented DAC

Comparison 4: Power Consumption

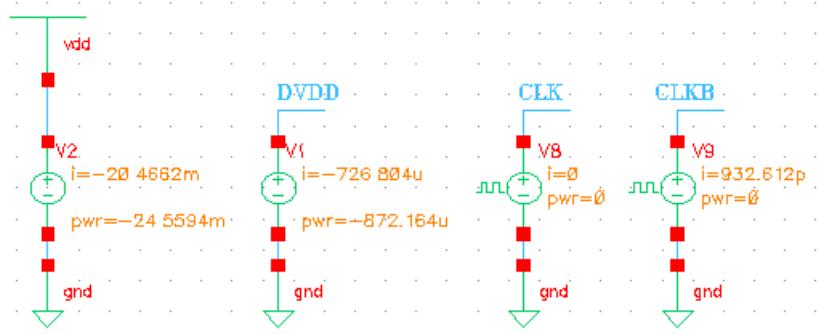


Figure 88: Power consumption of Final Segmented DAC
Power consumption is 24.559mW.

Comparison 5: Area

BINARY UNIT CELL				CURRENT SOURCE				INVERTER			
MOS	W	L	AREA	MOS	W	L	AREA	MOS	W	L	AREA
M1	7000	45	315000	MB1	1820	1040	1892800	MP	430	45	19350
M2	7000	45	315000	MB3	1820	1040	1892800	MN	315	45	14175
MB2	21300	1920	40896000	TOTAL AREA E-18			3785600	TOTAL AREA			
MB4	21300	1920	40896000	CLOCK MOS				TOTAL AREA			
TOTAL AREA E-18			82422000	NMOS	315	45	14175	TOTAL AREA			
TRANSMISSION GATE (nm)				NOR GATE				NAND GATE			
MOS	W	L	AREA	MOS	W	L	AREA	MOS	W	L	AREA
NMOS	210	45	9450	MP1	860	45	38700	MP1	430	45	19350
PMOS	210	45	9450	MP2	860	45	38700	MP2	430	45	19350
TOTAL AREA E-18			18900	MN1	315	45	14175	MN1	630	45	28350
TOTAL AREA E-18				MN2	315	45	14175	MN2	630	45	28350
TOTAL AREA E-18				TOTAL AREA E-18			105750	TOTAL AREA E-18			
BINARY TO THERMO CONVERTER				THERMO CURRENT CELL				DECODING LOGIC			
COMPONENT	TIMES	AREA	TOTAL AREA	BINARY UNIT CELL	4	82422000	329688000	COMPONENT	TIMES	AREA	TOTAL
INVERTER	4	33525	134100	DECODING LOGIC				NOR	2	105750	211500
NOR	5	105750	528750	COMPONENT				INVERTER	1	33525	33525
NAND	5	95400	477000	TOTAL AREA E-18				TOTAL AREA E-18			
TOTAL AREA E-18				TOTAL AREA E-18				TOTAL AREA E-18			
TOTAL AREA E-18				TOTAL AREA E-18				TOTAL AREA E-18			

BUFFER				BUFFER bar			
PMOS	W	L	AREA	PMOS	W	L	AREA
1	500	45	22500	1	500	45	22500
2	1360	45	61200	2	1360	45	61200
3	3700	45	166500	3	3700	45	166500
4	10060	45	452700	4	10060	45	452700
5	27370	45	1231650	5	27370	45	1231650
6	74440	45	3349800	6	65010	45	2925450
NMOS	W	L	AREA	NMOS	W	L	AREA
1	315	45	14175	1	315	45	14175
2	855	45	38475	2	855	45	38475
3	2330	45	104850	3	2330	45	104850
4	6340	45	285300	4	6340	45	285300
5	17240	45	775800	5	17240	45	775800
6	46900	45	2110500	6	46900	45	2110500
TOTAL AREA E-18		8613450		TOTAL AREA E-18		8189100	

THERMO UNIT CELL				THERMO DAC AREA			
COMPONENT	TIMES	AREA	TOTAL	COMPONENT	TIMES	AREA	TOTAL
DECODING LOGIC	2	245025	490050	BINARY UNIT CELL	3	82422000	247266000
INVERTER	3	33525	100575	BUFFER	2	8613450	17226900
NMOS	2	14175	28350	BUFFEER BAR	2	8189100	16378200
CURRENT CELL	1	329688000	329688000	INVERTER	6	33525	201150
MP1	2	19350	38700	CLOCK MOS	4	14175	56700
MN1	2	14175	28350	TRANMISSION GATE	2	18900	37800
MP2	2	166500	333000	CURRENT SOURCE	1	3785600	3785600
MN2	2	104850	209700	BIN2 THERMP CONV	2	1139850	2279700
TOTAL AREA E-18		330916725		THERMO UNIT CELL	64	330916725	21178670400
TOTAL AREA				E-18		21465902450	
IN UM^2				E-12		21465.9025	

Figure 89: Area of Final DAC

Comparison Between Two DAC design

Sr. no.	Parameter	BINARY DAC (8 bits)	Segmented DAC (6 +2 bits)
1	Offset error	0.1567LSB	-0.3825LSB
2.	Full scale error	0.7045LSB	0.4419LSB
3.	Gain error	1.0021	1.0031
4.	INL (transient)	0.2630LSB	0.2702LSB
5.	DNL (transient)	0.0142LSB	0.257LSB
6.	INL _{rms} (MC Simulation)	0.2732LSB	0.2486LSB
7.	DNL _{rms} (MC simulation)	0.0315LSB	0.0352LSB
8.	Frequency Response 58.10MHz	SFDR (dBc) = 50.3951	SFDR (dBc) = 55.2954
		SNDR (dB) = 45.74	SNDR (dB) = 46.82
		ENOB (bits) = 7.3063	ENOB (bits) = 7.485
9.	Frequency Response 401.855MHz	SFDR (dBc) = 44.3429	SFDR (dBc) = 42.458
		SNDR (dB) = 40.20	SNDR (dB) = 39.96
		ENOB (bits) = 6.471	ENOB (bits) = 6.345
10.	Power consumption	24.6226mV	25.43mV
11.	Area	21179.9486 μm^2	21465.9025 μm^2

Table 21: Comparison of Final Binary and Segmented DAC

As we can see from results

1. Best SFDR in Segmented DAC
2. Glitches reduced in Segmented DAC
3. Power consumption is more in Segmented DAC
4. If the segmented DAC design with 4:4 power consumption will be low
5. Area is more in segmented DAC than Binary weighted DAC

[Click here](#) to access complete project folder.

Project Folder

1. Binary weighted DAC design
 - a. Simulation results
 - b. MOSFETs sizes and area
 - c. Simulation excels sheets
 - d. Screenshots and internal schematic images of components
2. Segmented DAC design
 - a. Simulation results
 - b. MOSFETs sizes and area sheet
 - c. Simulation excels sheets
 - d. Screenshots and internal schematic images of components
3. Cadence library zip for simulation