Junjun Zou

Email: zjj19_tsinghua@163.com
Personal website: https://zou-junjun.github.io
Research interest: Mixed-Signal Circuit, Noise-Shaping ADC, Buck Converter, LDO, PLL, Sensors.

EDUCATION

Tsinghua University, Beijing, China Sep. 2019 - Jun. 2022
M.E. (Instrument and Meter Engineering) GPA: 3.85/4
Advisor: Prof. Qi Wei

Tsinghua University, Beijing, China Sep. 2014 - Jun. 2018
B.E. (Measurement, Control Technology and Instruments) GPA: 87/100

RESEARCH EXPERIENCE

A study on high-precision bandgap reference circuit, Tsinghua University
Advisor: Prof. Qi Wei Aug. 2020 - Jun. 2022

- Analyze the main noise resource and noise transfer function of traditional bandgap reference (BGR).
- Propose a novel BGR topology by removing the error amplifier in the traditional BGR.
- Present a simplified but accurate noise model of proposed BGR to optimize output noise performance.
- Utilize the temperature characteristic of the current gain factor β to accomplish high-order temperature compensation.
- Tape-out in 180 nm BCD process.
- Simulation and chip tests verify low output noise and low output temperature variation of proposed BGR.

A study on an auto-tuning continuous-time bandpass sigma-delta modulator, Tsinghua University
Advisor: Prof. Qi Wei Sep. 2019 - Jun. 2020

- Propose a continuous-time SDM with a 3-bit flash ADC and a second-order loop filter, which is composed of cascaded 2-stage RC integrator. And resistors in the loop filter are voltage-controlled MOS resistors.
- Propose a pseudo-PLL circuit to alleviate the difference between input signal's frequency and notch frequency of SDM. The pseudo-PLL circuit can trace input signal's frequency and output a control voltage to modulate the notch frequency of the loop filter.
- Tape-out in 180 nm CMOS process.
- Simulation and chip tests verify the SNDR performance of proposed sigma-delta modulator.

WORK EXPERIENCE

Analog IC Design Engineer, Joulwatt Microelectronics Co. Ltd, China Jun. 2023 - Present

- Transistor-level circuit design and simulation (**Dual-phase PLL-based Adaptive Constant-on-time Buck Converter**)
- Architect, implement and analyze trade-offs of circuits
- Designed in 180 nm CMOS process

Analog IC Design Engineer, Zeku Technology Co. Ltd, China Aug. 2022 - May 2023

- Transistor-level circuit design and simulation (**Comparator/Thermal Protection Circuit/Low Dropout Regulator**)
- Oversee and support layout
- Designed in 90 nm CMOS process

PUBLICATIONS

[1] **J. Zou**, Q. Wei, C. Ju, et al. A 0.82 μVrms ultralow 1/f noise bandgap reference for a MEMS gyroscope. *Microsystem Nanoengineering* 9, 48 (2023). https://www.nature.com/articles/s41378-023-00505-3 (*Journal*)

[2] **J. Zou**, Q. Wei, B. Zhou, et al. A 442.1 nVpp, 13.07 ppm/°C Ultra-Low Noise Bandgap Reference Circuit in 180 nm BCD Process. *2021 IEEE International Symposium on Circuits and Systems (ISCAS)*, (2021). https://ieeexplore.ieee.org/abstract/document/9401631 (*Conference*)

[3] Q. Wei, B. Zhou, **J. Zou**, et al. A bandgap reference circuit, CN112947667B[P].(2021)(*Innovative Patent*)

[4] C. G. Ju, X. Li, **J. Zou**, et al. An Auto-Tuning Continuous-Time Bandpass Sigma-Delta Modulator with Signal Observation for MEMS Gyroscope Readout Systems[J]. *SENSORS*, (2020). https://www.mdpi.com/1424-8220/20/7/1973 (*Journal*)

HONORS & AWARDS

2022 Outstanding Graduates from Tsinghua University
2021 National Scholarship
2020 1st Comprehensive Excellent Scholarship from Tsinghua University
2020 Samsung Scholarship
2017 Academic Excellent Scholarship from Tsinghua University
2016 Academic Excellent Scholarship from Tsinghua University
2016 National Inspirational Scholarship

SKILLS & LANGUAGE

Software: Cadence, Verilog, Matlab, C/C++, SIMPLIS
Hardware: FPGA
Language: Mandarin**,** English **(**Tofel: 100, best score 103)
Graduate Courses: Advanced Analog Circuit Design, Digital Large Scale Integrated Circuit Design, Microprocessor Design