A 442.1 nV_{pp} , 13.07 ppm/°C ultra-low noise bandgap reference circuit in 180 nm BCD process

Junjun Zou, Qi Wei, Bin Zhou, Xiang Li, Chunge Ju, Rong Zhang, Zhiyong Chen
Department of precision instrument, Tsinghua University, Beijing, China
Email: zjj19@mails.tsinghua.edu.cn

2021 IEEE International Symposium on Circuits and Systems (ISCAS) | 978-1-7281-9201-7/20/$31.00 ©2021 IEEE | DOI: 10.1109/ISCAS51556.2021.9401631

***Abstract*—This paper proposed an ultra-low noise bandgap reference (BGR), which could achieve a sub-microvolt level of peak-to peak output noise in the low frequency region and have good load capacity. The noise performance is improved by using a negative feedback loop rather than traditional operational amplifier, which eliminates the noise from operational amplifier. Additionally, detailed analysis of noise is used to optimize the noise performance of the BGR. The driving ability is improved by using current mirrors to avoid the effect of load current on the behavior of BGR. Simulation results show operating at a 5 V supply voltage, over the range from -40 °C to 125 °C, output voltage of the BGR is 1.3345 V of mean value and temperature coefficient is 13.07 ppm/°C. The peak-to-peak output noise of the BGR is 442.1 nV in the band of 0.1 Hz to 10 Hz. The maximum output load current is 444.6 mA. Monte-Carlo simulation illustrates process-invariance of this design.**

Keywords—ultra-low noise, load capacity, bandgap reference, BGR, high PSRR, temperature coefficient

I. INTRODUCTION

Bandgap reference could produce a stable output voltage when supply voltage and temperature change. It's an important block in analog circuits, digital circuits and mix-mode circuits, which could be used in data converters, operational amplifiers, DC-DC converters and low drop-out regulators. Previous researches about bandgap reference mainly focus on how to reduce the temperature coefficient [1] [2]. However, with the increasing accuracy of integrated circuit, low noise bandgap reference is urgently needed. For example, noise contributed by reference voltage should be less than 1/2 LSB to achieve an accurate and usable analog-to-digital converter. For a 16-bit ADC, the accuracy of reference voltage should be less than 7.6 ppm.

Noise of bandgap voltage reference consists of thermal noise and low frequency 1/f noise. In practice, buffer circuit is needed at the output of BGR to improve driving ability, which increases the noise source. Some methods have been proposed to improve noise performance of BGR in prior-art studies. Analog devices company [3] proposed a method to reduce circuit noise by using dual-threshold JFET instead of bipolar transistor or MOSFET to produce a proportional-to-absolute-temperature (PTAT) current. But special process is needed. Chopping technology is proposed by Yueming Jiang [4] to modulate low frequency noise to high frequency region, and then to filter it by low-pass filter. However, multipliers and filters would increase the complexity and power consumption of the circuit. In this paper, an ultra-low noise bandgap voltage reference is proposed, which could achieve a sub-microvolt level of peak-to peak output noise in the band of 0.1 Hz to 10 Hz and have good load capacity.

II. PROPOSED BANDGAP REFERENCE

A. Principal of proposed bandgap reference

Fig. 1 presents the circuit topology of proposed ultra-low noise bandgap reference. The BGR consists of BGR-core circuit and start-up circuit. In BGR-core circuit, the topology of transistors Q_1, Q_2 and resistor R_3 produce the PTAT part and the emitter-base voltage of transistor Q_1 provide the complementary-to-absolute-temperature (CTAT) part. Operating in the forward active region, the base-emitter voltage V_{BE} of a bipolar transistor could be described as a function of the collector current I_c.

$$V_{BE} = \frac{kT}{q}\ln(\frac{I_c}{I_s}), \tag{1}$$

where I_s is a constant used to describe the transfer characteristic of transistor, which is proportional to the cross-sectional area of the emitter, T is absolute temperature, k is Boltzmann constant and q is electron charge.

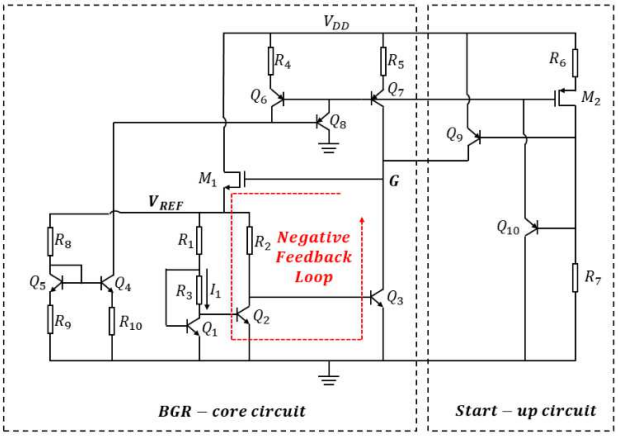

Fig. 1. Proposed bandgap reference

According to (1), the difference between V_{BE} of bipolar transistors Q_1, Q_2 would produce a PTAT current I_1 in R_3. Neglecting base currents, the current in R_1 is the same as the current in R_3. The collector currents of transistors Q_1 and Q_5 are equal when the sum of resistances R_8, R_9 is equal to R_1 and Q_1, Q_5 have same parameters. Q_5, Q_4 and Q_6, Q_7 form current mirrors respectively, which makes the collector currents of transistors Q_3 and Q_5 equal. Thus, the collector current of Q_3 is the same as the collector current of Q_1. By making parameters of Q_1 and Q_3 identical, V_{BE} of Q_1 and Q_3 are equal so that the voltages across R_1 and R_2 are same. Consequently, the PTAT current I_1 could be expressed as

$$I_1 = \frac{kT}{qR_3}\ln(\frac{I_{c1}A_2}{I_{c2}A_1}) = \frac{kT}{qR_3}\ln(\frac{R_2A_2}{R_1A_1}), \tag{2}$$

where A_1, A_2 are the emitter cross-sectional area of Q_1 and Q_2, I_{c1}, I_{c2} are collector's current of Q_1 and Q_2. R_1, R_2 need to be resistors of the same type. The PTAT current could be modified by changing the ratio of R_1, R_2 and the ratio of A_1, A_2. The output reference voltage V_{REF} equals

$$V_{REF} = V_{BE1} + I_1R_1 = V_{BE1} + \frac{kTR_1}{qR_3}\ln(\frac{R_2A_2}{R_1A_1}). \tag{3}$$

978-1-7281-9201-7/21/$31.00 ©2021 IEEE

Y. P. Tsividis proposed the detailed temperature behavior of bipolar transistor parameter in [5]. V_{BE} consists of a constant term, a term negatively related to T and a high order term TlnT. The drift of V_{REF} with temperature could be expressed as

$$V_{REF} = V_{GOr} + [\frac{kR_1}{qR_3}\ln(\frac{R_2 A_2}{R_1 A_1}) + \frac{V_{BE}(T_r) - V_{GOr}}{T_r}]T - \frac{(\gamma-\delta)k}{q} T\ln(\frac{T}{T_r}), \quad (4)$$

where V_{GOr} is the bandgap voltage of certain reference temperature T_r, γ and δ are appropriate constants. Generally, the high-order term TlnT could be neglected. Thus, V_{REF} is superposed by a PTAT part and a CTAT part. And the BGR could have a small temperature coefficient by modifying the ratio of R_1 and R_3, the ratio of R_1 and R_2 and the ratio of A_1 and A_2.

B. Negative feedback loop and high PSRR

Unlike the traditional BGR circuit, which uses operational amplifier to stabilize output voltage, there is a negative feedback loop used in this design. Assuming that there is an increment ΔV_{REF} at the output voltage, ΔV_{REF} would affect the collector currents of transistors Q_1, Q_2, Q_3 and change the gate voltage V_G of transistor M_1. According to Kirchhoff's law and the voltage gain function of NPN transistor, the variation of V_G could be expressed as

$$\Delta V_G = -[1 + \frac{g_{m2}R_2(g_{m1}R_3 - 1)}{1 + g_{m1}R_1}]g_{m3}R_L\Delta V_{REF}, \quad (5)$$

where g_{m1}, g_{m2}, g_{m3} are transconductance of Q_1, Q_2 and Q_3, R_L is the equivalent resistance of node G. Thus, V_G decreases as V_{REF} increases when $g_{m1}R_3>1$. When there is no load variation at output node, M_1 acts as a voltage follower so the decrease of V_G would restrain the increase of V_{REF}, which means output voltage are stable with the negative feedback loop regardless of any interference sources. With greater g_{m2}, g_{m3}, R_2 and R_L, there is a larger gain factor of the negative feedback loop and the circuit could operate more stably.

Due to the negative feedback loop, this design could achieve a high PSRR without operational amplifier. Assuming that there is a variation of supply voltage ΔV_{DD}, V_{REF} would be affected by ΔV_{DD} through three pathways. (i) ΔV_{DD} would affect V_G and V_{REF} through affecting the gate voltage of M_2. (ii) ΔV_{DD} would directly affect the collector-emitter voltage of Q_7 to affect V_G and V_{REF}. (iii) ΔV_{DD} would directly affect V_{REF} by affecting the drain-source voltage of M_1. The effect of the three paths on output reference could be all reduced by this negative feedback loop according to aforementioned discussion.

C. Driving ability and start-up circuit

In Fig. 1, neglecting base currents, the current mirrors formed by transistors Q_4, Q_5, Q_6, Q_7 could mirror to Q_3 the collector current of Q_5. The collector currents of transistors Q_1, Q_2 and Q_5 depends on V_{REF}. Due to the current mirrors, the collector currents of all bipolar transistors in BGR-core circuit are controlled by V_{REF}. Transistor M_1 drives the output load of BGR, and the variation of output load current would affect the gate voltage V_G of transistor M_1 in turn. As long as transistor Q_7 could operate in forward-active region when V_G varies, the negative feedback loop operates normally and makes V_{REF} keep almost invariant so the collector currents of all the bipolar transistors are scarcely changed. Thus, to some extent, the output load current doesn't obviously affect the behavior of BGR-core circuit with the current mirror and the negative feedback loop. In this design, M_1 use a large size NMOSFET to achieve good driving ability.

Start-up circuit helps BGR-core circuit operate at normal state. After the circuit is powered on, Q_9 turns on and injects current into BGR-core circuit. Then V_G increases and Q_6, Q_7 turn on. Q_{10} is used to decrease the base voltage of Q_6, Q_7. And the drain-source current of M_2 increases so that the base voltage of Q_9, Q_{10} decreases. To a certain extent, the base-emitter voltage of Q_9 and Q_{10} become less than threshold voltage and then Q_9, Q_{10} turn off. The branch of R_6, M_2 and R_7 provides bias voltage for Q_6 and Q_7.

III. ANALYSIS AND OPTIMATION OF NOISE

The small-signal circuit of this design in Fig. 2 could be used to calculate output noise of the proposed circuit. The small parasitic base resistor and collector resistor of bipolar transistors are not included because shot noise and 1/f noise are the major noise contributors of bipolar transistor.

According to theory proposed by Paul R. Gray [6], the spectral density of each noise source in Fig. 2 is

$$E_{Ri} = \sqrt{4kT \times R_i}, i = 1,2,3,8,9 \quad (6)$$

$$I_{nbi} = \sqrt{2q \times \frac{I_{ci}}{\beta_i} + \frac{K_1}{f} \times (\frac{I_{ci}}{\beta_i})^{\alpha}}, i = 1,2 \quad (7)$$

$$I_{nci} = \sqrt{2q \times I_{ci}}, i = 1,2 \quad (8)$$

$$I_{d5} = \sqrt{2q \times I_{c5} \times (\frac{1+\beta_5}{\beta_5}) + \frac{K_1}{f}(\frac{I_{c5}}{\beta_5})^{\alpha 1}} \quad (9)$$

$$I_{M1} = \sqrt{4kT \times (\frac{2}{3}g_{mM1}) + \frac{K}{f} \times (I_D)^{\alpha 2}}, \quad (10)$$

where K, K_1 are device constants of MOSFET and bipolar transistor, α_1 and α_2 are constants in the range 0.5 to 2, I_{ci} is the collector region's current density of transistor Q_i, β_i is the current gain factor of transistor Q_i, g_{mM1} is transconductance of M_1. Noise sources could be superposed directly to calculate the output reference noise due to their uncorrelation.

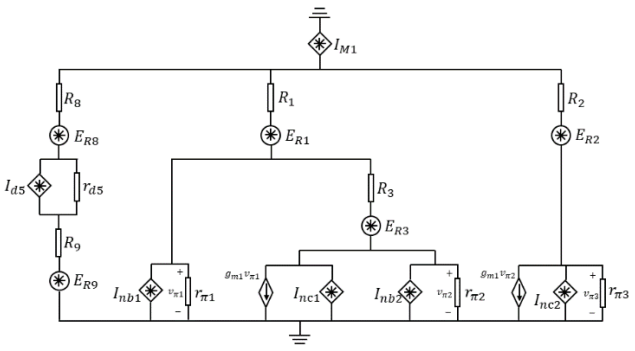

Fig. 2. Small signal circuit with RMS noise

The total RMS output reference noise $VREFnoise^2$ is equal to

$$V_{REFnoise}^2 = \left(\frac{R_{eq2} \parallel R_{eq3}}{R_{eq1} + R_{eq2} \parallel R_{eq3}}\right)^2 \times [E_{R8}^2 + E_{R9}^2 + (I_{d5} r_{d5})^2] + \left(\frac{R_{eq1} \parallel R_{eq3}}{R_{eq2} + R_{eq1} \parallel R_{eq3}}\right)^2 \times \{I_{nb1}^2 \times [r_{\pi 1} \parallel (R_3 + r_{\pi 2})]^2 + \frac{(I_{nc1}^2 + I_{nb2}^2) \times r_{\pi 2}^2 + E_{R3}^2}{(R_3 + r_{\pi 2})^2} \times [r_{\pi 1} \parallel (R_3 + r_{\pi 2})]^2 + E_{R1}^2\} + \left(\frac{R_{eq1} \parallel R_{eq2}}{R_{eq3} + R_{eq1} \parallel R_{eq2}}\right)^2 \times (E_{R2}^2 + I_{nc2}^2 r_{\pi 3}^2) + (R_{eq1} \parallel R_{eq2} \parallel R_{eq3})^2 \times I_{M1}^2. \quad (11)$$

And the R_{eq} factors in (11) are

$$R_{eq1} = R_8 + R_9 + r_{d5} \quad (12)$$

$$R_{eq2} = R_1 + r_{\pi 1} \parallel (R_3 + r_{\pi 2}) \quad (13)$$

$$R_{eq3} = R_2 + r_{\pi 3}, \quad (14)$$

where $r_{\pi 1}$, $r_{\pi 2}$, $r_{\pi 3}$ are the input resistance of Q_1, Q_2, Q_3, r_{d5} is the equivalent resistance of diode-connected Q_5. In general, the input resistance of bipolar transistor is considerably large so that R_{eq} factors could be nearly expressed as $R_{eq2} \approx r_{\pi 1} \parallel r_{\pi 2}$, $R_{eq3} \approx r_{\pi 3}$. Consequently, the equation (11) could be simplified as (15).

$$V_{REFnoise}^2 = (R_{eq1} \parallel r_{\pi 1} \parallel r_{\pi 2} \parallel r_{\pi 3})^2 \times [\frac{E_{R8}^2 + E_{R9}^2 + I_{d5}^2 r_{d5}^2}{R_{eq1}^2} + I_{nb1}^2 + I_{nc1}^2 + I_{nb2}^2 + I_{nc2}^2 + \frac{E_{R3}^2 + E_{R2}^2}{r_{\pi 3}^2} + \frac{E_{R1}^2}{(r_{\pi 1} \parallel r_{\pi 2})^2} + I_{M1}^2] \approx (R_{eq1} \parallel r_{\pi 1} \parallel r_{\pi 2} \parallel r_{\pi 3})^2 \times (I_{nb1}^2 + I_{nc1}^2 + I_{nb2}^2 + I_{nc2}^2 + I_{M1}^2) \quad (15)$$

According to (15), I_{nb1}, I_{nb2}, I_{M1} are the main sources of low frequency noise. And I_{nc1}, I_{nc2}, I_{M1} is the major contributors of flat-band noise. In order to reduce the total output noise, I_{nb1}, I_{nb2}, I_{nc1}, I_{nc2} and I_{M1} should be decreased, which could be implemented by reducing the collector currents of Q_1, Q_2, Q_5 and the drain-source current of M_1. But a small collector current would result in a large input resistance of bipolar transistor r_π, which makes a greater output noise. There is a trade-off between transistors' operation current and output noise. Additionally, the low frequency noise could be reduced by increasing the size of M_1.

IV. SIMULATION RESULTS

The proposed ultra-low noise bandgap reference was implemented in 180 nm bipolar CMOS DMOS process (BCD process). The area of the entire design is 545 µm×423 µm. The layout of BGR is presented in Fig. 3. Post-layout simulation results show that with output load of 1 kΩ resistor and 1µF capacitor, the temperature drift curve has a typical parabola shape. Fig. 4 illustrates the temperature-voltage curve of output reference voltage when circuit operates at a supply voltage of 5 V. Over the range from -40 °C to 125 °C, the mean value of output voltage is 1.3345 V and the temperature coefficient is 13.07 ppm/°C. When the circuit operates for 1000 s with noise in the band of 0.1 Hz-10 Hz, the variation of output voltage compared to mean value is shown in Fig. 5. The peak-to-peak noise of output voltage is 442.1 nV. Table. I illustrate the noise performance comparison of this work and prior-art work. The noise performance of this design is much better than previous work and achieves a sub-microvolt level. Fig. 6 shows the noise spectrum and the PSRR performance of BGR. PSRR is 89.26 dB at 0.1 Hz and 81.28 dB at 10 Hz, which means output voltage has a great supply voltage insensitivity. Fig. 7 presents that the BGR has good driving ability, the maximum output load current is 444.6 mA.

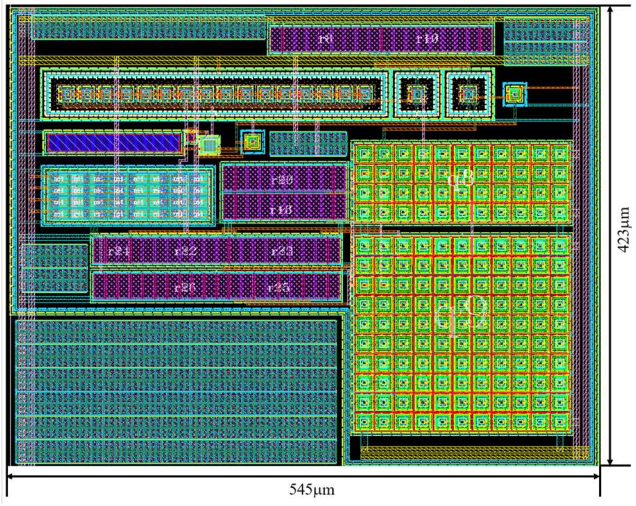

Fig. 3. Layout of proposed bandgap reference

Monte-Carlo simulation has run using 200 points to simulate the process variations and mismatch effects. The temperature-voltage curves and output noise drifts are given in Fig. 8. This design could have 17.55 ppm/°C temperature coefficient of mean value (σ=6.80 ppm/°C) and 476.8 nV_{pp} noise performance of mean value (σ=20.6 nV_{pp}) with process variations and mismatch.

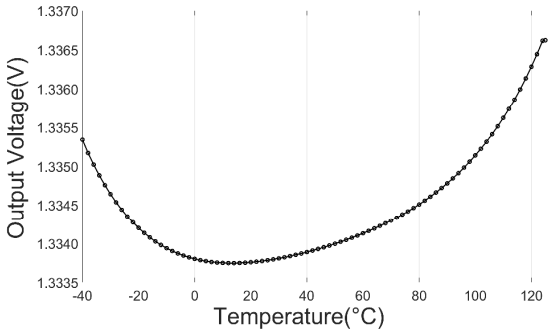

Fig. 4. Proposed bandgap reference temperature drift curve

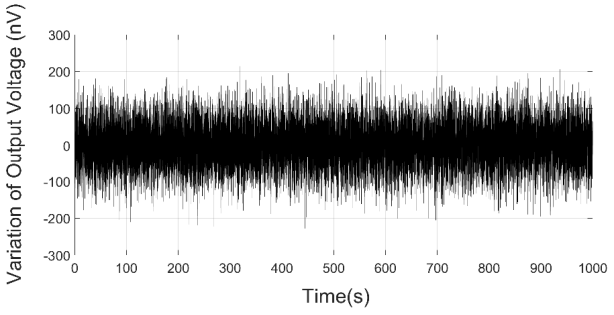

Fig. 5. Output voltage versus time curve

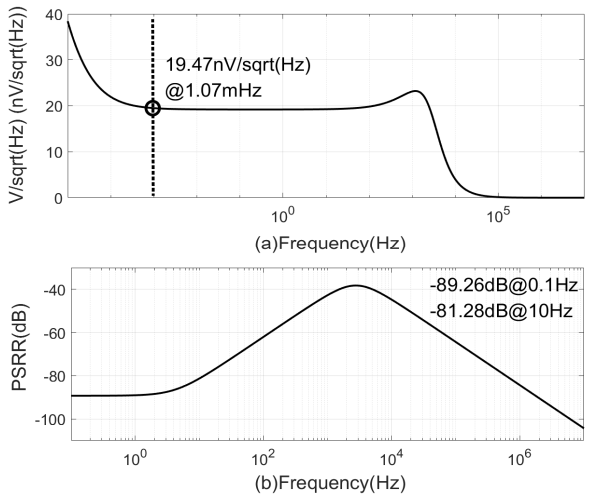

Fig. 6. (a) noise spectrum of BGR (b) PSRR performance of BGR

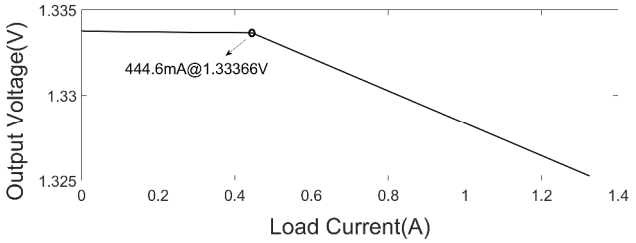

Fig. 7. Output voltage versus load current

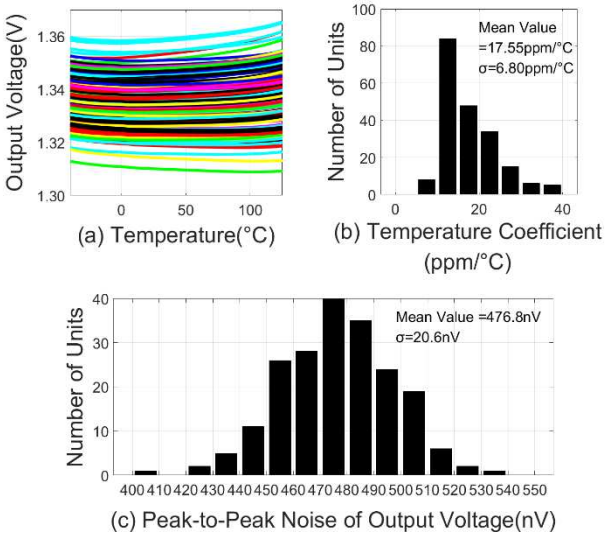

Fig. 8. Monte-Carlo simulation.(a) temperature drift curve of 200 samples (b) statisical result of temperature coefficient (c) statisical result of peak-to-peak output noise

V. CONCLUSION

An ultra-low noise bandgap reference is proposed. The BGR has great noise performance and driving ability. And detailed noise analysis of BGR is used to improve the noise performance. Simulation results show in the band of 0.1 Hz to 10 Hz, the peak-to-peak output noise of BGR is 442.1 nV. The BGR has good driving ability, and the maximum output load current is 444.6 mA. Over the range from -40 °C to 125 °C, the mean value of output voltage is 1.3345 V and the temperature coefficient is 13.07 ppm/°C. PSRR is 89.26 dB at 0.1 Hz and 81.28 dB at 10 Hz. Monte-Carlo simulation illustrates BGR has a great characteristic of process-invariance.

TABLE I. PERFORMANCE SUMMARY AND COMPARISON

	2011 [7]	2015 [8]	2019 [1]	2019 [9]	[10]	**This work***
Process	0.16μm CMOS	0.18μm CMOS	0.35μm CMOS	0.18μm CMOS	XFET	**0.18um BCD**
Supply Voltage (V)	1.8	1.3-2.6	2.6-5	1.0[2]	4-18	**5**
V_{REF} (V)	1.0875	1.1402	2.47	0.6926	2.048	**1.3345**
Area(mm^2)	0.12	0.05	0.0616	0.0045	NA	**0.23**
TC (ppm/°C)	4.7 (-40°C ~125°C)	4.1 (-55°C ~125°C)	3 (-40°C ~125°C)	33 (-20°C ~100°C)	2 (-40°C ~125°C)	**13.07 (-40°C ~125°C)**
Noise[1] (0.1Hz-10Hz)	6.1 μV_{rms}	10.23 μV_{rms}	3.6 μV_{rms}	26.8 μV_{rms}	1.75 μV_{pp}	**442.1 nV_{pp}**

*. Simulation work
1. Statistically $1V_{rms}=6.6V_{pp}$
2. minimum supply voltage

REFERENCES

[1] L. Liu, X. Liao and J. Mu, "A 3.6 μVrms Noise, 3 ppm/°C TC Bandgap Reference With Offset/Noise Suppression and Five-Piece Linear Compensation," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 66, no. 10, pp. 3786-3796, Oct. 2019.

[2] C. M. Andreou, S. Koudounas and J. Georgiou, "A Novel Wide-Temperature-Range, 3.9 ppm/°C CMOS Bandgap Reference Circuit," in IEEE Journal of Solid-State Circuits, vol. 47, no. 2, pp. 574-581, Feb. 2012.

[3] D. F. Bowers, "A 37nV/sqrtHz 2.5V reference based on dual-threshold JFET technology," 2008 IEEE Bipolar/BiCMOS Circuits and Technology Meeting, Monteray, CA, 2008, pp. 13-16.

[4] Yueming Jiang and E. K. F. Lee, "A low voltage low 1/f noise CMOS bandgap reference," 2005 IEEE International Symposium on Circuits and Systems, Kobe, 2005, pp. 3877-3880 .

[5] Y. P. Tsividis, "Accurate analysis of temperature effects in I_C-V_{BE} characteristics with application to bandgap reference sources," in IEEE Journal of Solid-State Circuits, vol. 15, no. 6, pp. 1076-1084, Dec. 1980.

[6] GRAY P R. Analysis and Design of Analog Integrated Circuits[M]. 5th ed. New York: Wiley, pp. 736-795, 2009.

[7] G. Ge, C. Zhang, G. Hoogzaad and K. A. A. Makinwa, "A Single-Trim CMOS Bandgap Reference With a 3sigma Inaccuracy of +/- 0.15% From -40°C to 125°C," in IEEE Journal of Solid-State Circuits, vol. 46, no. 11, pp. 2693-2701, Nov. 2011.

[8] B. Wang, M. K. Law and A. Bermak, "A Precision CMOS Voltage Reference Exploiting Silicon Bandgap Narrowing Effect," in IEEE Transactions on Electron Devices, vol. 62, no. 7, pp. 2128-2135, July 2015.

[9] Y. Ji, J. Lee, B. Kim, H. Park and J. Sim, "A 192-pW Voltage Reference Generating Bandgap–Vth With Process and Temperature Dependence Compensation," in IEEE Journal of Solid-State Circuits, vol. 54, no. 12, pp. 3281-3291, Dec. 2019.

[10] ADR420 Data Sheet, Analog Devices.