Zou JunJun
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Education

- **Tsinghua University** — Beijing, China
  M.E. in Instrument and Meter Engineering, advised by Prof. Wei Qi (GPA :3.85/4.0) — *Sept. 2019 - June 2022*
- **Tsinghua University** — Beijing, China
  B.E. in Measurement, Control and Instruments (GPA :87/100) — *Sept. 2014 - June 2018*

Research Experience

- **Low-noise Bandgap Voltage Reference (BGR) for MEMS Sensors** — Tsinghua University
  Taped-out in 180nm BCD process — *Aug. 2020 - June 2022*
  - Proposed a novel low-noise BGR topology with second-order temperature compensation
  - Implemented theoretical analysis of noise transfer function and chip measurements to verify low-noise performance
  - Accomplished Chip-Sensor Co-measurements and verified BGR's 1/f noise linearly affects MEMS sensors' BI
- **Continuous-Time Bandpass Sigma-Delta ADC for MEMS Sensors** — Tsinghua University
  Taped-out in 180nm CMOS process — *Sept. 2019 - June 2020*
  - Proposed a continuous-time sigma-delta modulator with a 3-bit flash ADC and a second-order R-C loop filter
  - Added a pseudo-PLL circuit to alleviate PVT variation's effect on modulator's notch frequency

Publications

- **JunJun Zou**, Qi Wei, Chunge Ju, et al. *A 0.82 Vrms ultralow 1/f noise bandgap reference for a MEMS gyroscope,* in **Microsystem Nanoengineering** ,2023
- **JunJun Zou**, Qi Wei, Bin Zhou, et al. *A 442.1 nVpp, 13.07 ppm/°C Ultra-Low Noise Bandgap Reference Circuit in 180 nm BCD Process,* in IEEE International Symposium on Circuits and Systems**(ISCAS)** ,2021
- Chunge Ju, Xiang Li, **JunJun Zou**, et al. *An Auto-Tuning Continuous-Time Bandpass Sigma-Delta Modulator with Signal Observation for MEMS Gyroscope Readout Systems,* in **Sensors** ,2020

Industry Experience

- **Joulwatt Microelectronics** — Shanghai, China
  Analog IC design engineer — *June 2023 - Present*
  - Transistor-level circuit design and simulation **(Dual-phase PLL-based ACOT Buck Converter)**
  - Architect, implement and analyze trade-offs of circuits; Oversee and support layout (180nm BCD process)
- **Zeku Technology** — Shanghai, China
  Analog IC design engineer — *Aug. 2022 - May 2023*
  - Transistor-level circuit design and simulation **(Low Power Fast-Transient Low-Dropout Regulator/VCO)**
  - Architect, implement and analyze trade-offs of circuits; Oversee and support layout (90nm CMOS process)

Honor And Awards

- **Graduate**: Outstanding Graduates from Tsinghua University (2022), National Scholarship (2021), First Comprehensive Excellent Scholarship from Tsinghua University/Samsung Scholarship (2020)
- **Undergraduate**: Academic Excellent Scholarship from Tsinghua University (2016/2017), National Inspirational Scholarship (2016)

Skills And Language

- **Software/Hardware**: Cadence, Verilog, Matlab, C/C++, SIMPLIS, Vivado, FPGA
- **Language**: Mandarin, English (Tofel: 100, best score 103)