An Zou

Ph.D. Candidate

Department of Electrical & Systems Engineering — Phone: +1 (614) 736 9876

Washington University in St. Louis — Email: anzou@wustl.edu

Education

2016–present Ph.D. Candidate - Electrical Engineering
Washington University in St. Louis MO, U.S.
Advisor: Prof. Xuan Zhang

2013–2015 M.S. - Automation - (GPA:93/100 Rank: 1/161)
Harbin Institute of Technology Harbin, China
Advisor: Prof. Hui Zhao

2009–2013 B.S. - Automation - (GPA:91/100 Rank: 10/123)
Harbin Institute of Technology Harbin, China

Awards and Honors:

Micro Student Travel Award	2018
DAC Best Paper Nomination	2017
DAC Student Travel Award	2017
Graduate Fellowship The Ohio State University	2015
National Scholarship	2014
First Level Master Scholarship	2014,2013
People Scholarship	2013,2012,2011,2010
Outstanding Student	2012
88412 Scholarship	2011
Individual Scholarship	2011

Competition Awards:

2014 National Postgraduate Mathematic Contest in Modeling(China)	The Second Prize
2011 National College Mathematical Contest in Modeling(MCM, U.S.)	Meritorious Winner Prize
2010 Zhejiang Undergraduate Student Physics Competition	The Third Prize

Publications:

[1] **An Zou**, Jingwen Leng, Xin He, Yazhou Zu, Christopher D. Gill, Vijay Janapa Reddi, Xuan Zhang. Voltage-stacked GPUs: A Control Theory Driven Cross-Layer Solution for Practical Voltage Stacking in GPUs. IEEE 51th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO 2018) Fukuoka, Japan, Oct 20 - 24 2018.

[2] **An Zou**, Jingwen Leng, Xin He, Yazhou Zu, Vijay Janapa Reddi, Xuan Zhang. Efficient and Reliable Power Delivery in Voltage-Stacked Manycore System with Hybrid Charge-Recycling Regulators. The 55th Design Automation Conference (DAC 2018). San Francisco, CA. U.S. June 24-28 2018

[3] **An Zou**, Jingwen Leng, Yazhou Zu, Tao Tong, Vijay Janapa Reddi, David Brooks, Gu-Yeon Wei, Xuan Zhang. Ivory: Early-Stage Design Space Exploration Tool for Integrated Voltage Regulator. The 54th Design Automation Conference (DAC 2017). Austin, TX U.S. June 18-22 2017 **(Best Paper Nominations)**

[4] **Zou An**, Zhao Hui, Ma Yehan and Li Da. Analysis Calculation and Testing of Rotary Inductosyn Angle Measuring Errors. The 33rd Chinese Control Conference (CCC 2014). Nanjing, China, July 28-30 2014.

[5] Da Li, Hui Zhao, Honglin Xue and **An Zou**. The Design and Implementation of Universal Interface Circuit for Photoelectric Encoder. The 11th World Congress on Intelligent Control and Automation (WCICA 2014). Shenyang, China, June 29-July 4 2014.

Projects:

Oct. 2017 - Present **Meso-scale power management**
We use a layered approach for meso-scale systems to propose a power management technique including: 1. A malleable power distribution module layer 2. An optimal power distribution algorithm layer 3. An orchestration engine layer.

Feb. 2017 - Aug. 2018 **GPU Voltage Stacking**
Voltage stacking is an alternative on-chip power delivery solution that provides a single high voltage to a series stack of voltage domains. By recycling charge through the stack layers, voltage stacking offers several advantages. For the same chip power, an n-way stacked system reduces the current draw of the chip proportionally by n, reducing off-chip losses and alleviating power delivery impedance requirements. It also obviates a high step-down off-chip DC-DC converter. For high-power systems that draw power from a high-voltage rail (e.g., 12V), lower step-down ratios can improve offchip regulator efficiency. For battery-powered applications, there is an opportunity to power the chip directly off of the battery, eliminating losses due to off-chip voltage conversion all together and saving precious board space.

June. 2016 - Jan. 2017 **Integrated Voltage Regulator Power Delivery System Modeling**
With the demise of Dennard scaling, power and energy efficiency restricts single thread performance and designers are looking for new ways to deliver power more efficiently to microprocessors. Integrated voltage regulators (IVRs) can enhance supply integrity and enable exible voltage scaling by moving power conversion closer to the point-of-load. Distributed IVRs can deliver per-core, fine-grain, fast dynamic voltage and frequency scaling (DVFS) at a level unattainable with traditional off-chip regulators, and also suppress voltage noise more effiectively. Leveraging these benefits improves both performance and efficiency.

Mar. 2014 - June. 2015 **Software and Hardware co-design of an embedded signal processing system based on DSP for Inductosyn. The embedded system could compensate the errors automatically**
For the purpose of increasing the accuracy of Inductosyn, I am designing and programming an embedded signal processing system based on DSP(TMS320F28335). This embedded system could automatically compensate the errors of Inductosyn angular measuring errors.

Aug. 2013 – Nov. 2013 **Researching the compensation algorithms for the Inductosyn angular measuring errors**
For the purpose of compensating the Inductosyn angular measuring errors, I tried interpolation algorithm, FFT algorithm, filter algorithm and neural net algorithm. I am writing a paper about this research.

Aug. 2013 - Nov. 2013 **Design a new inductosyn angular measuring signal process circuit for a smart system**
For a special smart system, I designed a new Inductosyn angular measuring signal process circuit. The circuit is based on AD2S82 and gives out its output by orthogonal signal.

May 2013 - Jul. 2013 **Develop an errors automatic testing system for inductosyn**
I completed the C++ program of this errors automatic testing system.The system is based on an air bearing ultra-high accuracy rotary table which has the position accuracy better than 1 arc second. The rotary table is controlled by PMAC TURBO control board.

Aug. 2012 - May 2013 **Design and implement inductosyn angular measuring circuit**
Based on AD2S80 and CPLD, I designed and implement Inductosyn angular measuring signal process circuit. The circuit could successful output the angular information with 10, 12, 14 or 16 digit signal by ISA slot.

Mentored Students:

Master students: Duhong Xu, Yunshen Huang
Undergraduate students: Shuhe Tian, Chenyang Wang

Technical Skills:

Programming: C/C++; Verilog; M language; Python
Software: MATLAB; Cadence tools (Virtuoso, Encounter); Synopsys tools (Design Compiler, VCS); SPICE; CCS; Quartus2; Altium Designer
Operating System: Linux; Windows