

PD70210/A/AL and PD70211 System Layout Guidelines

Introduction

This application note provides detailed layout guidelines for the implementation of a Power over Ethernet (PoE) Powered Device (PD) system, based on Microchip's PD70210/A/AL or PD70211 controllers. PD70210/A/AL is a PD front-end controller, while PD70211 combines PD front-end and Pulse-Width Modulation (PWM).

The following table summarizes Microchip PD products offerings.

Table 1. PD Interface Device Family

Part	Type	Package	IEEE 802.3af	IEEE 802.3at	HDBaseT (PoH)	UPoE
PD70100	Front End	3 mm × 4 mm 12L DFN	x	—	—	—
PD70101	Front End + PWM	5 mm × 5 mm 32L QFN	x	—	—	—
PD70200	Front End	3 mm × 4 mm 12L DFN	x	x	—	—
PD70201	Front End + PWM	5 mm × 5 mm 32L QFN	x	x	—	—
PD70210	Front End	5 mm × 5 mm 16L DFN	x	x	x	x
PD70210A	Front End	4 mm × 5 mm 16L DFN	x	x	x	x
PD70210AL	Front End	5 mm × 7 mm 38L QFN	x	x	x	x
PD70211	Front End + PWM	6 mm × 6 mm 36L MLPQ	x	x	x	x
PD70224	Ideal Diode Bridge	7.5 mm × 10 mm 52L MLP	x	x	x	x

Note: Due to their high-power handling capability, ensure to follow the guidelines specified in this application note to have noise robustness and a solution with good thermal behavior. All the layout recommendations for the front section of PD70211 apply to PD70210/A/AL as well.

Microchip offers PD devices that integrate the front-end PD and the PWM into the product package. Additionally, Microchip offers standalone front-end PD devices that require an external PWM IC to convert the high PoE voltage down to the regulated supply voltage used by the application. The front-end section provides the necessary detection, classification, power up functions, and operating current levels compliant with the listed standards. The PWM section controls the conversion of the PoE high voltage down to regulated supply voltage used by the application.

Microchip offers a complementary product for PoE PD applications, the PD70224 Ideal Diode Bridge, which is a lowloss alternative to the dual diode bridges for input polarity protection.

Microchip offers complete reference design packages and Evaluation Boards (EVBs). For access to these design packages, device datasheets, or application notes, please consult your local Microchip Client Engagement Manager or visit our website at www.microchip.com/poe.

For technical support, consult your local Embedded Solutions Engineers or go to microchipsupport.force.com/s/.

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1. Ground Planes

PD70211-based systems include a number of “ground” types:

- VPN_IN

This is the negative rail of the voltage received from the PSE side. It is connected to VPN_OUT through the isolation switch under normal operation. This switch remains ON as long as the input voltage is a valid PSE voltage and there are no faults in downstream DC-DC.

- Power Ground (PGND)

This is the return of DC-DC power circuitry and PWM controller’s MOSFET gate driver’s PG and SG. PGND must be connected to VPN_OUT, the negative side output of the PD device front-end. Ideally, this connection must be done near the bulk capacitor Cin.

- Signal Ground (GND)

This is the PWM controller’s “quiet” ground used for the return path of the low-power control signals.

GND and PGND must be connected together in a single point near controller to eliminate the switching current affecting the control signals. Usually, this connection is done through a zero-ohm resistor to separate the nets.

- Digital ground

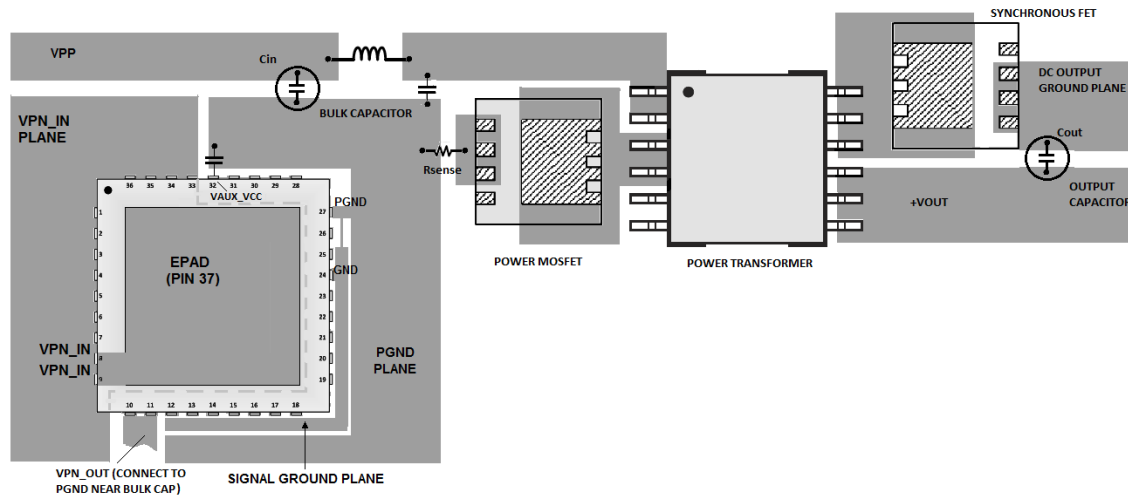
In isolated systems, there is also a secondary output (digital) ground of the DC-DC converter. The secondary ground must have 1500Vrms isolation from all of the above ground types.

- Earth ground

This ground may present only in systems with grounded metal enclosure. Earth ground connects to the shells of RJ45 connectors, to common mode filter capacitors, and to mounting screws. This ground must likewise have 1500Vrms isolation from all primary side grounds (VPN_IN, PGND, and GND), but it might be tied to the secondary digital ground.

The following figure shows an implementation of ground planes in PD70211-based flyback converter.

Figure 1-1. Example of Copper Planes Implementation in PD70211-Based System



Note: The copper planes for various grounds are just means for low impedance connections. They must not be poured over the entire board area and must only cover the areas under the components referenced to the respective grounds.

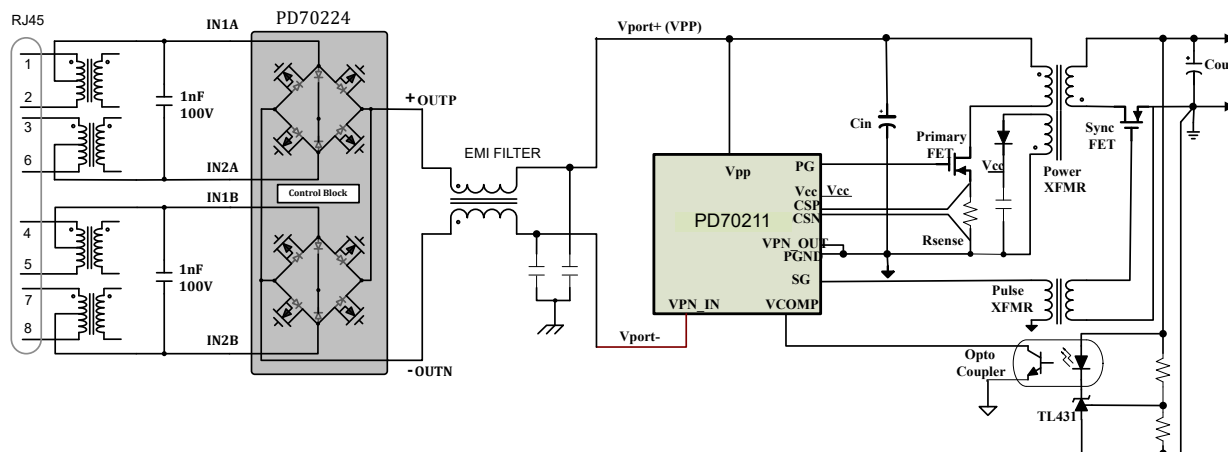
2. Power Flow in PD70211-Based Systems

A PD is comprised of the following generic stages:

- Input stage
- DC-DC converter stage
- Output stage

The following figure shows the current flow through these stages for a PD70211-based flyback converter. The stages are discussed in the subsequent sections.

Figure 2-1. Power Flow in a Typical PD70211-Based System



2.1 Input Stage

Input stage includes the following elements:

- Input RJ45 connectors
- Line transformer
- Diode bridge
- Common mode filter
- PD70210/A/AL or PD70211 device
- Bulk capacitor for DC-DC input filter

In this set of elements, the current is DC (non-switched), except for detection/classification and initial power up.

The first four elements must be placed next to each other to enable the common mode choke to filter the noise close to the RJ45 connector.

For low EMI radiation design, the positive and the negative rails must run parallel as close as possible to each other.

Among the above elements, the diode bridges and PD device are the main parts that dissipate power and get heated. These parts should have sufficient copper lands for heat sinking according to their datasheet recommendations.

Surge protection components must have the shortest possible path to input RJ45 connector and to earth ground, and must be physically located before the rectifier bridge and the remaining downstream components.

2.2 PD Controller 70210/A/AL or PD70211

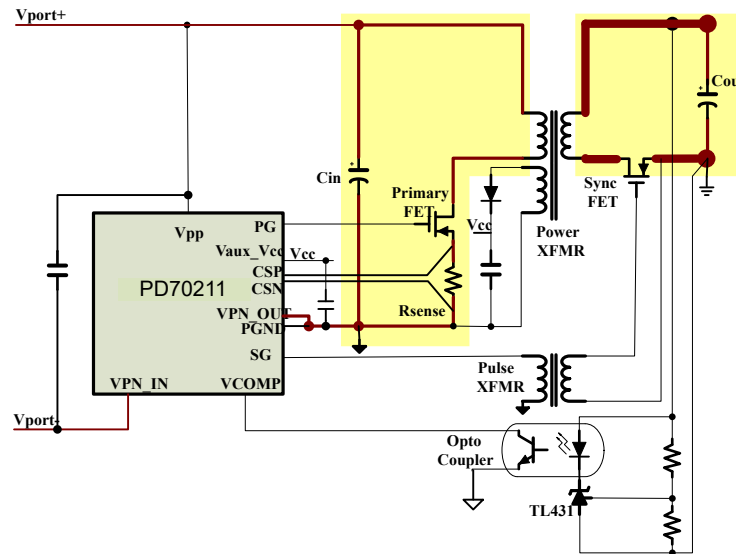
PD70210/A/AL or PD70211 power dissipation is mainly a function of the device's internal pass FET resistance and system current.

$$P = R_{ds(on)} \times (\text{Max current})^2$$

- Place both the PD chip and its peripheral at the top so that the bottom layer is used as a heat dissipation layer.
- Vias under the device are used for heat transfer between layers.
- If there are inner layers, use them too for the extended copper land under the device to improve heat dissipation.
- Place a 0.82 uF/100V ceramic capacitor between VPP and VPN_IN (pins 32 and 8-9 of PD70211 or pins 1 and 7-8 of PD70210/A/AL) as close as possible to the chip.
- Place a 4.7 uF/25V ceramic bypass capacitor between Vaux_Vcc pins and PGND as close as possible to the chip.

DC-DC section contains the high-frequency high-current switching loops as shown in the following figure.

Figure 2-2. High-Current Traces Layout



2.3 Sense Resistors

The primary loop current is sensed using $1\% \pm 100$ ppm low resistance resistors connected as shunt.

The following figure shows the proper way to layout the power supply sense resistors.

The designer must calculate the power dissipation of the sense resistor and choose the resistor size and the number of paralleled resistors according to the calculation result.

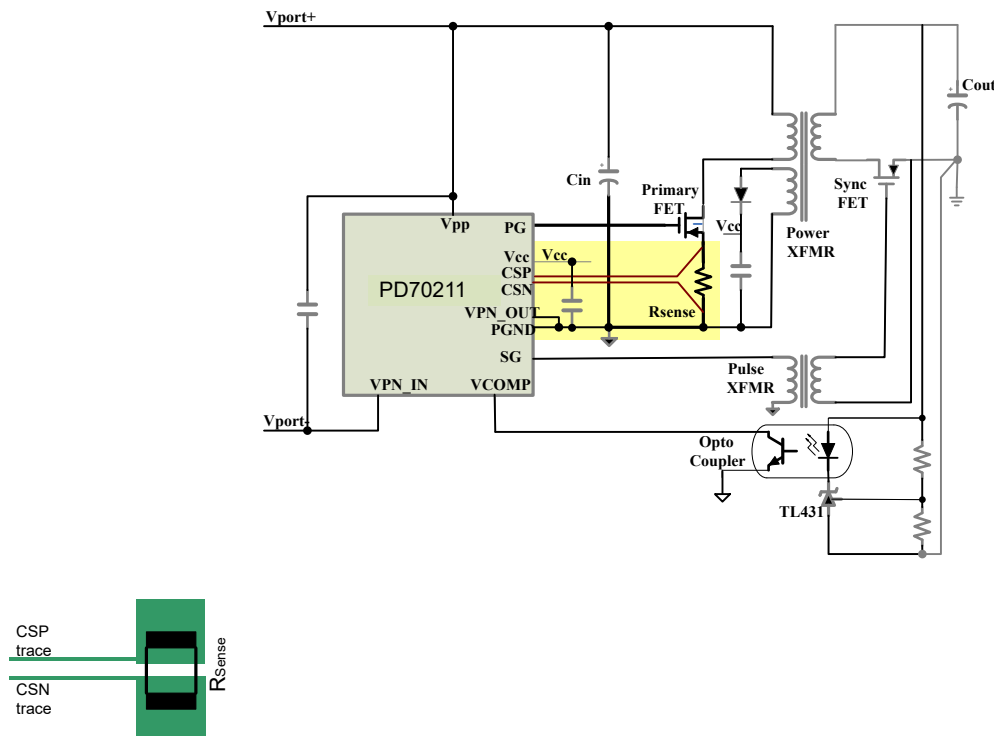
The voltage of the sense resistor is between 0 mV to 200 mV and exists in an environment of fast transitions of up to 180V. The form of the current sense signal is very important and its integrity must be maintained.

Therefore, the sense voltage traces layout must be maintained carefully. In order to simplify the integrity challenge, PD70211 has a differential sampling mechanism built of pins CSP and CSN.

Route differential traces from the sense resistor terminals to the CSN and the CSP input pins. They must be connected as a Kelvin connection, as close as possible to the resistors pads, and must not be part of the high current path to the resistors. This way, voltage measurement is not influenced by voltage drop on the high-power traces.

These two sense lines must be routed together close to each other to maintain good noise immunity. For the resistor high-current trace, use a wide trace or copper planes to decrease the trace voltage drop.

Figure 2-3. Sense Resistor Layout



2.4 Primary and Secondary MOSFETs

Primary and secondary MOSFETs are high-power devices. These devices must have sufficient copper lands to enable heat transfer from their junctions to the environment.

Copper land is a function of the MOSFET package power dissipation, junction to pad and junction to ambient thermal resistances, ambient temperature, and the system requirements.

For a given application, ensure to calculate power dissipation in the MOSFETs and choose their package and thermal pad size according to calculation results.

Note: Refer to the MOSFET manufacturers information for the required thermal pads. As a rule of thumb, power semiconductors in PD applications require 1 x 1" thermal pad preferably with vias to additional copper pads on other layers.

2.5 Isolation

For an isolated DC-DC design such as Flyback, isolation level is based on IEEE 802.3at standard.

IEEE 802.3at standard defines 1500Vrms isolation to be obtained between all the accessible external conductors including frame ground (if any), RJ45 connector leads, and all the internal leads of the PD such as secondary side traces.

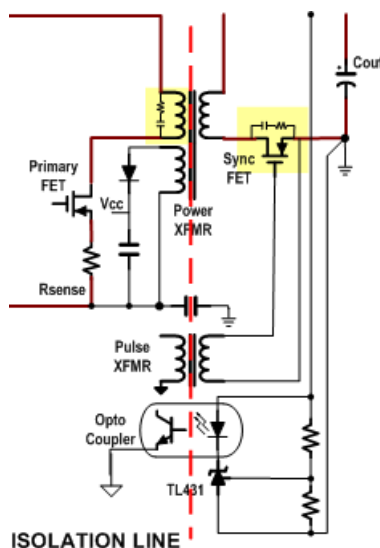
The isolation should be maintained between the DC-DC converter primary and secondary sides and between the frame ground and primary side.

1500Vrms isolation is obtained by having a gap of 60 mil between the traces of the primary domain and the secondary domain and the frame.

The isolation line must include power transformer, secondary gate pulse transformer, opto-couplers, and primary/secondary 2000V capacitor. The capacitor must be located close to the power transformer to help lowering conducted emission. Do not mix layout of the two isolated sides. Mixing the sides on PCB may cause unwanted signals coupling and difficulty in maintaining the isolation.

Use a physical isolation line as shown by dashed red line in the following figure.

Figure 2-4. An Example of the Isolation Line



From EMI standpoint, there must not be any copper planes, traces, and components under the power transformer and the power inductors (if any).

2.6 Driving MOSFETs

Gate drive pulses are supplied to the primary and the secondary gates and are generated by the PWM controller section of the PD70211 device.

In order to increase efficiency and decrease the temperature rise of the MOSFETs, a fast slew rate pulses should be obtained.

The PD70211 device drivers have internal serial output resistance. To overcome this internal resistance and also the distance of the controller from the MOSFETs, additional driving components may be used (for example, see *PD70211evb51F-12* user guide). For proper operation of the driving elements, pull up transistor, pull down transistor, and bypass capacitor should be as close as possible to the referenced FET.

2.7 Snubbers

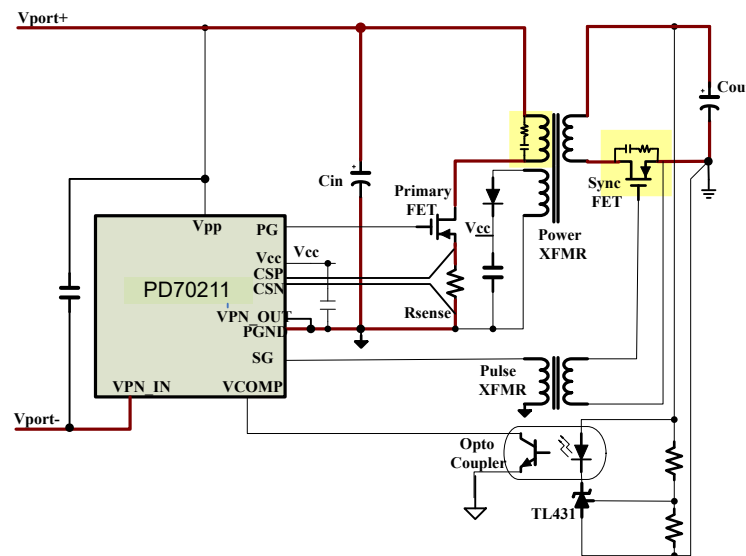
Snubbers are elements that are aimed to protect MOSFETs from high voltage spikes that are produced due to system parasitic, primarily transformer leakage inductance.

To lower the primary side spikes, a snubber is placed parallel to the primary winding as close as possible to it. This is very important to minimize the voltage spikes on the Drain-Source of the primary MOSFET.

The best location for primary snubber is in the bottom side under the transformer that yields a low inductance connection. The snubber can be comprised of serial resistor and capacitor (RC), resistor-capacitor-diode (RCD), or active snubber that also uses inductor.

The secondary side snubber is usually an RC snubber. It should be located very close to the secondary MOSFET, between its drain and source.

Figure 2-5. Snubbers Location



2.8 Heat Sinking

The components that dissipate the major portion of power and as a result heat up are:

- Input bridge
- Primary MOSFET
- Secondary MOSFET(s)
- Power transformer
- PD70211 device
- Primary snubber components
- Secondary snubber components

Board design should provide an adequate copper lands for dissipating the heat of those components.

3. References

- *PD70210/PD70210A/PD70210AL datasheet*
- *PD70211 datasheet*
- *PD70211EVB51F12_UG evaluation board user guide*
- *AN3468, Designing a Type 1/2 802.3 or HDBaseT Type 3 Powered Device Front End Using PD702x0 and PD701x0 ICs*
- *AN3471, Designing a Type 1/2 802.3 or HDBaseT Type 3 Powered Device Using PD702x1 and PD701x1 ICs*

4. Revision History

Revision	Date	Description
A	July 2020	The following is a summary of changes in revision A of this document. <ul style="list-style-type: none">• The document was migrated to Microchip template.• The document number was updated from AN-222 to AN3533.
1.01	September 2016	Fixed errors
1.0	July 2016	Initial Release – preliminary version

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