SAM R34/R35

SAM R34/R35 Errata Sheet

SAM R34/R35 Errata

The SAM R34/ R35 family of devices conform functionally to the current device data sheet, except for the anomalies described in this document.

The SAM R34/R35 contains a SAML21 ARM® Cortex®-M0+ processor and UHF Transceiver (SX1276)

For Errata information on UHF Transceiver – refer to SX1276 Errata Note.

Note: This document summarizes all silicon errata issues seen on SAM R34/R35 devices, revision C.

Table 1. SAM R34/35 Silicon Device Identification

Part Number	Device Identification (DID[31:0])	Revision ID (DID.REVISION[3:0])
		C
ATSAMR34J18B	0x10810x28	0x2
ATSAMR34J17B	0x10810x29	
ATSAMR34J16B	0x10810x2A	
ATSAMR35J18B	0x10810x2B	
ATSAMR35J17B	0x10810x2C	
ATSAMR35J16B	0x10810x2D	

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1. Silicon Errata Summary

Table 1-1. Silicon Errata Summary

Module	Feature	Issue Summary	C
2.1 Device Service Unit (DSU)	Wake up From Standby Retention Mode	When device is waking from Standby Retention mode, selected alternate function on PA30 (for example, SERCOM) will be lost and it functions as the SWCLK pin and can switch device to Debug mode. See 2.1.1 Wake-up From Standby Retention Mode Reference:16144.	X
2.2 48 MHz Digital Frequency-Locked Loop (DFLL48M)	Write Access to DFLL Register	The DFLL clock must be requested before being configured, otherwise a write access to a DFLL register can freeze the device. See 2.2.1 Write Access to DFLL Register Reference:9905.	X
2.2 48 MHz Digital Frequency-Locked Loop (DFLL48M)	Out of Bounds Interrupt	If the DFLL48M reaches the maximum or minimum COARSE or FINE calibration values during the locking sequence, an out of bounds interrupt will be generated. See 2.2.2 Out of Bounds Interrupt Reference:16192.	X
2.2 48 MHz Digital Frequency-Locked Loop (DFLL48M)	DFLL Status Bit in USB Clock Recovery Mode	The DFLL status bits in the STATUS register, during the USB clock recovery mode, can be wrong after a USB suspend state. (Only Applicable to SAM R34 device variants). See 2.2.3 DFLL Status Bit in USB Clock Recovery Mode (Only Applicable to SAM R34 Device Variants) Reference:16193 .	X
2.3 Direct Memory Access Controller (DMAC)	Linked Descriptor	When using many DMA channel, if one of these DMA channels has a linked descriptor, a fetch error can appear on this channel. See 2.3.1 Linked Descriptor Reference:15670.	X
2.3 Direct Memory Access Controller (DMAC)	Linked Descriptors	When at least one channel using linked descriptors is already active, enabling another DMA channel (with or without linked descriptors) can result in a channel Fetch Error (FERR) or an incorrect descriptor fetch. See 2.3.2 Linked Descriptors Reference:15683.	X
2.4 96 MHz Fractional Digital Phase Locked Loop (FDPLL96M)	DPLLRATIO Register	When FDPLL ratio value in the DPLLRATIO register is changed on the fly, the STATUS.DPLLLDRTO will not be set even though the ratio is updated. See 2.4.1 DPLLRATIO Register Reference:15753.	X

Module	Feature	Issue Summary	C
...........continued			
2.5 PORT - I/O Pin Controller	PORT Read/Write on Non-Implemented Register	PORT read/write attempts on non-implemented registers, including addresses beyond the last implemented register group (PA, PB), do not generate a PAC protection error. See 2.5.1 PORT Read/Write on Non-Implemented Register Reference:15611.	X
2.5 PORT - I/O Pin Controller	Pull-up and Pull-down Configurations on PA24 and PA25 Pins	On PA24 and PA25 pins, the pull-up and pull-down configuration is not disabled automatically when alternative pin function is enabled. See 2.5.2 Pull-up and Pull-down Configurations on PA24 and PA25 Pins Reference:15581.	X
2.6 Supply Controller (SUPC)	Buck Converter Mode	Digital Phase-Locked Loop (FDPLL96M) and Digital Frequency-Locked Loop (DFLL48M) PLL's cannot be used with main voltage regulator in Buck converter mode. See 2.6.1 Buck Converter Mode Reference: CHIP003-311 & CHIP003-314.	X
2.6 Supply Controller (SUPC)	Buck Converter as a Main Voltage Regulator	When Buck converter is set as main voltage regulator (SUPC.VREG.SEL=1), the microcontroller can freeze when leaving Standby mode. See 2.6.2 Buck Converter as a Main Voltage Regulator Reference:15264.	X
2.7 Analog-to-Digital Controller (ADC)	ADC Result in Unipolar Mode	The LSB of ADC result is stuck at zero in Unipolar mode for 8-bit and 10-bit resolution. See 2.7.1 ADC Result in Unipolar Mode Reference:14431.	X
2.7 Analog-to-Digital Controller (ADC)	Free-Running Mode	In Standby Sleep mode when the ADC is in free-running mode (CTRLC.FREERUN=1) and the RUNSTDBY bit is set to 0 (CTRLA.RUNSTDBY=0), the ADC keeps requesting its generic clock. See 2.7.2 Free-Running Mode Reference:15463.	X
2.7 Analog-to-Digital Controller (ADC)	SYNCBUSY.SWTRIG Bit	ADC SYNCBUSY.SWTRIG get stuck to one after wake-up from Standby Sleep mode. See 2.7.3 SYNCBUSY.SWTRIG Bit Reference:16027.	X
2.8 Timer/Counter (TC)	SYNCBUSY Flag	When clearing the STATUS.PERBUFV flag / STATUS.CCBUFx flag, the SYNCBUSY flag is released before the PERBUF / CCBUFx register is restored to its appropriate value. See 2.8.1 SYNCBUSY Flag Reference:15056.	X

	Module	Feature	Issue Summary	C
...........continued				
	2.9 Timer/ Counter for Control Applications (TCC)	Advance Capture Mode	Advance Capture mode (CAPTMIN CAPTMAX LOCMIN LOCMAX DERIV0) doesn't work if an upper channel is not in one of these modes. See 2.9.1 Advance Capture Mode Reference:14817.	X
	2.9 Timer/ Counter for Control Applications (TCC)	SYNCBUSY Flag	When clearing the STATUS.xxBUFV flag, SYNCBUSY is released before the register is restored to its appropriate value. See 2.9.2 SYNCBUSY Flag Reference:15057.	X
	2.9 Timer/ Counter for Control Applications (TCC)	MAX Capture Mode	In Capture mode while using max Capture mode, with the timer set in Up-Counting mode, if an input event occurred within two cycles before TOP, the value captured is zero instead of TOP. See 2.9.3 MAX Capture Mode Reference:15059.	X
	2.9 Timer/ Counter for Control Applications (TCC)	Dithering Mode	Using TCC in Dithering mode with external retrigger events can lead to unexpected stretch of right aligned pulses or shrink of left aligned pulses. See 2.9.4 Dithering Mode Reference:15625.	X
	2.10 Serial Communication Interface (SERCOM)	USART in Auto-Baud Mode	In USART Auto-Baud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors. See 2.10.1 USART in Auto-Baud Mode Reference:13852.	X
	2.10 Serial Communication Interface (SERCOM)	SDA and SCL Fall Time	When configured in HS or FastMode+, SDA and SCL fall times are shorter than I2C specification requirement and can lead to reflection. See 2.10.2 SDA and SCL Fall Time Reference:16225.	X
	2.11 External Interrupt Controller (EIC)	EIC_ASYNCH Register	Access to the EIC_ASYNCH register in 8-bit or 16-bit mode is not functional. See 2.11.1 EIC_ASYNCH Register Reference:14417.	X
	2.11 External Interrupt Controller (EIC)	Low Level or Rising Edge or Both Edges	When the EIC is configured to generate an interrupt on a low level or rising edge or both edges (CONFIGn.SENSEx) with the filter enabled (CONFIGn.FILTENx), a spurious flag might appear. See 2.11.2 Low Level or Rising Edge or Both Edges Reference:15278.	X
	2.11 External Interrupt Controller (EIC)	NMI Configuration	Changing the NMI configuration (CONFIGn.SENSEx) on the fly may lead to a false NMI interrupt. See 2.11.3 NMI Configuration Reference:15279.	X

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Module	Feature	Issue Summary	C
2.11 External Interrupt Controller (EIC)	Asynchronous Edge Detection	When the asynchronous edge detection is enabled, and the system is in Standby mode, only the first edge will generate an event. See 2.11.4 Asynchronous Edge Detection Reference:16103.	X
2.12 True Random Number Generator (TRNG)	Power Consumption in Standby Mode	When TRNG is enabled with configuration CTRL.RUNSTDBY = 0 (disabled during sleep), it could continue to operate resulting in over-consumption (~50uA) in Standby mode. See 2.12.1 Power Consumption in Standby Mode Reference: 14827.	X
2.13 Event System (EVSYS)	Synchronous Path	Using synchronous, spurious overrun can appear with generic clock for the channel always on. See 2.13.1 Synchronous Path Reference:14532.	X
2.13 Event System (EVSYS)	Overrun Flag	The acknowledge between an event user and the EVSYS clears the CHSTATUS.CHBUSYn bit before this information is fully propagated in the EVSYS one GCLK_EVSYS_CHANNEL_n clock cycle later which triggers and overrun flag. See 2.13.2 Overrun Flag Reference:14835.	X

2. Silicon Errata Issues

The following issues apply to the SAM R34/R35 family of devices.

2.1 Device Service Unit (DSU)

2.1.1 Wake-up From Standby Retention Mode Reference:16144

When device is waking from Standby Retention mode, selected alternate function on PA30 (for example, SERCOM) will be lost and it functions as the SWCLK pin and can switch device to Debug mode.

Workaround

Disable the debugger hot plug-in detection by setting the security bit. Security is set by issuing the NVMCTRL SSB command.

2.2 48 MHz Digital Frequency-Locked Loop (DFLL48M)

2.2.1 Write Access to DFLL Register Reference:9905

The DFLL clock must be requested before being configured, otherwise a write access to a DFLL register can freeze the device.

Workaround

Write a zero to the DFLL ONDEMAND bit in the DFLLCTRL register before configuring the DFLL module.

2.2.2 Out of Bounds Interrupt Reference:16192

If the DFLL48M reaches the maximum or minimum COARSE or FINE calibration values during the locking sequence, an out of bounds interrupt will be generated. These interrupts will be generated even if the final calibration values at DFLL48M lock are not at maximum or minimum, and might therefore be false out of bounds interrupts.

Workaround

Check the lock bits, DFLLLCKC and DFLLLCKF, in the OSCCTRL Interrupt Flag Status and Clear register (INTFLAG) are both set before enabling the DFLLOOB interrupt.

2.2.3 DFLL Status Bit in USB Clock Recovery Mode (Only Applicable to SAM R34 Device Variants) Reference:16193

During the USB Clock Recovery mode, the DFLL status bits in the STATUS register can be wrong after a USB suspend state.

Workaround

Do not monitor the DFLL status bits in the STATUS register during the USB Clock Recovery mode.

2.3 Direct Memory Access Controller (DMAC)

2.3.1 Linked Descriptor Reference:15670

When using many DMA channel, if one of these DMA channels has a linked descriptor, a fetch error can appear on this channel.

Workaround

Do not use linked descriptors, instead make a software link. Replace the channel which used the linked descriptor by a two-channel DMA (with linked descriptor disabled) handled by a two-channel event system:

- DMA channel 0 transfer completion can send a conditional event for DMA channel 1 (through event system with configuration of BTCTRL.EVOSEL=BLOCK for channel 0 and configuration CHCTRLB.EVACT=CBLOCK for channel 1)
- On the transfer complete reception of the DMA channel 0, immediately re-enable the channel 0
- Then DMA channel 1 transfer completion can send a conditional event for DMA channel 0 (through event system with configuration of BTCTRL.EVOSEL=BLOCK for channel 1 and configuration CHCTRLB.EVACT=CBLOCK for channel 0)
- On the transfer complete reception of the DMA channel 1, immediately re-enable the channel 1
- The mechanism can be launched by sending a software event on the DMA channel 0

2.3.2 Linked Descriptors Reference:15683

When at least one channel using linked descriptors is already active, enabling another DMA channel (with or without linked descriptors) can result in a channel Fetch Error (FERR) or an incorrect descriptor fetch.

This happens if the channel number of the channel being enabled is lower than the channel already active.

Workaround

When enabling a DMA channel while other channels using linked descriptors are already active, the channel number of the new channel enabled must be greater than the other channel numbers.

2.4 96 MHz Fractional Digital Phase Locked Loop (FDPLL96M)

2.4.1 DPLLRATIO Register Reference:15753

When FDPLL ratio value in the DPLLRATIO register is changed on the fly, the STATUS.DPLLLDRTO will not be set even though the ratio is updated.

Workaround

Monitor the INTFLAG.DPLLLDRTO instead of STATUS.DPLLLDRTO to get the status for DPLLRATIO update.

2.5 PORT - I/O Pin Controller

2.5.1 PORT Read/Write on Non-Implemented Register Reference:15611

PORT read/write attempts on non-implemented registers, including addresses beyond the last implemented register group (PA, PB), do not generate a PAC protection error.

Workaround

None.

2.5.2 Pull-up and Pull-down Configurations on PA24 and PA25 Pins Reference:15581

On PA24 and PA25 pins, the pull-up and pull-down configuration is not disabled automatically when alternative pin function is enabled.

Workaround

For PA24 and PA25 pins, the GPIO pull-up and pull-down must be disabled before enabling alternative functions on them.

2.6   Supply Controller (SUPC)

2.6.1   Buck Converter Mode Reference: CHIP003-311 & CHIP003-314

Buck Converter mode is not supported when using FDPLL96M and DFLL48M. As a result, Table 46-7 and Table 47-2 "Active Current Consumption - Active Mode" data for Buck Converter mode with DFLL48M configuration is not valid and must be disregarded.

Workaround

Use the LDO Regulator mode when using FDPLL and DFLL.

2.6.2   Buck Converter as a Main Voltage Regulator Reference:15264

When Buck converter is set as main voltage regulator (SUPC.VREG.SEL=1), the microcontroller can freeze when leaving Standby mode.

Workaround

Enable the main voltage regulator in Standby mode (SUPC.VREG.RUNSTDBY=1) and set the standby in PL0 bit to one (SUPC.VREG.STDBYPL0=1).
Note: When SUPC.VREG.STDBYPL0=1, in Standby Sleep mode, the voltage regulator is used in PL0.

2.7   Analog-to-Digital Controller (ADC)

2.7.1   ADC Result in Unipolar Mode Reference:14431

The LSB of ADC result is stuck at zero in Unipolar mode for 8-bit and 10-bit resolution.

Workaround

Use 12-bit resolution and take only least 8 bits or 10 bits, if necessary.

2.7.2   Free-Running Mode Reference:15463

In Standby Sleep mode when the ADC is in free-running mode (CTRLC.FREERUN=1) and the RUNSTDBY bit is set to 0 (CTRLA.RUNSTDBY=0), the ADC keeps requesting its generic clock.

Workaround

Stop the free-running mode (CTRLC.FREERUN=0) before entering Standby Sleep mode.

2.7.3   SYNCBUSY.SWTRIG Bit Reference:16027

ADC SYNCBUSY.SWTRIG get stuck to one after wake-up from Standby Sleep mode.

Workaround

Ignore ADC SYNCBUSY.SWTRIG status when waking up from Standby Sleep mode. ADC result can be read after INTFLAG.RESRDY is set. To start the next conversion, write a '1' to SWTRIG.START.

2.8 Timer/Counter (TC)

2.8.1 SYNCBUSY Flag Reference:15056

When clearing the STATUS.PERBUFV flag / STATUS.CCBUFx flag, the SYNCBUSY flag is released before the PERBUF / CCBUFx register is restored to its appropriate value.

Workaround

Clear successively twice, the STATUS.PERBUFV flag / STATUS.CCBUFx flag to ensure that, the PERBUF / CCBUFx register value is properly restored before updating it.

2.9 Timer/Counter for Control Applications (TCC)

2.9.1 Advance Capture Mode Reference:14817

Advance Capture mode (CAPTMIN CAPTMAX LOCMIN LOCMAX DERIV0) doesn't work if an upper channel is not in one of these modes, for example, when CC[0]=CAPTMIN, CC[1]=CAPTMAX, CC[2]=CAPTEN, and CC[3]=CAPTEN, CAPTMIN and CAPTMAX won't work.

Workaround

Basic Capture mode must be set in the lower channel and Advance Capture mode in the upper channel. Example: CC[0]=CAPTEN , CC[1]=CAPTEN , CC[2]=CAPTMIN, CC[3]=CAPTMAX

All capture will be done as expected.

2.9.2 SYNCBUSY Flag Reference:15057

When clearing the STATUS.xxBUFV flag, SYNCBUSY is released before the register is restored to its appropriate value.

Workaround

To ensure that the register value is properly restored before updating this same register through xx or xxBUF with a new value, the STATUS.xxBUFV flag must be cleared twice.

2.9.3 MAX Capture Mode Reference:15059

In Capture mode while using max Capture mode, with the timer set in Up-Counting mode, if an input event occurred within two cycles before TOP the value captured is zero instead of TOP.

Workaround

Two possible options are as follows:

1. If event is controllable, the capture event should not occur when counter is within 2 cycles before TOP value.
2. Use timer in down Counter mode and capture MIN value instead of MAX.

2.9.4 Dithering Mode Reference:15625

Using TCC in Dithering mode with external retrigger events can lead to an unexpected stretch of right-aligned pulses or shrink of left-aligned pulses.

Workaround

Do not use retrigger events or actions when TCC is configured in Dithering mode.

2.10 Serial Communication Interface (SERCOM)

2.10.1 USART in Auto-Baud Mode Reference:13852

In USART Auto-Baud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors.

Workaround

None

2.10.2 SDA and SCL Fall Time Reference:16225

When configured in HS or FastMode+, SDA and SCL fall times are shorter than I2C specification requirement and can lead to reflection.

Workaround

When reflection is observed a 100 ohms serial resistor can be added on the impacted line.

2.11 External Interrupt Controller (EIC)

2.11.1 EIC_ASYNCH Register Reference:14417

Access to the EIC_ASYNCH register in 8-bit or 16-bit mode is not functional.

Workaround

- Writing in 8-bit mode also writes this byte in all bytes of the 32-bit word.
- Writing higher 16-bits also writes the lower 16-bits
- Writing lower 16-bits also writes the higher 16-bits The following two workarounds are available:
- Use 32-bit Write mode
- Write only lower 16-bits (This will write upper 16-bits also, but does not impact the application).

2.11.2 Low Level or Rising Edge or Both Edges Reference:15278

When the EIC is configured to generate an interrupt on a low level or rising edge or both edges (CONFIGn.SENSEx) with the filter enabled (CONFIGn.FILTENx), a spurious flag might appear for the dedicated pin on the INTFLAG.EXTINT[x] register immediately the EIC is enabled using the CTRLA ENABLE bit.

Workaround

Clear the INTFLAG bit once the EIC is enabled and before enabling the interrupts.

2.11.3 NMI Configuration Reference:15279

Changing the NMI configuration (CONFIGn.SENSEx) on the fly may lead to a false NMI interrupt.

Workaround

Clear the NMIFLAG bit once the NMI has been modified.

2.11.4 Asynchronous Edge Detection Reference:16103

When the asynchronous edge detection is enabled, and the system is in Standby mode, only the first edge will generate an event. The following edges will not generate events until the system wakes up.

Workaround

Asynchronous edge detection does not work; instead, use the synchronous edge detection (ASYNCH.ASYNCH[x]=0). To reduce power consumption when using synchronous edge detection, either set the GCLK_EIC frequency as low as possible or select the ULP32K clock (EIC CTRLA.CKSEL=1).

2.12 True Random Number Generator (TRNG)

2.12.1 Power Consumption in Standby Mode Reference:14827

When TRNG is enabled with configuration CTRL.RUNSTDBY = 0 (disabled during sleep), it could still continue to operate resulting in over-consumption (~50uA) in Standby mode.

Workaround

Disable the TRNG before entering Standby mode.

2.13 Event System (EVSYS)

2.13.1 Synchronous Path Reference:14532

Using synchronous, spurious overrun can appear with generic clock for the channel always on.

Workaround

- Request the generic clock on demand by setting the CHANNEL.ONDEMAND bit to one
- No penalty is introduced

2.13.2 Overrun Flag Reference:14835

The acknowledge between an event user and the EVSYS clears the CHSTATUS.CHBUSYn bit before this information is fully propagated in the EVSYS one GCLK_EVSYS_CHANNEL_n clock cycle later. As a consequence, any generator event occurring on that channel before that extra GCLK_EVSYS_CHANNEL_n clock cycle will trigger the overrun flag.

Workaround

For applications using event generators other than the software event, monitor the OVR flag.

For applications using the software event generator, wait one GCLK_EVSYS_CHANNEL_n clock cycle after the CHSTATUS.CHBUSYn bit is cleared before issuing a software event.

3. Revision History

Revision	Date	Section	Description
A	05/2019	All	Initial Revision

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