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How to Design Buck-Boost Converter Using MCP19061

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BASIC OPERATION OF A FOUR SWITCH BUCK-BOOST CONVERTER

A four-switch buck-boost converter is a versatile DC-DC converter that can efficiently step up or step down the input voltage to maintain a stable output voltage. It uses four switches (typically MOSFETs) to control the power flow and can operate in three distinct modes: buck, boost, and buck-boost. The following sections detail the operation of the converter in each mode.

Buck Mode (VIN > VOUT)

Active Switches: The left leg of the converter is active.

High-Side Switch (SW1): ON during the energy storage phase.

Low-Side Switch (SW2): OFF during the energy storage phase, ON during the energy release phase.

Inactive Switches: The right leg of the converter is not actively switching but still plays a role in power transfer.

High-Side Switch (SW3): ON to provide a path for current to the output.

Low-Side Switch (SW4): OFF.

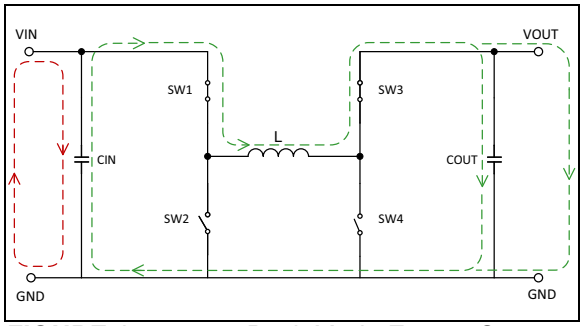

FIGURE 1: *Buck Mode Energy Storage Phase.*

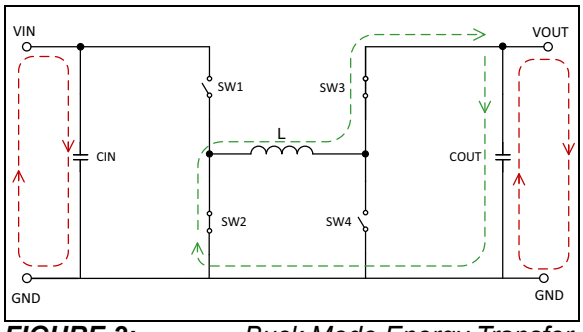

FIGURE 2: *Buck Mode Energy Transfer Phase.*

Boost Mode (VIN < VOUT)

Active Switches: The right leg of the converter is active.

High-Side Switch (SW3): ON during the energy release phase.

Low-Side Switch (SW4): OFF during the energy release phase, ON during the energy storage phase.

Inactive Switches: The left leg of the converter is not actively switching but still plays a role in power transfer.

High-Side Switch (SW1): ON to provide a path for current from the input.

Low-Side Switch (SW2): OFF.

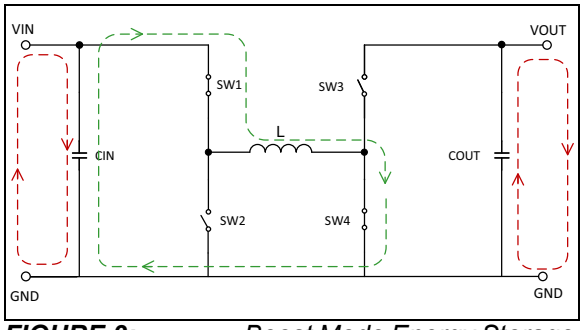

FIGURE 3: *Boost Mode Energy Storage Phase.*

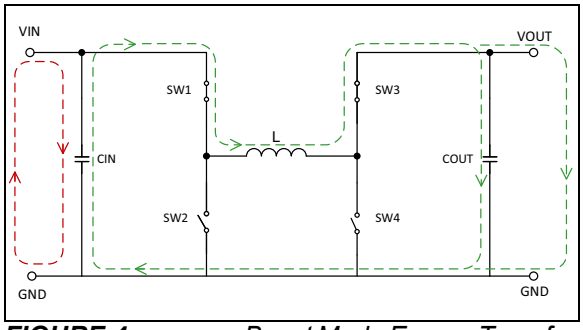

FIGURE 4: *Boost Mode Energy Transfer Phase.*

Buck-Boost Mode (VIN ≈ VOUT)

Active Switches: Both legs of the converter are active.

High-Side Switch (S1): ON during the buck phase.

Low-Side Switch (S2): OFF during the buck phase, ON during the boost phase.

High-Side Switch (S3): ON during the boost phase.

Low-Side Switch (S4): OFF during the boost phase, ON during the buck phase.

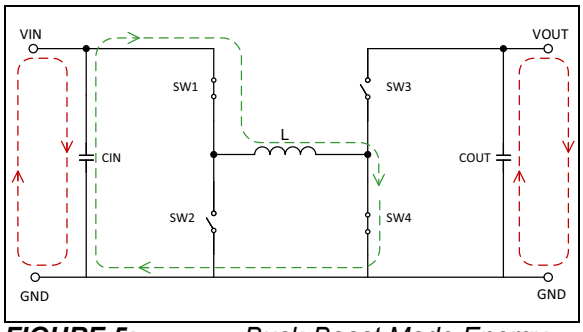

FIGURE 5: *Buck-Boost Mode Energy Storage Phase.*

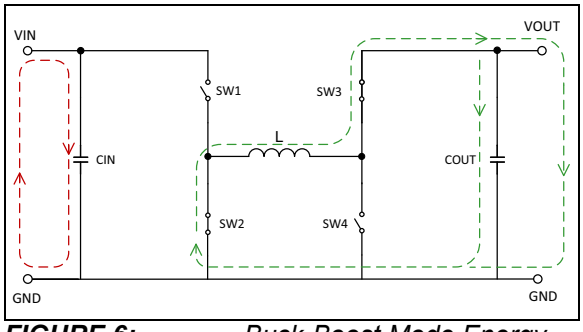

FIGURE 6: *Buck-Boost Mode Energy Transfer Phase.*

MCP19061 DESIGN EXAMPLE

To design the power stage using MCP19061, the following parameters are necessary:

1. Input Voltage Range
2. Nominal Output Voltage
3. Maximum Load Current
4. Switching Frequency

In this design example, let us assume:

- V_{IN_MIN} = 6V, V_{IN_NOM} = 12V, V_{IN_MAX} = 18V
- V_{OUT_NOM} = 12V
- I_{LOAD_MAX} = 5A
- F_{SW_NOM} = 450 kHz

DUTY CYCLE CALCULATION

In a non-inverting four-switch buck-boost converter, the duty cycle (D) is a crucial parameter that determines the relationship between the input voltage (V_{IN}) and the output voltage (V_{OUT}). The converter operates in Buck mode when the input voltage is higher than the output voltage, and Boost mode when the input voltage is lower than the output voltage. The duty cycle for each mode can be calculated using the following formulas:

EQUATION 1:

$$D_{Buck} = \frac{V_{OUT\_NOM}}{V_{IN\_MAX}}$$

EQUATION 2:

$$D_{Boost} = 1 - \frac{V_{IN\_MIN}}{V_{OUT\_NOM}}$$

In the Buck-Boost mode, the converter operates at approximately a 50% duty cycle. Considering our design parameters, the minimum duty cycle in buck mode is:

$$D_{Buck\_min} = \frac{12V}{18V} = 0.66$$

In Boost mode, the maximum duty cycle is calculated as follows:

$$D_{Boost\_max} = 1 - \frac{6V}{12V} = 0.5$$

For simplicity, the converter is assumed to operate at 100% efficiency. In practice, losses due to switching, conduction and other factors will reduce efficiency, but these are neglected in this analysis for ease of calculation.

INDUCTOR SELECTION

Selecting the appropriate inductor is critical for the efficient operation of a power converter. Key parameters to consider when selecting an inductor include inductance value, current rating, and core material.

Selecting a higher inductance value allows for a higher maximum output current, enhancing the converter's performance under heavy load conditions. Conversely, choosing a lower inductance value results in a smaller physical inductor size, contributing to a more compact overall solution.

The inductor value for Buck mode can be estimated using the following equation:

EQUATION 3:

$$L > \frac{V_{OUT\_NOM} \times (V_{IN\_MAX} - V_{OUT\_NOM})}{\Delta I \times F_{SW\_NOM} \times V_{IN\_MAX}}$$

ΔI is the inductor ripple current. A good design will have the inductor ripple current between 20% and 40% of the load current.

The inductor value for Boost mode can be estimated using the following equation:

EQUATION 4:

$$L > \frac{V_{IN\_MIN} \times (V_{OUT\_NOM} - V_{IN\_MIN})}{\Delta I \times F_{SW\_NOM} \times V_{OUT\_NOM}}$$

ΔI represents the inductor ripple current.

Considering an inductor ripple current of 30%, the calculated inductor values using Equations 3 and 4 are 5.9 µH and 4.4 µH, respectively. To ensure optimal performance, it is recommended to select an inductor value that is slightly higher than the calculated values. In this case, a standard available inductor value of 6.8 µH can be selected. It is important to note that the inductor must be able to handle the peak current without saturating. The peak inductor current can be calculated as:

EQUATION 5:

$$I_{Peak\_Buck} = I_{LOAD\_MAX} + \frac{\Delta I_{max}}{2}$$

EQUATION 6:

$$I_{Peak\_Boost} = I_{LOAD\_MAX} \times \left(\frac{V_{OUT\_NOM}}{V_{IN\_MIN}}\right) + \frac{\Delta I_{MAX}}{2}$$

MOSFET CURRENT

In the Buck mode, the maximum switch current can be calculated as:

EQUATION 7:

$$I_{FET\_BUCK\_Max} = I_{LOAD\_MAX} + \frac{\Delta I_{max}}{2}$$

Where,

$$\Delta I_{max} = \frac{V_{OUT\_NOM} \times (V_{IN\_MAX} - V_{OUT\_NOM})}{L \times F_{SW\_NOM} \times V_{IN\_MAX}}$$

In our example, with a 6.8 µH inductor the maximum calculated MOSFET current in Buck mode is 5.65A.

In Boost mode, the maximum switch current is the input current and not the maximum load current. The switch current is at its maximum when the input voltage is at its minimum, Therefore, the maximum switch current in Boost mode can be calculated as:

EQUATION 8:

$$I_{FET\_BOOST\_Max} = \frac{I_{LOAD\_MAX}}{1 - D_{Boost\_max}} + \frac{\Delta I_{max}}{2}$$

Where,

$$\Delta I_{max} = \frac{V_{IN\_MIN} \times (V_{OUT\_NOM} - V_{IN\_MIN})}{L \times F_{SW\_NOM} \times V_{OUT\_NOM}}$$

In our example, with a 6.8 µH inductor, the maximum calculated MOSFET current in Boost mode is 10.49A. When selecting a MOSFET, it is important to choose one with a current rating that exceeds the higher peak current value.

INPUT CAPACITOR

Input capacitors play two crucial roles in power supplies: energy storage and noise reduction. It is essential to maintain a stable input voltage regardless of fluctuations in output current or sudden drops in input voltage, such as those caused by automotive transients like cranking pulses at the battery terminals. To achieve this stability, bulk electrolytic capacitors are employed. Additionally, high di/dt from high-frequency switching and rapid rise and fall times generate noise on the input rail. To mitigate this noise, ceramic capacitors are typically used.

Selection of Ceramic Capacitors

The size of the ceramic capacitance will depend on the expected peak-to-peak ripple in the input voltage. For Buck mode, the capacitance can be calculated as:

EQUATION 9:

$$C_{in\_buck} = \frac{I_{LOAD\_MAX} \times D_{Buck\_min} \times (1 - D_{Buck\_min})}{F_{SW\_NOM} \times \Delta V_{in\_pk\_pk}}$$

The capacitance for Boost mode can be calculated using the following equation:

EQUATION 10:

$$C_{in\_boost} = \frac{I_{LOAD\_MAX} \times r}{8 \times F_{SW\_NOM} \times \Delta V_{in\_pk\_pk} \times (1 - D_{Boost\_max})}$$

Where:

Current Ripple Ratio, $r = \frac{\Delta I_{max}}{IL}$

IL = Average Inductor Current

Assuming a 100 mV peak-to-peak ripple in the input voltage:

$$C_{in\_buck} = 25\ \mu F$$

Assuming a 100 mV peak-to-peak ripple in the input voltage and a ripple current ratio of 30%:

$$C_{in\_boost} = 8.3\ \mu F$$

It is recommended to use capacitance values significantly higher than the calculated ones to compensate for any loss of capacitance due to DC bias.

Selection of Electrolytic Capacitors

Electrolytic bulk capacitors are essential for compensating for the increased energy demand during a sudden load step. Adequate bulk capacitance at the input ensures that the input voltage does not drop below a certain level, even during a sudden increase in load current. Additionally, these capacitors help prevent significant voltage drops during temporary dips in line voltage, maintaining stability for a fixed duration known as hold-up time.

ESTIMATION OF BULK CAPACITANCE BASED ON LOAD STEP

The total “extra” energy needed to transition from a lower load current to a higher load current can be expressed as:

EQUATION 11:

$$W = V_{OUT\_NOM} \times \Delta I_{LOAD} \times t$$

Where:

W	=	Work Done or Energy needed during the Load Step
V_{OUT_NOM}	=	Nominal Output Voltage
ΔI_{LOAD}	=	Difference between the New Load Current and the Original Load Current
t	=	Amount of Time the Input Voltage is allowed to dip by ΔV_{IN} and Recover

Therefore, the input bulk capacitors would need to provide a minimum of “W” amount of energy to sustain the load step for a duration “t,” leading to an acceptable drop of ΔV_{IN} on the input rail.

EQUATION 12:

$$\Delta V_{IN} = V_{IN\_INITIAL} - V_{IN\_FINAL}$$

To facilitate operation according to the above requirement, the difference between the initial and final energy must be equal to the energy stored by the capacitor. Therefore:

EQUATION 13:

$$W = \frac{1}{2} \times C_{bulk} \times V_{IN\_INITIAL}^{2} - \frac{1}{2} \times C_{bulk} \times V_{IN\_FINAL}^{2}$$

Let us now calculate the bulk capacitance based on our requirements. In Buck mode, assuming a load step of 1A to 3A and t = 50 µs, we get:

$$W = 12 \times (3 - 1) \times 50\ \mu s$$
$$W = 1.2\ mJ$$

Assuming $V_{IN\_INITIAL}$ = 18V and ΔV_{IN} = 500 mV, V_{IN_FINAL} = 17.5V, substitute these values in Equation 13 we get:

$$C_{bulk} = 135\ \mu F$$

It is crucial to recognize that electrolytic capacitors exhibit a broad range of tolerances. Therefore, it is advisable to select an appropriate value that is higher than the calculated requirement during the design process.

ESTIMATION OF BULK CAPACITANCE BASED ON HOLD-UP TIME

The approach remains the same as above. We must estimate the amount of energy that needs to be stored by the capacitor so that after time "t" our input voltage does not drop below a certain voltage, for example V_{IN_MIN}.

Assuming our starting voltage as V_{IN_NOM}, the amount of energy needed to be stored can be given by:

EQUATION 14:

$$W = \frac{1}{2} \times C_{bulk} \times V_{IN\_NOM}^{2} - \frac{1}{2} \times C_{bulk} \times V_{IN\_MIN}^{2}$$

Where:

W = P_{OUT} × t

P_{out} = Output Power

Let us now calculate the bulk capacitance based on our requirements, assuming I_{Load} of 2A and a hold-up time "t" of 10 ms.

$$P_{out} = V_{OUT\_NOM} \times I_{LOAD} = 24W$$

$$W = 240\ mJ$$

Considering starting voltage of V_{IN_NOM} and a maximum allowed dip up to V_{IN_MIN}, we get C_{bulk} as 4440 µF. This is a far too large value because $W \propto V^2$. Therefore, this may not be a feasible option for low-power designs, as results are unfeasibly large.

OUTPUT CAPACITOR

The output capacitor determines the desired ripple in the output voltage. For Buck mode, the capacitor value for the desired output ripple can be calculated using the following formula:

EQUATION 15:

$$C_{out\_buck} = \frac{\Delta I}{8 \times F_{SW\_NOM} \times \Delta V_{out\_Ripple}}$$

The output transient response also dictates the output capacitor value. Deviation in the output voltage is caused by the time it takes for the inductor to catch up with increased or decreased output current needs. In this case, the following formula should be used to calculate the necessary output capacitance for a desired maximum overshoot caused by the removal of the load current.

EQUATION 16:

$$C_{out\_overshoot} = \frac{I_{LOAD\_MAX}^{2} \times L}{2 \times V_{OUT\_NOM} \times \Delta V_{overshoot}}$$

In the case of a drop in output voltage due to a sudden increase in load, the capacitor value can be calculated for a maximum drop of ΔV_{droop} as:

EQUATION 17:

$$C_{out\_droop} = \frac{3 \times I_{LOAD\_MAX}}{2 \times F_{SW\_NOM} \times \Delta Vdroop}$$

In Boost mode the following equation can be used to adjust the output capacitor values for a desired output voltage ripple.

EQUATION 18:

$$C_{out\_boost} = \frac{I_{LOAD\_MAX} \times (1 - D_{Boost\_max})}{F_{SW\_NOM} \times \Delta V_{out\_Ripple}}$$

Based on the above equations, the maximum capacitance value calculated for our design parameters, with a ΔV_{out_Ripple} of 100 mV and both ΔV_{droop} and $\Delta V_{overshoot}$ of 500 mV, is 56 µF. When selecting a capacitor, it is advisable to choose one with a higher value, accounting for tolerance and the effects of DC bias.

LAYOUT GUIDELINES

The following image shows a typical layout for a Buck-Boost converter using MCP19061.

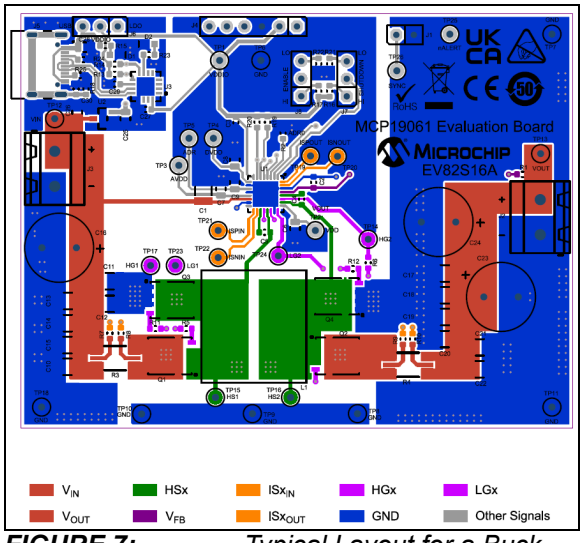

FIGURE 7: *Typical Layout for a Buck Boost Converter using MCP19061.*

The red traces represent the input (VIN) and output (VOUT) sides. The input capacitors should be placed between the input shunt resistor and the input connector. The output capacitors should be placed between the output shunt resistor and the output connector.

The orange traces represent the input and output current. It is measured using the ISPIN and ISNIN differential pair for the input side and the ISPOUT and ISNOUT differential pair on the output side.

Note:	A differential pair refers to two parallel signal traces with matched lengths and a characteristic impedance of 100Ω to the ground plane, designed to minimize EMI, crosstalk, and common-mode noise.

The phase (HSx) and bootstrap (HBx) signals are marked in green. The phase signals going to the controller should be as short as possible. It is recommended to route them on the same layer as the controller and the power train. The bootstrap capacitor should be placed as close to the controller as possible. The connection between the MOSFETs and the inductor should be kept small but large enough to dissipate the heat, depending on the power requirements of the board. If necessary, this connection can be doubled on another layer (especially when using more than two layers).

The magenta traces represent the MOSFET gate drivers (HGx for high-side and LGx for low-side) and should be kept reasonably short. Avoid routing them under the inductor and avoid making them too narrow in width.

The blue color represents the ground plane (GND). It is recommended to have a layer with an uninterrupted ground plane to which all the GND islands on other layers connect, in order to reduce noise propagation. For 2-layer PCBs, the bottom layer is usually selected. For 4-layer PCBs, it is recommended to use the first internal layer and the bottom layer as GND planes.

The input and output capacitors should be connected between the half bridge formed by the source of the low side MOSFET and the drain of the high side MOSFET, in the buck leg and boost leg, respectively.

The purple trace represents the positive voltage feedback (V_{FB}). Together with the negative trace (VOUT_REF), these should be connected after the output capacitors, usually next to the output connector.

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