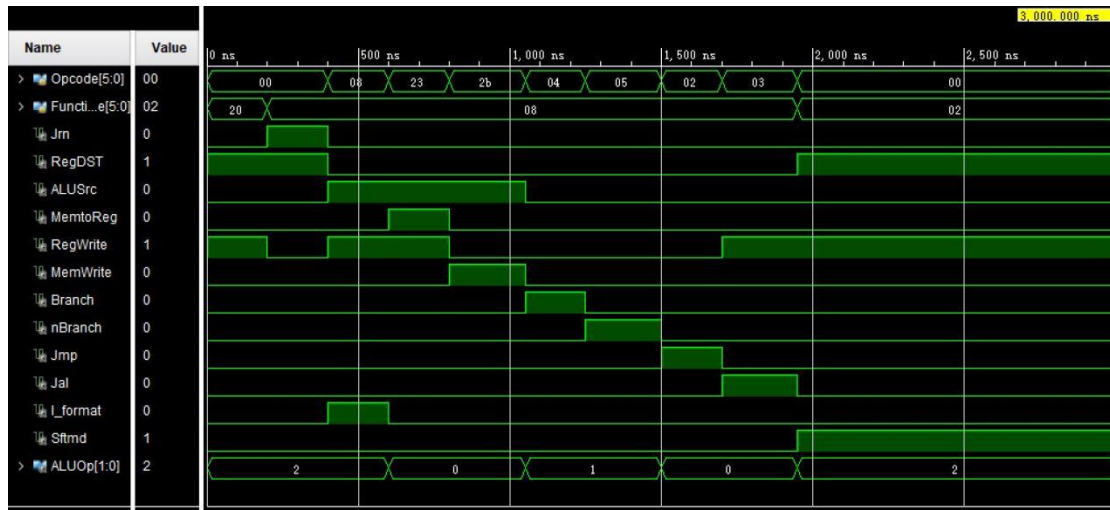


控制器的设计仿真时序

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1. 设计的控制单元的仿真波形图



2. control32.v

```
`timescale 1ns / 1ps
/////////////////////////////////////////////////////////////////
module
control32(Opcode,Function_opcode,Jrn,RegDST,ALUSrc,MemtoReg,RegWrite,M
emWrite,Branch,nBranch,Jmp,Jal,I_format,Sftmd,ALUOp);
    input[5:0]    Opcode;                // 来自取指单元 instruction[31..26]
    input[5:0]    Function_opcode;       // r-form instructions[5..0]
    output        Jrn;                   // jr
    output        RegDST;                // 为 1 时选 rd 为目标寄存器，为 0 选 rt
    output        ALUSrc;                // 决定第二个操作数是寄存器还是 imm
    output        MemtoReg;              // lw
    output        RegWrite;              // 写寄存器
    output        MemWrite;              // sw
    output        Branch;                // beq
    output        nBranch;               // bne
    output        Jmp;                   // j
    output        Jal;                   // jal
    output        I_format;              // 001xxx 的 I 型指令
    output        Sftmd;                 // 移位指令:sll,srl,sra
    output[1:0]   ALUOp;                 // lw,sw:00;beq,bne:01;R 型,I-format:10

    wire Jmp,I_format,Jal,Branch,nBranch;
    wire R_format,Lw,Sw;
```

```

//R 型指令:
assign R_format = (Opcode==6'b000000)? 1'b1:1'b0;      //R 型指令
assign RegDST = R_format;                               //说明目标是 rd, 否则是 rt
assign Jrn = (Opcode==6'b000000 && Function_opcode==6'b001000)?
1'b1:1'b0;

//I 型指令:I_format+Branch+nBranch+Lw+Sw
assign I_format = (Opcode[5:3]==3'b001)? 1'b1:1'b0;    //001xxx 的 I 型指令
assign Lw = (Opcode==6'b100011)? 1'b1:1'b0;           //lw 指令
assign Sw = (Opcode==6'b101011)? 1'b1:1'b0;           //sw 指令
assign Branch = (Opcode==6'b000100)? 1'b1:1'b0;       //beq 指令
assign nBranch = (Opcode==6'b000101)? 1'b1:1'b0;       //bne 指令

//J 型指令
assign Jmp = (Opcode==6'b000010)? 1'b1:1'b0;          //j 指令
assign Jal = (Opcode==6'b000011)? 1'b1:1'b0;          //jal 指令

assign RegWrite = (R_format&&!Jrn)||I_format||Lw||Jal;
assign MemtoReg = Lw;
assign MemWrite = Sw;
assign Sftmd = (Opcode==6'b000000)&&(Function_opcode[5:3]==3'b000);
assign ALUSrc = I_format||Lw||Sw;
assign ALUOp = {(R_format||I_format),(Branch||nBranch)};

endmodule

```