Latch-up Improvement For Tap Less Library Through Modified Decoupling Capacitors Cells

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CMOS technology has evolved as the top choice for chip manufacturers. There are multiple reasons for its emergence to its current status, continuous reduction in feature size being one of them. SoC manufacturers have always endeavored to reduce the feature size through technology and topology.

This article refers to a feature size reduction topology and resulting degradation in latch-up performance. The article proposes a layout for decoupling capacitors so as to improve the latch-up performance of the SoC.

To understand the issue in completeness, one needs to understand the basic layout of a CMOS Device (Fig 1) and the role played by the parasitic thyristor (fig 2) which may induce latch-up. This thyristor when triggered gives rise to a phenomenon called latch-up which causes heavy current flow from VDD to GND.

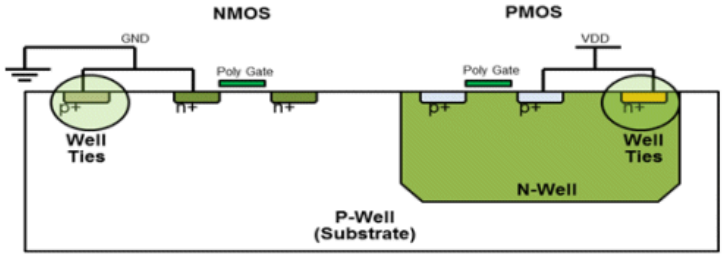

Fig 1: Fundamental Structure of CMOS Device

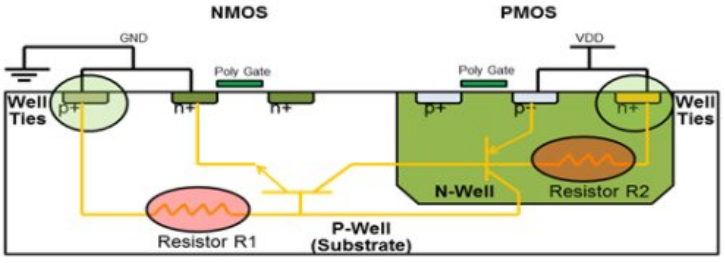

Fig 2: Parasitic Thyristor Formation

For detailed explanation of latch-up phenomenon, the reader is requested to refer other sources. To appreciate the proposal, it would suffice to know that any spurious current flow in well resistors R1 and R2, would develop a finite voltage across the Base-Emitter junction which may turn on any of the transistors and a positive feedback from the other transistor would give rise to latch-up phenomenon manifested as high 'VDD' to 'GND' current inrush.

Analysis of the Layout for Area Reduction: Tap-Less Library

As it can be seen that 'WELL TIES' are needed to tie N-WELL and P-WELL to a known potential. The layout in figure 1 suggests that they are a part of each and every CMOS standard cell. However, the stdcells are placed in well defined rows of uniform height where wells are continuous and thus, standard cells placed in a row can share these 'WELL TIES'. This topology reduces the standard cell size and allows the SoC to accommodate more standard cells. This type of standard cell library is called Tap-Less library. To provide the much required well connections, cells known as 'Well Taps' are placed at uniform interval. The spacing between these 'Well Taps' should not be too high as this would increase the resistance R1 and R2 and this could make the circuit susceptible to latch-up. Refer figure 3 for a typical CMOS device for Tap-Less library.

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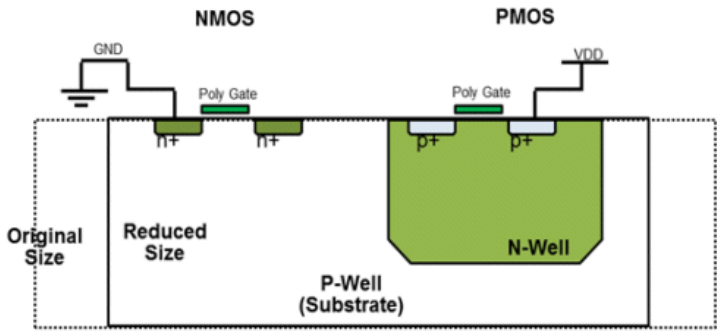

Fig 3: Notice the removal of 'WELL TIES' on the edges and the reduction in size of the cell

Figure 4 exemplifies symbolic representation and layout implementation of a standard cell in Tap-Less library. PUN stands for Pull Up Network consisting PMOS devices and PDN stand for Pull Down Network consisting NMOS devices.

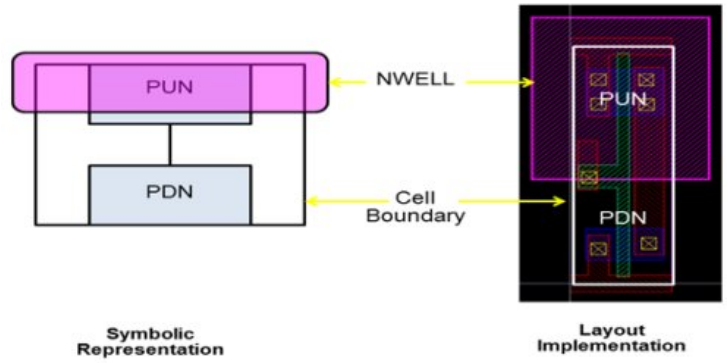

Fig 4: Symbolic Representation and Layout Implementation for Tap-Less Library

The stdcell placement in a Tap-Less library is exemplified in figure 5.

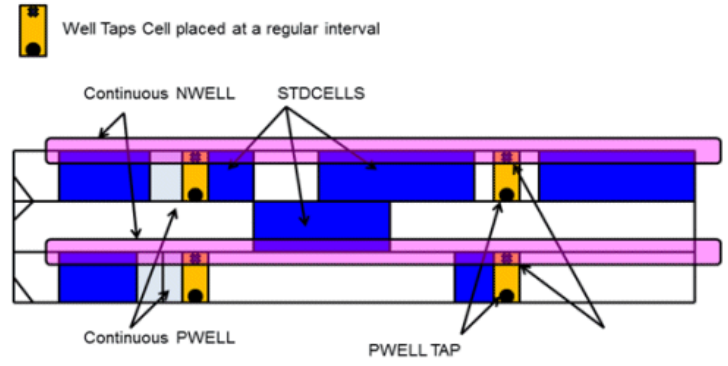

Fig 5: Standard Cell Placement before Decoupling Capacitor/Filler Addition

After the standard cells (for logic implementation) are placed in the rows, the next step is to add decoupling capacitors to take care of dynamic power consumption. These decoupling capacitors (decaps) follow the similar topology as exemplified in figure 3 and 4 i.e. they are devoid of any 'WELL TIES'. The row area after decap addition is exemplified in figure 6.

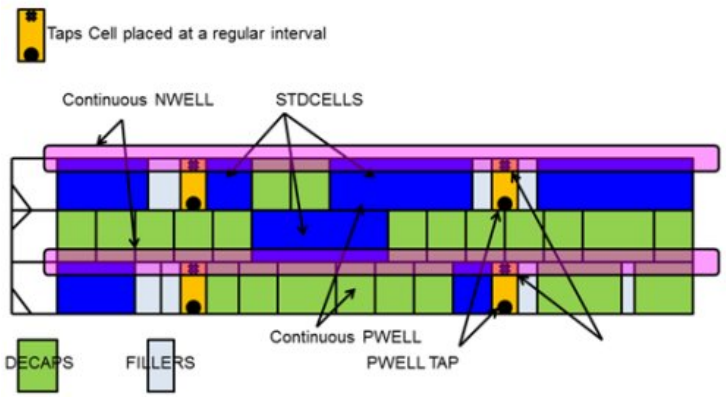

Fig 6: Standard Cell Placement after Decoupling Capacitor/Filler Addition

Proposal:

As indicated in the above figures, Well-Taps placed at regular interval are just sufficient to avoid latch-up but, it is no way better than a library in which each standard cell has its own well-tap. But, this would cost us the highly valued silicon area. The proposal is to find a midway between these two extremes. It proposes to have the standard cells devoid of 'WELL TIES' but decoupling capacitors can be modified to have these 'WELL TIES' so that the extra WELL TIES are added on silicon area left after logic placement. These extra WELL TIES strengthened well connections to respective supplies. The proposal is to have decaps layout to be modified as below :

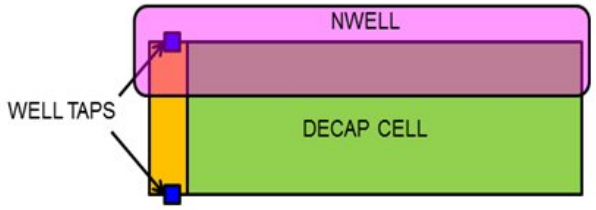

Fig 7: Decap Cell Extended to include 'Well Taps'

The cell placement would now appear as below:

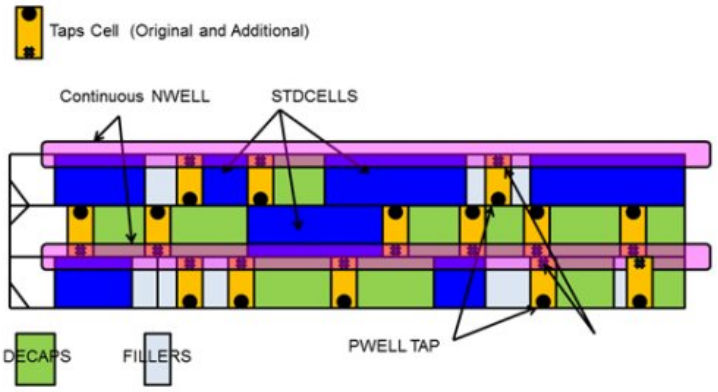

Fig 8: Standard Cell Placement After Modified Decap Addition

Conclusion:

As the well tap placement is significantly higher than it would have been for a typical Tap-Less library with existing placement methodology, the latch-up performance of the SoC with the proposed implementation is expected to improve.

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