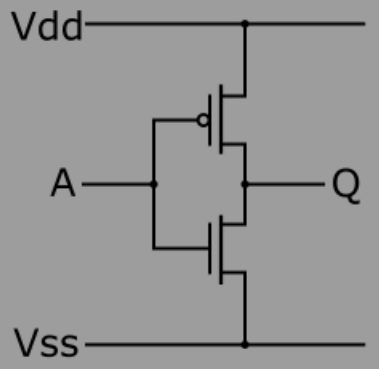
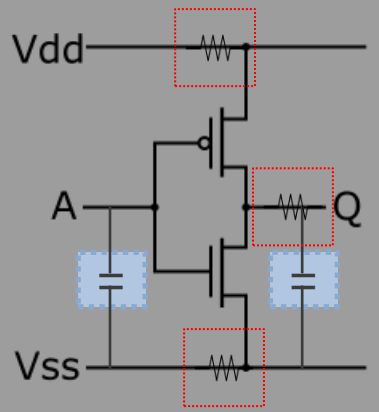
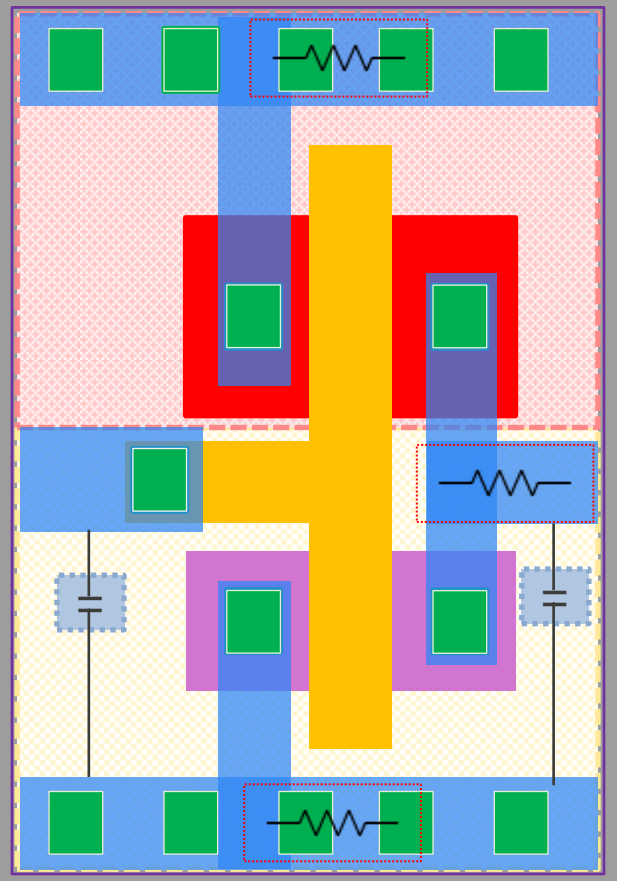
PHYSICAL DESIGN
PHYSICAL VERIFICATION

UNDERSTANDING THE BASIC KNOWLEDGE

(INTERNAL USED ONLY)







2016 DEC 25TH
TRAN HUY
ASE PHYSICAL DESIGN
BACKEND3
RENESAS DESIGN VIETNAM CO., LTD.

Approver	Checker	Author
		RVC/BackEnd3 Tran Quoc Huy 2016 – Apr - 21

INTRODUCTION

WHAT IS PHYSICAL VERIFICATION

After routing, layout is completed. Now a number of checks are performed to verify that the drawn layout works as intended. Three of them are:

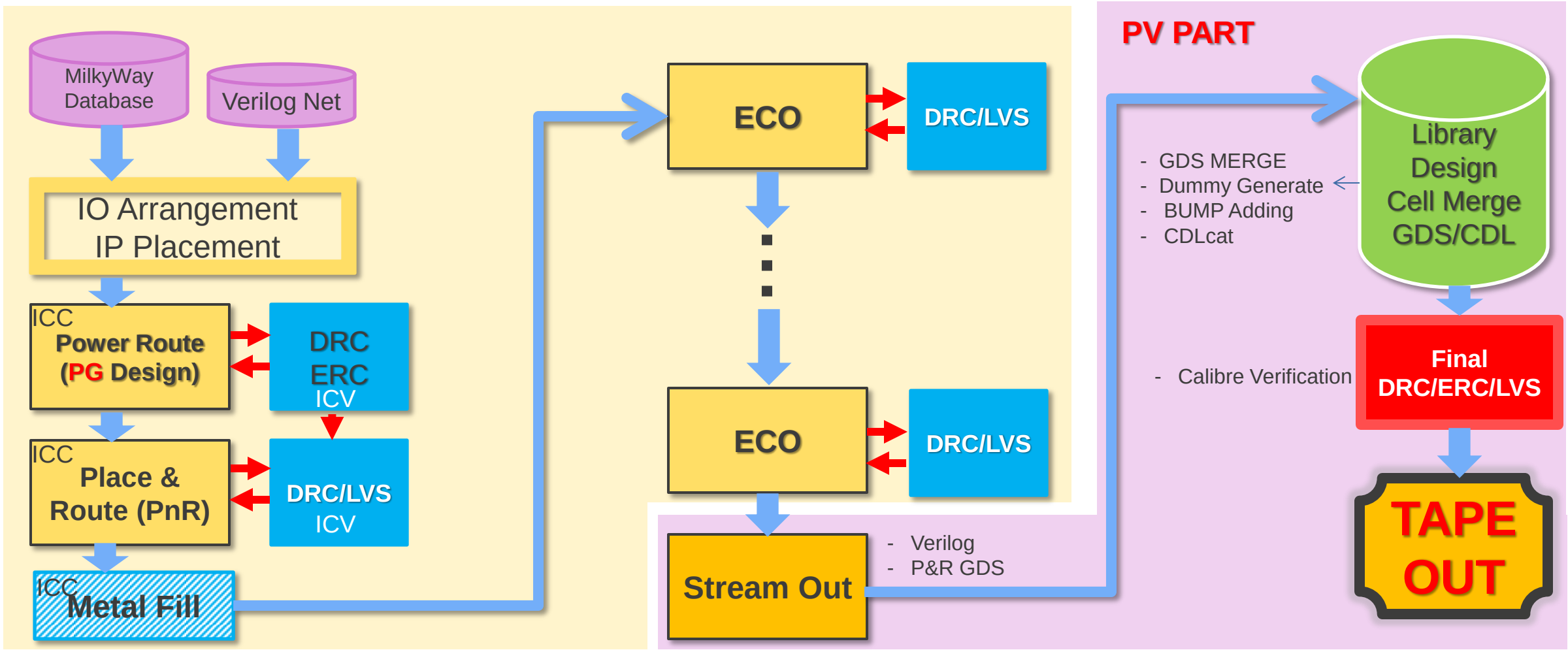
- ✓ **Physical verification**
- ✓ **Equivalence Checking**
- ✓ **Timing Analysis**

- Equivalence check will compare the netlist we started out with (pre-layout/synthesis netlist) to the netlist written out by the tool after P&R(post-layout netlist).
- Physical verification will verify that the post-layout netlist and the layout are equivalent. i.e. all connections specified in the netlist is present in the layout.
- Within this document, I will intend to explains physical verification and basic knowledge need to know.

P/s: *PV will work on GDSII file (GDS), is a database file format which is the de facto industry standard for data exchange of integrated circuit or IC layout artwork. It is a binary file format representing planar geometric shapes, text labels, and other information about the layout in hierarchical form. The data can be used to reconstruct all or part of the artwork to be used in sharing layouts, transferring artwork between different tools, or creating photo-masks.*

PHYSICAL VERIFICATION IN DESIGN FLOW

- DRC: Design Rule Check
- LVS: Layout versus Schematic
- ERC: Electrical Rule Check
- ICV: IC Validator
- ECO: Engineer change order



WHAT IS PHYSICAL VERIFICATION (CNT.,)

After routing, your PnR tool should give you zero DRC/LVS violations. However, the PnR tool deals with abstracts like FRAM or LEF views. We use dedicated physical verification tools for signoff LVS and DRC checks. Some of these are **Hercules** from Synopsys, **Assura** from Cadence and **Calibre from MentorGraphics.**

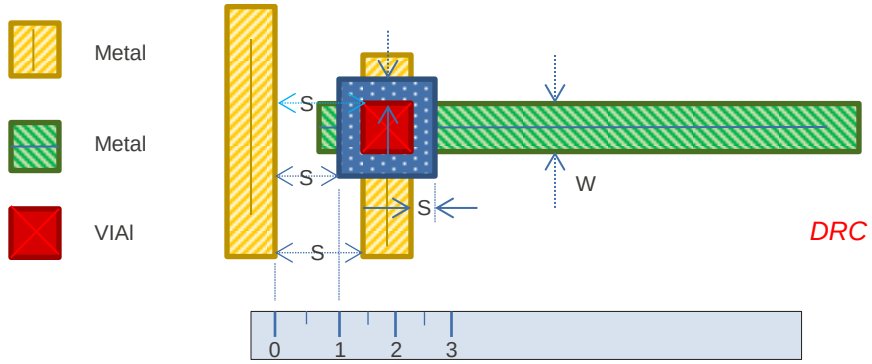
The major checks are:

1. DRC
2. LVS
3. Antenna
4. ERC
5. and so on…

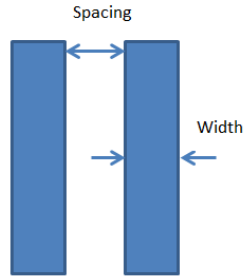
1. WHAT IS DRC

***D**ESIGN **R**ULE **C**HECK*

THE OPERATION CHECKS FOR DESIGN RULE VIOLATION



DRC spacing & min width check

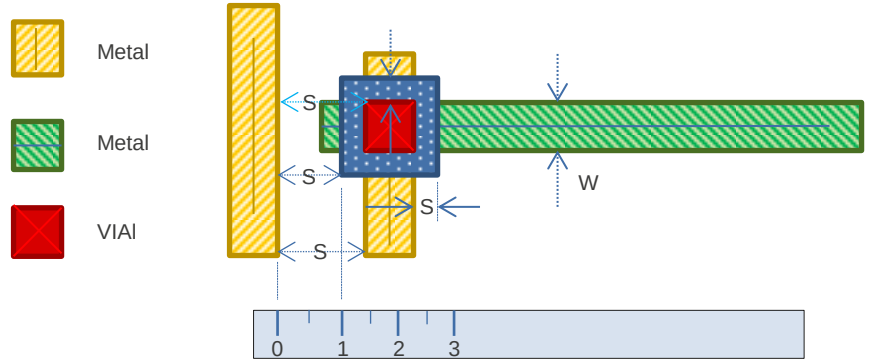


DRC checks determine if the layout satisfies a set of rules required for manufacturing. The most common of these are spacing rules between metals, minimum width rules, via rules etc. There will also be specific rules pertaining to your technology. An input to the design rule tool is a 'design rule file' (called a runset by Synopsys' hercules). The design rules ensure sufficient margins to correctly define the geometries without any connectivity issues due to proximity in the semiconductor manufacturing processes, so as to ensure that most of the parts work correctly. The minimum width rules exists for all mask layers, and spacing between the same layers are also specified. Spacing rules may change depending on the width of one or both of the layers as well. There can also be rules between two different layers, and specific via density rules etc. If the design rules are violated, the chip may not be functional.

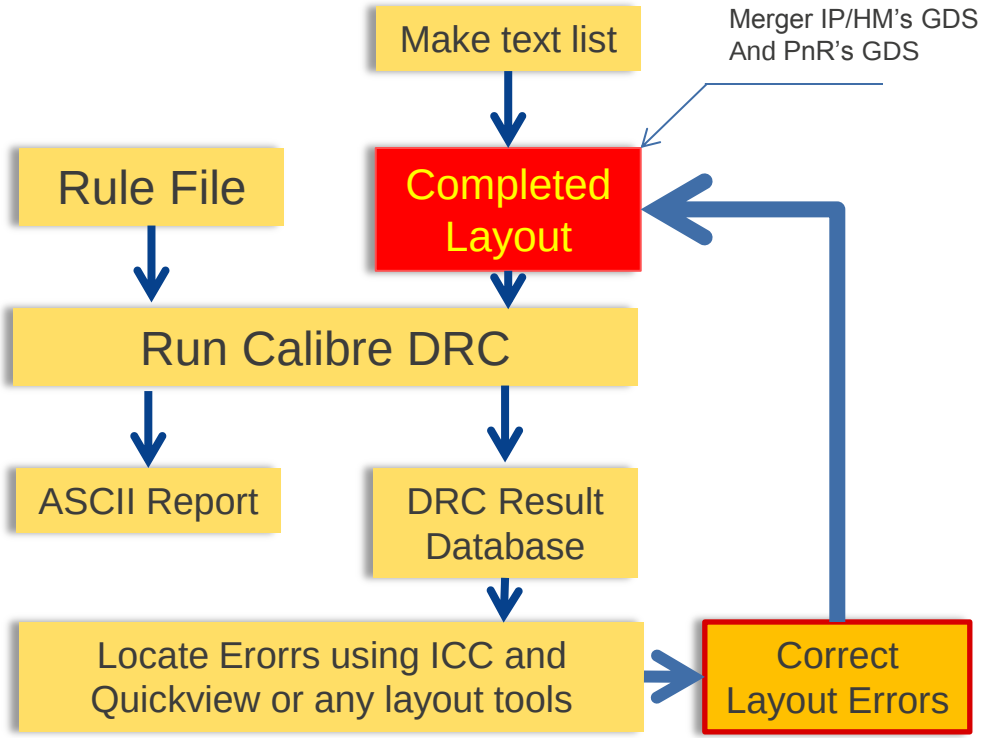
DRC – Spacing & Width checks

DRC checking software, like Assura, Hercules or ***Calibre*** usually takes the layout in any of the supported formats, like GDSII.

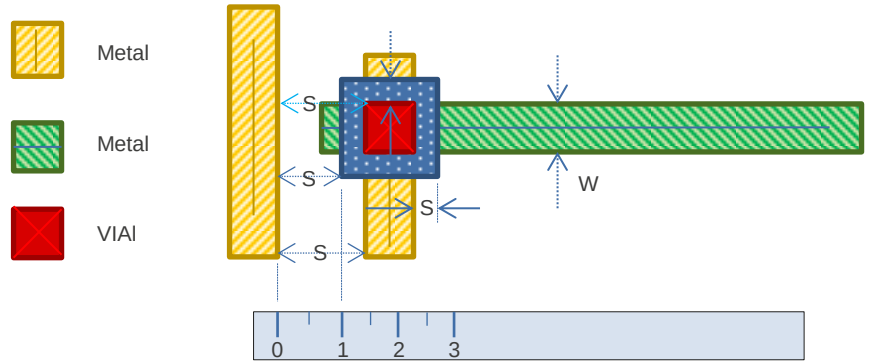
1.1. DRC INVOKE FLOW



- ✓ **Prepare layout (PnR data)**
  - *- Add label (text layer)*
  - *- stream out GDS.*
- ✓ **Prepare DRC rule file**
  - *- Modified specification statement*
- ✓ **Invoke Calibre DRC**
- ✓ **DRC report**
- ✓ **Fix DRC Errors**
  - *- DRC summary*



1. 2. COMMON DEFINITION



Minimum width (W) : Detects the minimum width of lines and other shapes. Any polygon with opposing edges less than the minimum width causes a violation. For this rule, only one layer is specified.

Spacing (S) : Checks for the minimum separation between two shapes on either the same layer or different layers. You can also use this rule to detect small gaps in metal layers that are too small to be seen by visual examination. This rule requires specification of two layers (the two layers can be the same layer if desired).

Overlap (R,O): Checks for the minimum overlap of one layer over another layer. This rule is often used to ensure that different layers overlap enough to make a manufacturable connection. This rule requires specification of two different layers. The rule does not depend on the order of the layers in the rule specification.

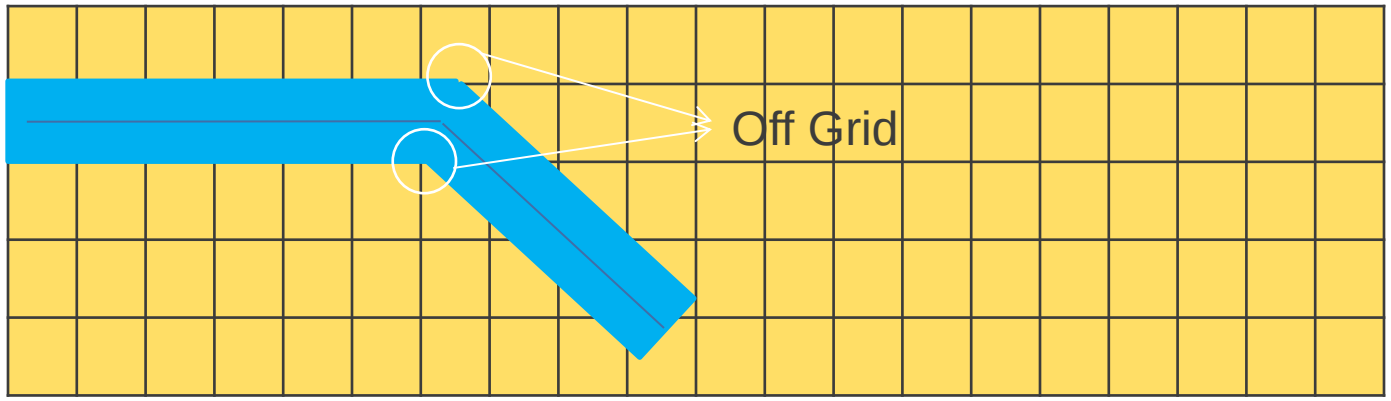
Extension : Checks for a minimum extension of shapes on one layer over shapes on another layer. The following figure shows the distance being checked. This rule is often used to ensure that process layers are inset by a sufficient amount (for example, when plating a line). This rule requires specification of two different layers. The order of the layers in the rule is considered.

Notch: Checks for a minimum width of an intruding or protruding notch within a shape as shown in the following diagram. This rule requires specification of only one layer.

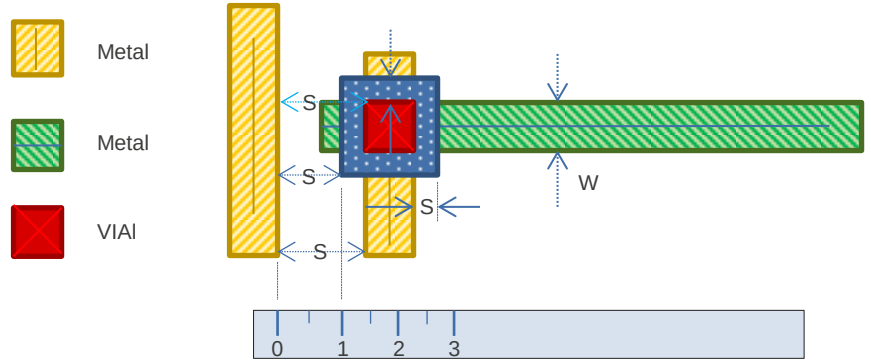
1. 3 *GENERAL RULES*

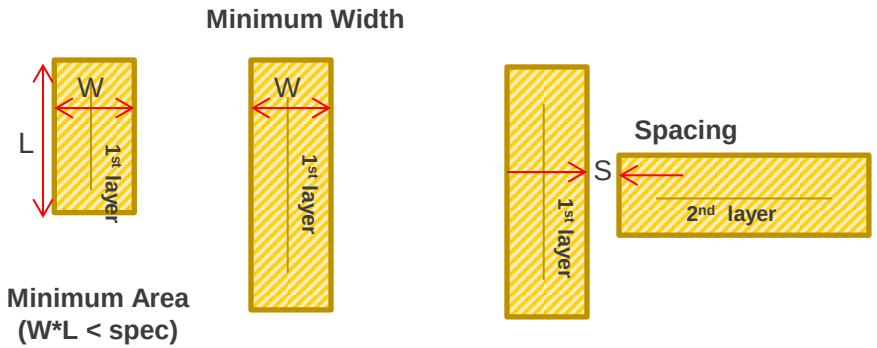
- **Angles:**
  - Usually only multiples of 45 degree are allowed

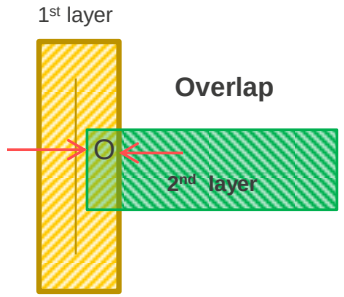
- **Grid:**
  - All corner points must lie on a minimal grid (at least when the chip will be produced.
  - Otherwise an “Off Grid Error” is produced
  - Circles can be draw, but are converted later to Polygons with on-grid points.
  - Attention: If a path of width d is drawn in 45 degree, the corners can be off grid. It is better to draw by polygons

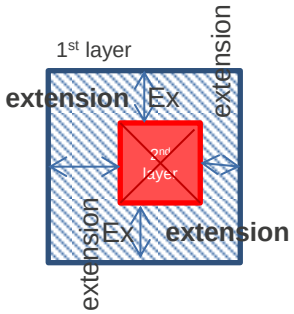


1. 4 *RULES IN ONE LAYER*

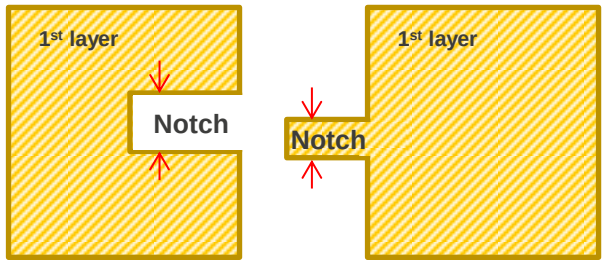


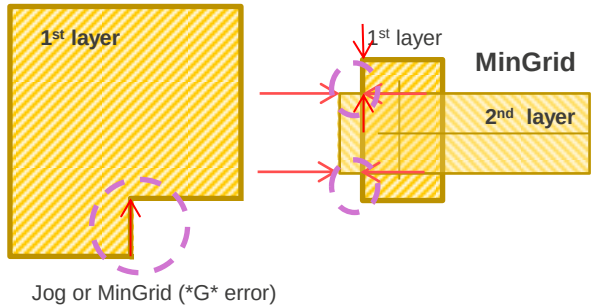


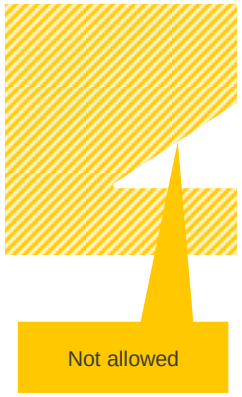


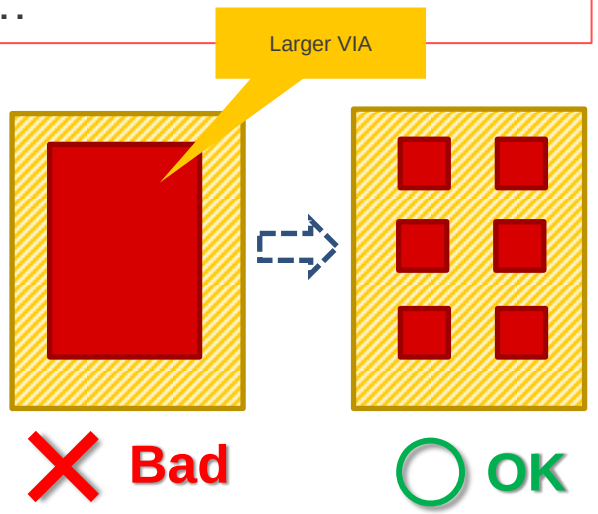


Other errors:
- Minimum Polygon Area
- Polygon holes
- Polygon on grid
- Minimum Angle
- …





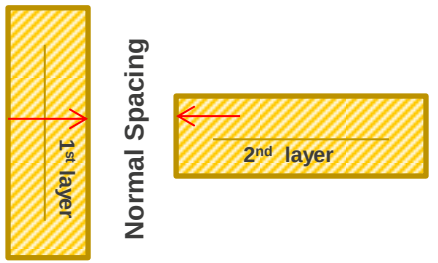


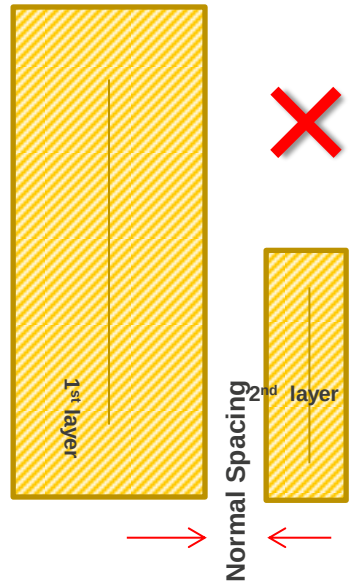


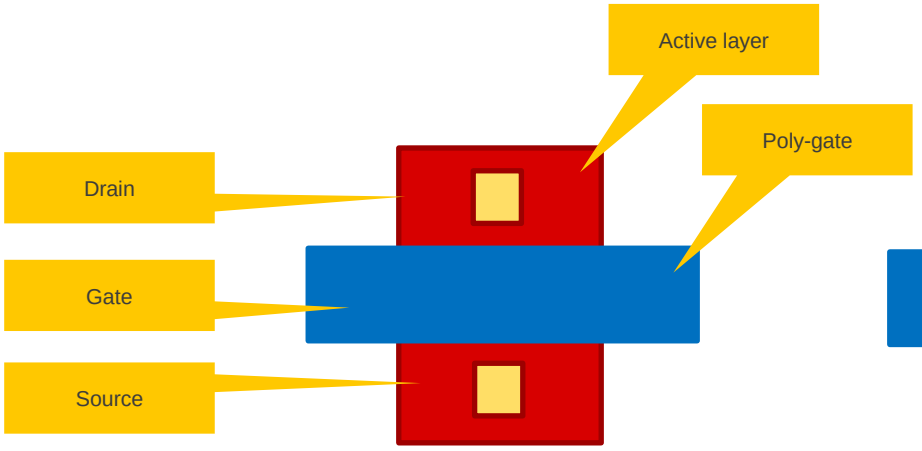
- Caused by manufacturing limits (lithography, etching,…)
- Rules: Spacing, Width, Notch between same net
  - ✓ Finest structure is Poly-silicon for gates
- Larger structures must be created by repetition (mosaic)

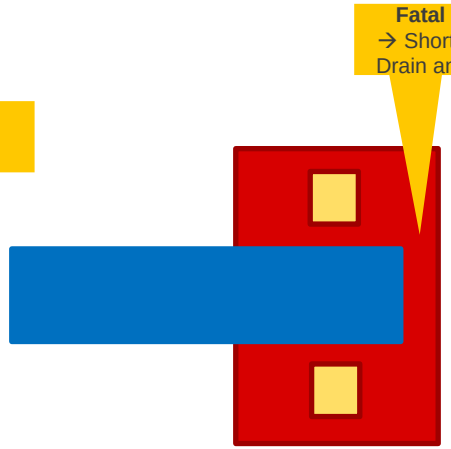
1. 4 *RULES IN ONE LAYER*

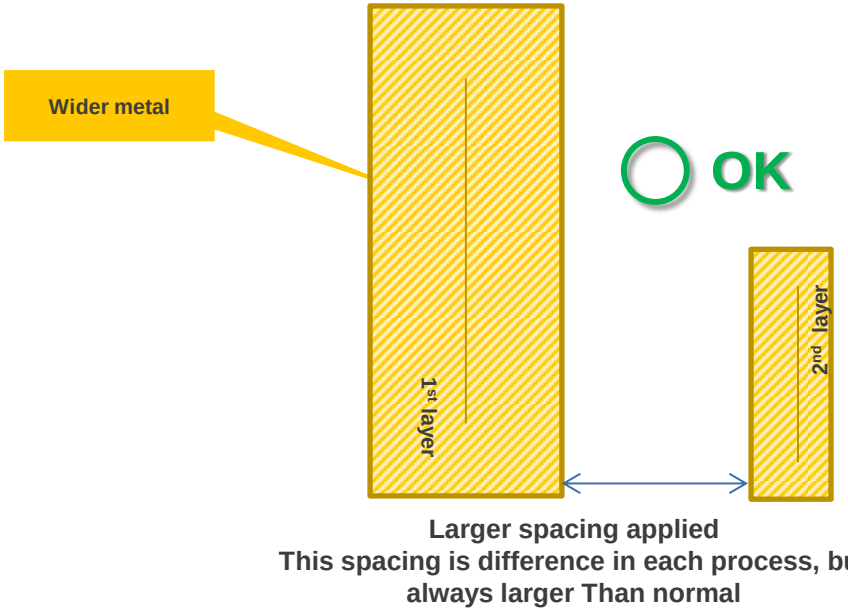
- **Spacing rules often apply for 'large' = wide structures**
- **For instance**
  - *Gate spacing for gates > Lmin is different (larger)*
  - *Metal spacing for metal wider Wmin can be different*
  - *Via overlap can be more for wide metal*
- **Caused by alignment precision of different masks**







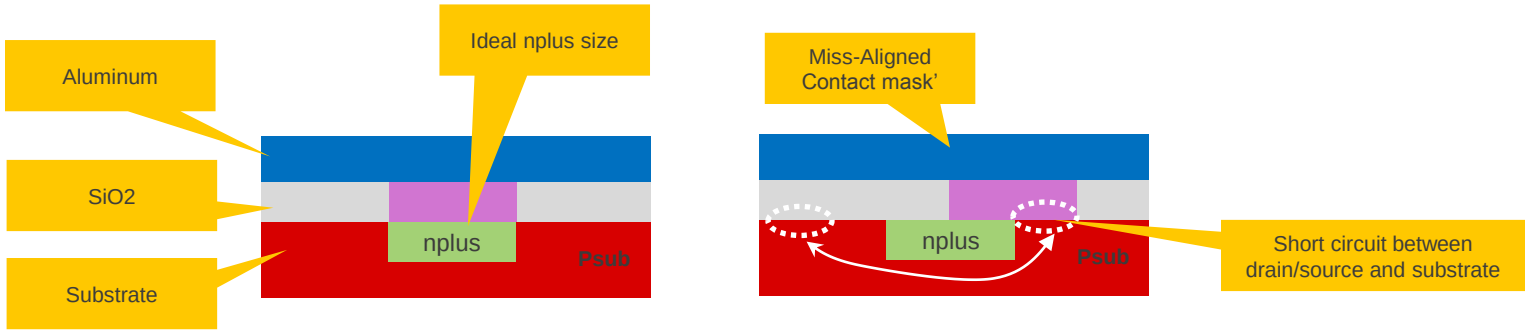




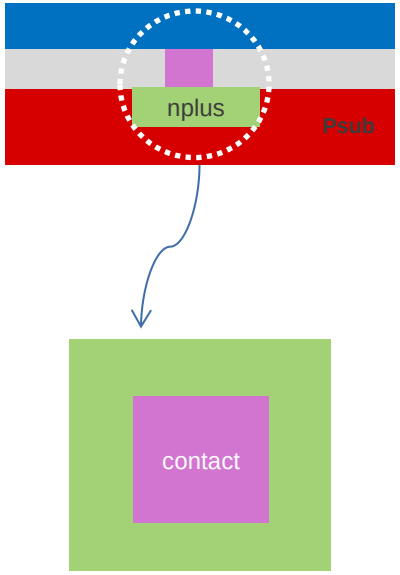
Larger spacing applied
This spacing is difference in each process, but always larger Than normal

1. 5 OVERLAP REQUIRED ON DRAIN/SOURCE-DIODES

- Consider contacts of Drain / Source (NMOS)



- **Solution:**
  - *Contact hole must be smaller than active area.*



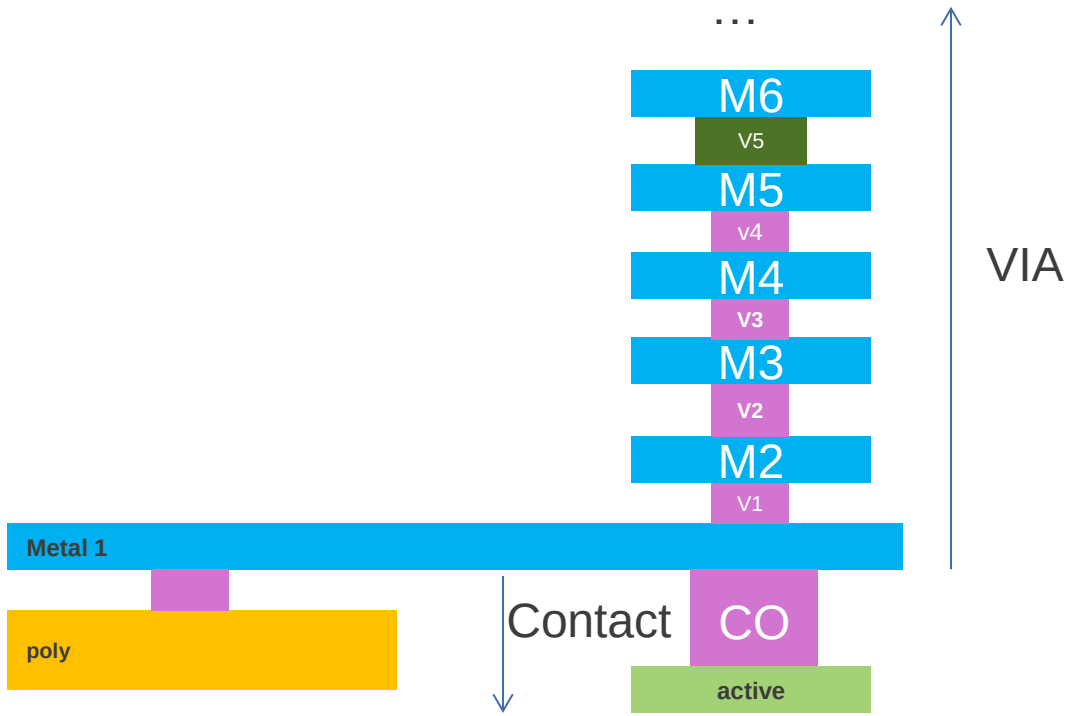
1. 6 VIAS AND CONTACTS

- M1 → p-diffusion
- M1 → n-diffusion
- M1 → poly1
- M1 → poly2

→ One Mask → CONTACT (CO)

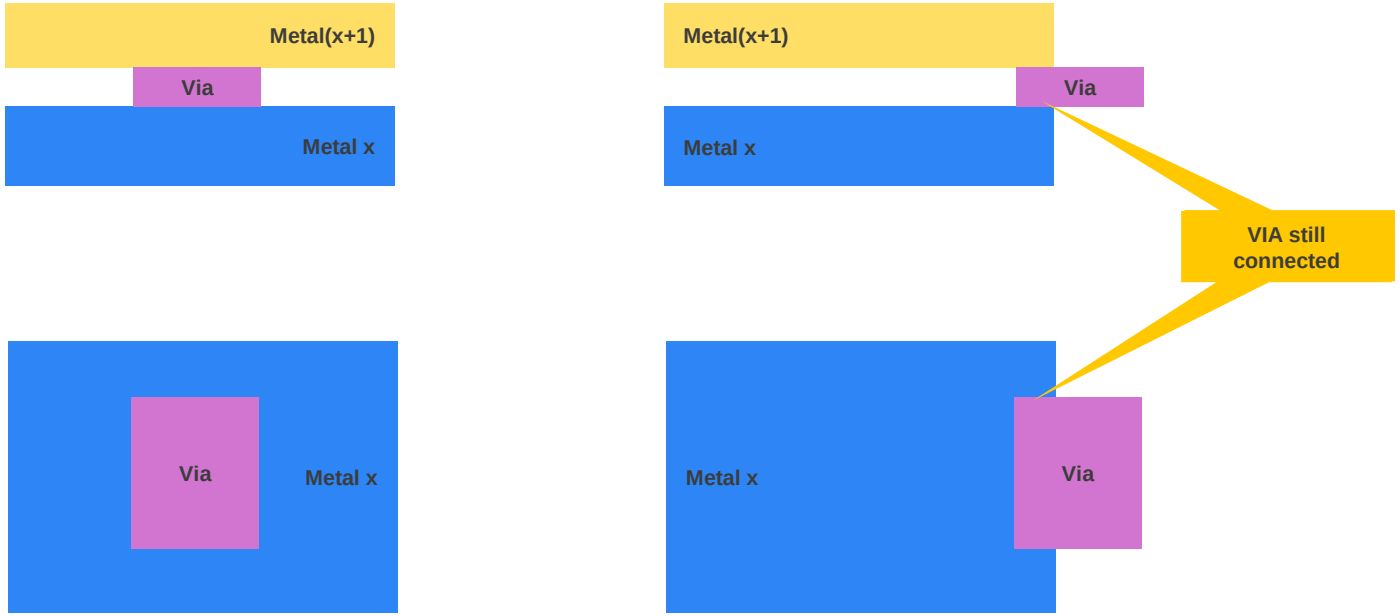
- M1 → M(x+1)

→ One mask per pair → VIA (V)

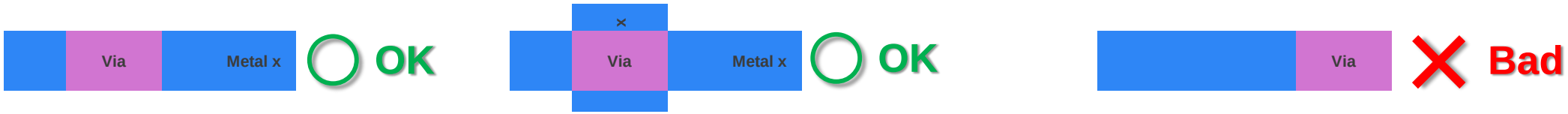


1. 7 SHIFED VIAS AND CONTACTS

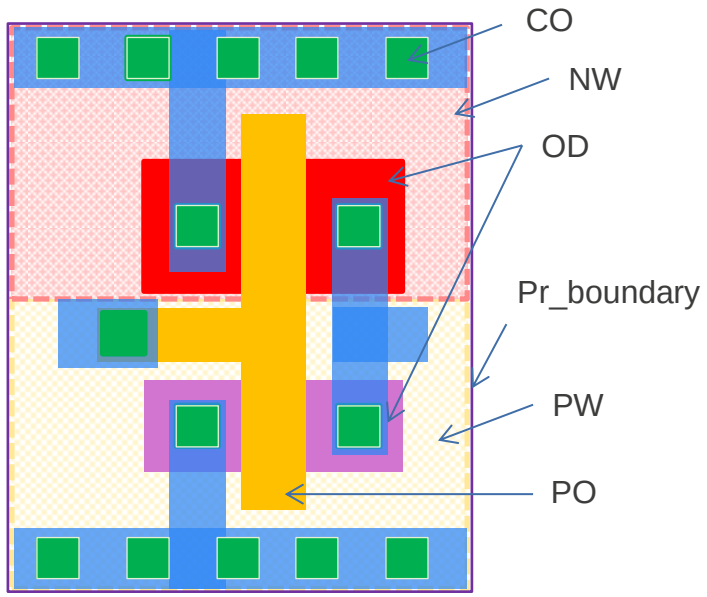
The Via/contact can – in principle – be shifted and there is still contact.



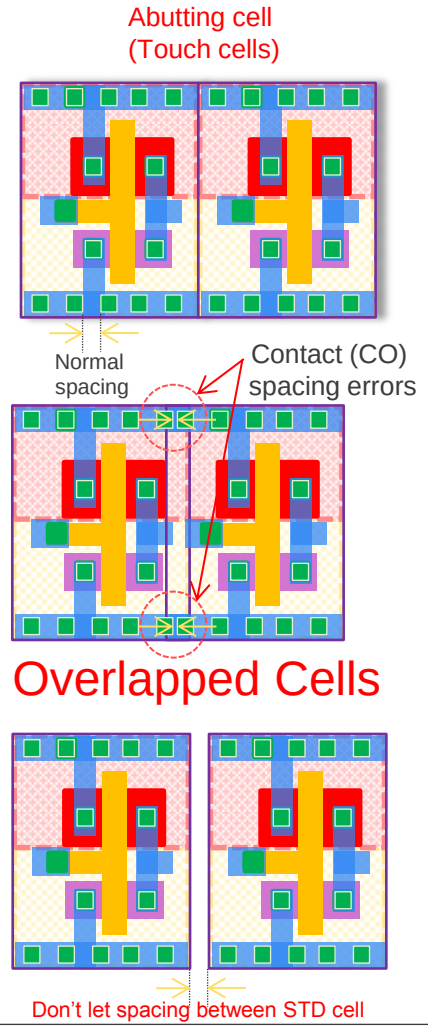
Therefore, DRC rules for contact are aggressive and complicated.Metal mus extend VIA on at least 2 opposite sides.

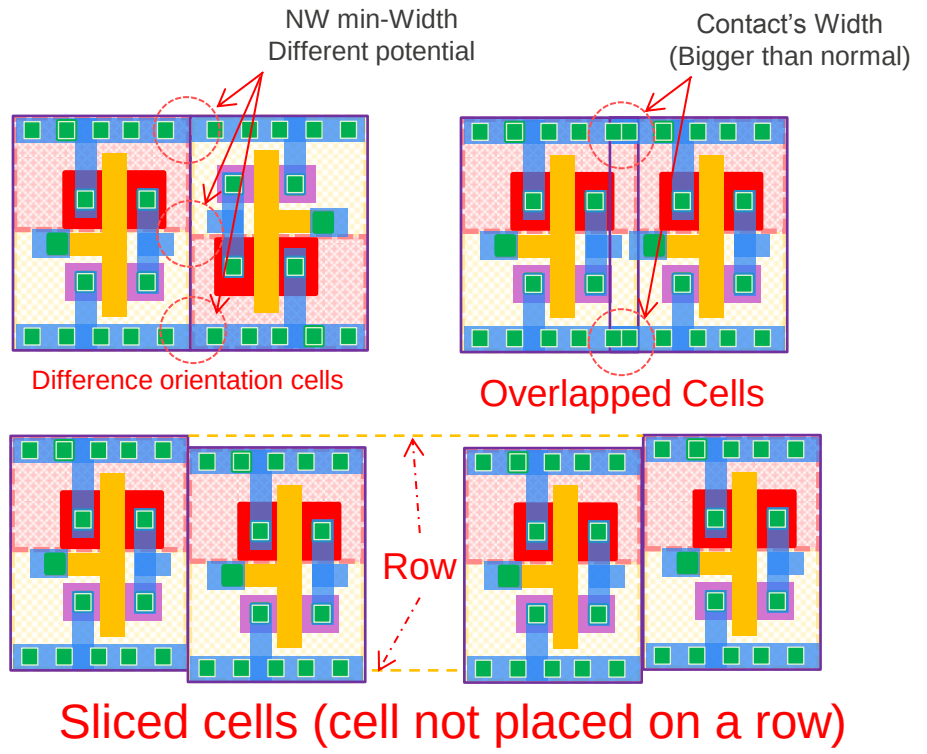


1.8 COMMON ERRORS (CNT.)



STD cell is designed to satisfy
All DRC errors when abutting (touching)
If cells are overlapped, errors may
Occurred.

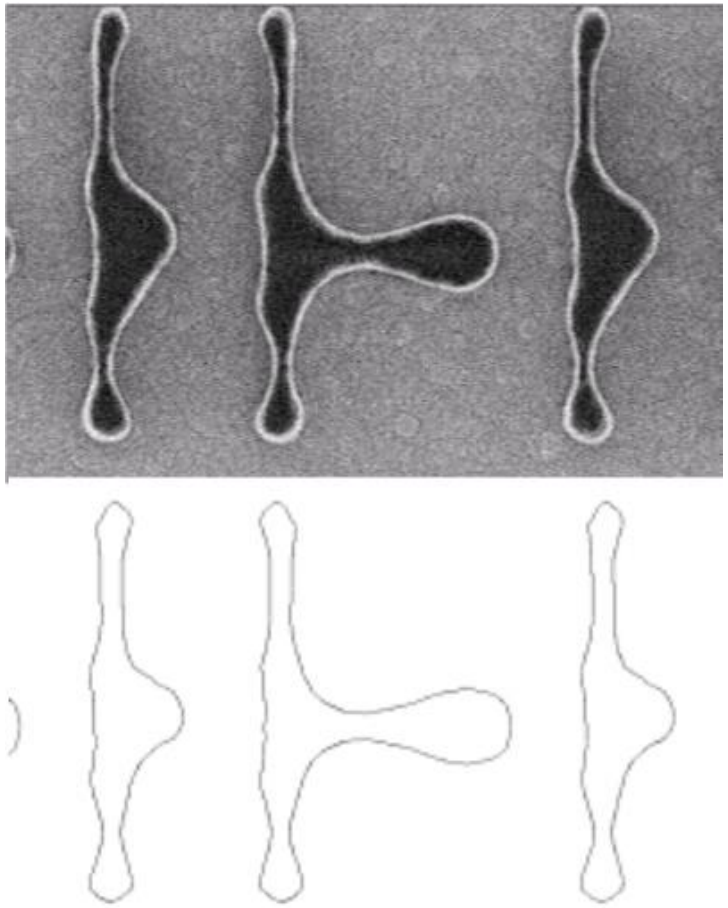


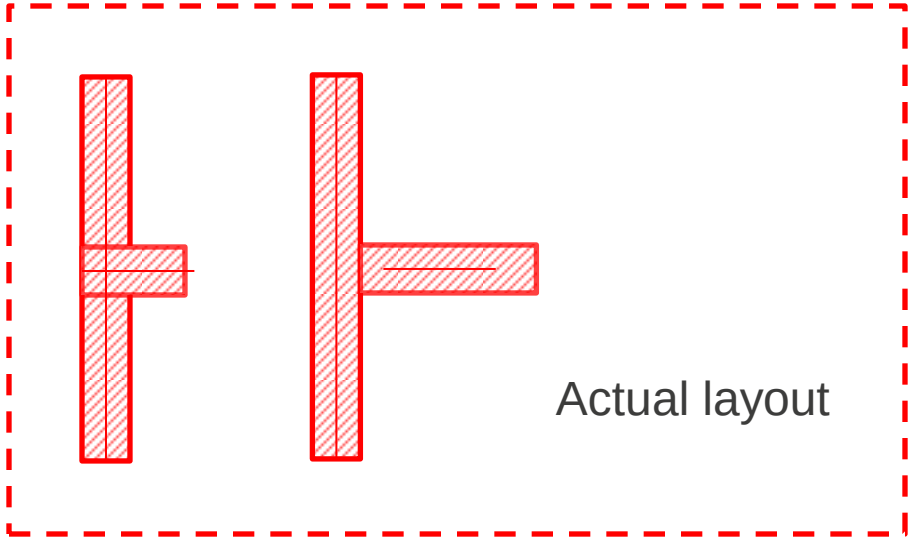


DRC lower errors are detected by behavior of placement of STD cell quickly. Please focus on below errors type:

- CO.W.*, CO.S.*, NP.W.*, PP.W.*, NW.S.*, VTH.*,UVTH.*

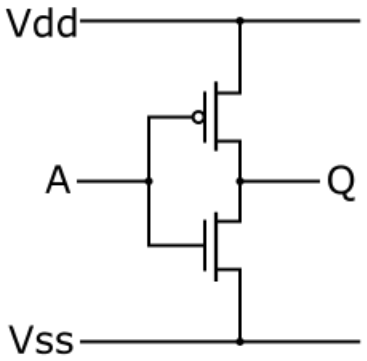
1.9 MANUFACTURING PRINTING AND SIMULATION



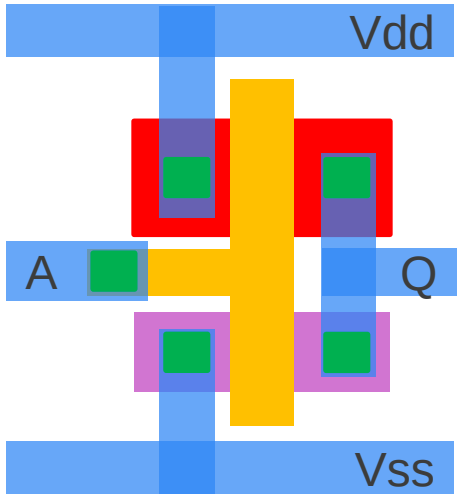


2. WHAT IS LVS

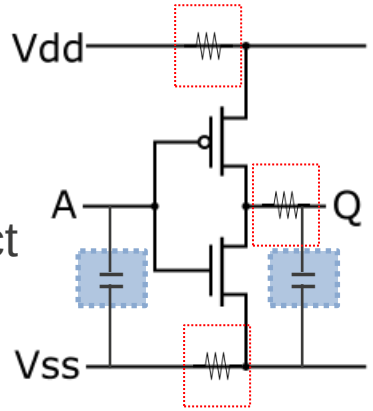
LAYOUT VERSUS SCHEMATIC



Compare with



RC extract

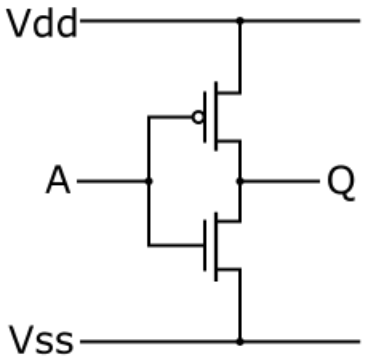


LVS is another major check in the physical verification stage. Here you are verifying that the ***layout you have created is functionally the same as the schematic/netlist of the design-that you have correctly transferred into geometries your intent while creating the design***. So all the connections should be proper and there shouldn't any missing connections etc.

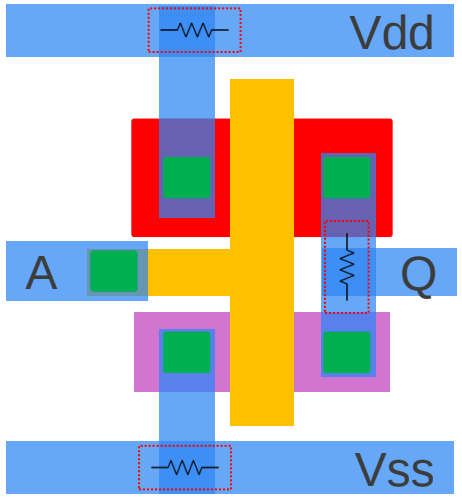
The LVS tool creates a layout netlist, by extracting the geometries. This layout netlist is compared with the schematic netlist. The tool may require some steps to create either of these netlists(e.g. nettran run in Synopsys).

If the two netlists match, we get an LVS clean result (CORRECTED). Else the tool reports the mismatch and the component and location of the mismatch. Along with formal verification, which verifies if your pre-layout netlist matches the post-layout netlist,LVS verifies the correctness of the layout with respect to intended functionality.

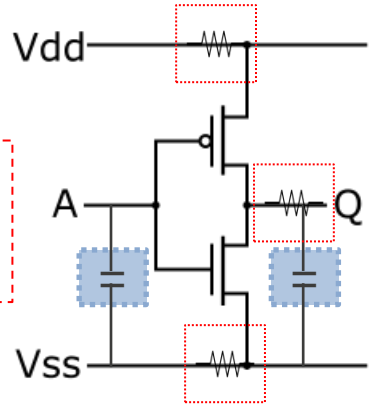
2.1 LVS FLOW



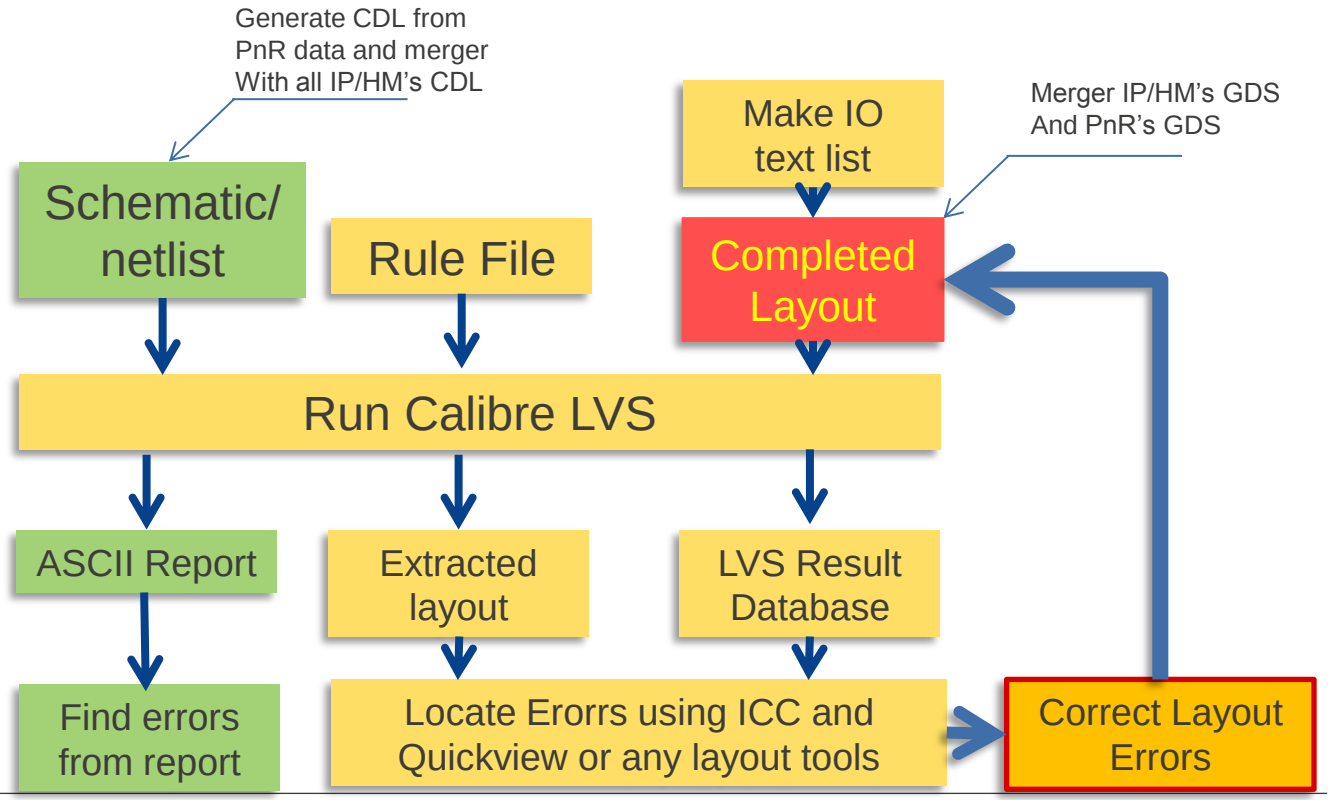
LVS



LPE
Or
RC
Extract



- ✓ **Prepare layout (PnR data)**
  - *Add all I/O text*
  - *stream out GDS.*
- ✓ **Prepare netlist (LVSNET) (.v or .cdl)**
  - *Make LVSNET by output netlist from ICC MW, then merge them with IP/HM's CDLs.*
- ✓ **Invoke Calibre LVS**
- ✓ **Invoke ICC LVS**
- ✓ **LVS report**
- ✓ **View LVS Errors**
  - *LVS summary*

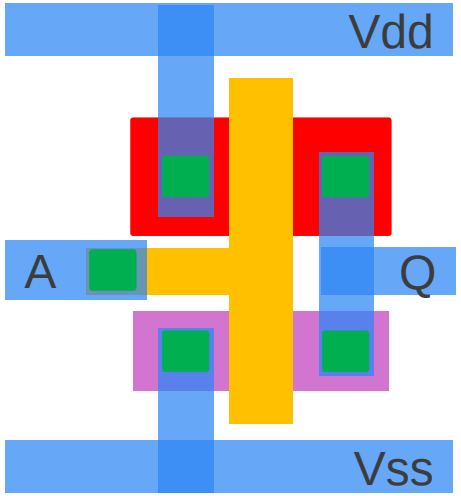


RENESAS CONFIDENTIAL

2.2 WHAT LVS DOES

1. Extract schematic netlist → spice model

- travel down the hierarchy until a view is in the stop list.
- for instance, we can keep an inverter as a cell, not resolve it into MOS!
- ignore symbols for instance in analogLib

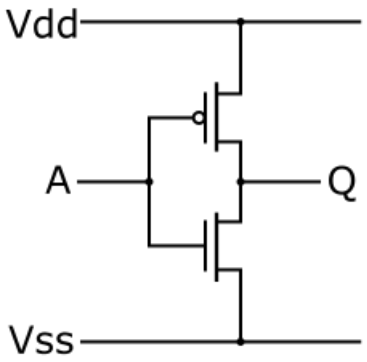


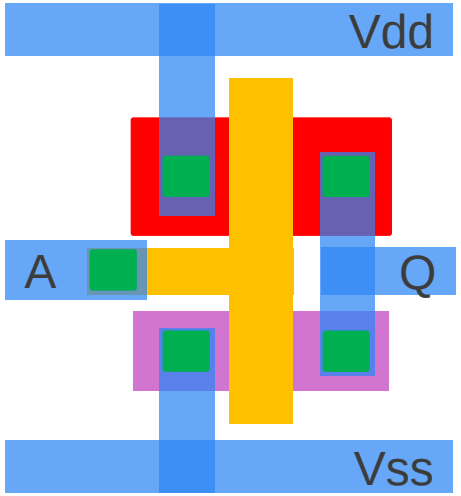
2. Extract the layout netlist → spice model

3. Compare the two netlists (same spice model)

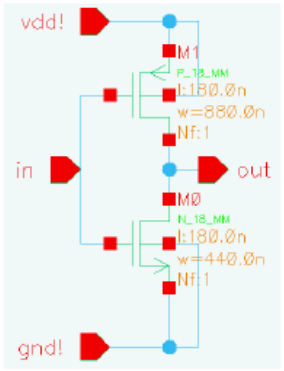
- Devices and nets without labels have different names!
- Difficult task!
- Naively, require 1:1 match
- In reality, allow certain topological differences
  - the order of serial connected resistors does not matter
  - two serial resistors are equivalent to one with sum resistivity

2.3 EXAMPLE-1





Schematic

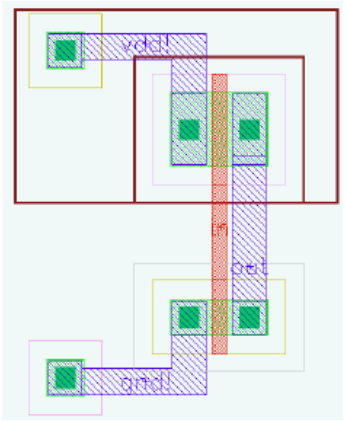


Extracted To spice model

Extracted schematic netlist:

```
* 2 instances
i M1 P_18_MM out  in vdd! vdd!
  L 1.8e-07  M 1 W 8.8e-07
i M0 N_18_MM out  in gnd! gnd!
  L 1.8e-07  M 1 W 4.4e-07
```

Layout



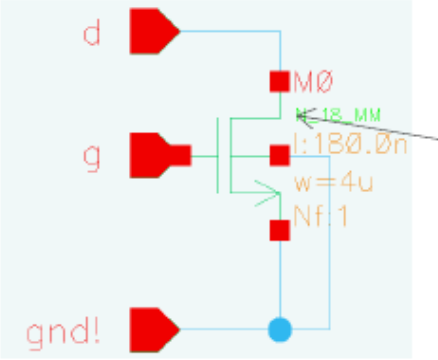
Extracted To spice model

Extracted layout netlist:

```
* 2 instances
i av1 N_18_MM out in gnd! gnd!
  l 1.8e-07  w 4.4e-07;
i av2 P_18_MM out in vdd! vdd!
  l 1.8e-07  w 8.8e-07;
```

2.3 EXAMPLE-2

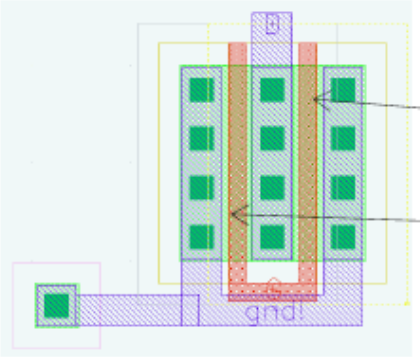
Schematic



Extracted schematic netlist:

```
* 1 instances
i M0 N_18_MM d  g gnd! gnd!
  L 1.8e-07  M 1  W 4e-06
```

Layout



Extracted layout netlist:

```
* 2 instances
i m0 N_18_MM gnd! G    D gnd!
   l 1.8e-07  w 2e-06
i m1 N_18_MM    D G gnd! gnd!
   l 1.8e-07  w 2e-06 ;
```

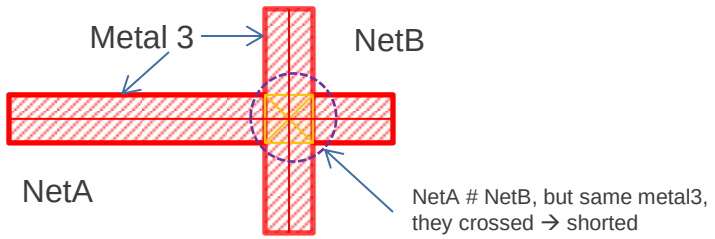
This is an example of single MOS in netlist (schematic), And there are multiple MOS in Layout

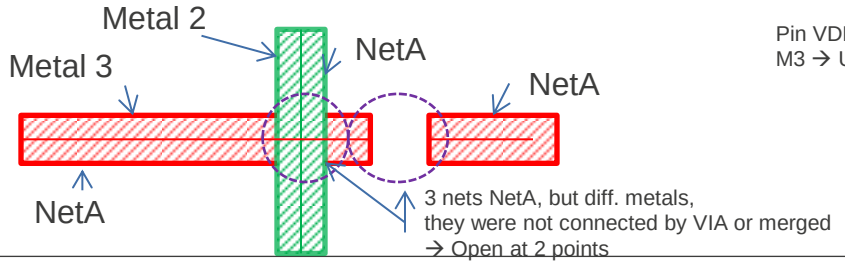
After finishing extract, Comparison will find parallel MOS and calculate W = W x m. Results are matched as the figures

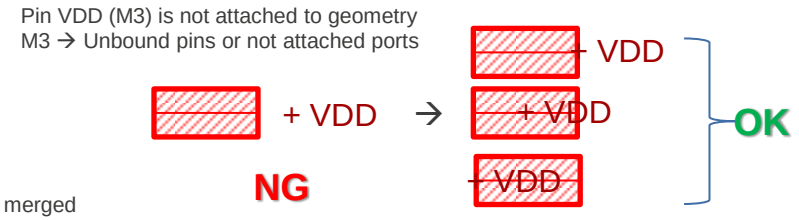
2.4 SOME OF THE LVS ERRORS

There are some of the LVS errors:

1. **Shorts** – Wires that should not be connected are overlapping.
   There are Power shorted or Signal shorted. We can not continue checking LVS without solving shorted errors.
2. **Opens** – Connections are not complete for certain nets.
3. **Parameter mismatch** – LVS also checks for parameter mismatches. e.g. It may match a resistor in both layout and schematic, but the resistor values may be different. This will be reported as a parameter mismatch.
4. **Unbound pins** – If the pins don't have a geometry, but all the connections to the net are made, and unbound pin is reported.







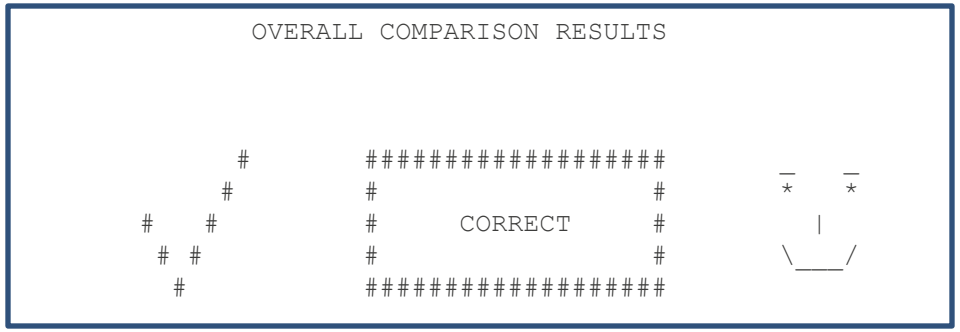
2.5. UNDERSTANDING ABOUT LVS REPORT

LVS report gives detailed information on the sources of error either in the layout or schematic by displaying the comparison results. All the errors can be tracked by understanding the LVS report.

The LVS report describes the comparison between the layout and schematic with respect to ports, nets and instances. If the schematic and layout doesn't match, the discrepancies are mentioned, separated by broken lines. The 'overall comparison results' gives the numerical details of the ports, nets and instances appearing in the layout and schematic (also referred as source). Below this information, 'incorrect objects' explains in detail the ports/nets/instances not matched in the comparison.

The format of the discrepancies (incorrect matching) is given as follows:

- **Unmatched nets**
- **Unmatched instances**
- **Component type**



2.5. UNDERSTANDING ABOUT LVS REPORT (CNT.)

UNMATCHED NETS

If the **nets** do not match, there is description of such discrepancies under ‘incorrect nets’. These are few types of errors likely to be encountered:

```
- - - - - - - - - - - - - - - - - - -- - - - - - - - - - - - - - - - - - - - - - - - - - -  - - - - - - -  -
5             ** missing net **                                     /N$716
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -- - - - - - - -
7             Net 2 (0.00,40.00)
                  3 (50.00, 60.00)                                  //VDD


- - - - - - - - -- - - -- - - --  - - - - -- - - - - - - - -- - - - - - - -- - - - - - - - -- - - -- - - - -
8              Net VDD                                               //VDD
                                                                     /N$87
- - - - - - -- - - - -- - - - - -- - - - - - -- - - - - - -- - - - - - - - - - - - - - - - -- - -- - - - - -
```

The number given under **DISC#** in the report gives the number of discrepancy. In the above example, the discrepancy relating to **N$716** is numbered **5**. The layout elements involved in the discrepancy appear on the left side of the report while the source/schematic elements appear on the right side. If a net in the layout is named and is involved in the discrepancy, it will be mentioned as **‘Net <name>’.** Discrepancy **#8** gives such example. The net is named in the layout as VDD. If the net is not named, it will be mentioned in the discrepancy with an id as ‘**Net <number>’** as given in discrepancy **#7**. Numbered nets (i.e. unnamed) have their net id followed by the X and Y coordinates at which net in the layout starts. In the schematic, a net is represented as ‘**N$<number>**’ if it’s not named or with a name if it is named

2.5. UNDERSTANDING ABOUT LVS REPORT (CNT.)

UNMATCHED NETS

Explanation of the above discrepancies:

Disc#5: The net (N$716) in the schematic has no layout counterpart. It might be due to wrong substrate connections or incorrect contacts or missing to lay it out altogether.

Disc #7: This indicates an open circuit in the layout. Two nets with id 2 and 3 in the layout are represented in the schematic as a single net VDD. But they are not connected in the layout. Either the schematic or the layout could have gone wrong.

Disc#8: This indicates a short circuit in the layout. The schematic has VDD and a net N$87 as distinct nets, but their counterparts in the layout have been connected together as net VDD.

2.5. UNDERSTANDING ABOUT LVS REPORT (CNT.)

UNMATCHED INSTANCES

If the **instances** do not match, the description on the incorrect instances follows. As the unnamed nets are represented in the schematic as ‘N$<number>’, unnamed instances are represented as ‘I$<number>’. The instances have pins. For eg. the pins of nMOS are G, B, S and D (gate, bulk, source and drain). Any pin of an instance in the schematic is represented as I$702:G, i.e. it refers to the G pin of instance numbered 702. Similarly, in the layout, unnamed instances have id followed by the coordinates of the device and the pin. For eg.

```
27(230, 540): B refers to pin B of device with id 27 at the specified X and Y coordinates in the layout.
```

Logic gate pin identification: If a schematic is used with inverter, nand and nor **symbols** (not transistor level) and there is an LVS error in one of the pins of the internal (transistor level) schematic of inverter, it shows up in the LVS report as follows on the source side:

```
- - - - - - - - - - -  - - -  - - - - - - - - - - - - - -- - - - -

(INV)

Transistors:

 /I$767/MP/MP/I$702:D

 /I$767/MN/MN/I$786:S

- - - - - - -- - - - - - -- - - - - - - - - - - - - - - - - - - -
```

This indicates the drain pin of pMOS (I$702) contained in the device ‘INV’ (I$767) and the source pin of the nMOS transistor (I$786) contained in the device ‘INV’ (I$767) are not matched in the layout.

2.5. UNDERSTANDING ABOUT LVS REPORT (CNT.)

COMPONENTS TYPES

In the '**Overall comparison results**' segment, there is a column titled 'component type'. For a simple inverter, there are just two types of components: MP and MN (pmos and nmos transistors). However, as the schematics get bigger, there are different type of components that are different forms of pMOS or nMOS. Listed below are different types typically encountered

1. **SUPn** - (serial up) n-input CMOS serial pull up.

   *Eg. SUP2 indicates two serial pull up transistors i.e., two pMOS transistors serially connected **to VDD***

2. **SDWn** - (serial down) n-input CMOS serial pull down. (**to GND**)

3. **SPUP_n1_n2_…._nm** - (Serial parallel up) CMOS serial parallel pull up.Series of m parallel groups each consisting of n1, n2, …, nm transistors respectively pulled up **to VDD**

   Eg. SPUP_3_2 has two parallel groups in series and each with 3 and 2 pMOS transistors respectively in parallel leading to power net. (3 pMOS transistors are nearer to VDD).

4. **SPDW_n1_n2_…._nm** - (serial parallel down) n-input CMOS serial parallel pull down.

5. **SMPn** - series of n MP devices (**NOT pulled up to VDD**)

6. **SMNn** - series of n MN devices (**NOT pulled down to GND**)

7. **SPMP_n1_n2_…_nm** - series of m parallel groups each consisting of n1, n2, …, nm pMOS transistors respectively between any two nets (not pulled up).

   Eg. SPMP_2_3_1 has 3 parallel groups in series and each parallel group has 2, 3 and 1 pMOS transistors respectively and they are NOT pulled up.

8. **SPMN_n1_n2_…._nm** - series of m parallel groups of nMOS transistors NOT pulled down.

4. ANTENNA

Process antenna effect or “plasma induced gate oxide damage” is a manufacturing effect. i.e. ***this is a type of failure that can occur solely at the manufacturing stage.*** This is a gate damage that can occur due to charge accumulation on metals and discharge to a gate through gate oxide.

In the manufacturing process, metals are built layer by layer. i.e. metal1 is deposited first, then all unwanted portions are etched away, with plasma etching. The metal geometries when they are exposed to plasma can collect charge from it. Once metal1 is completed, via1 is built, then metal2 and so on. So with each passing stage, the metal geometries can build up static electricity. The larger the metal area that is exposed to the plasma, the more charge they can collect. If the charge collected is large enough to cause current to flow to the gate, this can cause damage to the gate oxide. This happens because since the layers are built one-by-one, a source/drain implant may not be available for discharge as in figure in next slide.

Antenna rules are normally expressed as an allowable ratio of metal area to gate area. Each foundry sets a maximum allowable antenna ratio for its processes. If the metal area–which is cumulative, i.e. the sum of the ratios of all lower layer interconnects in addition to the layer in check–is greater than the allowable area, the physical verification tool flags an error.

4. ANTENNA (CNT)

During the IC manufacturing process, the metal layer is exposed to conditions that lead to the build-up of an electrostatic charge. The amount of charge that builds up depends on a number of factors; **the most important from an antenna standpoint is how much metal is exposed**. As more metal is exposed, the maximum charge that accumulates on the net that the metal is part of also increases. The substrate remains at ground since it is connected to the fabrication device. As a result a voltage gradient develops across the gate oxide. When this gradient becomes large enough, it is relieved via an explosive discharge (i.e. "lightning"). The problem is more significant at smaller technologies because the damage resulting from the discharge is more likely to extend across the entire length of the gate.

Antenna rule checking is different for every process technology because the method for expressing antenna ratio is not standardized.

Antenna repair is accomplished by inserting a reverse-bias diode on the violating net as close to the gates being protected as practical. During normal chip operation, the reverse bias prevents electrons from flowing from the net through the diode and into the chip's substrate. During fabrication, however, the charge on the net can build to the point where the voltage drop across the diode exceeds its break-down voltage.

4. ANTENNA (CNT.)

This voltage is greater than the normal operating voltage, but less than the voltage at which an electrostatic discharge at the gate can be expected. When this happens, the diode allows electrons to flow from the net to the substrate and thus limits how much charge can accumulate on the net. The process is non-destructive, and it's possible that the net could discharge through the diode several times during the fabrication process.

The other way to repair is to "break up" the antenna by shifting briefly to a different metal. When this metal layer is fabricated, the long piece on one side is no longer electrically connected to the gate and does not contribute to any antenna effects. When it is eventually connected through the higher-level metal "bridge," it is no longer exposed to the charge accumulation and again does not contribute to an antenna violation.

How to fix antenna error:

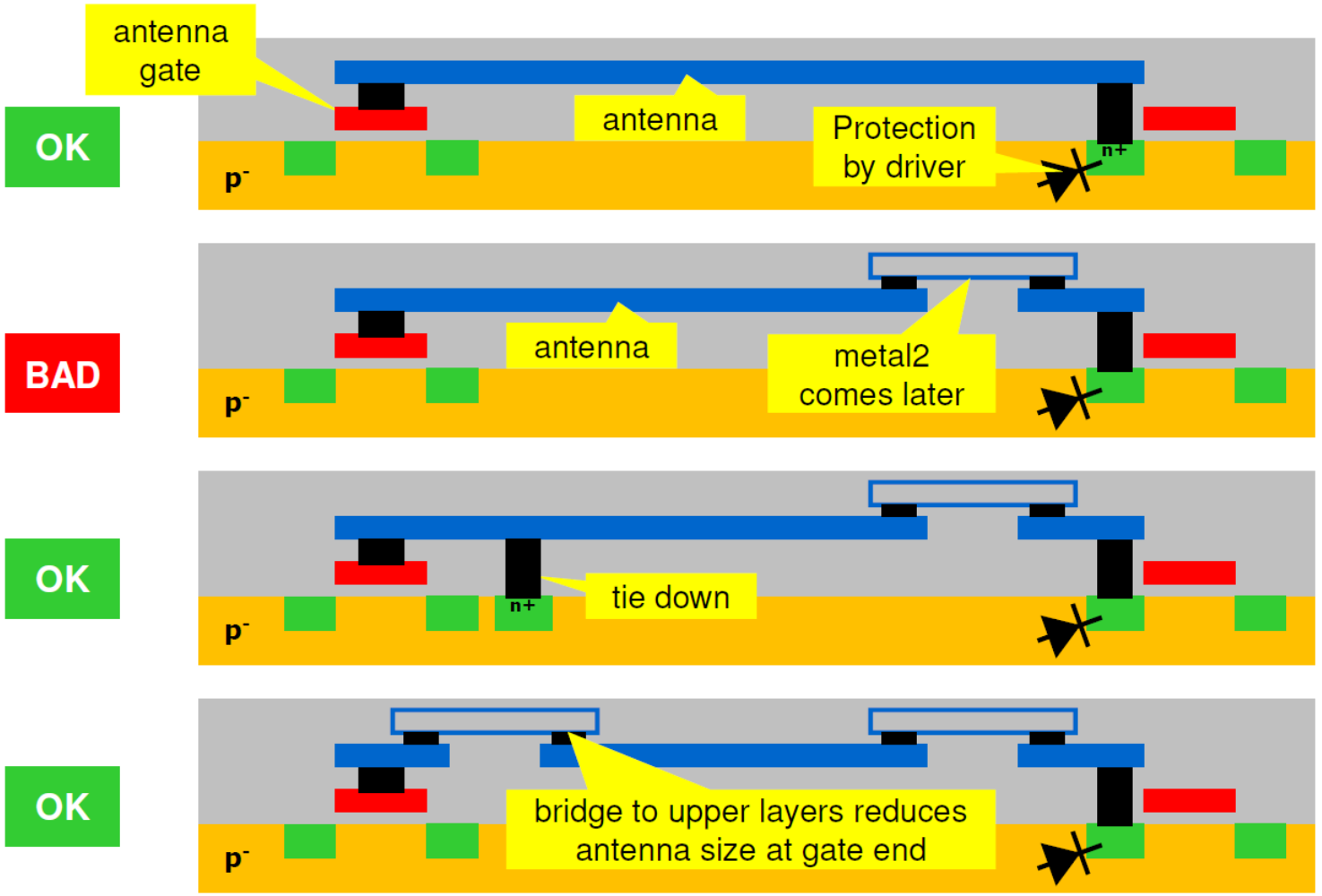
- Using jumpers to break up long wires connected to gates (Jumpers are a short metal segment inserted onto a long route of another metal layer).

- Using diodes to provide a discharge path to the substrate by contact to a diffusion area.

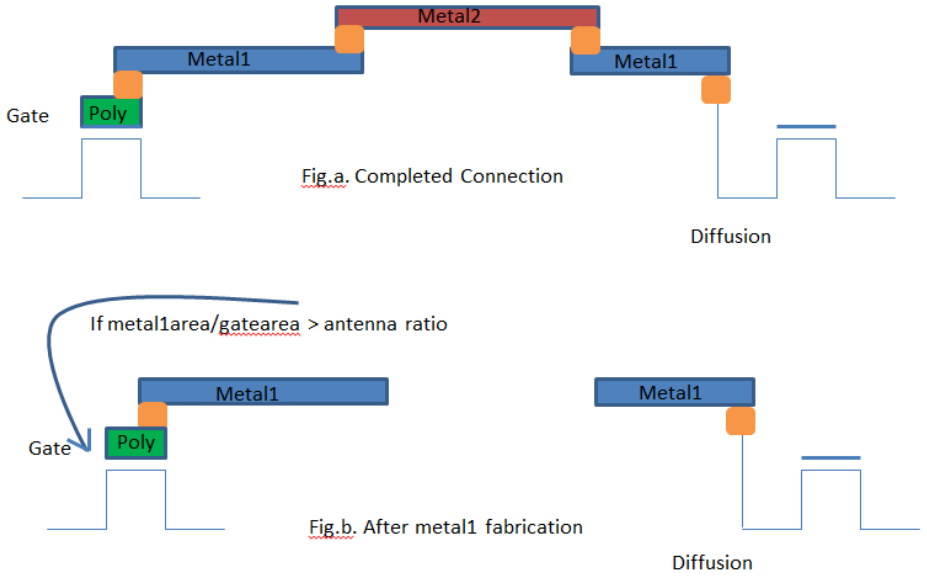
ANTENNA (CNT.)

- **Some process steps can deposit static charge on structures**
  - Amount of charge can depend on *area* or on *periphery*
- **The charge Q leads to a voltage U = Q/C which can destroy transistor gates**
  - Most dangerous for *large structure* (large Q) and *small gate* (small C)
- **The ratio is calculated for each gate. If it exceeds a value, there is danger for an *antenna error*.**
- **Antenna errors are eliminated if:**
  - A drain of a MOS is connected directly. The drain diode has enough leakage to discharge the gate. Often, the 'driver' is connected through higher metals and is not 'seen' in the early process steps
  - An explicit 'tie-down' diode is added (n+ in p-substrate)
  - Signals are fed through higher metals, so that the driving gate is seen when the metal connects (see next page)

ANTENNA (EXAMPLE FOR NMOS)



4. ANTENNA EXAMPLE



For example:

Let's say maximum allowable antenna ratio for metal1 is 400. If the gate area is 1 sq.u and if the metal area connecting to the gate is 500 sq.u, there will be a process antenna violation.

5. WELL ANTENNA

There are Polysilicon antenna, Contact antenna, Via antenna and **Well antenna**, other than metal antenna. What are these antennas refer to? How to correct these antenna violations in layout?

Well antenna means charging of NWELL with respect to gate during fabrication. If the Nwell to substrate leakage current is high enough compared to gate leakage it will destroy the poly gate.

During Reactive ion beam/ion beam etching, this structure connected to the gate will gather enough charge to damage the dielectric of gate, ie, thin oxide. So the problem can be reduced by decreasing the area ratio.

A solution is make nwell to substrate leakage less than gate leakage. For this generally the Nwell is tied down to substrate using M1 (Metal 1). That means we are creating a reverse biased diode.

6. ERC

ERC (**E**lectrical **R**ule **C**heck) involves checking a design for all electrical connections that are considered dangerous. Some errors can be waived, but others ay be fatal errors. So, designers must review every error or warning in LVS/ERC report.

- ***Floating gate error*** – If any gate is unconnected, this could lead to leakage issues.
- ***VDD/VSS errors*** – The well geometries need to be connected to power/Ground and if the PG connection is not complete or if the pins are not defined, the whole layout can report errors like "NWELL not connected to VDD.
- **ERC rules will check below:**
  - Soft connect checking
  - Path checking
  - Ptap/ntap checking
  - MOS S/D power and ground checking
  - Gate directly connecting to power or ground checking
  - Floating well checking
- **Difference between DRC and ERC → DRC is a MUST. ERC is soft, sometimes.**

ERC EXAMPLES:

- Floating Metal, Poly,...
- Antenna rules
- Shorted Drain & Source of a MOS
- No substrate- or well contact ('figure having no stamped connection')
- Different contacts of substrate / well are connected to different nets ('Figure having multiple stamped connections')

(No automatic connection of these nets to avoid circuit parts which are only connected via substrate – can be fatal!)

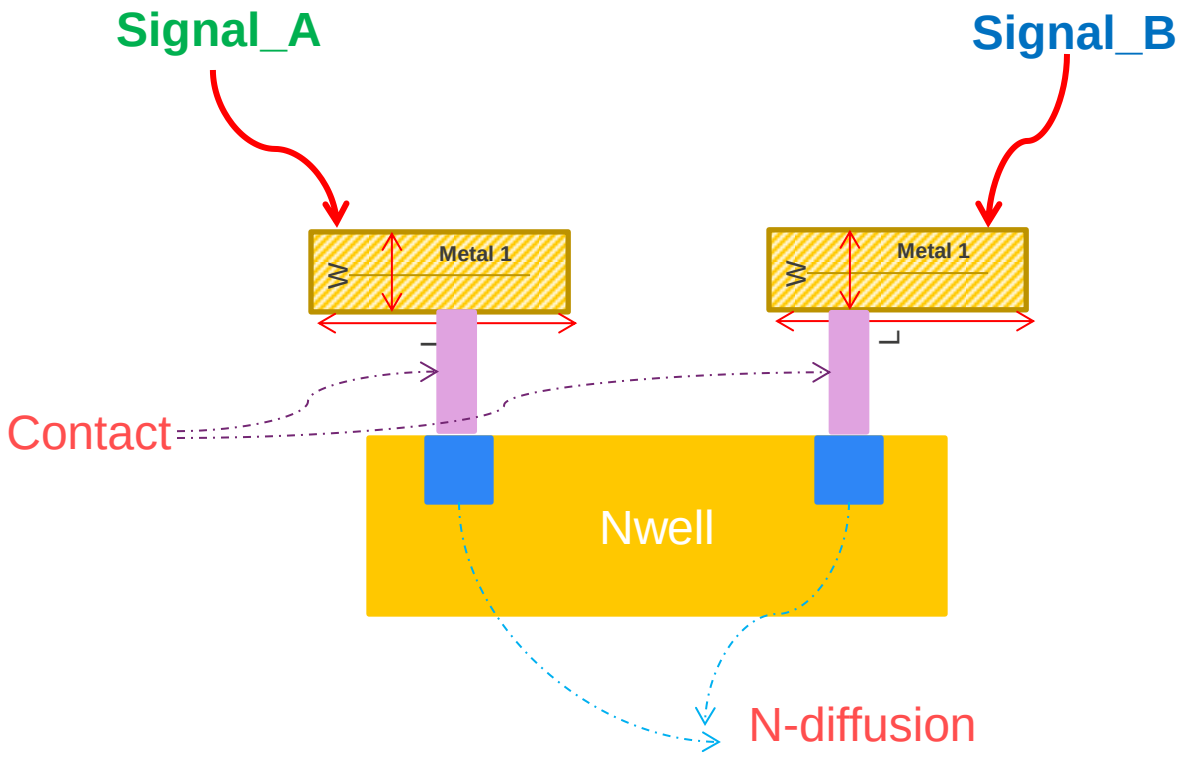
- Distance of MOS to next substrate / well contact too large (Latchup rule)

6. ERC (CNT.)

SOFT CONNECT AND SOFT CHECK

Soft connect and Soft check

❑ Nwell and Pwell are high resistor materials



Case 01:

- Signal_A connects to Signal_B.
- Signal_A connects to Power & Signal_B connects to IP's Power.

→ IP will get high resistor but IR-Drop is very Serious.

Case 02: (Open)

- Signal_A connects to Power.
- Signal_B connects to Ground.

→ Signal_A and Signal_B will be shorted

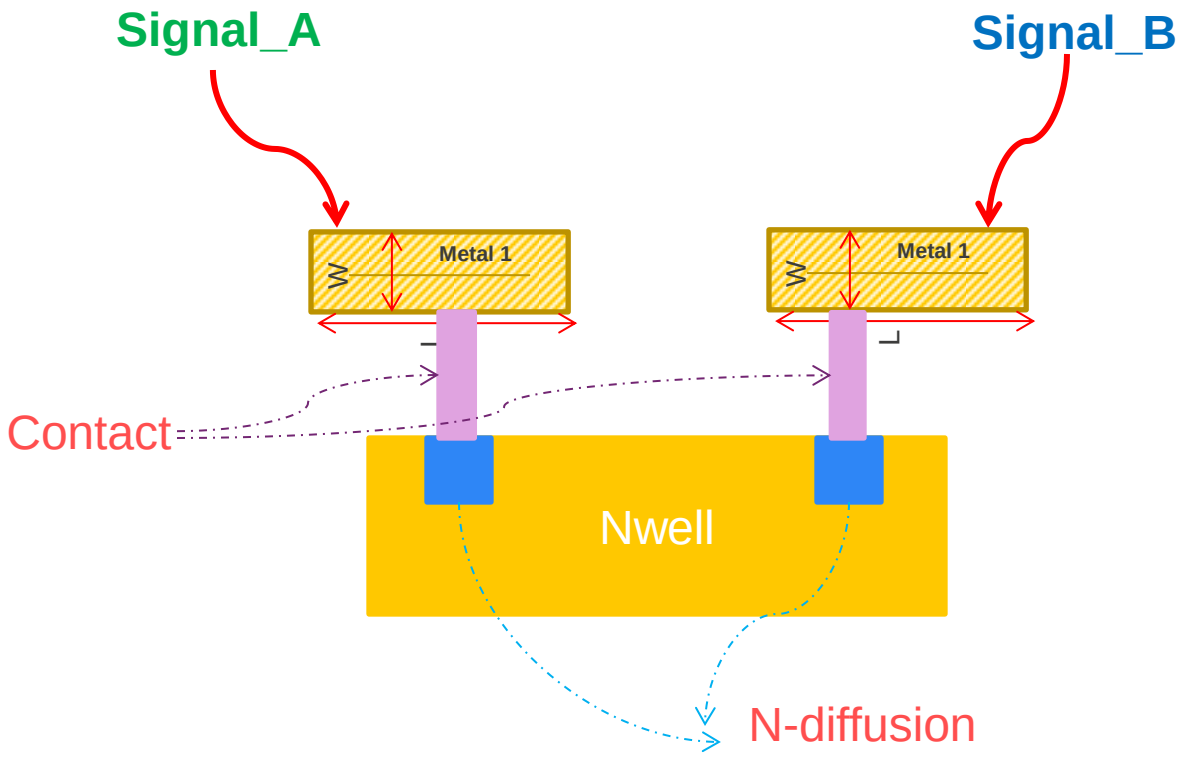
➔ **Error.**

6. ERC (CNT.)

SOFT CONNECT AND SOFT CHECK

Soft connect and Soft check

❑ Nwell and Pwell are high resistor materials



Case 01:

- Signal_A connects to Signal_B.
- Signal_A connects to Power & Signal_B connects to IP's Power.

→ IP will get high resistor but IR-Drop is very serious.

Case 02: (Open)

- Signal_A connects to Power.
- Signal_B connects to Ground.

→ Signal_A and Signal_B will be shorted

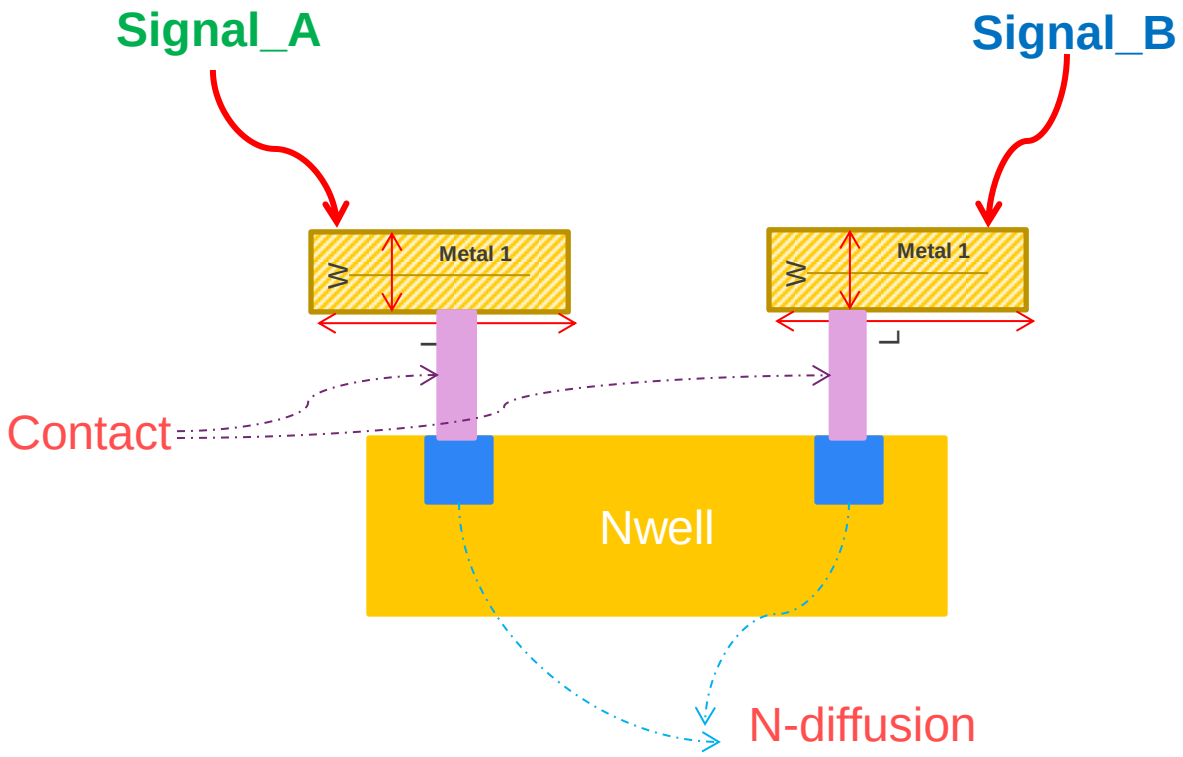
➔ **Error.**

6. ERC (CNT.)

SOFT CONNECT AND SOFT CHECK

Soft connect and Soft check

❑ Nwell and Pwell are high resistor materials



Case 01:

- Signal_A connects to Signal_B.
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Case 02: (Open)

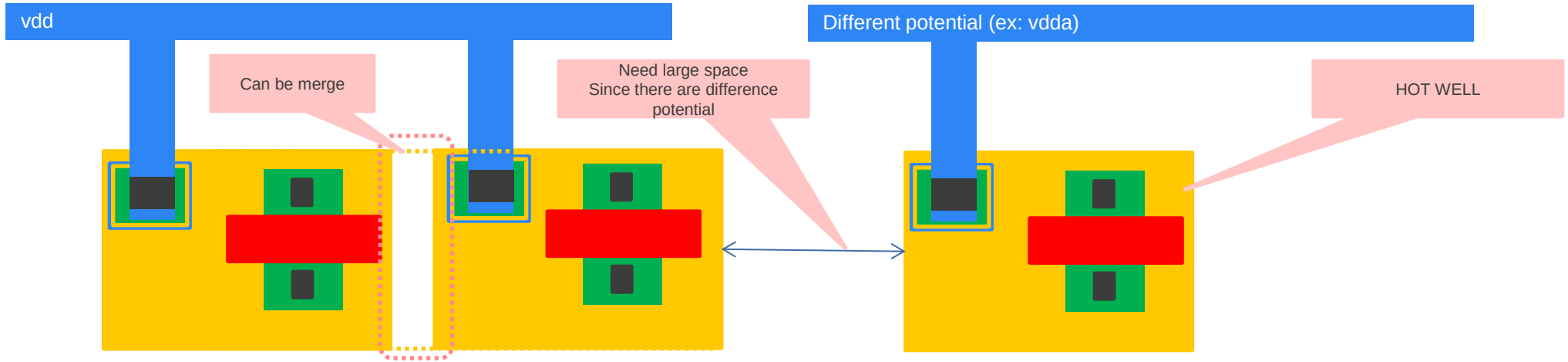
- Signal_A connects to Power.
- Signal_B connects to Ground.

→ Signal_A and Signal_B will be shorted

➔ **Error.**

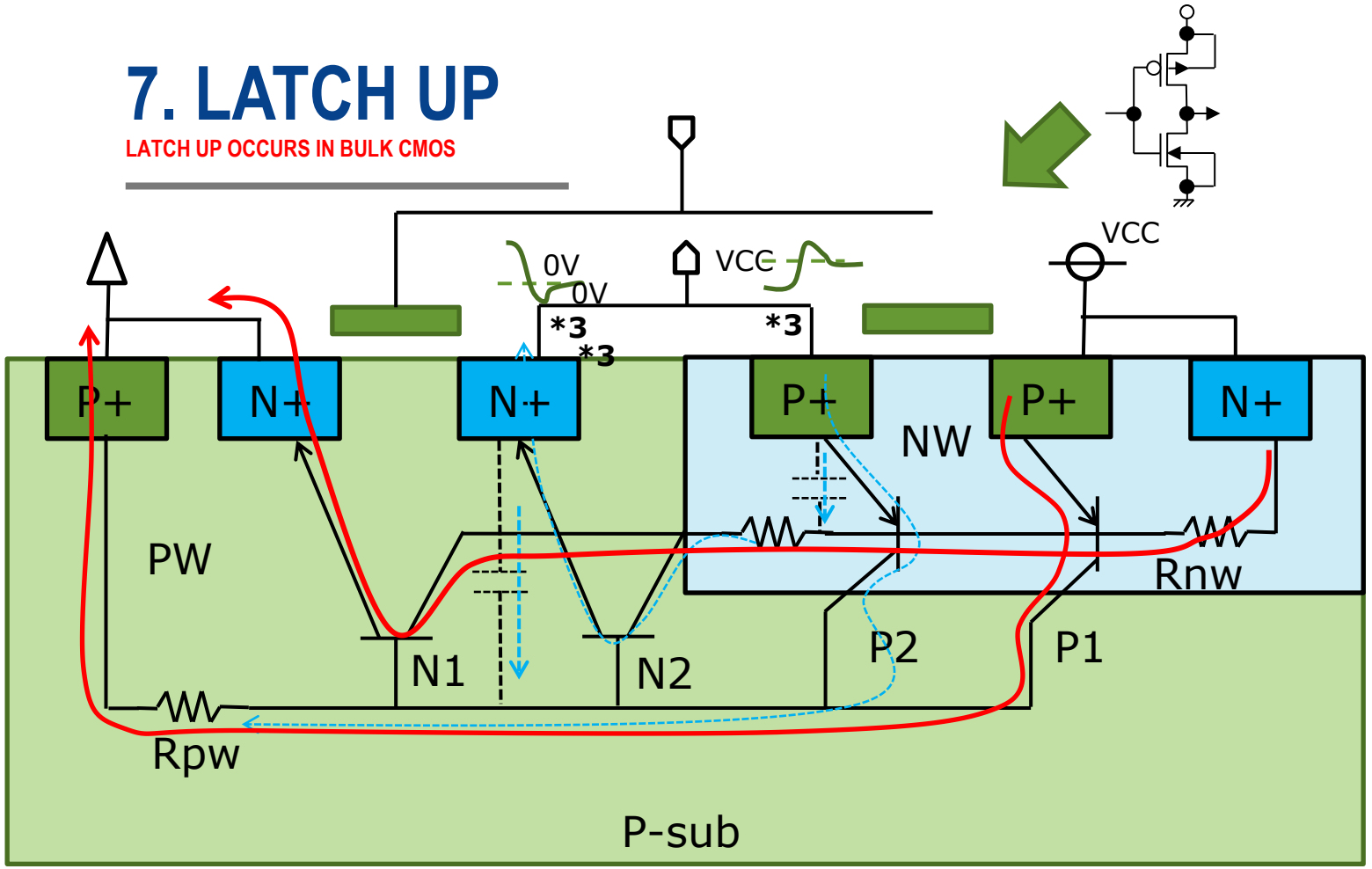
NOTE FOR NWELL

- **Most NWELLs are connected to positive supply.**
  - Shorts between such wellls are no problem, and best merge wells in layout.
- **Sometimes NWELLs are on different potential (Analogue designs, source follower).** So these NWELL may not be merged → Larger distance required.
- **Such wells are called hot wells**
- **There are sometimes symbolic layers to tell the tool explicitly that a well is hot and that more severe rules must be applied**



7. LATCH UP

LATCH UP OCCURS IN BULK CMOS



Trigger current

LUP large current

A byproduct of the Bulk CMOS structure is a pair of parasitic bipolar transistors. The collector of each BJT is connected to the base of the other transistor in a positive feedback structure. A phenomenon called latchup can occur when:

- Both BJT's conduct, creating a low resistance path between Vdd and GND **and,**
- The product of the gains of the two transistors in the feedback loop, b1 x b2, is greater than one. The result of latchup is at the minimum a circuit malfunction, **and in the worst case, the destruction of the device.**

7. LATCH UP (CNT.)

LATCH UP OCCURS IN BULK CMOS

Latchup may begin when Vout drops below GND due to a noise spike or an improper circuit hookup (Vout is the base of the lateral NPN Q2). If sufficient current flows through Rpw to turn on Q2 (I Rpw > 0.7 V), this will draw current through Rnw. If the voltage drop across Rnw is high enough, Q1 will also turn on, and a self-sustaining low resistance path between the power rails is formed. If the gains are such that b1 x b2 > 1, latchup may occur. Once latchup has begun, the only way to stop it is to reduce the current below a critical level, usually by removing power from the circuit.

“The most likely place for latchup to occur is in pad drivers, where large voltage transients and large currents are present.”

At summarize, If current flow in well resistors Rpw and Rnw, would develop a finite voltage across the Base-Emitter junction which may turn on any of the transistors and a positive feedback from the other transistor would give rise to latch-up phenomenon manifested as high ‘VDD’ to ‘GND’ current inrush.

7. LATCH UP (CNT.)

HOW TO PREVENT LATCH UP (LUP) ERRORS

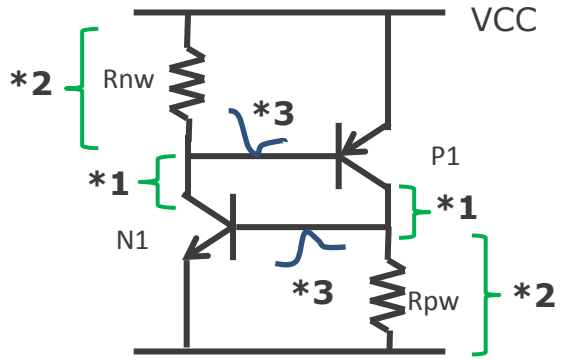
Reduce the gain product b1 x b1

- Move n-well and n+ source/drain farther apart increases width of the base of N1 and reduces gain beta2 > also reduces circuit density
- Buried n+ layer in well reduces gain of P1

Reduce the well and substrate resistances, producing lower voltage drops

- Higher substrate doping level reduces Rpw
- Reduce Rnw by making low resistance contact to GND
- Guard rings around p- and/or n-well, with frequent contacts to the rings, reduces the parasitic resistances.

Separate Nmos and Pmos from I/O (IO is noise source)



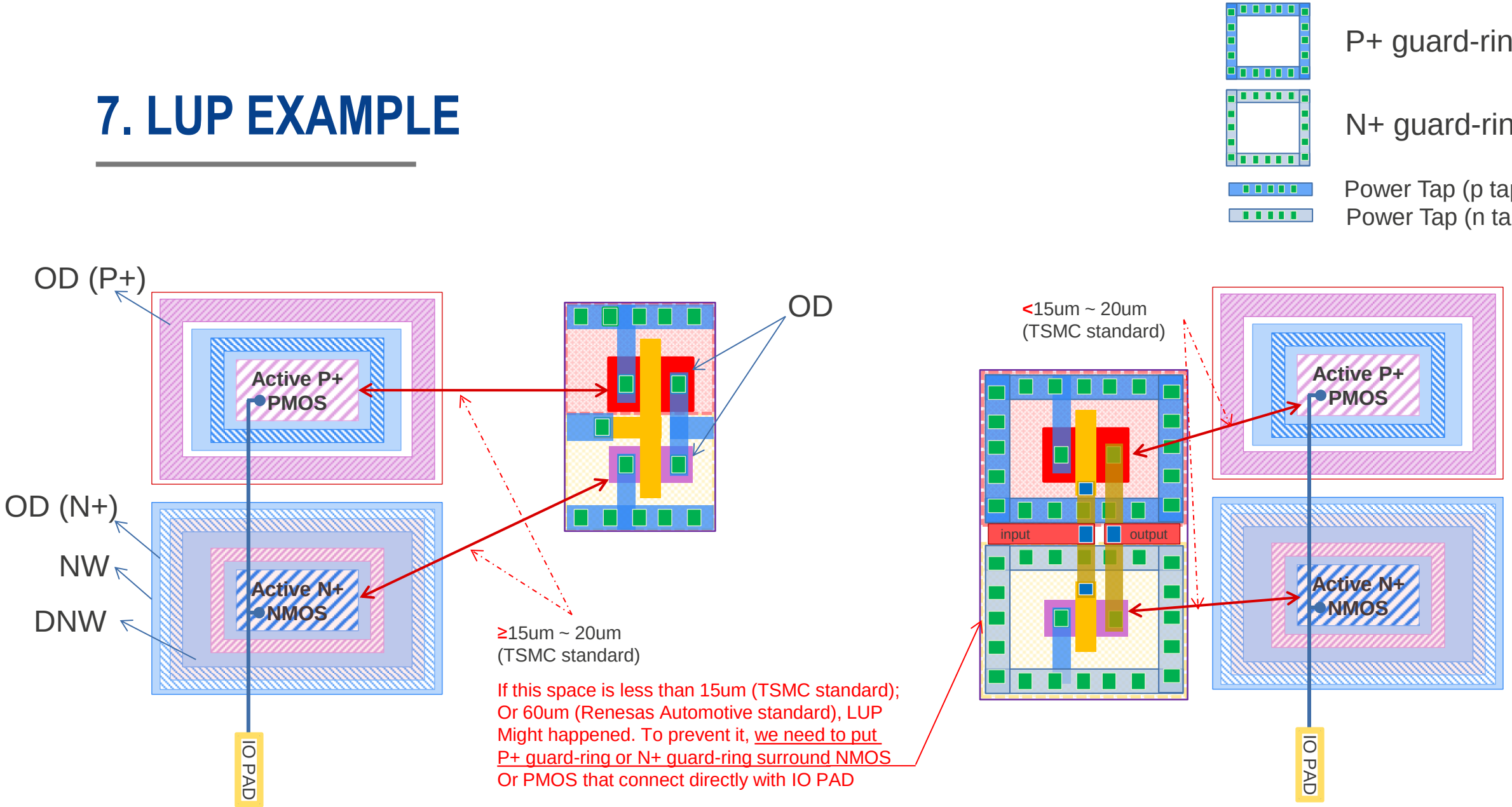
TAPCELL

The CMOS FETs are actually 4 terminal devices, source, gate, drain and body. TAP cells provide a low resistance connection path to the body. In digital circuits, body of MOSFETs are usually connected to the power or ground. That is why if you look closely at the digital P&R layout, you'll see the TAP cells are usually on the power rails of standard cells.

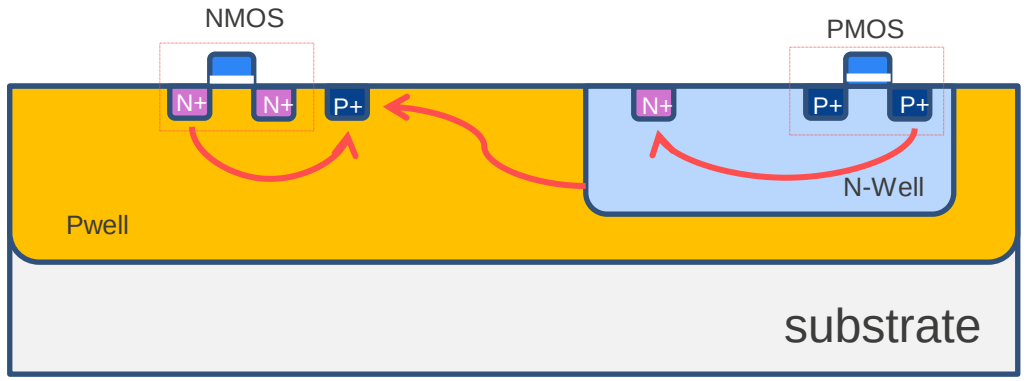
tap cells gives reverse bias to the nwell and p well .
This is to avoid latchup

Nowadays, Standard cells do not have internal tap to N well (P substrate process) to reduce design complexity of standard cells. Hence tap to wells is done by external cells called "TAP cells". These TAP cells are sprinkled all over core area at regular distance (decided by foundry).

7. LUP EXAMPLE



8. DEEP N-WELL



Substrate noise currents are shown as red lines.

On a conventional CMOS process (see above figure), NMOS devices are formed in a P well or substrate connected to ground (or the most negative supply in the circuit). PMOS devices are formed in an N well connected to the most positive supply.

Substrate noise caused by minority carrier injection into the substrate and well can be collected by the use of well taps and/or guard rings. An additional problem exists in that capacitive coupling of noise from the well to the substrate means more noise reaches the supply. In digital circuitry this is usually not a problem owing to the relatively high noise immunity of logic gates. However in analog design, for example a 12 bit ADC, noise can be a serious problem. A variety of techniques can be used to minimize this noise, for example by keeping analog devices surrounded by guard rings, or using a separate supply for the substrate/well taps. However guard rings alone cannot prevent noise coupling deep in the substrate, only surface currents.

Another problem is that it is not possible to isolate NMOS devices. So relatively noisy digital logic cannot be isolated completely from more sensitive analog areas.

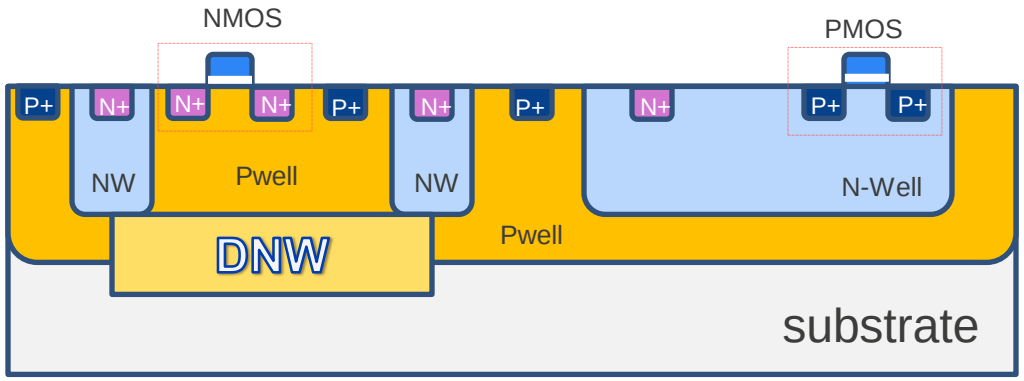
A solution is to isolate the NMOS devices by using an extra well – a '**deep N well**'. So in figure 2 the NMOS device is fabricated in a P well or substrate completely surrounded by an N type diffusion.

8. DEEP N-WELL (CNT.)

In this case, the deep N well is formed by a high energy ion implantation to give peak impurity concentration deep enough to un-affect the NMOS device performance. Connection to the deep N well is formed by a N well ring that is connected to VDD. The deep N well has the effect of decreasing the noise coupling through it to the substrate and giving the advantage of fully isolated NMOS devices – which can in theory be at a different potential from ground.

The implications on layout are of course larger area for Nmos devices due to the extra N well rings used to connect to the deep N well. However the noise performance improvements justify this for sensitive analog design.

In summary, the use of deep N well devices can significantly reduce noise coupling between sensitive analog areas and more noisy digital regions in mixed-signal designs.



8. DNW (CNT.)