Latch-up method

IO Technical Meeting

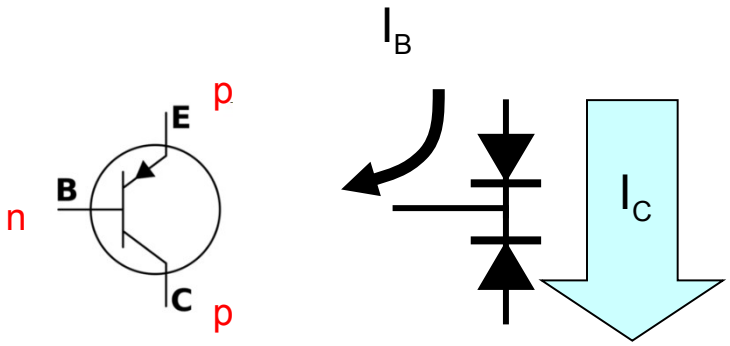
Renesas Electronics Corporation
Department name

09/11/12 Rev. 0.00

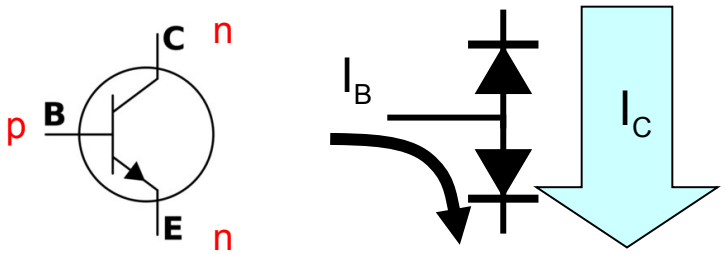
RENESAS Group CONFIDENTIAL

Summary of Device basic characteristics

- Bipolar Transistor



Majority carrier = Hole



Majority carrier = Electron

The direction of hole and electric current is same.
The direction of electron and electric current is opposite

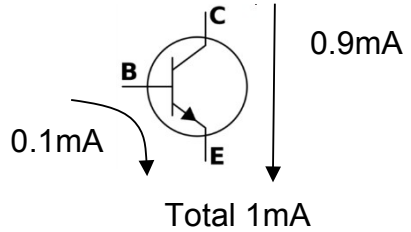
Bip Tr		MOS Tr
Emitter	: emit carrier	= Source
Collector	: collect carrier	= Drain
Base	: base of electric current	= Gate

I_C / I_B = Current amplification factor(h_{FE})

$I_2 = h_{21} * I_1$

Forward (F) element of H parameter @common Emitter

$$\begin{pmatrix} V_1 \\ I_2 \end{pmatrix} = \begin{pmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{pmatrix} \begin{pmatrix} I_1 \\ V_2 \end{pmatrix}$$



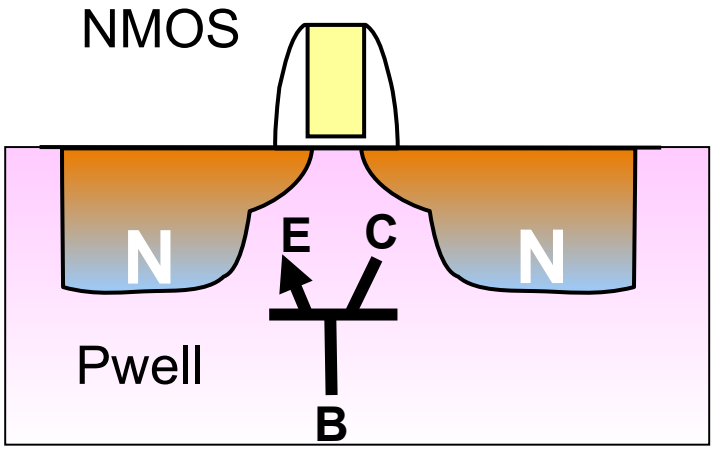
$I_B = I_E - I_C = 0.1$

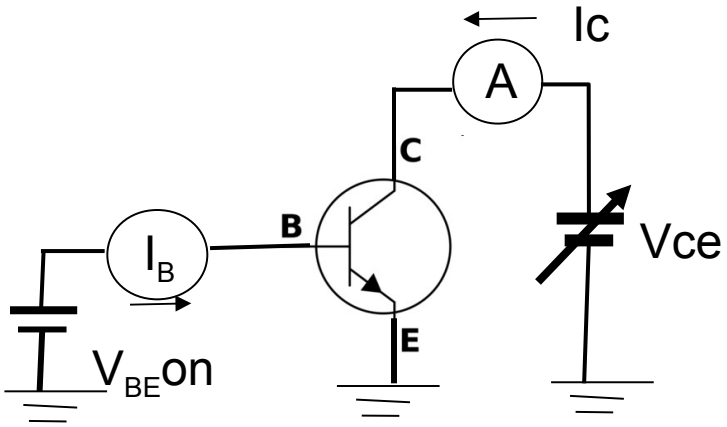
$h_{FE} = I_C / I_B = 0.9/0.1 = 9$

Summary of Device basic characteristics

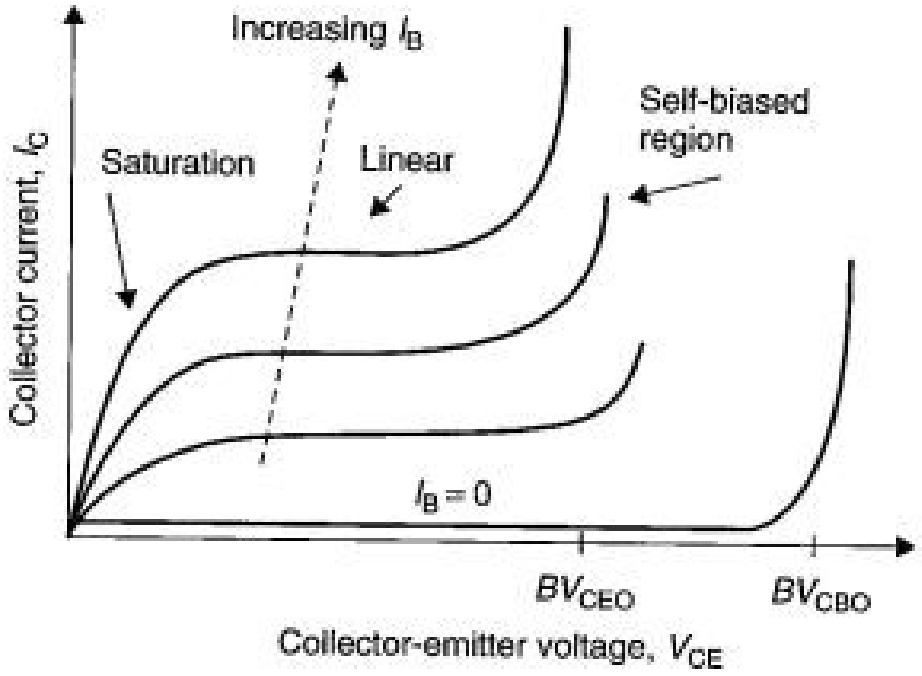
- Bipolar Transistor

N(P)MOS Transistor is horizontal NPN(PNP)Transistor.



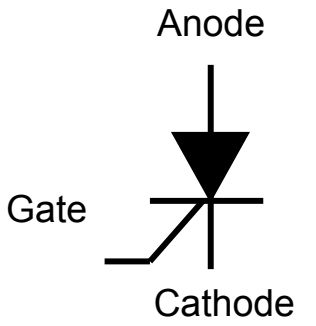


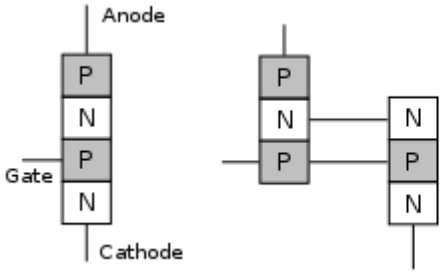
Parasitic NPN Transistor
Vce-Ic Charactaristics



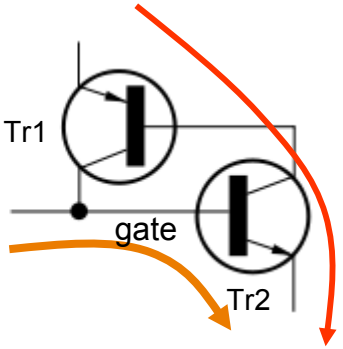
Summary of Device basic characteristics

■ SCR (Silicon Controlled Rectifier) or Thyristor

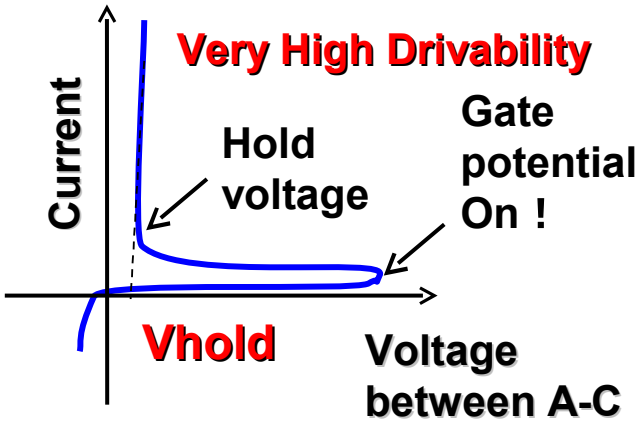




The electric current flows in succession.



Once switched on,
the thyristor can only
be turned off by removing
the supply voltage



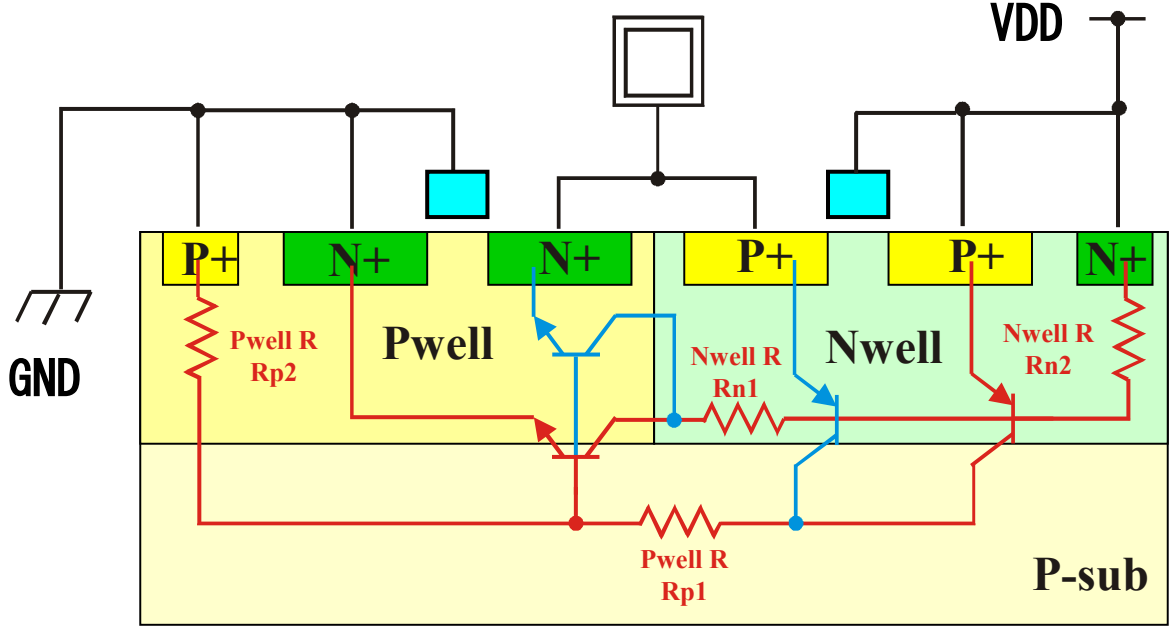
(1)When Gate current is equal zero,
neither transistor is conducting.

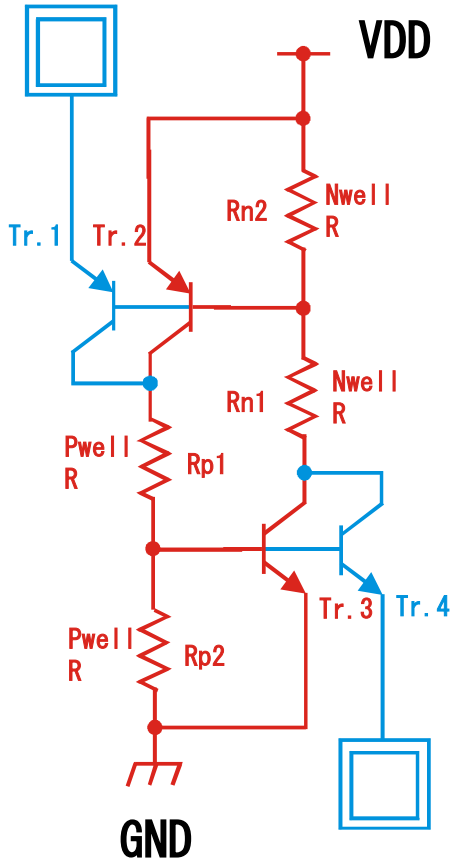
(2) When a small current is through Gate,
Turn on the transistor Tr2
and Turn on the transistor Tr1 weakly.

(3) When a sufficient current is through Gate,
Turn on Tr2 and Tr1.
TR2 and Tr1 "on" state is maintained all the time.

Parasitic SCR component into CMOS Inverter

There are 4 parasitic SCR into one Inverter.
This is the factor of the latch up phenomenon.

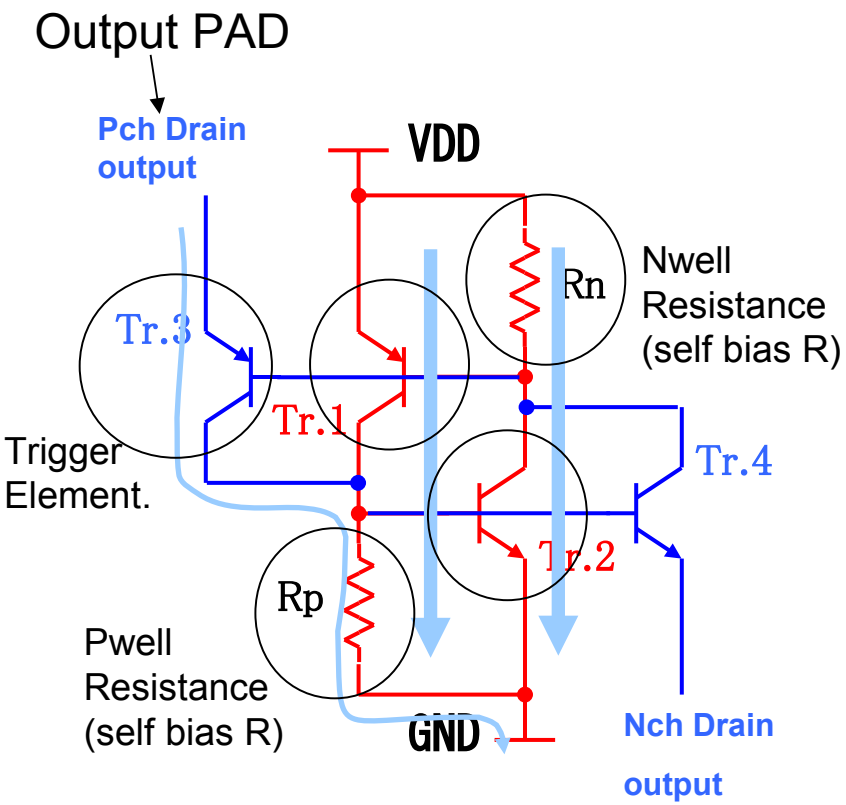




There are resisters between SCRs.
SCR characteristic depend on resistance.
↓
We can prevent latch up.

Latch up behavior explanation

When Output Level is higher than VDD level.



SCR + Trigger Circuit

(1) Surge Current flow Rp through Tr.3

(2) Current is through base of Tr.2 by (1) and Tr.2 turn ON

(3) Current is through base of Tr.1 by (2) and Tr.2 turn ON

(4) Large current continues flowing forever unless we switch it off.

The Cause that Latch up occur

1. Noise of I/O pin from LSI outside

   Noise become trigger when over Voltage or Current is generated from Main board to LSI signal pin during LSI movement.

2. Noise of LSI Power Line

   Noise from Power pin from LSI outside (same 1.).
   Noise become trigger When IR-Drop occur.

3. Noise of LSI GND Line

   Float of the board by the large outbreak of the board electric current.

Latch up countermeasure

(1) Reduce WELL Resistance

Reduce Rp2 and Rn2 resistance as smaller as possible.
Because Well Resistance cause bias of VBE.
(Using low resistance Wafer)

(2) Placement of WELL contact effectively

Placement of Well contact prevent that electric potential of well rise.
This is not easy to bias VBE.

(3) Separate Distance between PMOS and NMOS

Separating distance between PMOS and NMOS is equal to increase Rp1 resistance.
Rp1 limit Collector of Tr.2 and can't supply Base current of Tr.3 sufficiently.

(4) Placement of Guard Ring

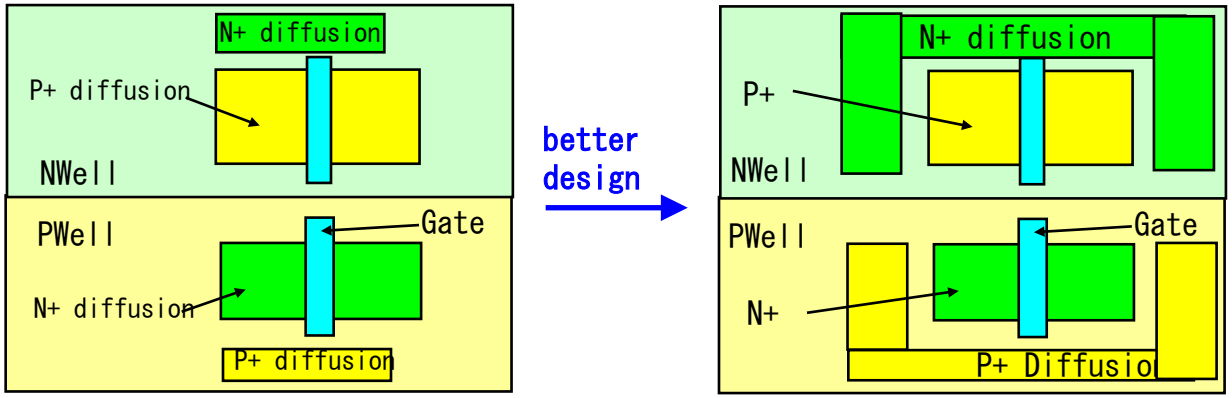
Big MOS such as Main Buffers or Driver should be surrounded it by Guard Ring
Because They are ease to be affected by Nise from LSI outside.

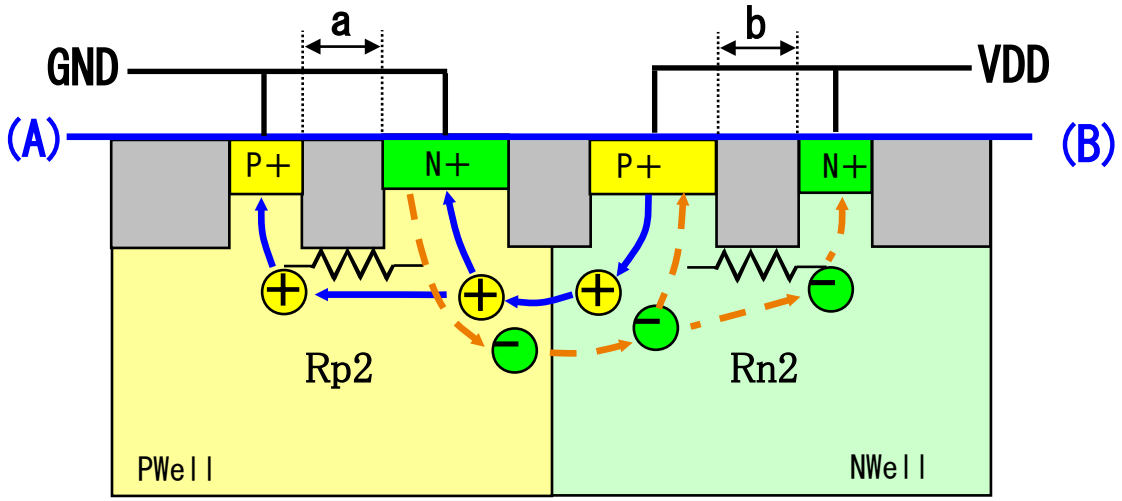
(5) Proper placement of PMOS、NMOS

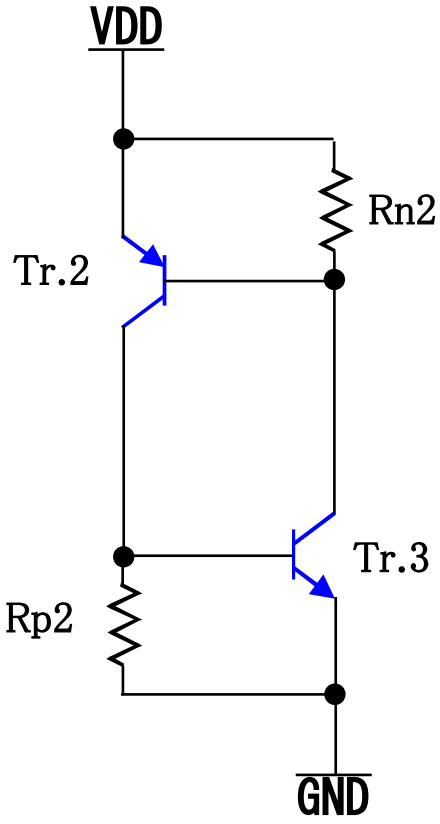
We should layout IO to become PNNP.

Example of Latch up measures (1) (2)

- Place Tap as many as possible.
- Rp2, Rn2 as smaller as possible.
  →Minimize the distance between a and b.

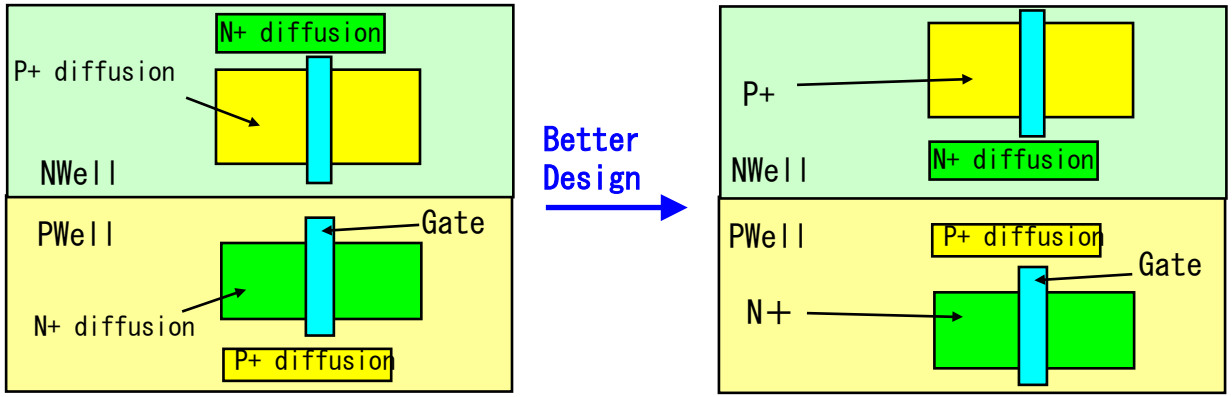


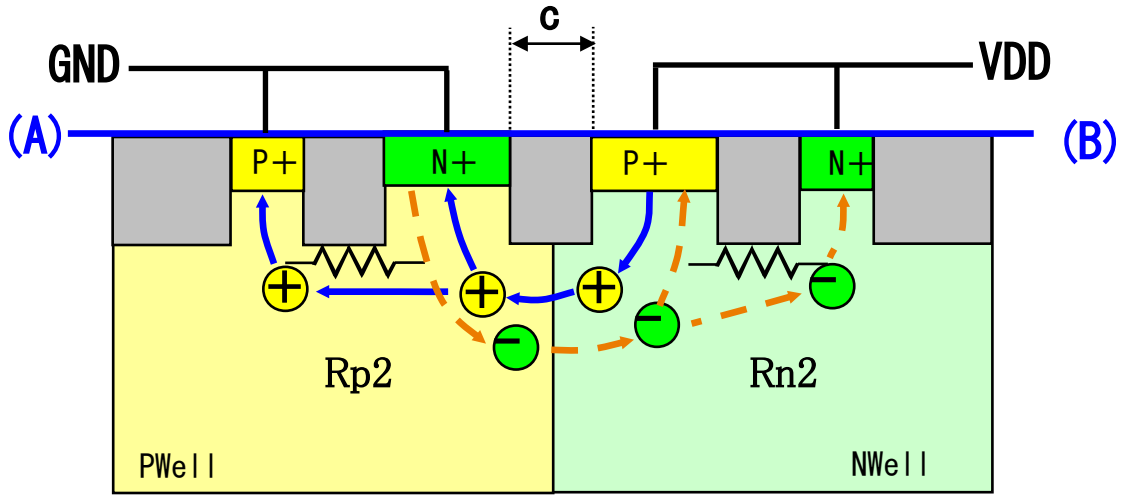




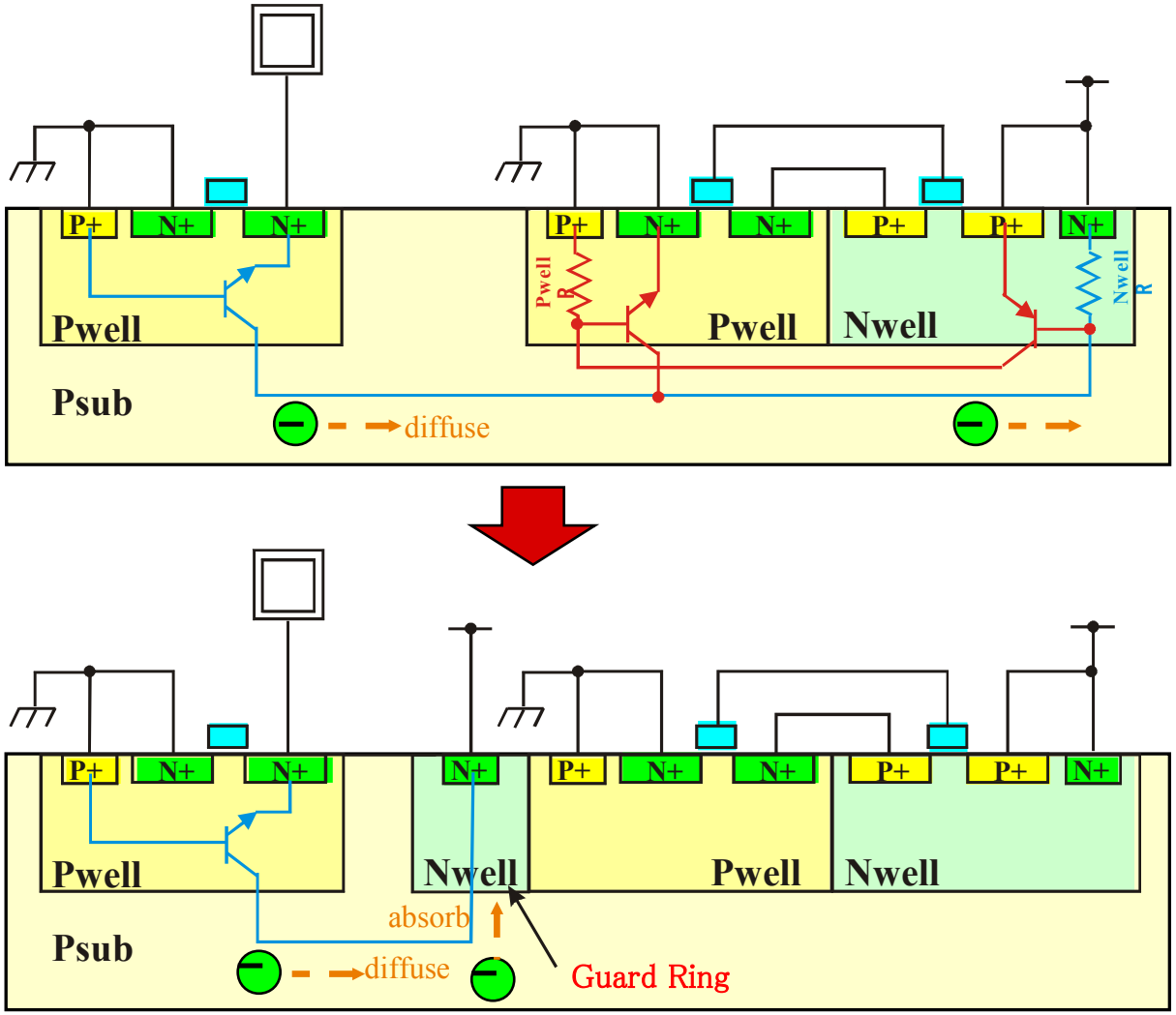
Example of Latch up measures (1) (2) (3)

- Place Tap between CMOS Tr.
- Maximize distance of C (PN separation width)





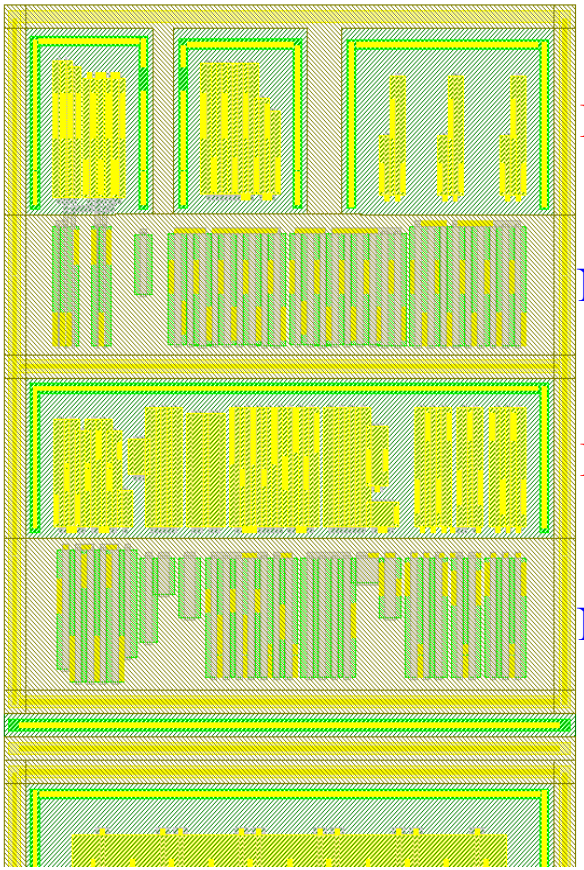
Example of Latch up measures (4)



Example of Latch up measures (5)

Proper placement of PMOS、NMOS placement

This placement can reduce PN contact from 4 to 2



Pre Buffer Area

Main Buffer Area

PMOS area

NMOS area

PMOS area

NMOS area

PMOS buffer

You'd better opposite place

PMOS area

NMOS area

PMOS buffer

Testing of Latch up

Latch up Testing at Renesas

－JEDEC standard　JESD78

(1) Pulse electric current injection method (I-Test)

Inject 150mA (@ Ta) current each I/O pin.
If Power supply current is over 10mA
or 1.4 times current before testing,
It is NG.

(2) Power supply overvoltage method (Vsupply overvoltage test)

voltage up to biggest rated 1.5 times
of recommended operating power supply voltage.
Judge is same as (1)

－other

(3) Condenser voltage mark addition

This test is optional.
Inject ESD surge current in the state of supplying voltage.

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