PHYSICAL DESIGN BIAS LIBRARY INVESTIGATION

(INTERNAL USED ONLY)

2016 DEC 25TH
TRAN HUY
ASE PHYSICAL DESIGN
BACKEND3
RENESAS DESIGN VIETNAM CO., LTD.

Approver	Checker	Author
		RVC/BackEnd3 Tran Quoc Huy 2016 – Apr - 21

NWELL – PWELL BIAS

Some process technologies allow dedicated voltage supplies, instead of normal rail voltages, to be applied to n-well and p-well regions of the chip. Applying a bias voltage to a well changes the threshold voltage (Vth) for transistors in the well, affecting the performance and leakage current.
The synthesis and physical implementation tools offer an optional mode to specify the n-well and p-well bias supply infrastructure using UPF commands. In this mode, the tool automatically makes supply connections to the n-well and p-well bias pins.

To enable the UPF-based well bias mode, set the
`enable_bias` design attribute to `true` in the UPF command file as follows:

```
set_design_attributes -elements {.} -attribute enable_bias true
```

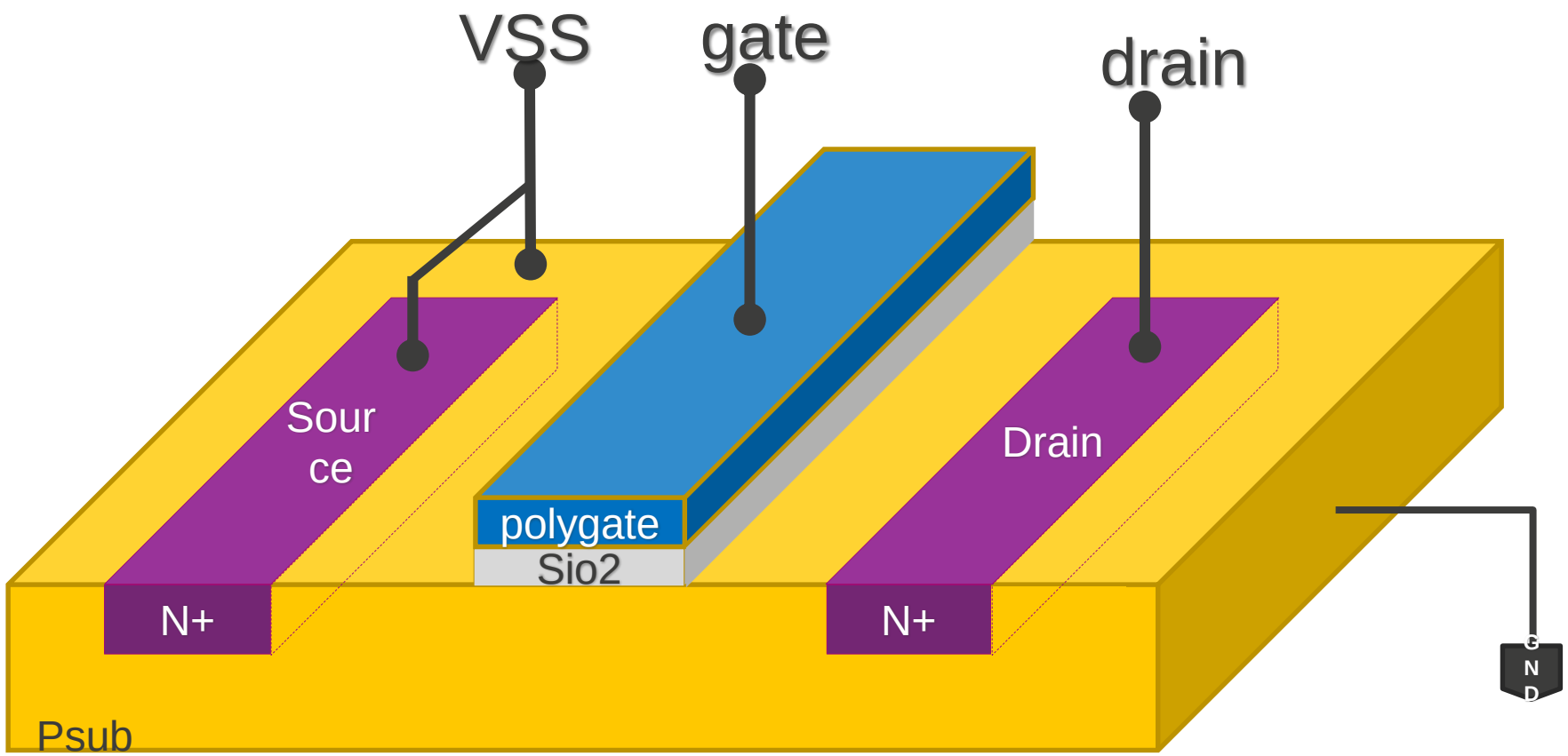
or in the IC Compiler II tool:

```
set_app_options -name mv.upf.bias_support -value true
```

With the enable_bias design attribute set to true, supply sets and supply set handles can be used to specify the bias supply connections. The well bias pins, along with the power supply and ground pins, are connected automatically for standard cells, macros, and other types of cells.

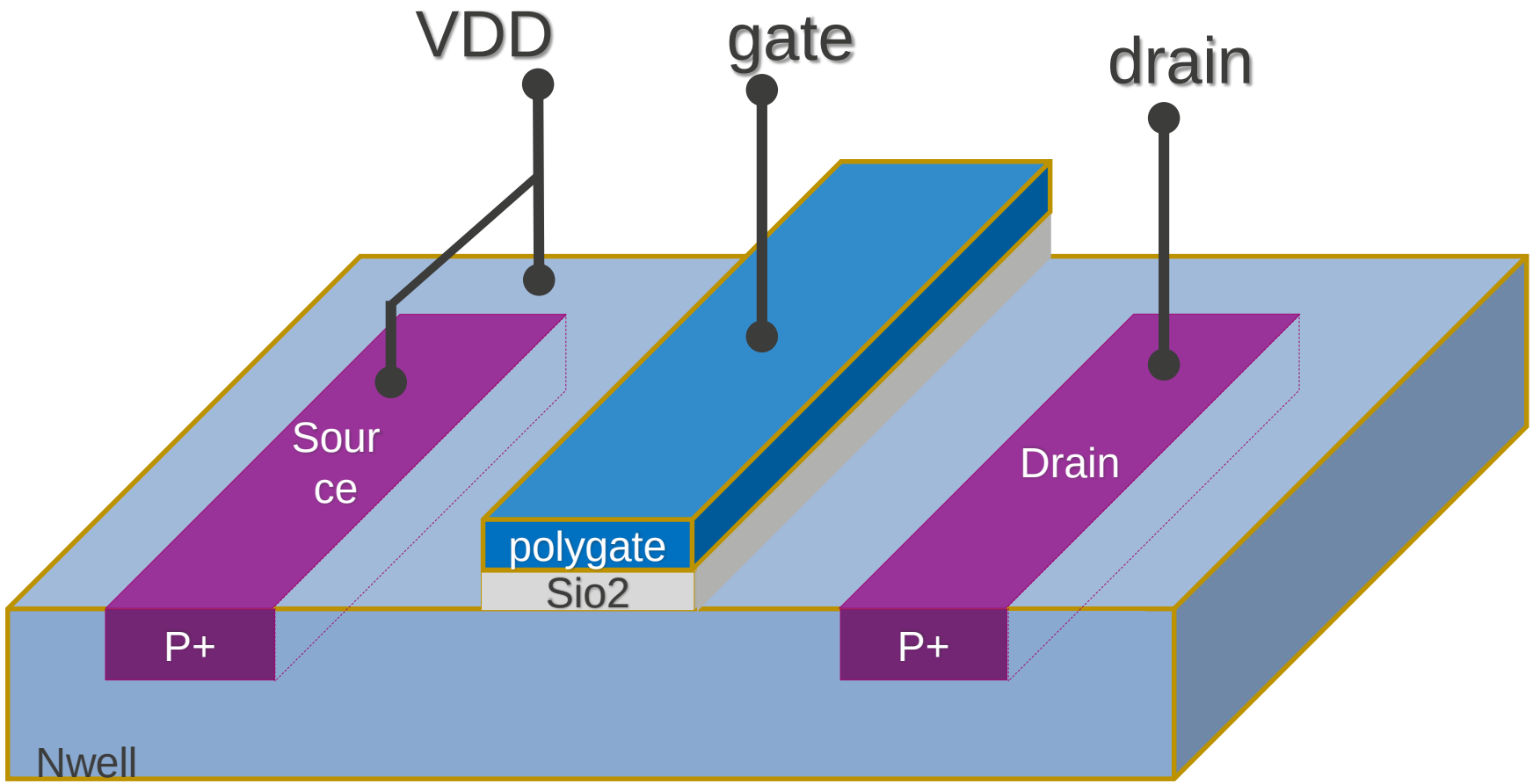
In simpler CMOS process technologies, the NMOS transistors are typically built on a p-type silicon substrate and PMOS transistors are built in n-type wells embedded in the p-type substrate, as shown in below figure

The p-type substrate is connected to the ground voltage, which prevents the p-n junctions from becoming forward biased between the p-type substrate and each of the n-type terminals of the NMOS transistor.



In simpler CMOS process technologies, the NMOS transistors are typically built on a p-type silicon substrate and PMOS transistors are built in n-type wells embedded in the p-type substrate, as shown in below figure

The n-well is connected to the positive rail voltage, which prevents the p-n junctions from becoming forward biased between each of the p-type terminals of the PMOS transistor and the n-well. The n-well is reverse biased with respect to the p-type substrate.



BIAS LIBRARY DEVICES THEORY

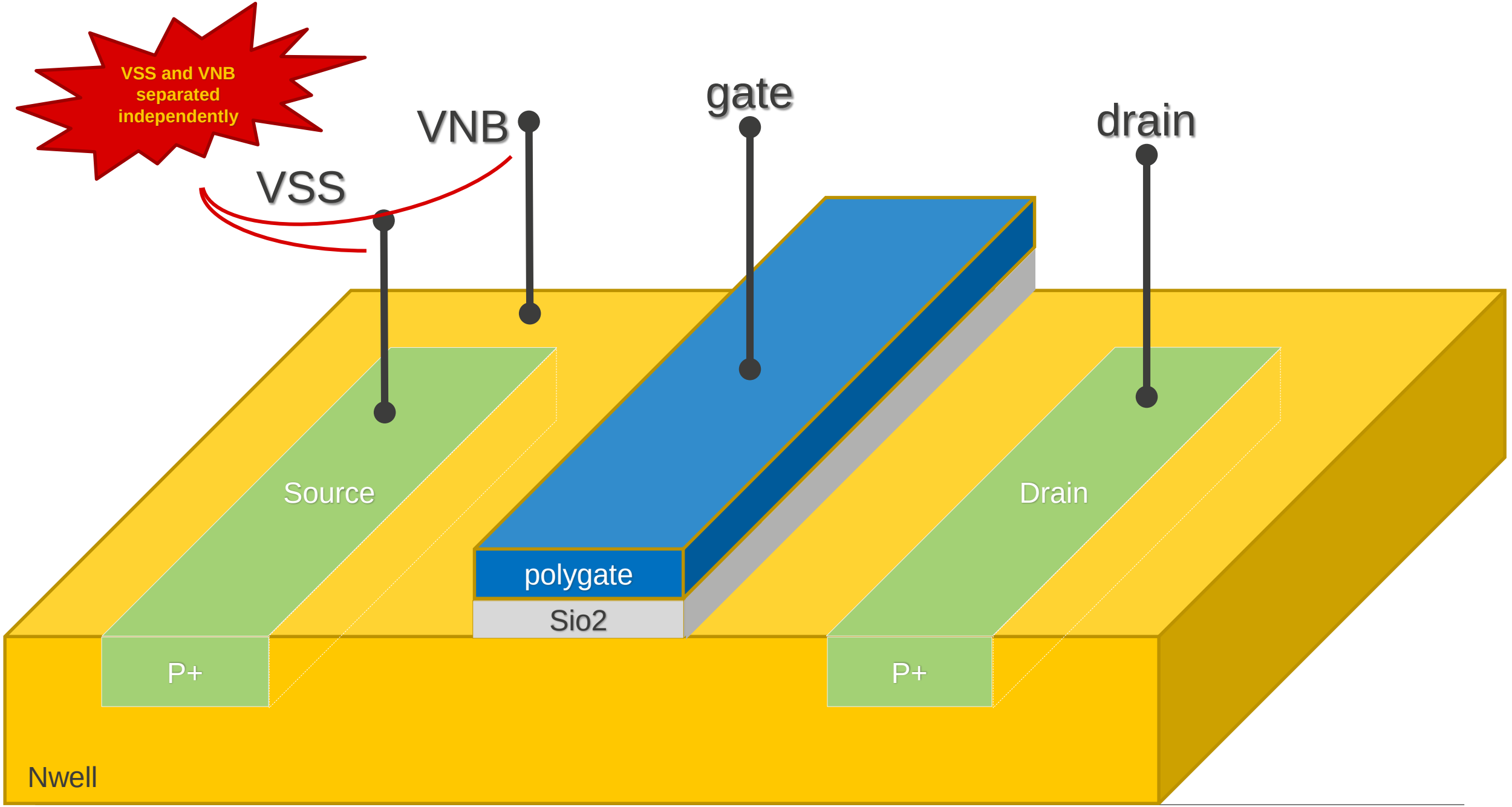
Below figures shows how to build NMOS transistors in p-wells and PMOS transistors in n-wells, where the n-well and p-well voltages can be independently controlled. This type of construction requires the use of an advanced process technology. (T16FF)

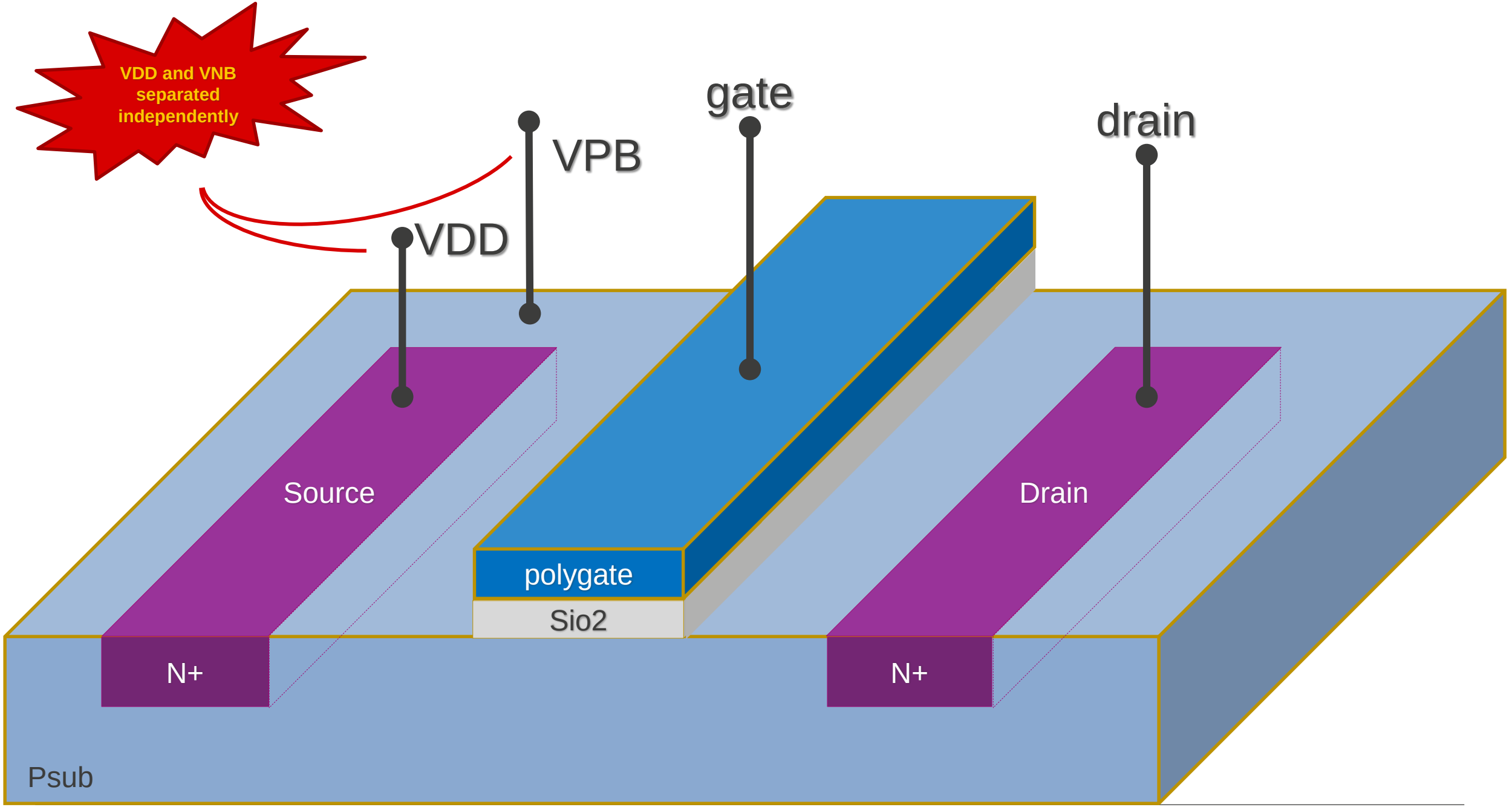
As in simpler CMOS technologies, the n-well can be connected to the rail voltage and the p-well can be connected to ground. However, the technology can allow different voltages to be applied to the wells to modify the behavior of the transistors, using the terminals labeled VNB (voltage n-well bias) and VPB (voltage p-well bias) in the figure.

For example, applying a voltage slightly above ground to the p-well using the VPB pin lowers the NMOS transistor threshold voltage, resulting in faster switching at the cost of higher leakage current. Conversely, applying a voltage slightly below ground on the same pin raises the NMOS transistor threshold voltage, reducing leakage current at the cost of speed.

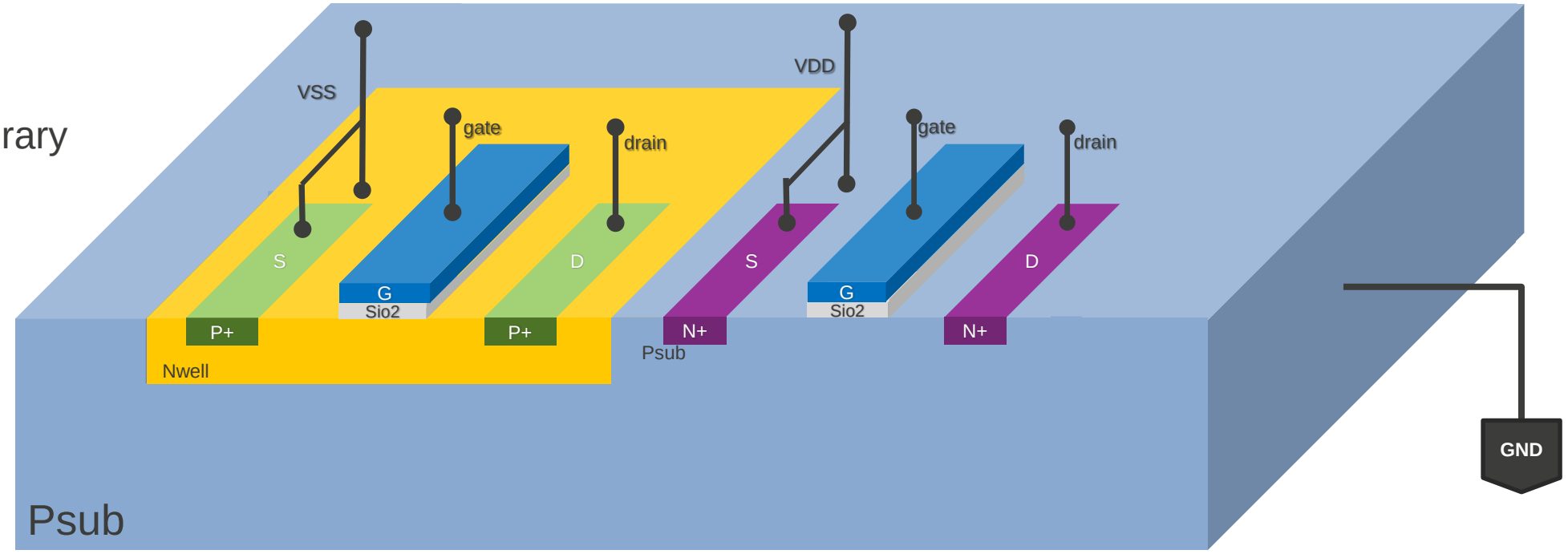
Similarly, applying a voltage slightly above or below the rail voltage to the n-well using the VNB pin modifies the threshold voltage of the PMOS transistors to achieve better speed or less leakage.

The well voltages can be modified dynamically to increase the speed when needed or to reduce leakage during standby mode. Alternatively, the bias voltage might be applied statically to compensate for process variations or for other adjustment purposes.

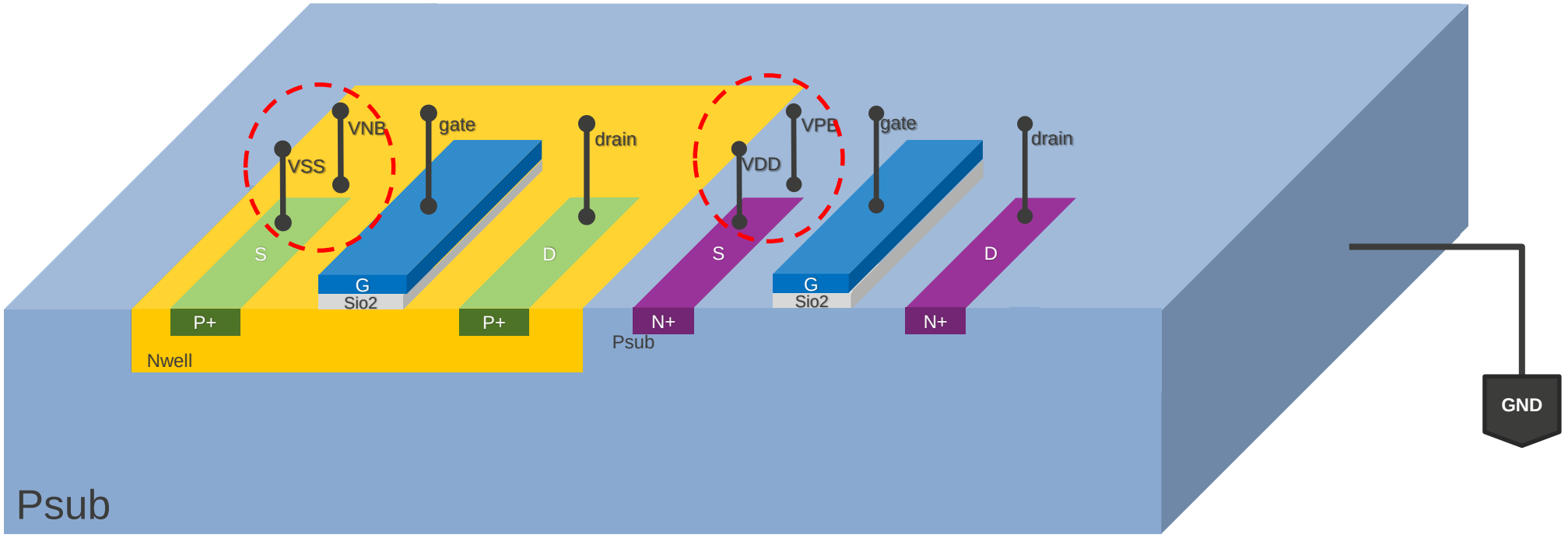




Normal Library



Bias Library
VNB - VPB



Enabling the UPF Well Bias Flow

By default, the UPF-based n-well and p-well bias feature is disabled.
To enable it, set the enable_bias design attribute to true at the top level of the design, preferably using a command in the UPF file:
set_design_attributes -elements {.} -attribute enable_bias true

For the IC Compiler II tool, you must also do the following to enable UPF bias support:
icc2_shell> **set_app_options -name mv.upf.upf_bias_support -value true**

This command makes the design a *bias design* and effectively designates all cell instances in the design as bias blocks.
You can selectively disable the well bias feature for lower-level blocks as follows:

set_design_attributes -elements {blkA blkB} -attribute enable_bias false

To enable this feature for a block, the feature must also be enabled for all parent blocks up to the top level.
In the UPF-based well bias feature, a *bias library cell* is a logic library cell that has one or more bias pins defined as PG pins. **A *nonbias library cell* is a logic library cell that does not define any bias pins. Bias and nonbias cells cannot be mixed within a given power domain. A hierarchical cell containing bias cells is called a *bias block*.**
A nonbias block inside a bias design cannot use a bias supply set from a higher level of the design. It is restricted to using its own domain-dependent supply set, just like a domain created with the create_power_domain -supply {extra_supplies ""} command.

BIAS DESIGN RULES

Each bias supply must be more always-on or equally always-on compared to the corresponding primary supply of the domain. Well bias must be achieved by changing the supply voltages connected to the well bias pins, not by changing the primary power or ground rail voltages.

Within a given power domain, any two logic elements whose bias wells physically abut must use the same bias supplies. This rule ensures electrical continuity. When you specify a supply set for an isolation or retention strategy, ensure that the bias functions of the supply set match those of the domain where the cell is placed.