04 *Laboratory: Operational Amplifiers*

Student	**Zev Pogrebin**
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Course	EE 0022
Professor	Sameer Sonkusale
T.A.	Wenxin Zeng

Contents

Purpose

The purpose of this laboratory is to design a discrete MOS operational amplifier to meet certain specifications. Furthermore, this lab seeks to understand a number of testing methods for finding specifications of such devices.

Design and Simulation

Goals

table 1 **Proposed Specifications**

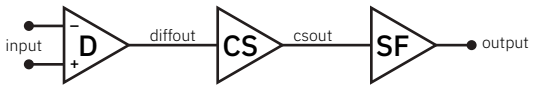
Attribute	Values
Technology	MOSFET
Class	A
Stages	3
Voltage Rails	±5V
Open Loop Voltage Gain	>80dB
Bandwidth (Unity)	>1MHz
Effective Frequency Response	>100kHz
Output Resistance @1kHz	<500Ω
THD	<0.75%

A number of other goals were also set. The amplifier should use a minimum number of capacitors and attempt to minimize frivolous usage of other passives, and be able to operate with DC signals. These goals were developed in conjunction with professor Sankusale and Sam Cohen, who is building a similar circuit using bipolar junction transistors. at Tufts University.

Design Process

The first element of the design process was the selection of the circuit topology. BS170/250 MOSFETs were chosen for their accessibility and familiarity. The stages were as follows:

figure 1



In order to simplify biasing and stability, source degeneration in the common source stage was selected. Through experimentation, it was found that this stage wouldn't provide much gain. Luckily, the differential gain stage would provide a significant amount of voltage gain if an active load was selected.

Overall, there were significant challenges with biasing this design. First, the transistors had very large threshold voltages, so getting rail-to-rail voltage swing was nearly impossible with the selected topology. Next, the common source amplifier and source follower needed to both have their DC bias point centered in their swings while the source follower's output stage had to biased at 0V DC. This set of constraints proved especially pernicious. Iterative design and simulation were used to determine this biasing. A sequence of directives were written in LTSpice to step through a range of possible bias conditions and then automatically determine the best ones. The results were unremarkable but acceptable maximum voltage swings.

Once the op-amp was simulated, high frequency oscillation was occurring in the output. The solution was to include a 5nF capacitor to ground. Such a

capacitor removed the high frequency ringing. To find the appropriate capacitor value, iterative design was used to find the lowest capacitor value that would suppress oscillations. Using the "reverse miller effect," a far smaller capacitor could have been used (one that wasn't tied to any ground node, however this caused serious instabilities in simulation and the idea was abandoned. In any case, this is a discrete op-amp and 4.7nF capacitors are small enough avoid causing either cost or footprint problems.

There are a number of shortcomings to this design. Future iterations of this design could use BJT or JFET designs instead of, or in concert with MOSFETs. This would improve the voltage swing, circuit linearity, stability, and bandwidth. Other classes of output stage could also be selected for improved current performance.

Circuit Design

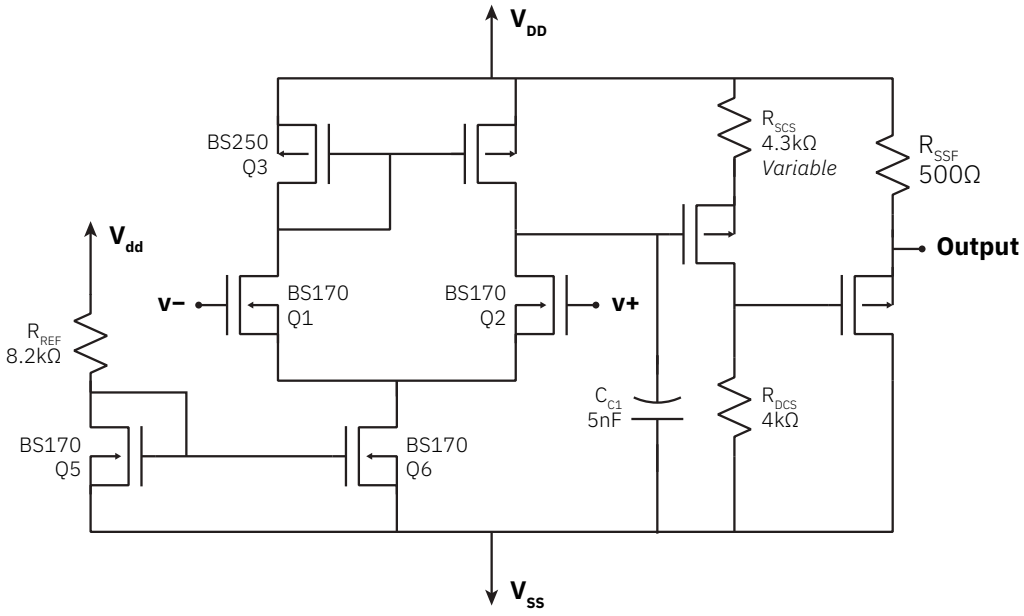


figure 2: Master Schematic

Simulation Results

METHODOLOGY

The circuit was simulated using the LTSpice tool. First, an operating point simulation was realized to determine the DC properties of the circuit. Then, in open loop conditions, transient analysis was conducted. In the transient analysis, the load was varied and the output was measured, allowing output impedance to be computed. increasing the input to a large value allowed measurement of voltage swing. AC analysis allowed easy computation of the unity gain bandwidth frequency.

Other tests were executed by placing the circuit in various op-amp configurations. This allowed the measurement of THD (using Fourier analysis), CMRR, and slew rate.

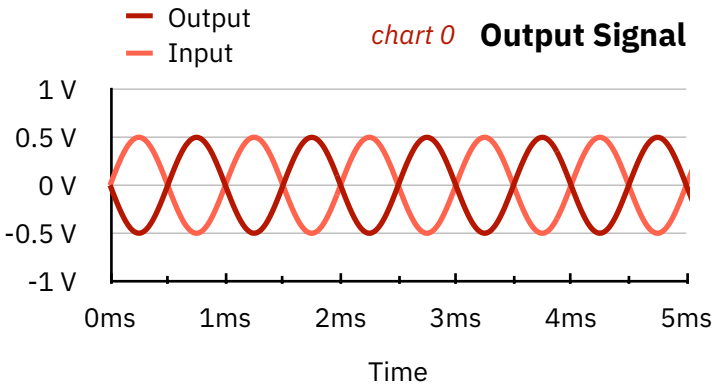


chart 0 **Output Signal**

chart 1 **Frequency Response**

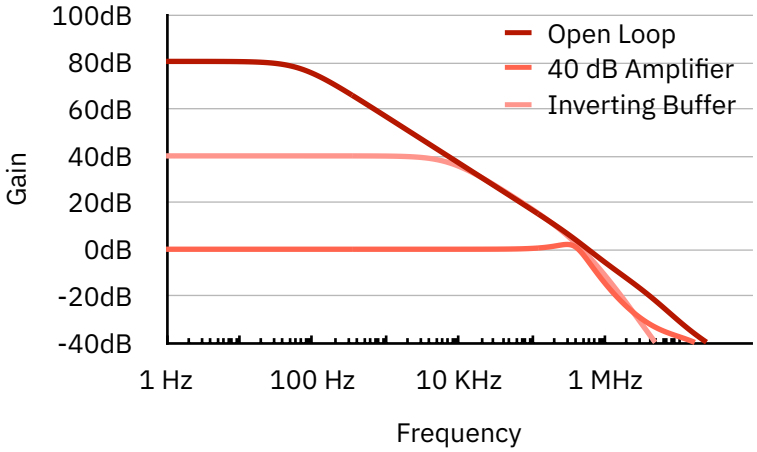


chart 2 **Pulse Slew Profile**

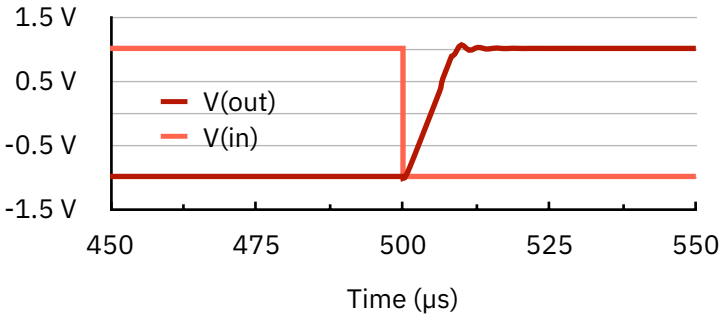
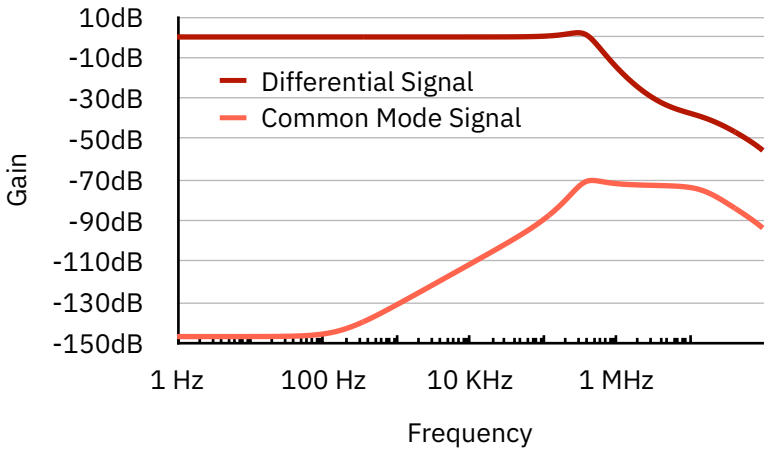


chart 3 **Differential Performance**



DC BIASING ANALYSIS

The first test was to determine the DC biasing. The results were as follows:

table 2 **DC Bias Specifications**

Attribute	Value
$V_{diffout}$	0.42 V
V_{csout}	-3.01 V
V_{out}	-0.2 mV
I_{diff}	0.47 mA
I_{cs}	0.47 mA
I_{sf}	10 mA

There are a few troubling factors: first, the maximum absolute voltage swing must be <2V, since the common source output stage is centered on -3V and the minimum voltage that can be provided at any stage is -5V. Second, the source follower current is very large. This is to minimize the output impedance, but makes this circuit unsuitable for low-power applications. Using a push-pull or class D output stage would be the correct solution for such applications.

OPEN LOOP CHARACTERISTICS

Next, the open loop gain was determined. This was possible in simulation by providing a very small differential input so that the output would not clip. The overall gain was determined to be **80.2dB**. The simulated output impedance was **223Ω**. The open loop frequency response and unity gain bandwidth were found next using AC analysis. This frequency response is shown in *chart 1*. The unity gain bandwidth frequency is **490kHz**.

APPLICATION CHARACTERISTICS

Finally, the amplifier was put into an application circuit. The selected circuit was an inverting amplifier with an 0.5V 1KHz input amplitude. The following parameters were measured: Frequency response at unity gain, total harmonic distortion, and slew rate. The THD was low, only **0.05%**, and the frequency response at unity gain confirmed the **0.49 MHz** UGBW result. The slew rate was simulated as a very sluggish **0.23mV/µs** and its profile can be seen in *chart 2*.

COMMON-MODE REJECTION

The common-mode rejection of this circuit is quite good at low frequencies, however, at high frequencies, the common-mode rejection falls. At 1kHz, the CMRR is -**101dB**. A frequency plot of common mode rejection can be seen in *chart 3*.

SHORTCOMINGS

There were a number of shortcomings with both the operational amplifier design and the measurement techniques and available tools. First, the open loop frequency response of this amplifier is very poor. This is the only parameter that is out of spec. The reason for this is likely the transistors themselves. BS170 and 250 variants are not designed for this application. They likely have a very large process size, which in turn results in larger capacitances between terminals. This is evident in the variation and number of visible poles in the frequency chart. Poor high frequency performance also manifested in a very abysmal slew rate. In the future, using different transistors would likely improve several aspects of the devices' performance.

There are many measurements that could not be completed with the instrumentation and skills at hand. No temperature dependencies could be measured on the actual circuit, and neither could the input impedance, so these measurements were omitted from simulation. In future iterations of this op-amp, learning how to take these measurements is a priority.

SPECIFICATIONS

table 3 **Spice Results**

Attribute	Goal	Value
Technology	*MOSFET*	
Class	*A*	
Stages	*3*	
Voltage Rails	*±5V*	
Open Loop Gain	*>80dB*	80.2
Bandwidth (Unity)	*>1MHz*	4.9E+05
Unity Response	*>100kHz*	4.9E+05
Output Resistance	*<500Ω*	223
THD	*<0.75%*	0.05%
Slew Rate	*N/A V/µs*	0.21
Maximum Swing	*N/A V*	-1.8/3.5
CMRR	*N/A dB*	101
Current Draw	*N/A mA*	12.2

OVERVIEW

This design is functional as an op-amp, and while it has poor high frequency performance, the circuit is capable of producing low distortion output signals.

chart 4 **Inverting Amplifier**

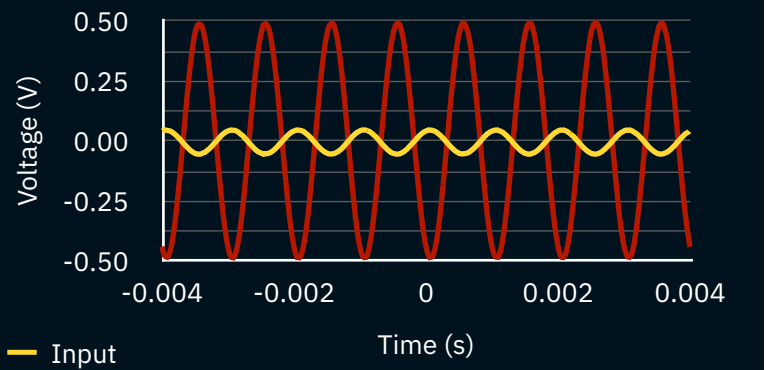


chart 5 **Normalized Slew**

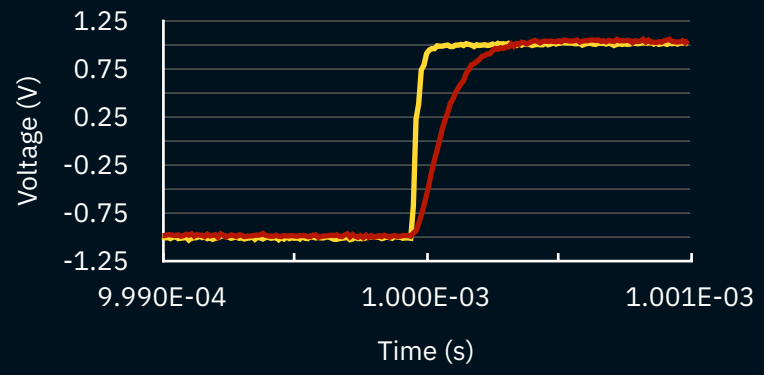


chart 6 **Clipping Profile**

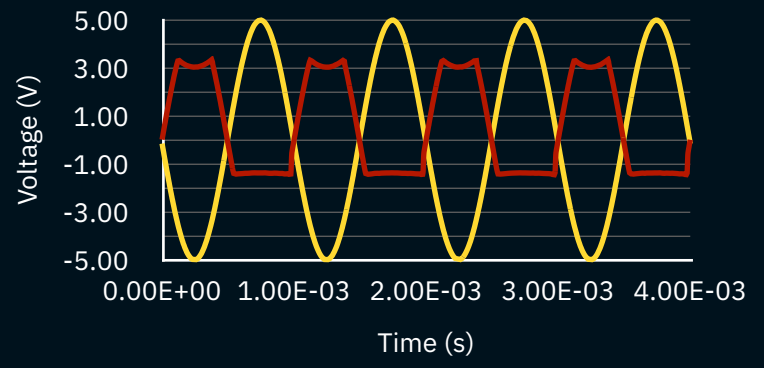
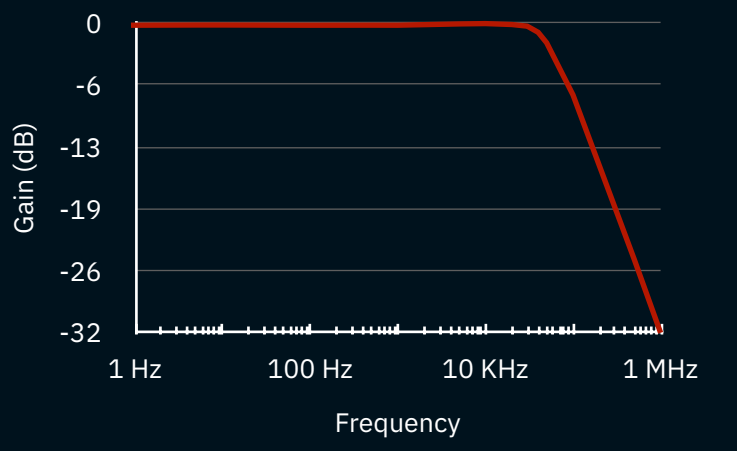


chart 7 **UG Frequency Response**



⚠ Oscilloscope Output Data

In The Laboratory

The purpose of this laboratory was to build an operational amplifier using MOSFET's to specifications that would make it useful in an audio application. While this op-amp certainly has shortcomings, it is functional in its role.

DC Analysis

The first step to ensure that the circuit was built correctly is to check that the circuit is performing properly in a DC condition.

table 4 **Specifications**

Attr	Sim	In Circuit	Error
$V_{diffout}$	0.42 V	1.2 V	186%
V_{csout}	-3.01 V	-3.2 V	6%
V_{out}	-0.2 mV	2.5 mV	Tuned
I_{diff}	0.47 mA	0.42 mA	-11%
I_{cs}	0.47 mA	0.42 mA	-11%
I_{sf}	10 mA	10mA	Tuned

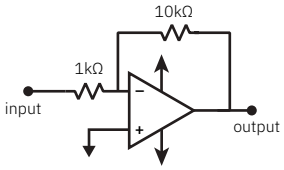
Instabilities were discovered in the output stage of the differential amplifier. After the instabilities were corrected by changing the physical placement of the transistors, the in-circuit output bias was significantly different than that of the simulation, however this didn't significantly affect the remaining biasing.

The circuit was realized using several potentiometers, so it is feasible that the bias points could be tuned for optimal performance.

Application Circuit I

To ensure the circuit was functional, the following application circuit was built, which produced the waveform in *chart 4*

figure 3

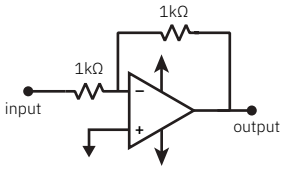


The circuit was driven with a 50mV sine wave, and as expected, the output had an amplitude of **0.485V**, which puts the gain within the resistors' 5% component error. There was, however, an output offset of approximately 0.4V. This output offset could not be trimmed away, and only appears when the circuit was connected. This output offset is not shown in the chart.

Slew Rate

The application circuit in *figure 4* was used to determine the slew rate for the circuit.

figure 4



The slew rate was measured to be about **7.6V/µs**, much better than that of the SPICE simulation. A possible reason for this is SPICE's method of transient simulation, or a flaw with the BS170 model. However, based on the frequency response, this is likely a measurement error. The slew profile can be seen in *chart 5*. Interestingly enough, in this circuit, the large offset found at the input nearly disappeared.

Maximum Swing

The application circuit in *figure 4* was provided a 5V sinusoidal input signal. The maximum voltage swing was determined to be the range from -**1.46V** to **3.3V**. The clipping profile of the operational amplifier is shown *chart 6*.

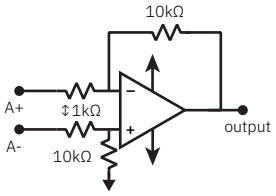
Frequency Response

Using the unity gain inverting amplifier, the bandwidth of the circuit can be deduced. The bandwidth was measured to be **56kHz**, far below the simulated value. Perhaps a smaller capacitor needs to be used. The plot shows one dominant pole, which indicates that C_C is the cause of this low frequency response.

Common Mode Rejection

To compute the common mode rejection, the following application circuit was used:

figure 5

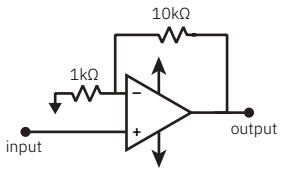


An input with 2V amplitude was applied to both inputs *A+* and *A-*. Then, the output was measured. The common mode rejection ratio was computed to be **53dB**, however this should be taken with low confidence. In order to properly take this measurement, high precision resistors should be used. Since high precision resistors were not accessible, standard 5% resistors were used, which likely caused a differential at the two inputs to the amplifier.

Open Loop Gain

The open loop gain cannot be computed directly because in real life, the high gain of the operational amplifier causes instability in the circuit. As a result, the gain must be computed using an op-amp configuration with gain and measuring the difference between the expected signal level and the actual signal level. Using the circuit in *figure 6*, the open loop gain was computed to be **63dB**, however this method is also highly susceptible to measurement errors.

figure 6



Distortion

The total harmonic distortion was computed using the circuit in *figure 6* at 1kHz. The total harmonic distortion was computed to be **0.12%**, and the THD+N was computed to be approximately **1%**. This high noise level is expected, given that the circuit is built on a breadboard.

Laboratory Design

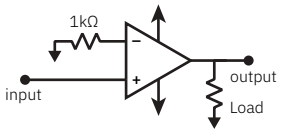
Why this project?

Instead of completing the usual final project for EE22, I talked with my professor about building an operational amplifier. One of the most interesting aspects of this class for me was the section about differential amplifiers and cascaded designs, and this project has offered me a chance to realize them!

Loading Effects

When a 100Ω load is applied to the output of the application circuit, the output is minimally affected, however this doesn't mean that the circuit has a minuscule output impedance. To measure the output impedance, the circuit was allowed to peak in the open loop case. Then, a 100Ω resistor was applied to the output. This caused the output voltage to drop. Using this drop, an output impedance of 110Ω was found.

figure 7



Overall

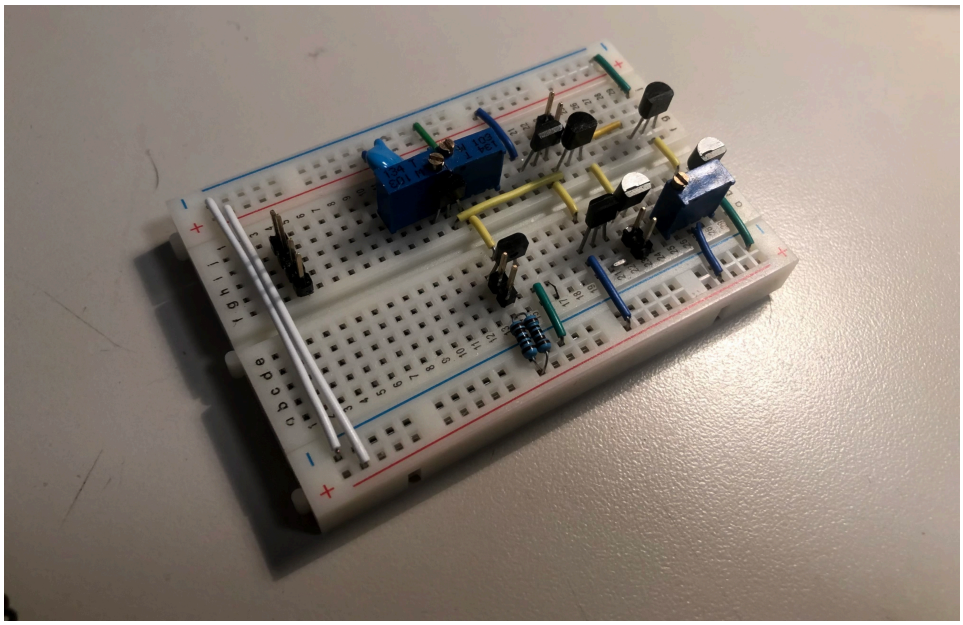
While the op-amp has some serious issues, which should be investigated in further labs, the goals of this lab were accomplished. The design functions as an op-amp while meeting most of the specifications. Furthermore, the lab explored the process and implications of measuring CMRR, output impedance and more.

Procedure

If you have any questions about the procedure of this lab, please contact me. This lab was created independently by myself (with the help of professor Sankusale and discussions with Sam Cohen).

Prototype Boards

FIGURE 8: PROTOTYPE BOARD



Inputs and outputs are denoted by headers. The right hand top and bottom terminals are the negative and positive input respectively; the center jumper is the output. Grounding can be achieved using the pins on the left.

Results

table 4 **Results**

		Spice			Circuit		
Attribute	**Values**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
Technology	MOSFET						
Class	A						
Stages	3						
Voltage Rails	±5V						
Open Loop Voltage Gain	>80dB		80.2			63	
Bandwidth (Unity)	>1MHz		4.9E+05			N/A	
Unity Frequency Response	>100kHz		4.9E+05			5.6E+06	
Output Resistance @1kHz	<500Ω		223			110	
THD @1kHz	<0.75%		0.05%			0.1209%	
Slew Rate	N/A V/µs		0.21			7.6	
Maximum Swing	N/A V	-1.82		3.45	-1.48		3.30
CMRR @1kHz	N/A dB		101			53	
Current Draw	N/A mA		12.2			11.70	

Appendixes

Appendix I: Spice Directives

Many spice directives were deleted or lost due to the unstructured nature of this lab. Here's what still exists in the file.

TRANSIENT SIM DIRECTIVE

```
;MAIN TRANSIENT SIMULATION
.tran 100ms 10ms
.four {freq} V(out)
;meas output AVG V(out)
;step param Rload 1 1k 10
.meas gain max V(out)/(2*V(il))
```

PARAM DECLARATION (FRAGMENTED)

```
;SETTINGS
.params dd=5 ss=5
.params cm=0
.param diff 0.001
.params freq=1k
.params Rdd=15k
.params Rdcs=6k
.params Rs2=4.3k
.params ref=8200
.params bias=-2
.params Rload=1E6
.param rsout 500
.param cc1 4.7nF
```

SOME STEPPING CODE (FRAGMENTED)

```
;STEPS
;step param diff list 0 0.1
;step param Rs2= 3k 4k 100
;step param ref 1k 10k 1k
;step param cc1 0.5n 5n 0.5n
;step param freq list 100 1000 10k
100k 1Meg
;step param Rload list 100 300 1000
10000 1E5
.meas outputlevel max V(out)
;meas outputimpedance {Rload}*(0.5
- outputlevel)/outputlevel
```

Appendix II: Note on Tools

It's apparent that these graphs weren't made in LTSpice and Waveforms, but I didn't just pull them out of thin air. For full details on my graphics creation toolchain, please reach out to me and I'd be happy to give you a demo.

Appendix III: List of Plates

***Figures*:**

***Charts*:**

***Tables*:**

Thank You!