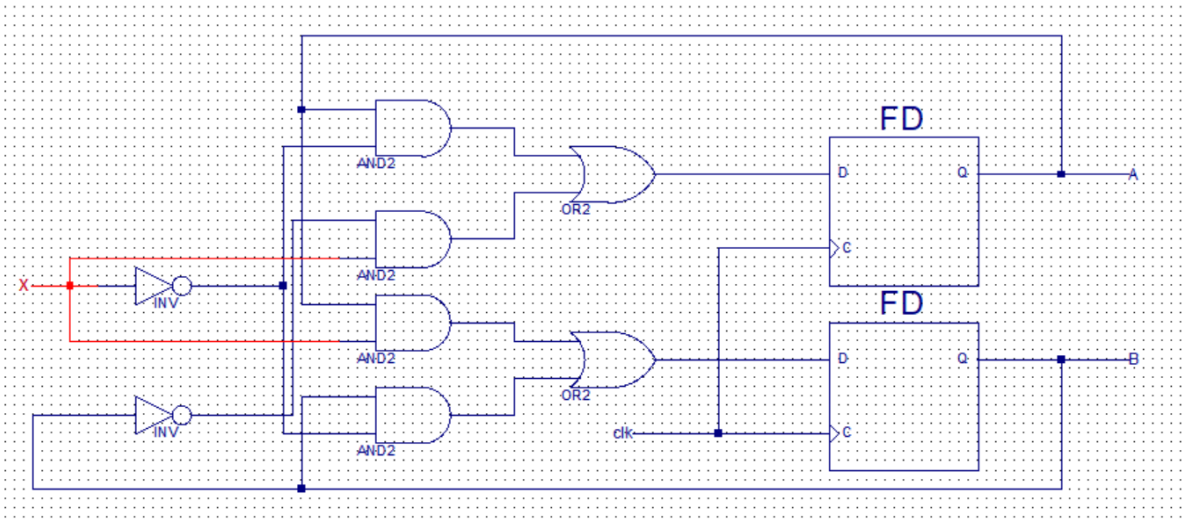
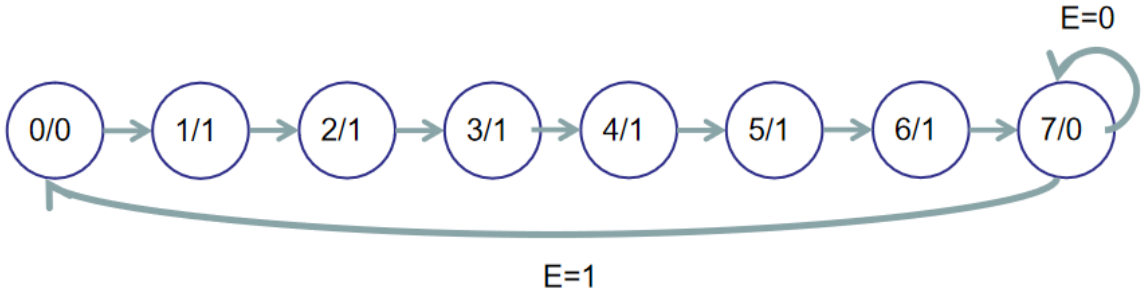
4-13



4-21

(a)

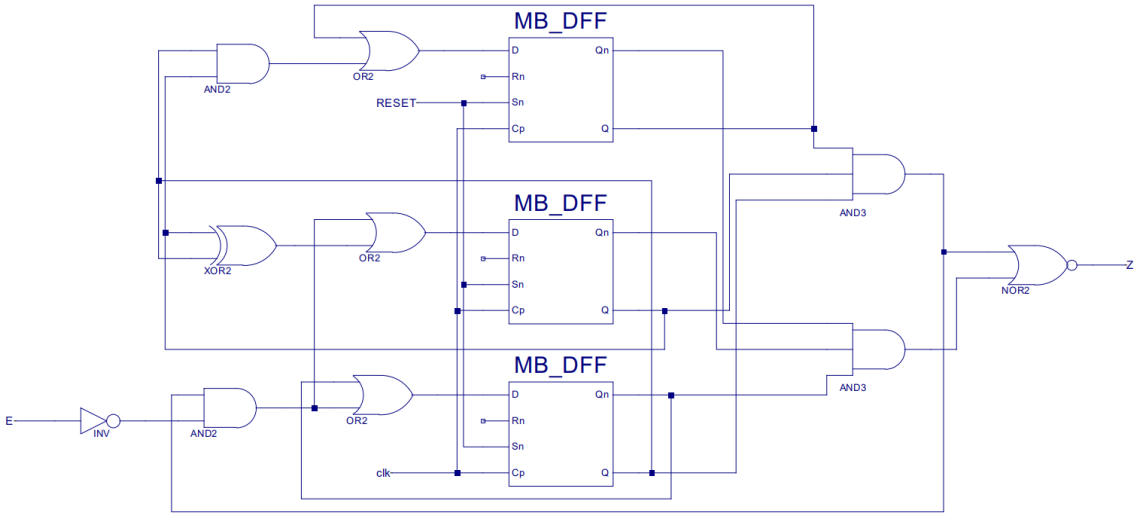
Like 4-20, I assume that output remains **0** if **E=0** when generating the last bit.



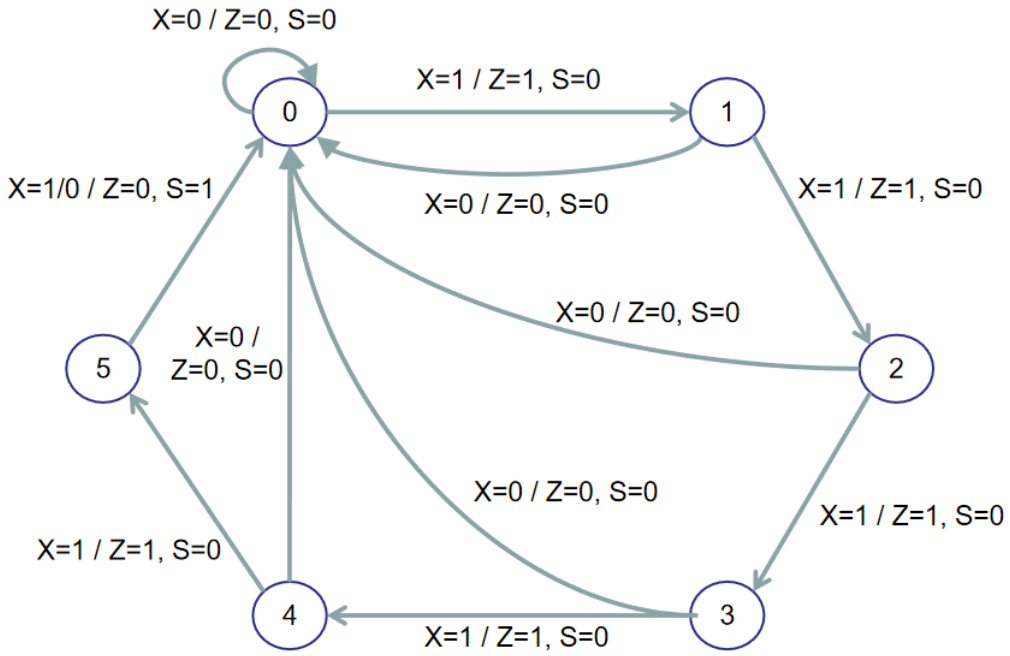
(b)

Present	Next(E=0)	Next(E=1)	Output
000	001	001	0
001	010	010	1
010	011	011	1
011	100	100	1
100	101	101	1
101	110	110	1
110	111	111	1
111	111	000	0

(c)


MB_DFF
MB_DFF
MB_DFF
D
Qn
Rn
Sn
Cp
Q
AND2
OR2
RESET
XOR2
AND3
NOR2
Z
E
INV
clk

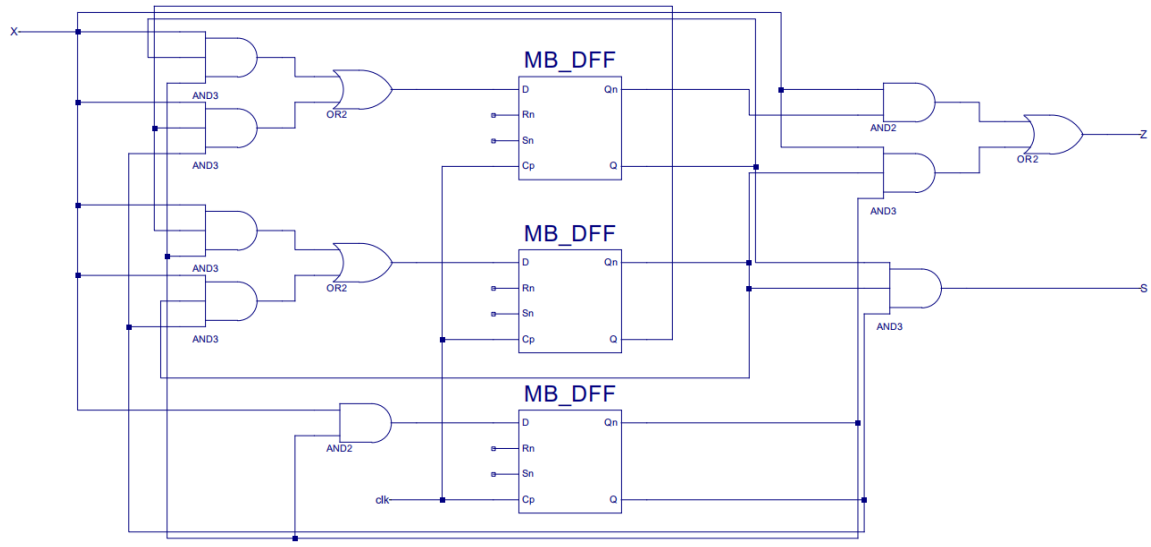
4-22


X=0 / Z=0, S=0
X=1 / Z=1, S=0
X=1/0 / Z=0, S=1
X=0 / Z=0, S=0
X=1 / Z=1, S=0
X=0 / Z=0, S=0
X=0 /
Z=0, S=0
X=0 / Z=0, S=0
X=1 / Z=1, S=0
X=1 / Z=1, S=0
X=1 / Z=1, S=0
0
1
2
3
4
5

(b)

Present	X	Next	Z	S
000	0	000	0	0
000	1	001	1	0
001	0	000	0	0
001	1	010	1	0
010	0	000	0	0
010	1	011	1	0
011	0	000	0	0
011	1	100	1	0
100	0	000	0	0
100	1	101	1	0
101	0	000	0	1
101	1	000	0	1

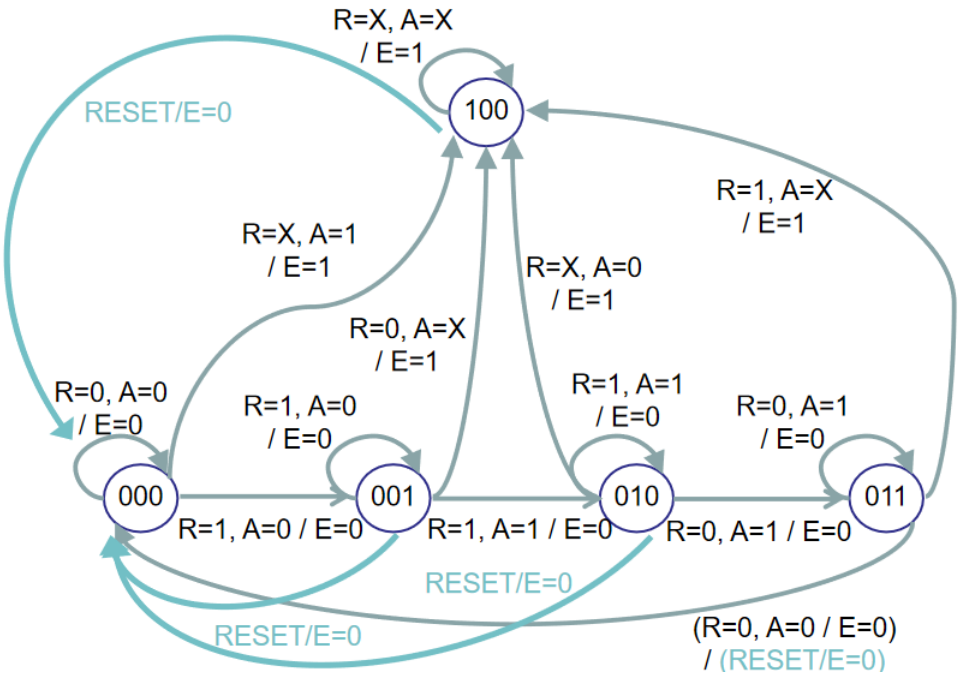
(c)



4-25

(a)

X means 0 or 1.



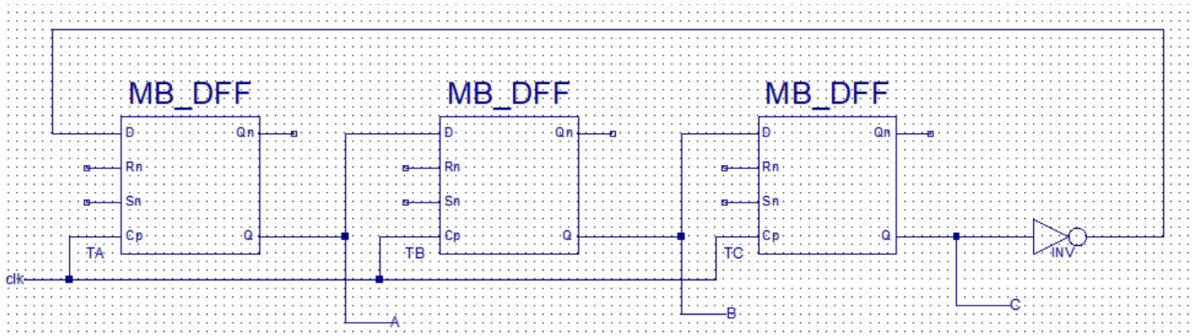
(b)

X means 0 or 1.

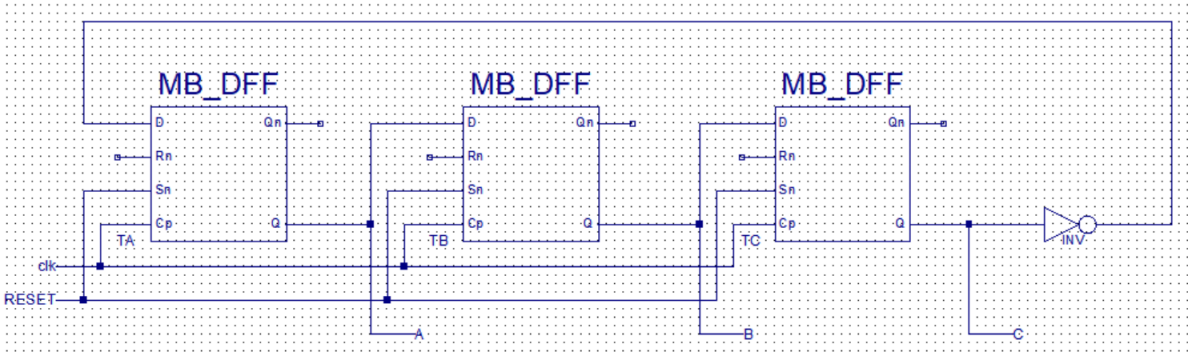
Present	R	A	RESET	Next	E
000	0	0	0	000	0
000	1	0	0	001	0
000	X	1	0	100	1
000	X	X	1	000	0
001	1	0	0	001	0
001	1	1	0	010	0
001	0	X	0	100	1
001	X	X	1	000	0
010	1	1	0	010	0
010	0	1	0	011	0
010	X	0	0	100	1
010	X	X	1	000	0
011	0	1	0	011	0
011	0	0	0	000	0
011	1	X	0	100	1
011	X	X	1	000	0
100	X	X	0	100	1
100	X	X	1	000	0

4-29

(a)



(b)



(c)

I would apply the first technique, the circuit is simple, independent and suitable for a toy. If an error happens and the circuit begins to loop between 010 and 101, the child just needs to reset the circuit. The error brings no harm.

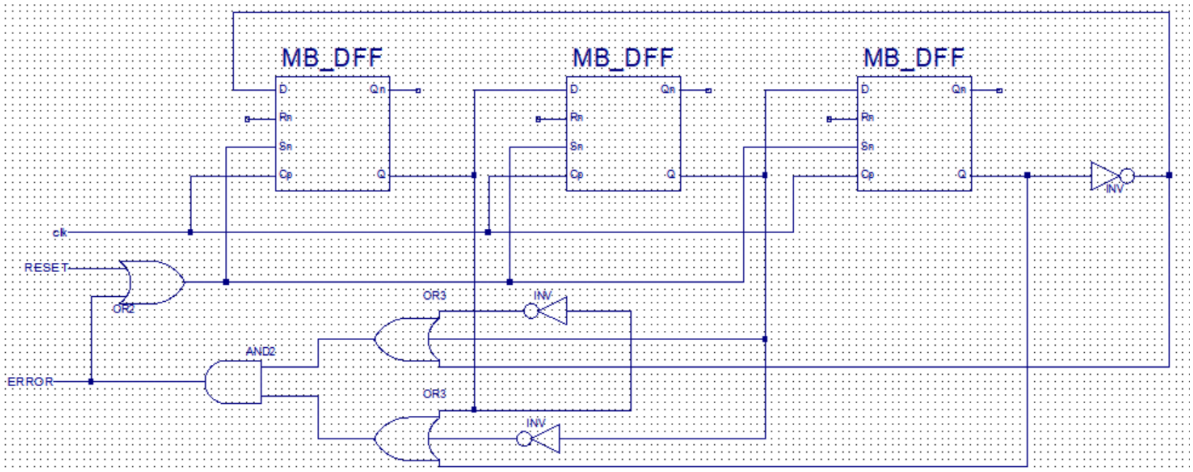
(d)

I think the circuit needs no modification.

(e)

I would apply both the second and the third technique. Since an error happening on the engine of an airliner could kill hundreds of passengers. A signal for error is needed to tell the engineer to check the circuit and the circuit should be able to reset itself when an error happens.

(f)



4-58

(a)

A timing violation at **28ns**.

(b)

Two timing violations: one at **16ns** and one at **24ns**.

4-59

(a)

t_d = 0.04ns + 0.04ns =0.08ns

(b)

t_d = 0.04ns + 0.01ns + 0.02ns = 0.07ns

(c)

t_d = 0.08ns + 0.04ns + 0.04ns = 0.16ns

(d)

t_d = 0.08ns + 0.04ns + 0.01ns +0.02ns = 0.15ns

(e)

$f = \frac{1}{0.15ns} = 6.67 \times 10^3 MHz$
