

## P607 25

To save time, I will only show one process and others are similar.

$$\begin{aligned} \text{a) } W1 \text{ is } \begin{bmatrix} 0 & 1 & 0 & 0 \\ 1 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 \end{bmatrix}, W2 \text{ is } \begin{bmatrix} 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix}, W3 \text{ is } \\ \begin{bmatrix} 0 & 1 & 0 & 1 \\ 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 1 & 0 \end{bmatrix} \text{ and } W4 \text{ is } \begin{bmatrix} 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \\ 1 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \end{bmatrix}. \end{aligned}$$

$$\text{The matrix of the transitive closure is: } \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 \end{bmatrix}.$$

b) The matrix of the transitive closure is:

$$\begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 1 & 1 \\ 1 & 0 & 1 & 1 \\ 1 & 0 & 1 & 1 \end{bmatrix}.$$

c) The matrix of the transitive closure is:

$$\begin{bmatrix} 0 & 1 & 1 & 1 \\ 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 \end{bmatrix}.$$

d) The matrix of the transitive closure is:

$$\begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 \end{bmatrix}.$$

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a) The matrix of the transitive closure is:

$$\begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 \end{bmatrix}.$$

b) The matrix of the transitive closure is:

$$\begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 1 & 1 \\ 1 & 0 & 1 & 1 \\ 1 & 0 & 1 & 1 \end{bmatrix}.$$

c) The matrix of the transitive closure is:

$$\begin{bmatrix} 0 & 1 & 1 & 1 \\ 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 \end{bmatrix}.$$

d) The matrix of the transitive closure is:

$$\begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 \\ 1 & 1 & 1 & 1 \end{bmatrix}.$$

P615 13

$xRx$  is obviously true, so  $R$  is reflexive.

Assume that  $xRy$  and  $yRz$  are true, which means  $x$  and  $y$ ,  $y$  and  $z$  are bit strings that agree in their first and third

bits. Then  $x$  and  $z$  are bit strings that agree in their first and third bits, which means  $xRz$  is true.  $R$  is transitive.

If  $x$  and  $y$  are bit strings that agree in their first and third bits,  $xRy$  and  $yRx$  are both true obviously.  $R$  is symmetric.

So we can conclude that  $R$  is an equivalence relation.

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- a) The set of all bit strings of length 3.
- b) The set of all bit strings of length 4 that end with 1.
- c) The set of all bit strings of length 5 that end with 11.
- d) The set of all bit strings of length 8 that end with 10101.

P630 9

No, because the relation with the directed graph is not transitive.

P630 13

- a)  $(\{0, 1, 2\}, \geq)$
- b)  $(\mathbb{Z}, \leq)$
- c)  $(P(\mathbb{Z}), \subseteq)$
- d)  $(\mathbb{Z}^+, \text{"is a multiple of"})$

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- a)  $\{1, 2\}, \{1, 3, 4\}, \{2, 3, 4\}$
- b)  $\{1\}, \{2\}, \{4\}$
- c) No.
- d) No.
- e)  $\{2, 4\}, \{2, 3, 4\}$
- f)  $\{2, 4\}$
- g)  $\{4\}, \{3, 4\}$
- h)  $\{3, 4\}$

P650 11

If:

Because  $R$  is symmetric,  $uRv$  and  $vRu$  are both true

and then the edges between  $u$  and  $v$  is undirected.

Because  $R$  is irreflexive, there are no loops, or there exists at least a  $u$  such that  $uRu$  is true.

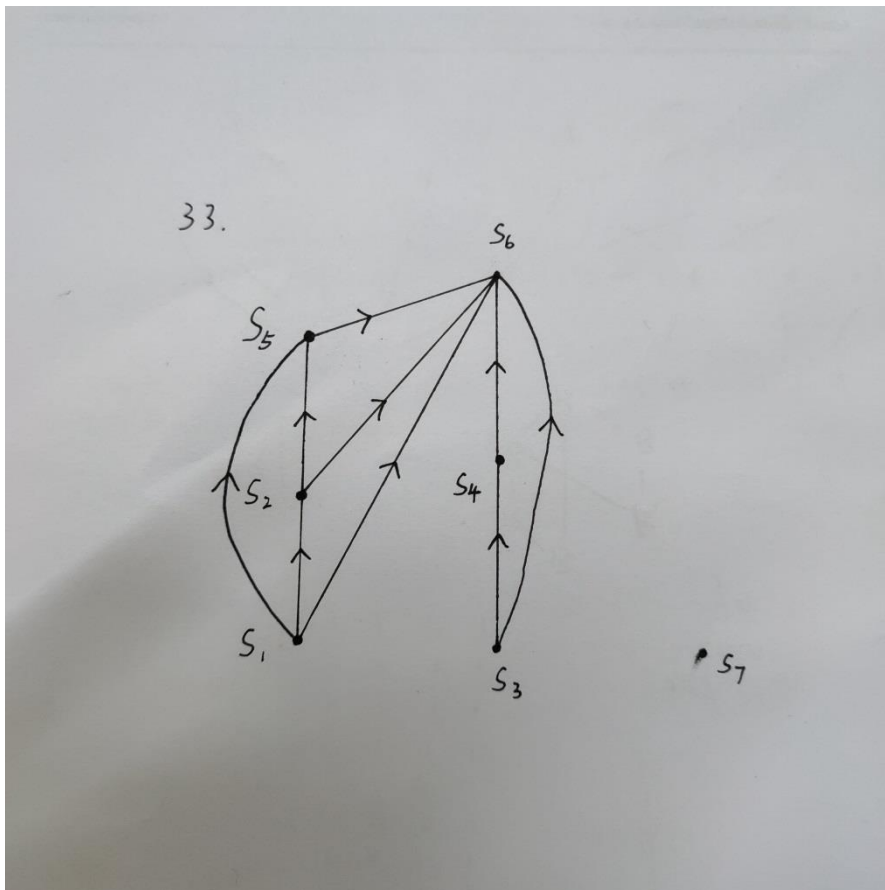
So we can conclude  $G$  is a simple graph.

Only if:

Because the edge is undirected, we can have  $\{u, v\} = \{v, u\}$  and if  $uRv$ , then  $vRu$  must be true. We have  $R$  is symmetric.

Because no loops exist in a simple graph,  $uRu$  never holds. We have  $R$  is irreflexive.

So we can conclude  $R$  is symmetric and irreflexive.



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No, because if we assign  $a$  a color first, then  $b$  and  $d$  are always assigned the same color.

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Assume that  $\{a_1, a_2, \dots, a_n\}$  is a nonincreasing sequence of nonnegative integers with an even sum.

For vertex  $v_i$ , we put  $\left\lfloor \frac{a_i}{2} \right\rfloor$  loops at it, for  $i=1, 2, \dots, n$ .

because the sum is even, we can know the number of vertices that  $\deg(v_i)=a_i-1$  is even. We randomly pair these vertices and put edges to connect the pair.

By far, we have constructed a pseudograph that satisfies the requirement.