

1. A memory and cache subsystem uses byte-addressing, 32-bit address. Each row of the table below indicates a kind of cache, the "Cache feature" column of table describes the total size of cache data (not containing tag and valid bit), cache kind, cache block size. A 32-bit memory address 0x22339AB contains 3 fields: tag, index, byte offset, some of these field's size(bit number of this field) or value should be filled into table blank below. You should use Hex-decimal number to fill into column "Index value(Hex)". Total cache size containing data block, tag and valid bit should also be filled into column "Tatal Size,KB"(KB means unit is KB-1024 byte, not byte), only number (not expression) is allowed to be filled into this colomn.

Cache feature	Index value(Hex)	Index size, bits	TAG size, bits	Tatal Size,KB
64KB cache data, Direct-mapped, 8 bytes/block	0x0735	13	16	81
512KB cache data, Direct-mapped, 64 bytes/block	0x0CE6	13	13	526
512KB cache data, 2-Way set associative 8 bytes/block	0x6735	15	14	632
1024KB cache data, 8-Way set associative 32 bytes/block	0x09CD	12	15	1088

Example value has been given in first question row.

2. A computer with multi-cycle CPU runs at 5 GHz , it has 2 levels of cache: the first level cache C1 ,and the second level cache C2. When a test program TP runs, total I instructions is executed with M memory accesses, here I=1000, M=1250. 1250 memory accesses include fetching instruction from memory, loading memory operand into register, etc. When this TP runs first in perfect cache mode that all instruction and

data are located in C1, all M memory accesses hit in C1, and CPI is 4.2.

Now TP runs in not perfect cache mode, 1250 memory accesses are divided into 3 parts:

Part-A: 1200 accesses hit in C1, they only need to access C1;

Part-B: 40 accesses hit in C2, they need to access C1 and C2;

Part-C: 10 accesses need to access C1, C2 and DRAM;

DRAM access time: 80ns, C2 access time: 5ns, C1 access time: 0.2ns. Please fill numbers (not expressions) into following blank (A)—(E).

(1).Total Clock cycles of 1200 accesses in Part-A is (A) 1200 ;

(2).Total Clock cycles of 40 accesses in Part-B is (B) 1040 , these 40 accesses need more Clock cycles than 40 accesses in perfect cache mode, the increased cycle number is noted as J, value of J is (C) 1000 .

(3).Total Clock cycles of 10 accesses in Part-C is (D) 4260 , these 10 accesses need more Clock cycles than 10 accesses in perfect cache mode, the increased cycle number is noted as K, value of K is (E) 4250 .

(4).Average CPI of TP run in not perfect cache mode is noted as L, L may be written as an arithmetic expression about I,J and K, please fill following blank with such an arithmetic expression:

$$L = \underline{(F) (4.2I+J+K)/I}$$