6-6

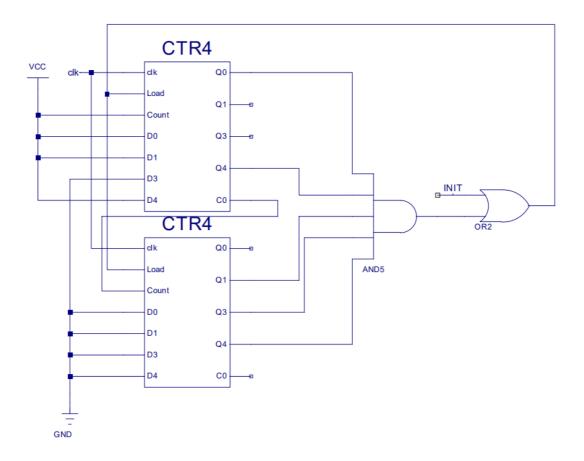
(a)

 $1000 \rightarrow 0100 \rightarrow 0010 \rightarrow 0001 \rightarrow 1000 \rightarrow \dots$

(b)

There are *n* states.

6-13



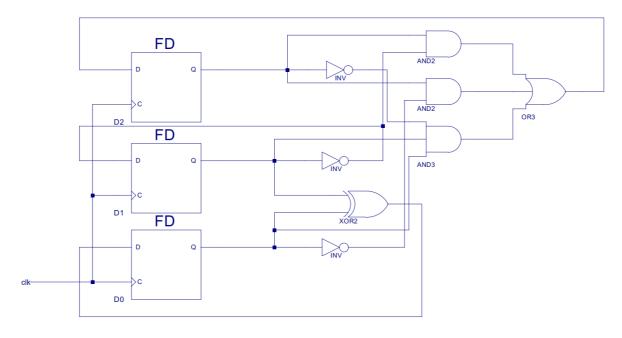
6-16

Present	Next
000	010
001	011
010	001
011	100
100	110
101	111
110	101
111	000

$$D_2 = D_2 \overline{D}_1 + D_2 \overline{D}_0 + \overline{D}_2 D_1 D_0$$

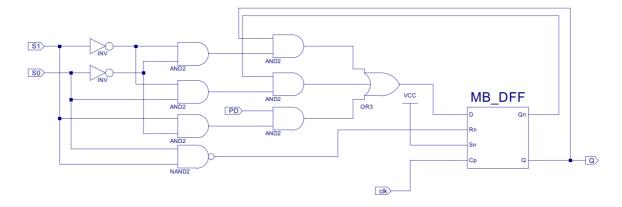
$$D_1 = \overline{D}_1$$

$$D_0 = D_1 \overline{D}_0 + D_0 \overline{D}_1$$

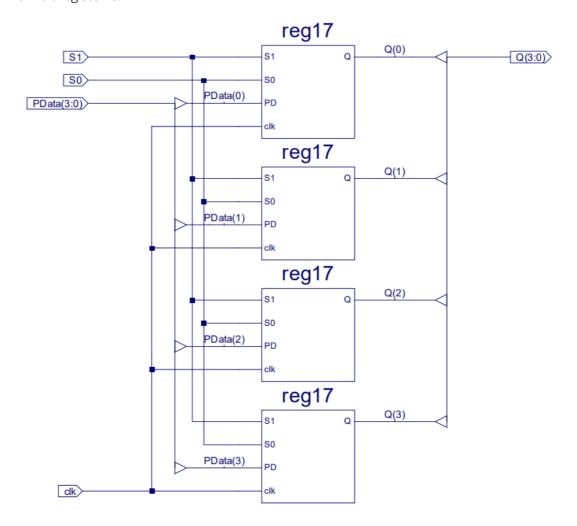


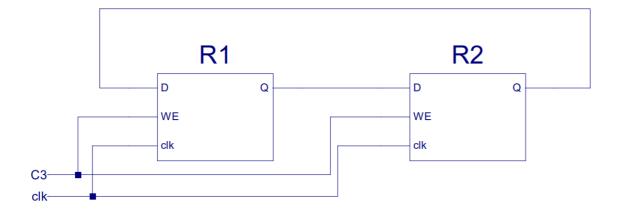
6-17

Such a one-bit register is:



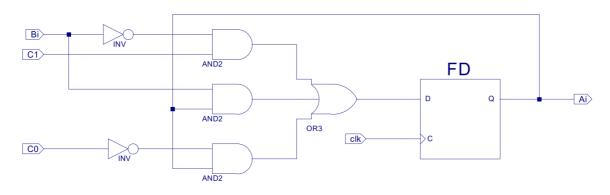
The 4-bit register is:





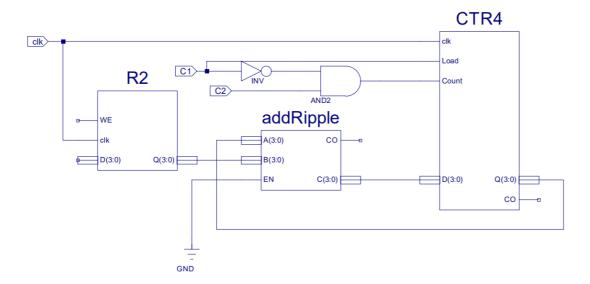
6-23

Instructions C1 and C0 won't be 1 at the same time.

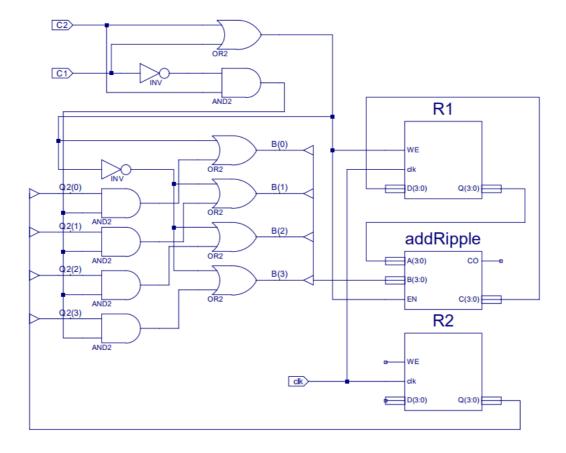


6-27

(a)



(b)



The design in **(a)** is simpler since CTR4 itself can achieve increment. Since the add component in **(a)** can achieve subtraction, the *S* signal must be 0 to implement addition.

6-34