6.3

x3000	0101 000 000 1 00000	; clear R0
x3001	0001 000 000 1 00001	; add 1 to R0
x3002	1010 001 000001011	; load M[x4000] to R1
x3003	1010 010 000001011	; load M[x4001] to R2
x3004	0001 001 001 1 11111	; add -1 to R1
x3005	0000 100 000000010	; if negative, end the loop
x3006	0001 000 000 000 000	; add R0 to itself
x3007	0000 111 111111100	; jump back to the loop
x3008	1001 000 000 111111	; NOT R0
x3009	1001 010 010 111111	; NOT R2
x300A	0101 010 010 000 000	
x300B	1001 010 010 111111	
x300C	1011 010 000000010	; store the result to M[x4001]
x300D	1111 0000 00100101	; halt
x300E	0100 0000 0000 0000	; x4000
x300F	0100 0000 0000 0001	; x4001

7.4

Symbol	Address
TEST	X301F
FINISH	X3027

SAVE3	X3029
SAVE2	X302A

7.7

```
        .ORIG   x3000
        AND     R1, R1, #0      ; clear R1
        AND     R2, R2, #0
        ADD     R2, R2, #1      ; mask
LOOP    AND     R3, R0, R2      ; detect each bit
        BRz     MASK
        ADD     R1, R1, #1      ; increment the result
MASK    ADD     R2, R2, R2      ; shift left
        BRz     DONE            ; end detection
        BRnzp   LOOP
DONE    HALT
        .END
```

7.18

(a) LDR   R3, R1, #0

(b) NOT   R4, R4

(c) ADD   R4, R4, #1