8.6

If KBSR[15] is 0 and the program does not check the Ready bit, the processor will load the same data in KBDR multiple times.

8.9

If KBSR[15] is 1 and the keyboard hardware does not check the Ready bit, the data in KBDR that has not been read may be covered by the new input, which means the input could be lost.

8.12

Let's assume that address xFE00 is reserved for the KBDSR. The input routine is as follow:

```
START   LDI     R0, KBDSR
        BRz     START       ; loop if KBDSR is 0
        AND     R1, R1, #0  ; clear R1
        STI     R1, KBDSR   ; clear KBDSR
        BRnzp   NEXT_TASK
KBDSR   .FILL   xFE00
```

8.14

xFE02 is mapped to the KBDR, so when an LC-3 Load instruction specifies the address xFE02, it's actually loading from the KBDR. The

address control logic will help to implement the instruction.

8.15

a. The keyboard is enabled to interrupt and the character ‘2’ is written to the screen repeatedly.

b. The typed character is written to the screen twice.

c. I could see consecutive ‘2’s followed by the typed character twice or three times (only if the interruption happens right after LD at x3002). The typed character is also followed by consecutive ‘2’s.

8.16

It outputs ‘ABCDEFGHI’.