Class: CSE320 Digital Design and Synthesis

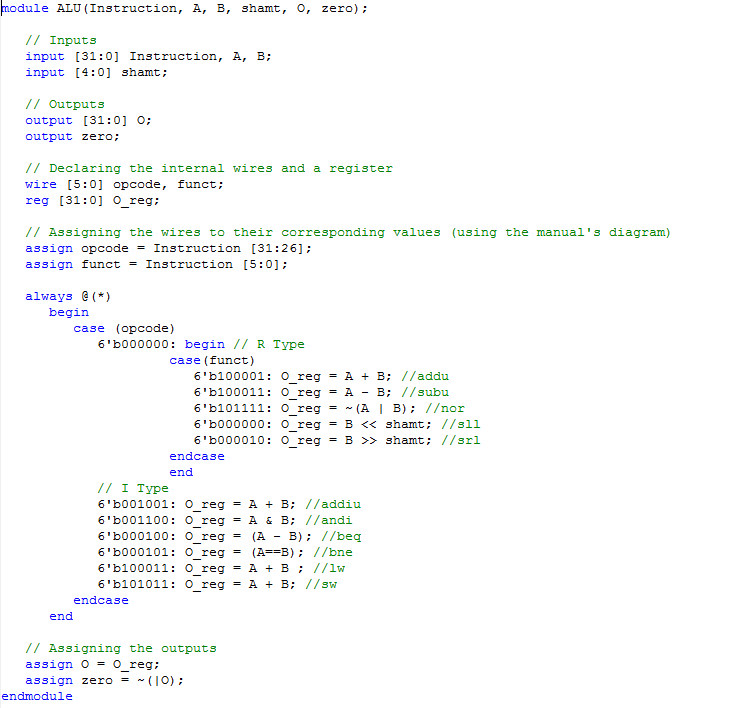
Time: T-TH 4:30PM

Semester: Spring 2014

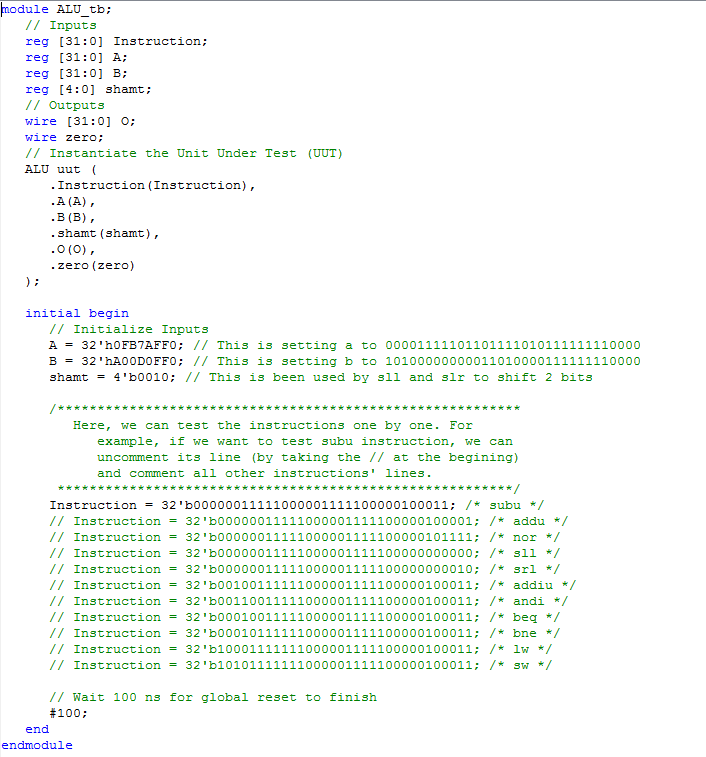
Lab 3 Report

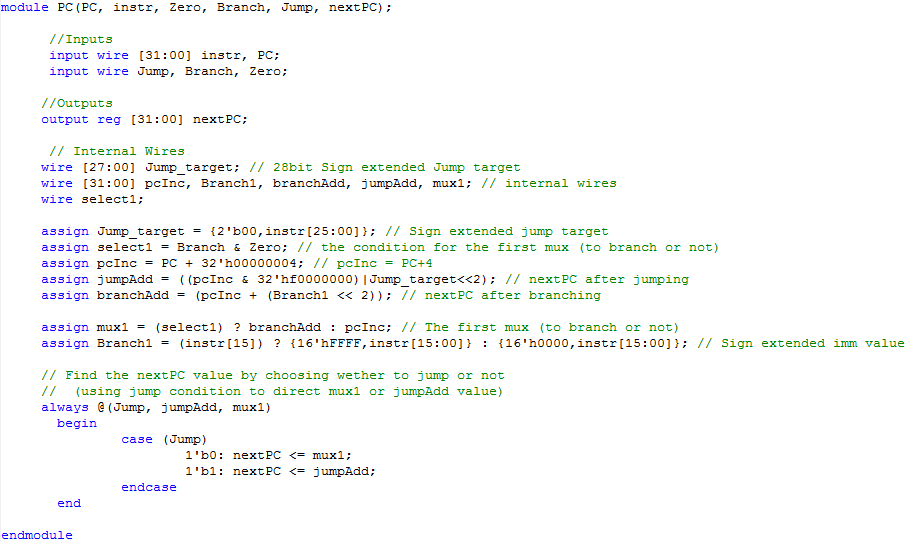
The purpose of this assignment is to design the control logic of the MIPS processor. We incorporate the ALU that was designed in the lab 2. This module contains: PC Selector, Instruction Decoder, and ALU modules, with some extra logic.

**Code: ALU.v code**

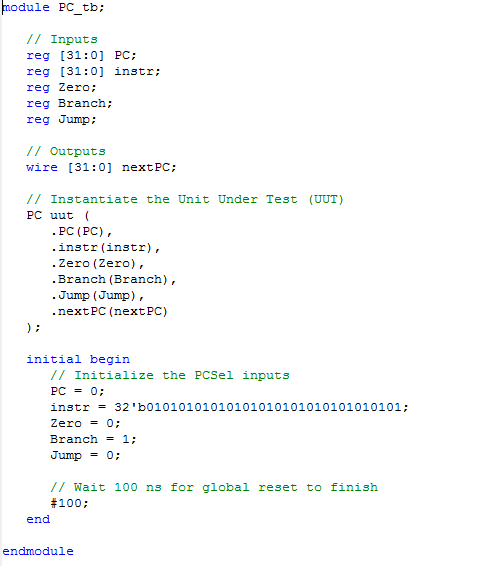
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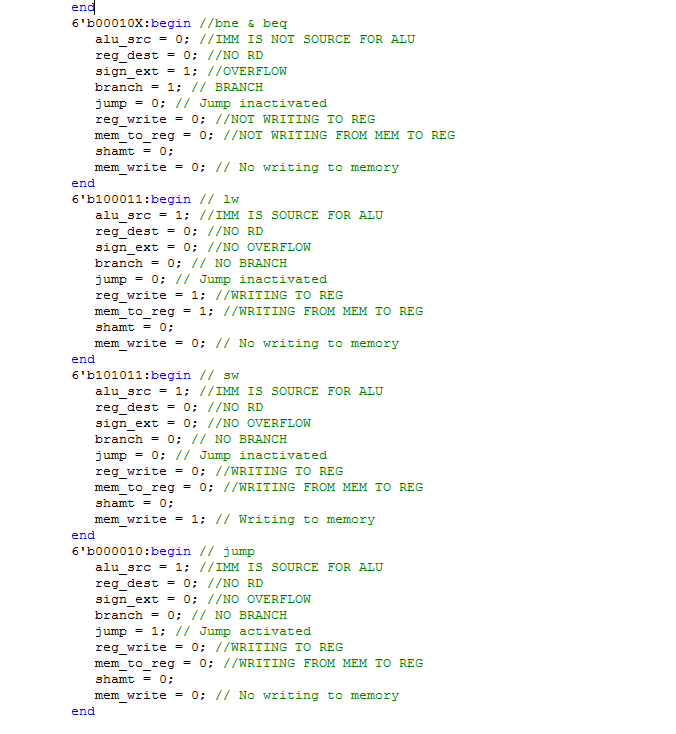
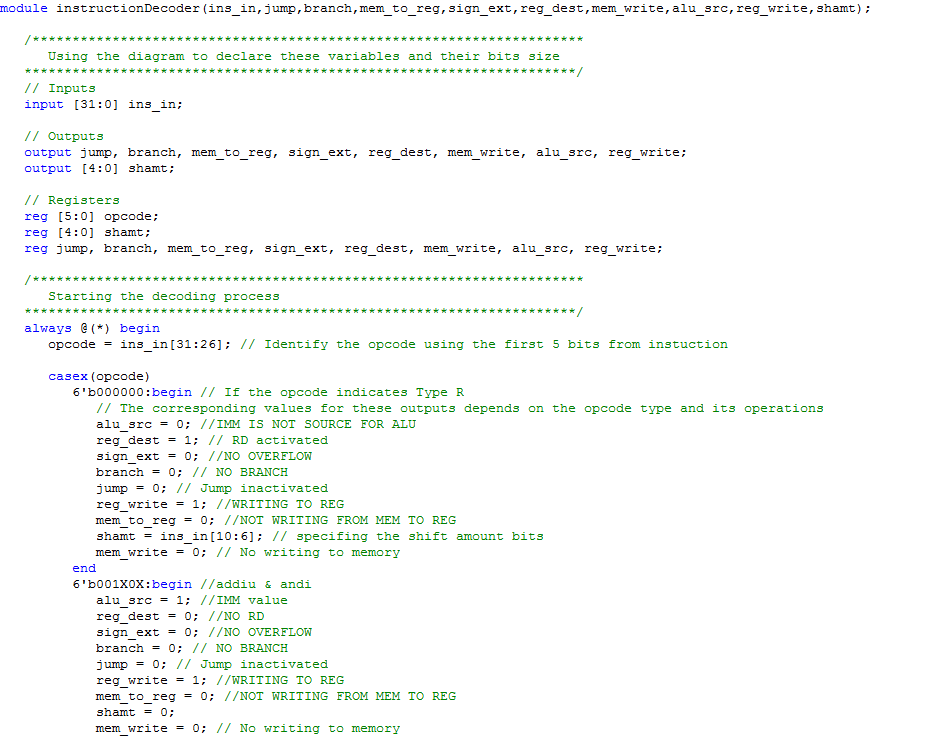
**ALU test bench code**

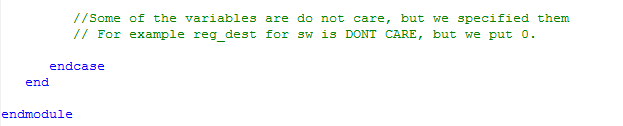


**PC.v code **

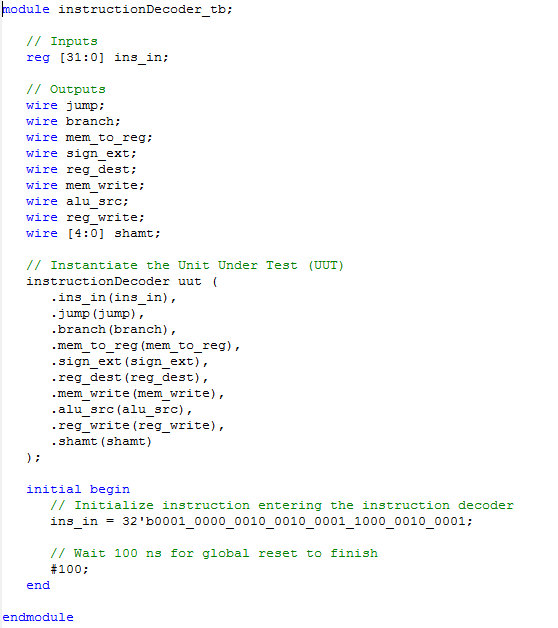
**PC test bench code**

****

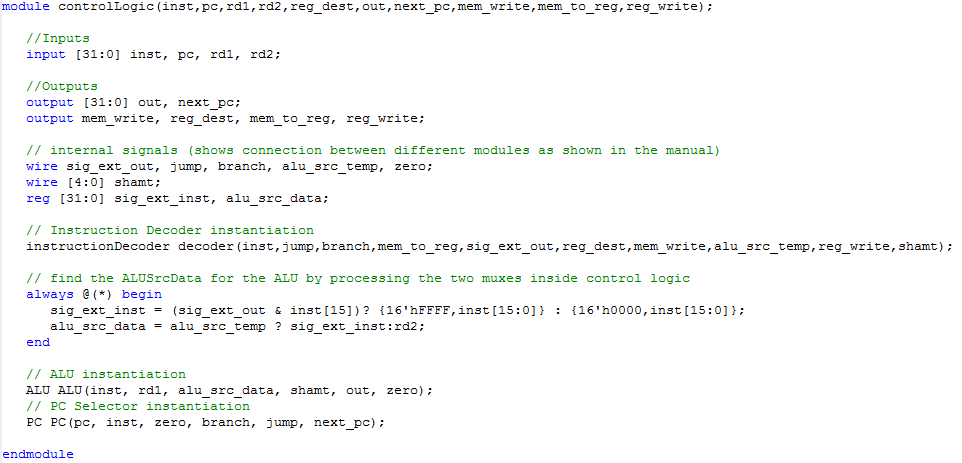
**instructionDecoder.v code **

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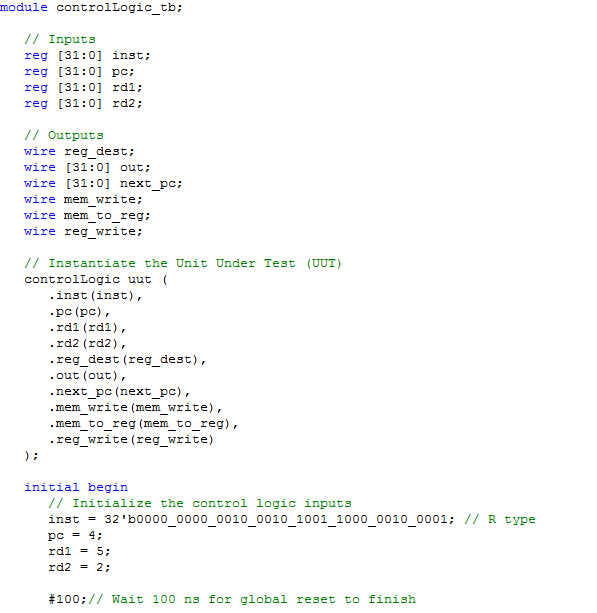
**instructionDecoder test bench code**

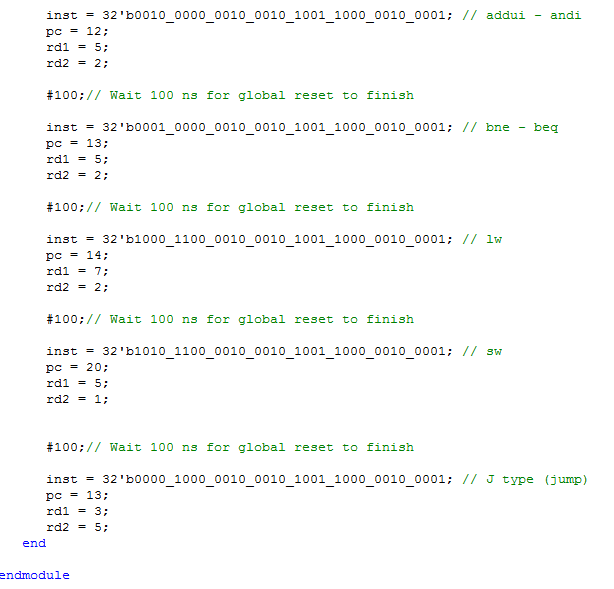
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**controlLogic.v code**

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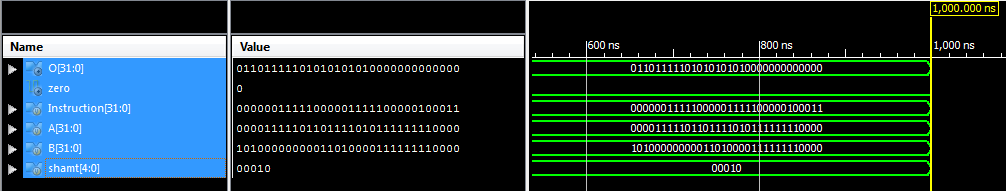
**controlLogic test bench code**

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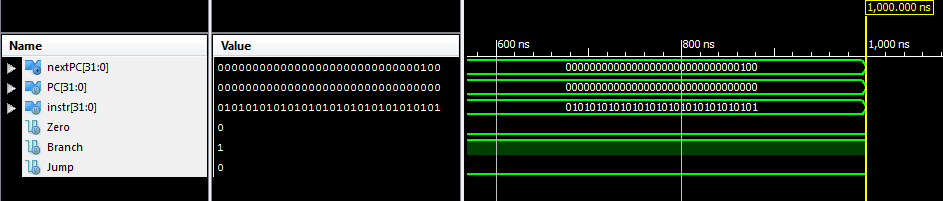
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**Wave forms:**

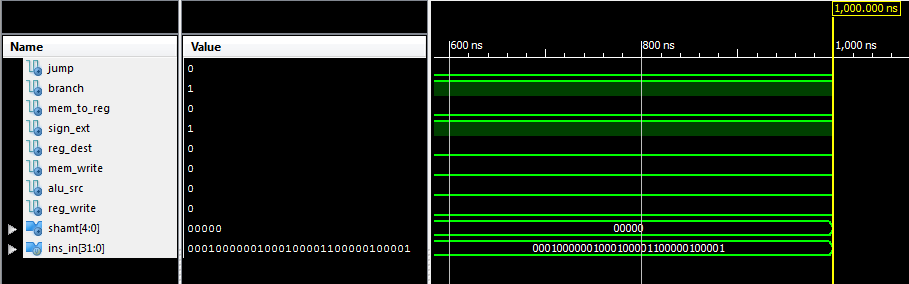
**ALU Module**

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**PC Module**

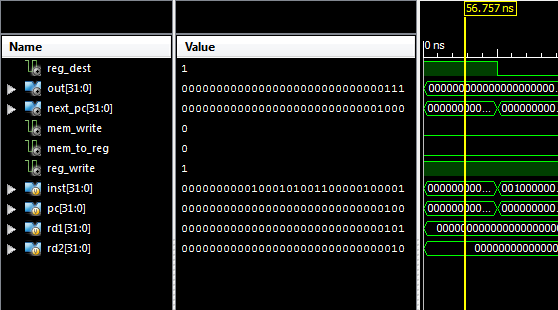
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**instructionDecoder Module**

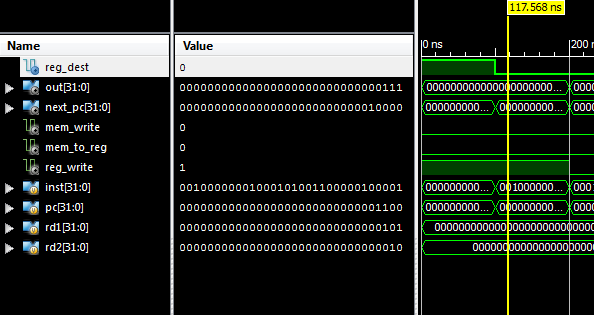
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**ControlLogic Module**

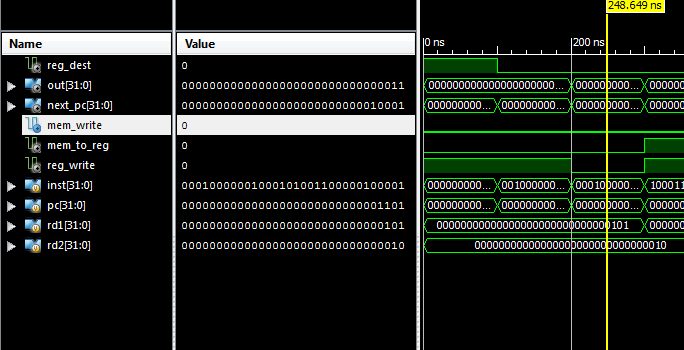
**R type (addu)**

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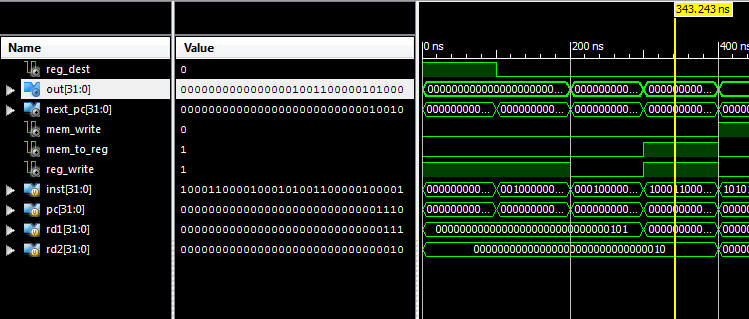
**Addui – andi**

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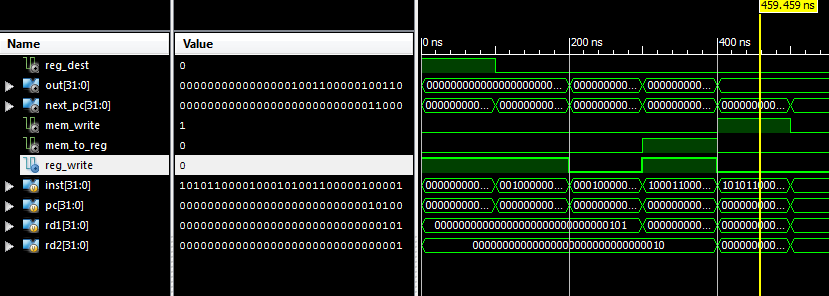
**bne – beq**

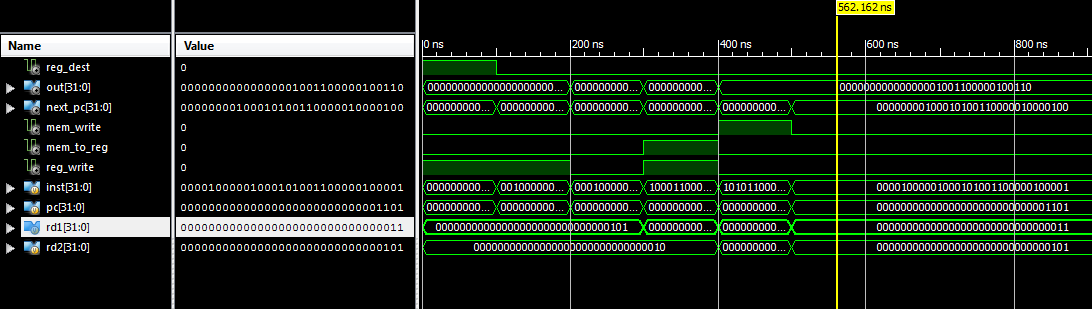
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**Lw**

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**Sw**

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**J type (jump)**

Last Page:

This is entirely our work and we have not received assistance in any form whatsoever.

Signatures:

Zachary Priddy Abdulla Al Braiki

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