Project #2

AUTHORS: ABDULLA ALBRAIKI & ZACAHARY PRIDDY

Question 1:

If DTMR0[PS] is set to 80 (decimal) rather than 79, the clkcnt would not be 1 MHz, the period would not be 1 µs – because it would be divided by (80+1) which is 81 rather than 80.

For DTMR0(PS) = 79_{10} = 0x4F (Actual delay)

$$Timeout\ Period = \frac{1}{\text{clock frequencies}}\ x\ (1\ or\ 16)\ x\ (DTMRn[PS] + 1)\ x\ (DTRRn[REF] + 1)$$

$$Timeout\ Period = \frac{1}{8\ x\ 10^6}\ x\ (1)\ x\ (79 + 1)\ x\ (1699 + 1) = \frac{17}{1000} = 0.017\ seconds$$

For DTMR0(PS) = 80_{10} = 0x50 (n delay – the questioned one)

$$Timeout\ Period = \frac{1}{\text{clock frequencies}}\ x\ (1\ or\ 16)\ x\ (DTMRn[PS] + 1)\ x\ (DTRRn[REF] + 1)$$

$$Timeout\ Period = \frac{1}{8\ x\ 10^6}\ x\ (1)\ x\ (80 + 1)\ x\ (1699 + 1) = \frac{1377}{80000} = 0.0172125\ second$$

$$Error\ Percentage = \frac{n\ Delay - Actual\ Delay}{Actual\ Delay}\ x\ 100\%$$

$$= \frac{0.0172125 - 0.017}{0.017}\ x\ 100\% = 1.2\%$$

Question 2:

(a) The name of the signal on SW4 pin 4 is MCU_RSTIN_b

(b) The _b means that it is an active low signal

(c) SW4 pin 4 is connect to pin 141 - 'RSTIN_b' or just simply "RSTIN"

(d) Primary reset input to the device. Asserting RSTI immediately resets the CPU and peripherals.

Question 3:

(a) The name of the signal from SW1 pin 4 is PB1_SW

(b) It is connected to pin 93 - 'IC0/OC0/PWM1'

(c) Primary: GPT0

Tertiary: PWM1

Quaternary: PTA0

(d) It is connected to GPIO Port TA pin 0

(e) Its connected to pin 0 of Port TA

(f) We would have to write to register MCF_GPIO_PTAPAR or hex 0x4010006E

(g) MCF_GPIO_PTAPAR &= MCF_GPIO_PTAPAR_ICOC0_GPIO;

(h) This register would be: MCF_GPIO_DDRTA

(i) MCF_GPIO_DDRTA &= ~(MCF_GPIO_DDRTA_DDRTA0);

(j) int sw1 = (!MCF_GPIO_SETTA_SETTA0); //sw1 is high when it is not pressed