
Pre-amp

朱启通

des i gn

- **The first stage comp design**



- **Comp design**
- Preamp design
- Autozero eliminate os

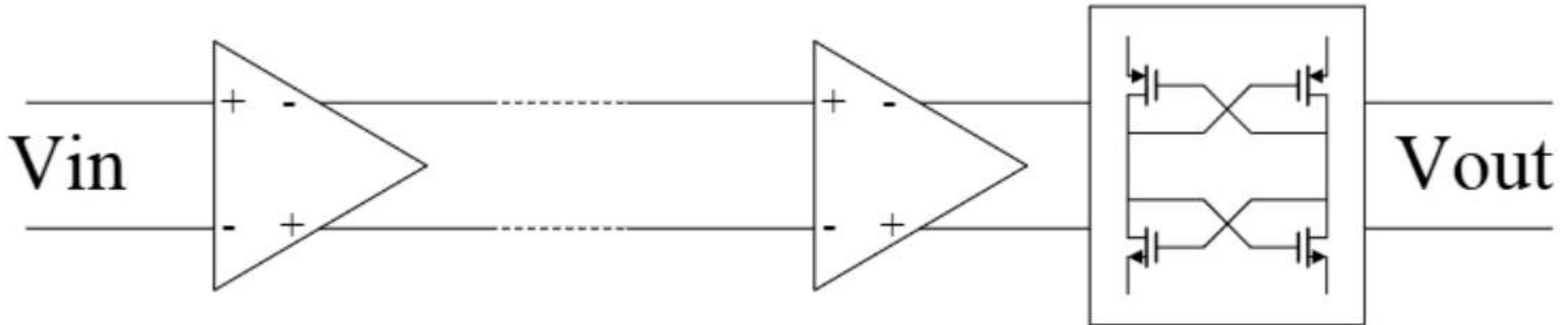
design

- The first stage comp choice, and spec analysis.
- $\text{current} \leq 50\mu\text{A}$, $\text{speed} \geq 800\text{MHz}$, $\text{offset } (3\sigma) \leq 4\text{mV}$, $\text{input reference noise } (3\sigma) \leq 1\text{mV}$, $\text{common mode voltage} = 0.9\text{V}$

Architecture

- architecture — preamp + strongarm latch

Decrease os of strongarm latch
Introduce os of preamp

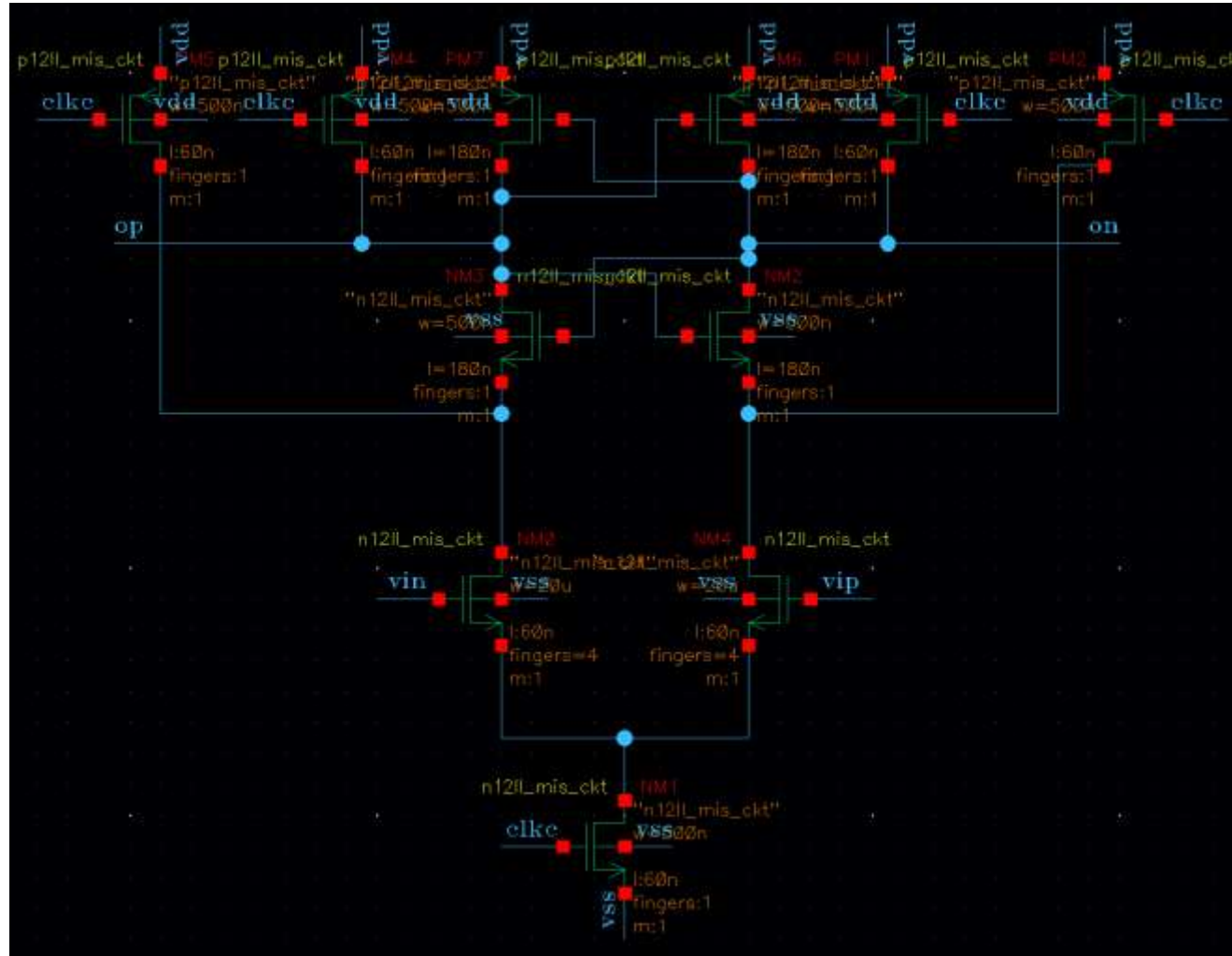


Strongarm latch design

- Strongarm latch os \approx 4.735mv (σ)
- Strongarm latch cycle=2.5ns
- Strongarm latch current=14.5uA

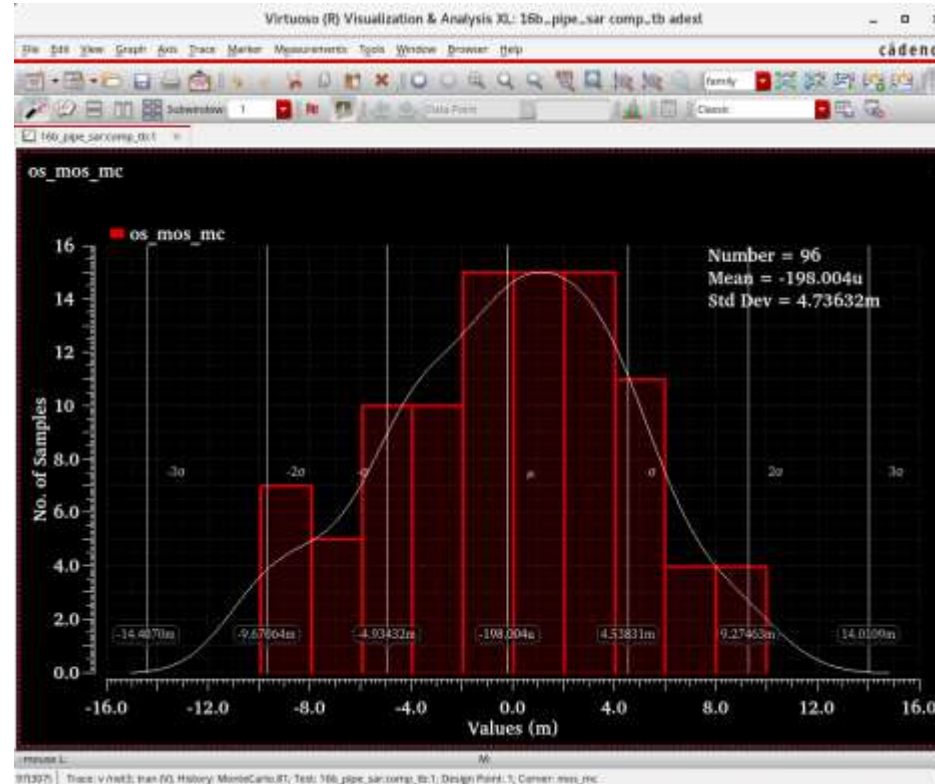
Strongarm latch design

- Circuits implementation



第一级比较器的设计

- Stimulate result



Strongarm latch offset mentor carlo
 $3\sigma=28.2m$

Preamp design

- **Strongarm latch os \approx 4.76mv (σ)**



Preamp gain=5

- **Strongarm latch cycle=2.5ns**



Preamp f-3db>1Ghz

- **Strongarm latch current=14.5uA**



Preamp current<35.5uA

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- **The first stage comp design**



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Preamp design

Preamp gain=5

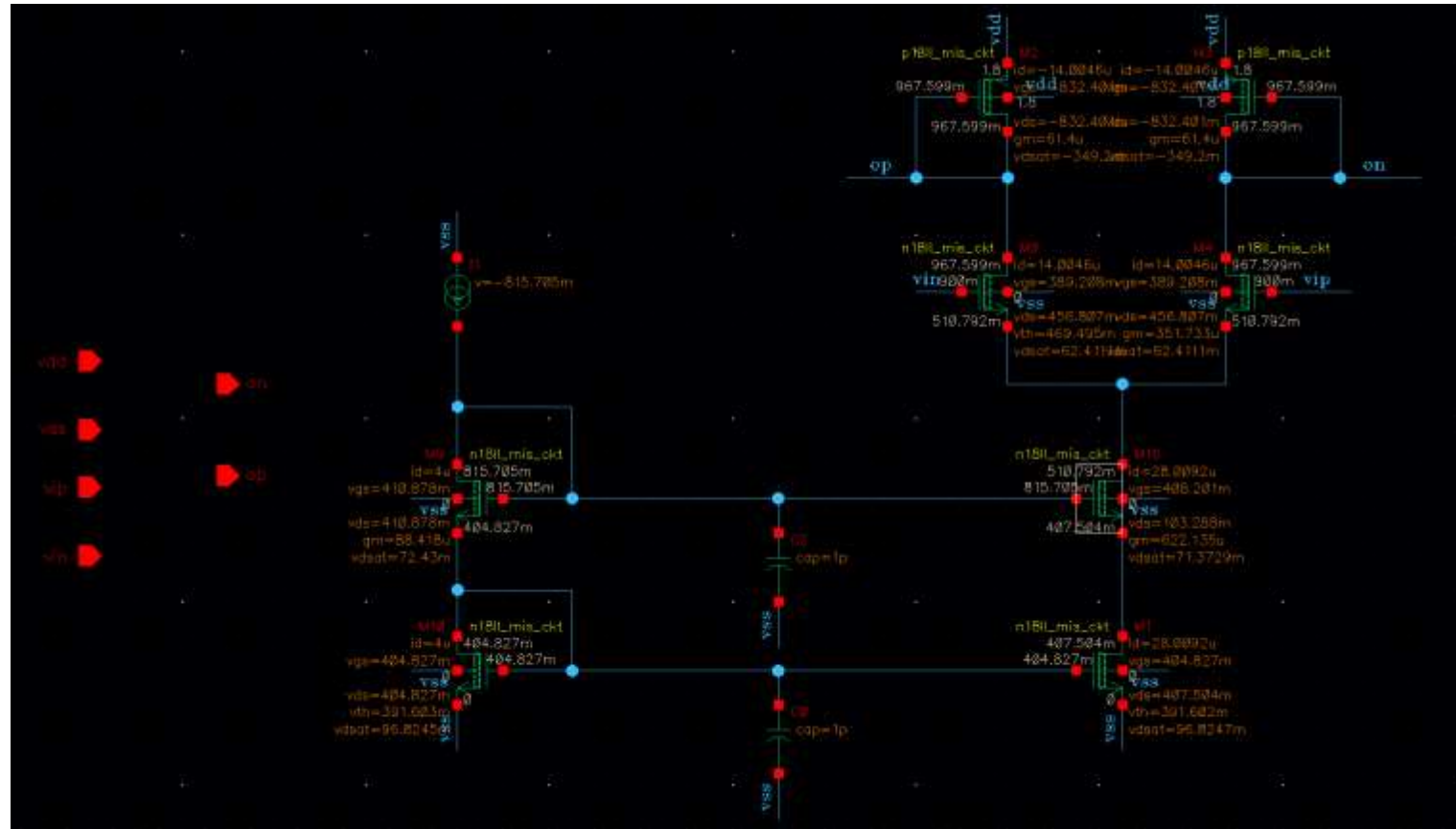
Preamp f-3db>1Ghz

Preamp current<24.5uA

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- **architecture: fully differential amp connecting diodes**

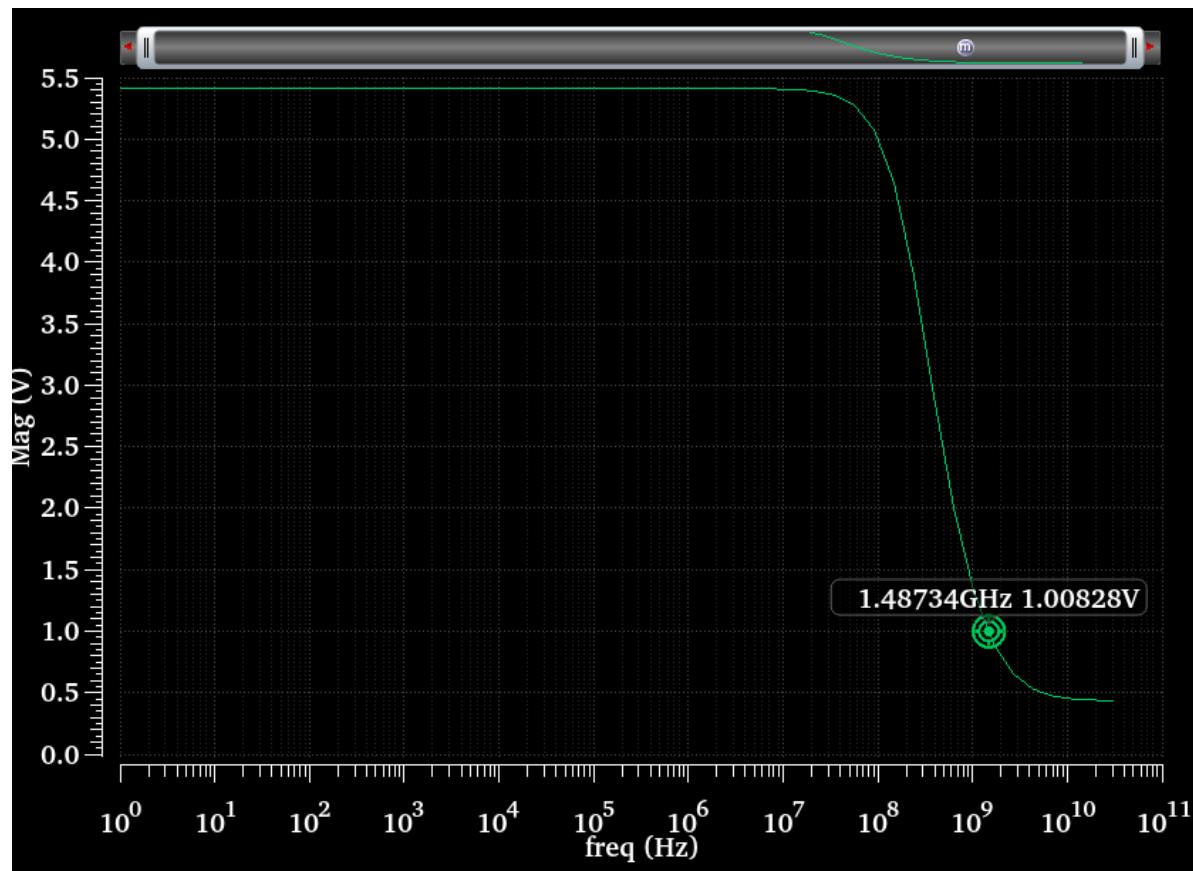
Preamplifier design

- Circuit implementation



第一级比较器的设计

- 仿真结果



Preamplifier gain=5.4

$f_{-3\text{dB}} = 1.5 \text{ GHz}$

第一级比较器的设计

- 利用oos技术消除preamp的offset

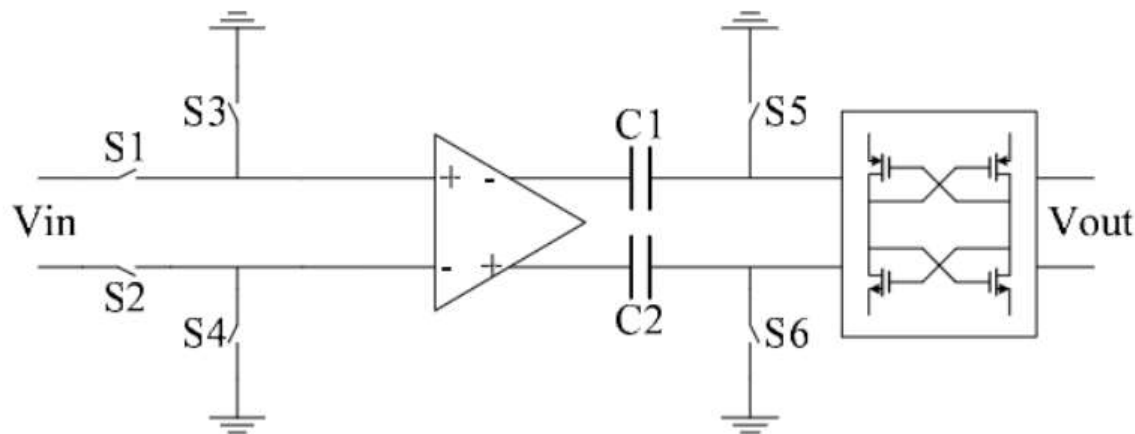


图 4.7 失调校准方法之 OOS

Offset 采样阶段: $S3$ - $S5$ 闭合, $S1$ - $S2$ 断开
Offset 消除阶段: $S3$ - $S5$ 断开, $S1$ - $S2$ 闭合

$$\Delta V_{os} = \frac{\Delta Q}{A_0 C} + \frac{V_{OSL}}{A_0}$$

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- **The first stage comp design**



- Comp design
- Preamplifier design
- **Autozero eliminate os**

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- Offset capacitor

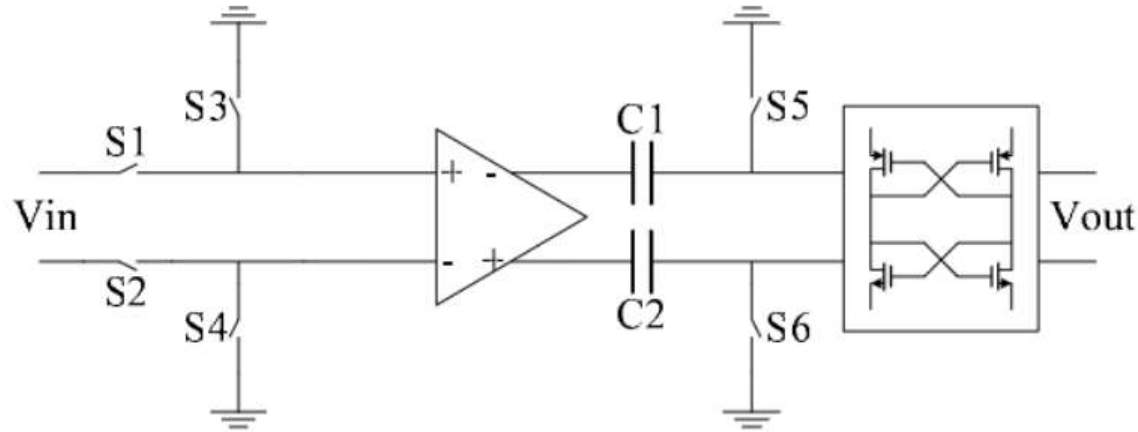


图 4.7 失调校准方法之 OOS

Add $2KT/C$



Referred input $\frac{\sqrt{\frac{2KT}{C}}}{6.3} < 0.1\text{mv}$



$C \geq 21\text{f}$

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- Offset capacitor

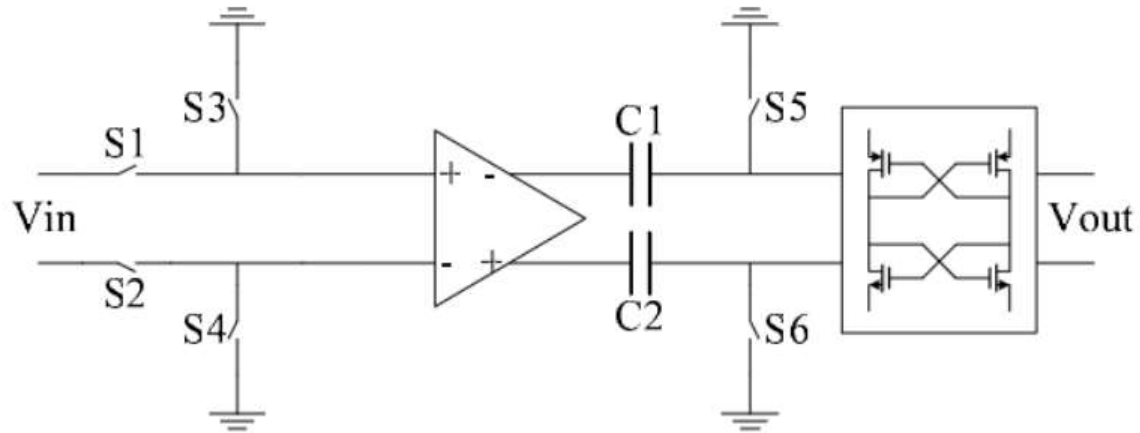


图 4.7 失调校准方法之 OOS

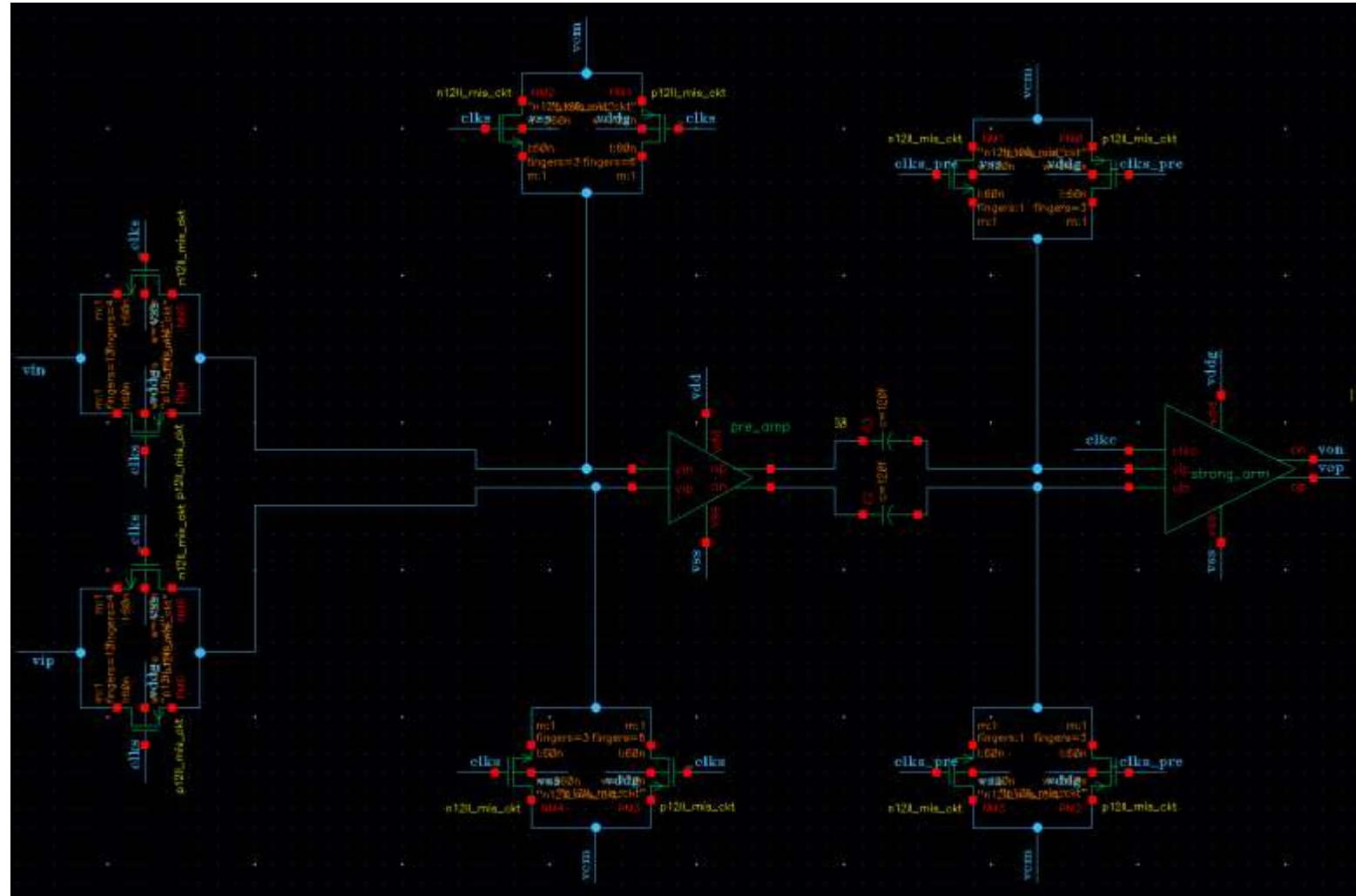


在offset 采样阶段，同时也是信号采样的阶段，采样阶段30ns，负载为存储offset电容，折中考虑速度和精度和功耗取offset电容为120f

Considering speed, resolution and power, the offset $c = 120f$

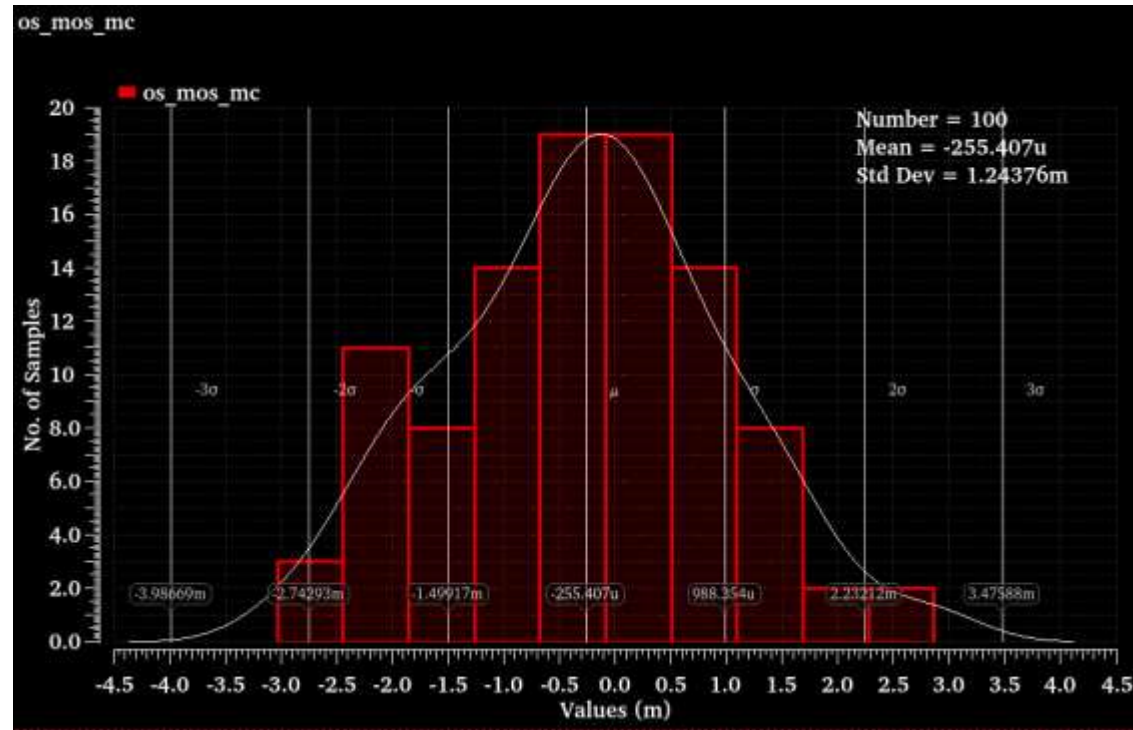
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- Circuits implementation



Comp design

- Stimulation result



offset=3.72mv (3σ)

input reference noise=600uv (3σ)

Total current=40.26uA

Thanks for attention