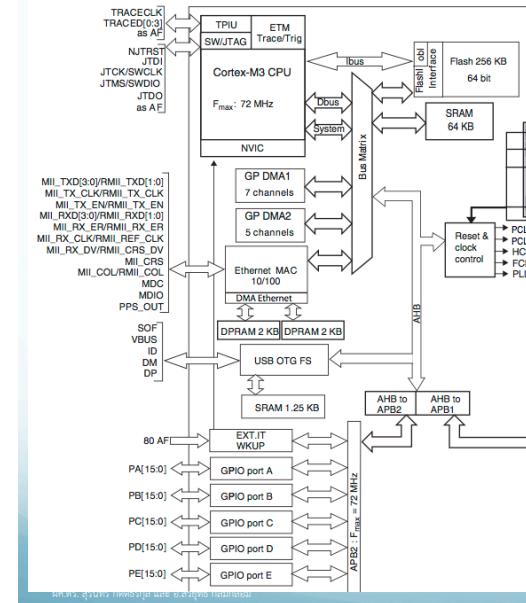


## ARM Cortex M3 & General Purpose Input/Output (GPIO)

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STM32F10x

& GPIO

- GPIO Port A – E
- Each port is 16 pins
- PA[0] – PA[15]
- PB[0] – PB[15]
- ...
- PE[0] – PE[15]

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## Memory and Bus Architecture

### □ Three masters:

Cortex™-M3 core DCode bus (D-bus) and System bus (S-bus)

GP-DMA1 (general-purpose DMA)

### □ Three slaves:

Internal SRAM

Internal Flash memory

AHB to APB bridges (AHB to APBx), which connect all the APB peripherals

## Definitions

### □ ICode bus

Connects the instruction bus of the Cortex™-M3 core to the Flash memory instruction interface. Instruction fetches are performed on this bus.

### □ DCode bus

Connects the DCode bus (literal load and debug access) of the

### ● Cortex™-M3 core to the Flash memory data interface

### □ System bus

Connects the system bus of the Cortex™-M3 core (peripherals bus) to a bus matrix which manages the arbitration between the core and the DMA

## Definitions

- DMA bus

Connects the AHB master interface of the DMA to the bus matrix which manages the access of CPU DCode and DMA to the SRAM, Flash memory and peripherals

- Bus matrix

Manages the access arbitration between the core system bus and the DMA master bus. The arbitration uses a round robin algorithm

- AHB/APB bridges (APB)

The two AHB/APB bridges provide full synchronous connections between the AHB and the two APB buses

APB buses operate at full speed (up to 24 MHz)

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## Memory Organization

- Program memory, data memory, registers and I/O ports are organized within the same linear 4-Gbyte address space

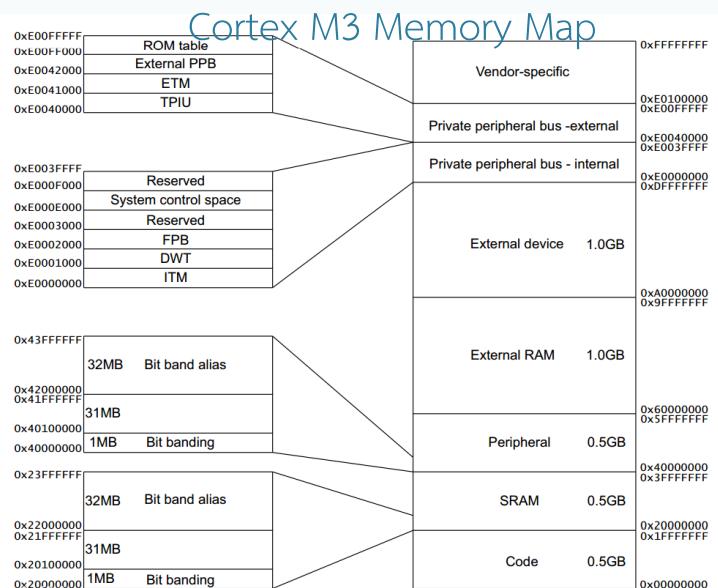
- Bytes are coded in memory in **little endian** format

The lowest numbered byte in a word is considered the word's least significant byte and the highest numbered byte, the most significant

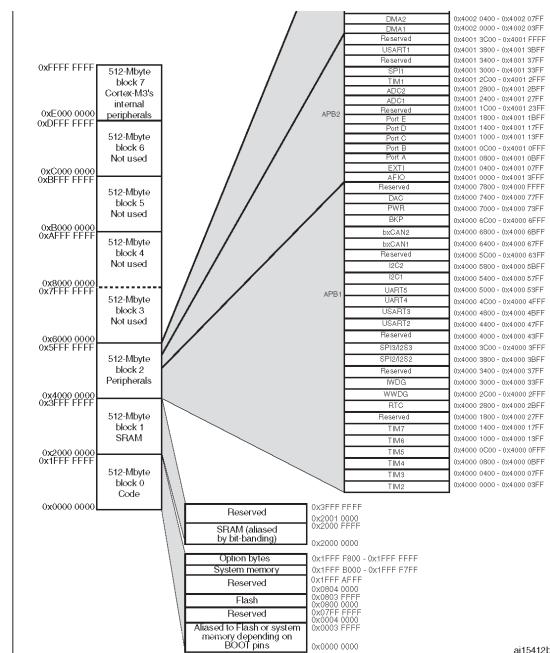
- Addressable memory space is divided into 8 main blocks, each of 512 MB

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## Memory Map

Boundary address	Peripheral	Bus
0x4002 3000 - 0x4002 33FF	CRC	
0x4002 2400 - 0x4002 2FFF	Reserved	
0x4002 2000 - 0x4002 23FF	Flash memory interface	AHB
0x4002 1400 - 0x4002 1FFF	Reserved	
0x4002 1000 - 0x4002 13FF	Reset and clock control RCC	
0x4002 0400 - 0x4002 0FFF	Reserved	
0x4002 0000 - 0x4002 03FF	DMA1	
0x4001 4C00 - 0x4001 FFFF	Reserved	
0x4001 4B00 - 0x4001 4BFF	TIM17 timer	
0x4001 4400 - 0x4001 47FF	TIM16 timer	
0x4001 4000 - 0x4001 43FF	TIM15 timer	
0x4001 3C00 - 0x4001 3FFF	Reserved	
0x4001 3800 - 0x4001 3BFF	USART1	
0x4001 3400 - 0x4001 37FF	Reserved	
0x4001 3000 - 0x4001 33FF	SPI1	
0x4001 2C00 - 0x4001 2FFF	TIM1 timer	
0x4001 2800 - 0x4001 2BFF	Reserved	
0x4001 2400 - 0x4001 27FF	ADC1	
0x4001 1C00 - 0x4001 23FF	Reserved	
0x4001 1800 - 0x4001 1BFF	GPIO Port E	
0x4001 1400 - 0x4001 17FF	GPIO Port D	
0x4001 1000 - 0x4001 13FF	GPIO Port C	
0x4001 0C00 - 0x4001 0FFF	GPIO Port B	
0x4001 0800 - 0x4001 0BFF	GPIO Port A	
0x4001 0400 - 0x4001 07FF	EXTI	
0x4001 0000 - 0x4001 03FF	AFIO	

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## Memory Organization

### □ Embedded Flash memory organization

Block	Name	Base addresses	Size (bytes)
Main memory	Page 0	0x0800 0000 - 0x0800 03FF	1 Kbyte
	Page 1	0x0800 0400 - 0x0800 07FF	1 Kbyte
	Page 2	0x0800 0800 - 0x0800 0BFF	1 Kbyte
	Page 3	0x0800 0C00 - 0x0800 0FFF	1 Kbyte
	Page 4	0x0800 1000 - 0x0800 13FF	1 Kbyte
Information block	.	.	.
	.	.	.
	.	.	.
Flash memory interface registers	Page 31	0x0800 7C00 - 0x0800 8000	1 Kbyte
	System memory	0x1FFF F000 - 0x1FFF F7FF	2 Kbytes
	Option Bytes	0x1FFF F800 - 0x1FFF F80F	16
	FLASH_ACR	0x4002 2000 - 0x4002 2003	4
	FLASH_KEYR	0x4002 2004 - 0x4002 2007	4
	FLASH_OPTKEYR	0x4002 2008 - 0x4002 200B	4
	FLASH_SR	0x4002 200C - 0x4002 200F	4
	FLASH_CR	0x4002 2010 - 0x4002 2013	4
	FLASH_AR	0x4002 2014 - 0x4002 2017	4
	Reserved	0x4002 2018 - 0x4002 201B	4
	FLASH_OBR	0x4002 201C - 0x4002 201F	4
	FLASH_WRPTR	0x4002 2020 - 0x4002 2023	4

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## Memory Organization

### □ Embedded SRAM

The STM32F100xx features up to 32 Kbytes of static SRAM. It can be accessed as bytes, half-words (16 bits) or full words (32 bits). The SRAM start address is 0x2000 0000

### □ Bit banding

The Cortex™-M3 memory map includes two bit-band regions. These regions map each word in an alias region of memory to a bit in a bit-band region of memory. Writing to a word in the alias region has the same effect as a read-modify-write operation on the targeted bit in the bit-band region.

In the STM32F100xx, both peripheral registers and SRAM are mapped in a bit-band region. This allows single bit-band write and read operations to be performed.

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## General-Purpose I/Os (GPIOs)

### □ Each of the general-purpose I/O ports has:

- Two 32-bit configuration registers (GPIOx\_CRL, GPIOx\_CRH)
- Two 32-bit data registers (GPIOx\_IDR, GPIOx\_ODR)
- 32-bit set/reset register (GPIOx\_BSRR)
- 16-bit reset register (GPIOx\_BRR)
- 32-bit locking register (GPIOx\_LCKR)

### □ Each port bit of GPIOs can be individually configured by software in several modes:

- Input floating
- Input pull-up
- Input-pull-down
- Analog
- Output open-drain
- Output push-pull
- Alternate function push-pull
- Alternate function open-drain

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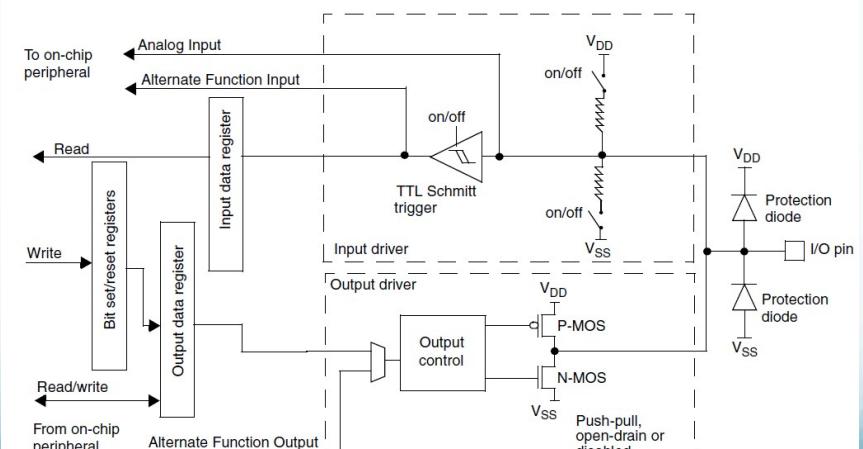
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## Pin Mapping Table

Table 5. Pin definitions (continued)						
Pins	Pin name	Type <sup>(1)</sup>	I/O Level <sup>(2)</sup>	Main function <sup>(3)</sup> (after reset)	Alternate functions <sup>(4)</sup>	
					Default	Remap
BGA100 LQFP64 LQFP100						
A8 50 77	PA15	I/O FT	JTDI	SPI3_NSS / I2S3_WS	TIM2_CH1_ETR / PA15 SPI1_NSS	
B9 51 78	PC10	I/O FT	PC10		UART4_TX	USART3_TX/ SPI3_SCK/I2S3_CK
B8 52 79	PC11	I/O FT	PC11		UART4_RX	USART3_RX/ SPI3_MISO
C8 53 80	PC12	I/O FT	PC12		UART5_TX	USART3_CK/ SPI3_MOSI/I2S3_SD
- - 81	PD0	I/O FT	PD0		-	OSC_IN <sup>(9)</sup> /CAN1_RX
- - 82	PD1	I/O FT	PD1		-	OSC_OUT <sup>(9)</sup> /CAN1_TX
B7 54 83	PD2	I/O FT	PD2		TIM3_ETR / UART5_RX	
C7 - 84	PD3	I/O FT	PD3		-	USART2_CTS
D7 - 85	PD4	I/O FT	PD4		-	USART2_RTS
B6 - 86	PD5	I/O FT	PD5		-	USART2_TX
C6 - 87	PD6	I/O FT	PD6		-	USART2_RX
D6 - 88	PD7	I/O FT	PD7		-	USART2_CK

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## Basic Structure of GPIO Bit



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## GPIO Bit Configuration Table

Configuration mode		CNF1	CNF0	MODE1	MODE0	PxODR register	
General purpose output	Push-pull	0	0	01	0 or 1		
	Open-drain		1		0 or 1		
Alternate Function output	Push-pull	1	0	10	don't care		
	Open-drain		1		don't care		
Input	Analog	0	00	0	don't care		
	Input floating			1	don't care		
	Input pull-down	1		0	0		
	Input pull-up			0	1		

Note: During and just after reset, the alternate functions are not active and the I/O ports are configured in Input Floating mode (CNFx[1:0]=01b, MODEx[1:0]=00b)

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## GPIO Configuration: Output MODE Bits

MODE[1:0]	Meaning
00	Reserved
01	Max. output speed 10 MHz
10	Max. output speed 2 MHz
11	Max. output speed 50 MHz

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## GPIO Operation

- During and just after reset, the alternate functions are not active and the I/O ports are configured in Input Floating mode (CNFx[1:0]=01b, MODEx[1:0]=00b)
- When configured as output, the value written to the Output Data register (GPIOx\_ODR) is output on the I/O pin.  
It is possible to use the output driver in Push-Pull mode or Open-Drain mode (only the N-MOS is activated when outputting 0).
- The Input Data register (GPIOx\_IDR) captures the data present on the I/O pin at every APB2 clock cycle
- All GPIO pins have an internal weak pull-up and weak pull-down which can be activated or not when configured as input

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## GPIO Atomic Bit Set or Reset

- Atomic Read/Modify access  
No interruption in the middle to cause errors
- Atomic operations ensure that the desired change is not interrupted resulting in partial set/reset of GPIOs
- There is no need for the software to disable interrupts when programming the GPIOx\_ODR at bit level:
- It is possible to modify only one or several bits in a single atomic APB2 write access
- This is achieved by programming to ‘1’ the Bit Set/Reset Register (GPIOx\_BSRR, or for reset only GPIOx\_BRR) to select the bits you want to modify.

Unselected bits will not be modified

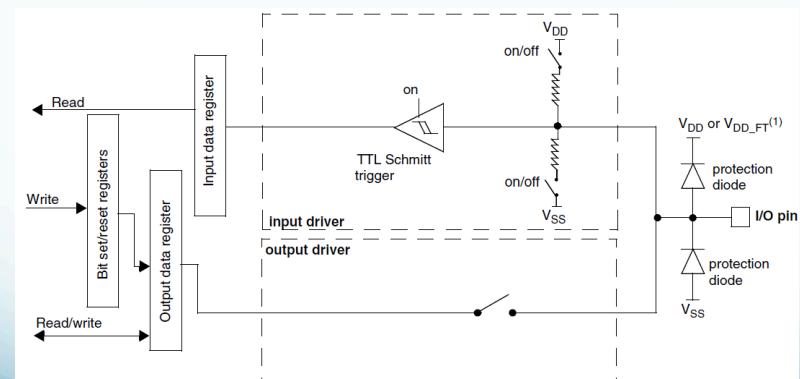
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## Input Configuration

- When the I/O Port is programmed as Input:
  - The Output Buffer is disabled
  - The Schmitt Trigger Input is activated
  - The weak pull-up and pull-down resistors are activated or not depending on input configuration (pull-up, pull-down or floating)
  - The data present on the I/O pin is sampled into the Input Data Register every APB2 clock cycle
  - A read access to the Input Data Register obtains the I/O State

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## Input Configuration



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## Output Configuration

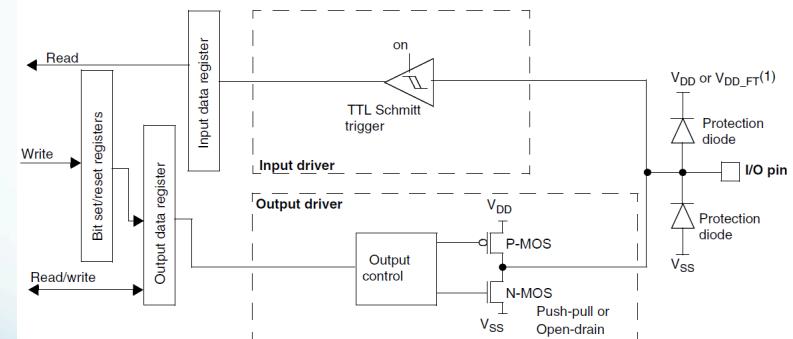
- When the I/O Port is programmed as Output:

- The Output Buffer is enabled:
  - Open Drain Mode: A "0" in the Output register activates the N-MOS while a "1" in the Output register leaves the port in Hi-Z. (the P-MOS is never activated)
  - Push-Pull Mode: A "0" in the Output register activates the N-MOS while a "1" in the Output register activates the P-MOS
- The Schmitt Trigger Input is activated.
- The weak pull-up and pull-down resistors are disabled.
- The data present on the I/O pin is sampled into the Input Data Register every APB2 clock cycle
- Read access to Input Data Register gets the I/O state in open drain mode
- Read access to Output Data register gets last written value in Push-Pull mode

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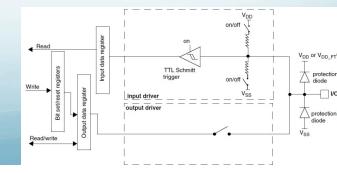
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## Output Configuration



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Compare to input configuration



## Alternate Function Configuration

- When the I/O Port is programmed as Alternate Function:

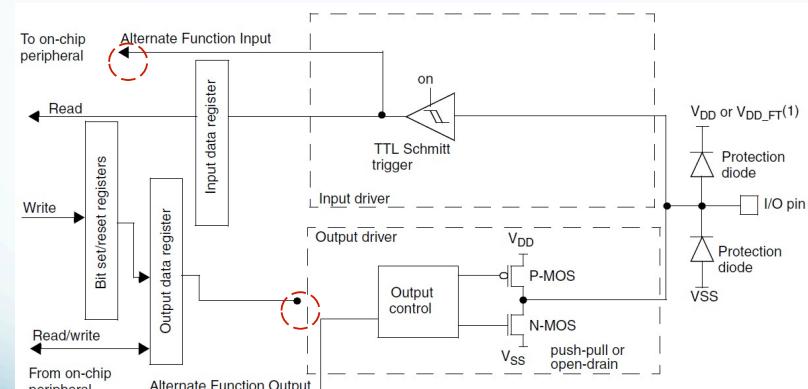
- The Output Buffer is turned on in Open Drain or Push-Pull configuration
- The Output Buffer is driven by the signal coming from the peripheral (alternate function out)
- The Schmitt Trigger Input is activated
- The weak pull-up and pull-down resistors are disabled
- The data present on the I/O pin is sampled into the Input Data Register every APB2 clock cycle
- A read access to the Input Data Register gets the I/O state in open drain mode

A read access to the Output Data register gets the last written value in Push-Pull mode

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## Alternate Function Configuration



អគ្គនាយកសារ និងវិទ្យាអបេដ និង និរនោត កម្មការណ៍

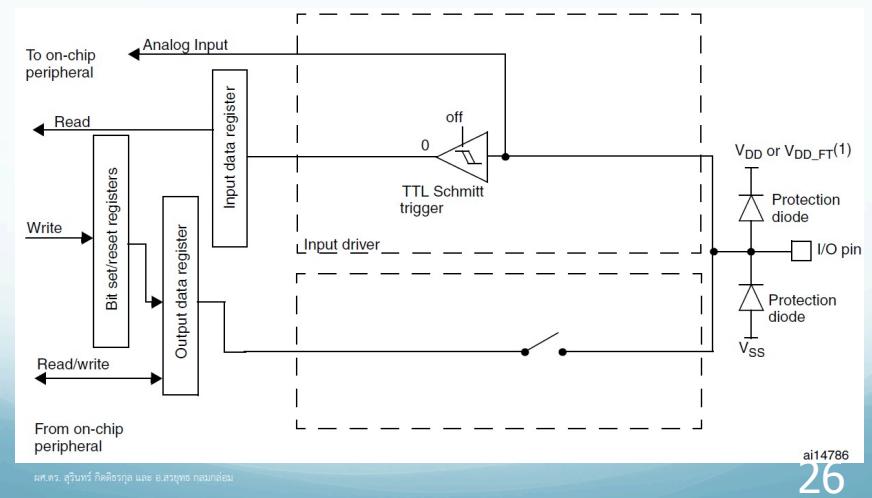
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## Analog Configuration

- When the I/O Port is programmed as Analog configuration:
  - The Output Buffer is disabled.
  - The Schmitt Trigger Input is de-activated providing zero consumption for every analog value of the I/O pin.
  - The output of the Schmitt Trigger is forced to a constant value (0).
  - The weak pull-up and pull-down resistors are disabled.
  - Read access to the Input Data Register gets the value “0”.

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## Analog I/O Configuration



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## GPIO Registers (Config Reg Low & High)

### 9.2.1 Port configuration register low (GPIOx\_CRL) (x=A..G)

Address offset: 0x00

Reset value: 0x4444 4444

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CNF7[1:0]	MODE7[1:0]	CNF6[1:0]	MODE6[1:0]	CNF5[1:0]	MODE5[1:0]	CNF4[1:0]	MODE4[1:0]								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

CNF3[1:0]	MODE3[1:0]	CNF2[1:0]	MODE2[1:0]	CNF1[1:0]	MODE1[1:0]	CNF0[1:0]	MODE0[1:0]
rw	rw	rw	rw	rw	rw	rw	rw

### 9.2.2 Port configuration register high (GPIOx\_CRH) (x=A..G)

Address offset: 0x04

Reset value: 0x4444 4444

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CNF15[1:0]	MODE15[1:0]	CNF14[1:0]	MODE14[1:0]	CNF13[1:0]	MODE13[1:0]	CNF12[1:0]	MODE12[1:0]								
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

CNF11[1:0]	MODE11[1:0]	CNF10[1:0]	MODE10[1:0]	CNF9[1:0]	MODE9[1:0]	CNF8[1:0]	MODE8[1:0]
rw	rw	rw	rw	rw	rw	rw	rw

## 4 LSB of GPIOx\_CRL (Config Reg Low)

3	2	1	0
CNFy[1:0]: Port x configuration bits (y= 0 .. 7)		MODEy[1:0]: Port x mode bits (y= 0 .. 7)	
rw	rw	rw	rw

### CNFy[1:0]: Port x configuration bits (y= 0 .. 7)

#### In input mode (MODE[1:0]=00):

00: Analog mode

01: Floating input (reset state)

10: Input with pull-up / pull-down

11: Reserved

#### In output mode (MODE[1:0] > 00):

00: General purpose output push-pull

01: General purpose output Open-drain

10: Alternate function output Push-pull

11: Alternate function output Open-drain

### MODEy[1:0]: Port x mode bits (y= 0 .. 7)

00: Input mode (reset state)

01: Output mode, max speed 10 MHz.

10: Output mode, max speed 2 MHz.

11: Output mode, max speed 50 MHz.

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## I/P Data Register of Port x (A-E)

### 9.2.3 Port input data register (GPIOx\_IDR) (x=A..G)

Address offset: 0x08h

Reset value: 0x0000 XXXX

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IDR15	IDR14	IDR13	IDR12	IDR11	IDR10	IDR9	IDR8	IDR7	IDR6	IDR5	IDR4	IDR3	IDR2	IDR1	IDR0

Bits 31:16 Reserved, must be kept at reset value.

Bits 15:0 **IDRy**: Port input data (y= 0 .. 15)

These bits are read only and can be accessed in Word mode only. They contain the input value of the corresponding I/O port.

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## O/P Data Register of Port x (A-E)

### 9.2.4 Port output data register (GPIOx\_ODR) (x=A..G)

Address offset: 0x0C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ODR15	ODR14	ODR13	ODR12	ODR11	ODR10	ODR9	ODR8	ODR7	ODR6	ODR5	ODR4	ODR3	ODR2	ODR1	ODR0

Bits 31:16 Reserved, must be kept at reset value.

Bits 15:0 **ODRy**: Port output data (y= 0 .. 15)

These bits can be read and written by software and can be accessed in Word mode only.

Note: For atomic bit set/reset, the ODR bits can be individually set and cleared by writing to the GPIOx\_BSRR register (x = A .. G).

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## Set/Reset Bit Register of Port x (A-E)

### 9.2.5 Port bit set/reset register (GPIOx\_BSRR) (x=A..G)

Address offset: 0x10

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
BR15	BR14	BR13	BR12	BR11	BR10	BR9	BR8	BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0

**BSy**: Port x Set bit y (y= 0 .. 15)

These bits are write-only and can be accessed in Word mode only.

0: No action on the corresponding ODRx bit

1: Set the corresponding ODRx bit

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## Reset Bit Register of Port x (A-E)

### 9.2.6 Port bit reset register (GPIOx\_BRR) (x=A..G)

Address offset: 0x14

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----

Bits 31:16 Reserved

Bits 15:0 **BRy**: Port x Reset bit y (y= 0 .. 15)

These bits are write-only and can be accessed in Word mode only.

0: No action on the corresponding ODRx bit

1: Reset the corresponding ODRx bit

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## Config Lock Register of Port x (A-E)

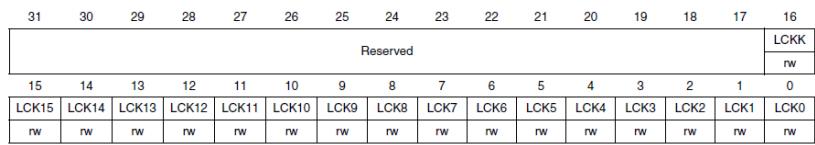
### 9.2.7 Port configuration lock register (GPIOx\_LCKR) (x=A..G)

This register is used to lock the configuration of the port bits when a correct write sequence is applied to bit 16 (LCKK). The value of bits [15:0] is used to lock the configuration of the GPIO. During the write sequence, the value of LCKR[15:0] must not change. When the LOCK sequence has been applied on a port bit it is no longer possible to modify the value of the port bit until the next reset.

Each lock bit freezes the corresponding 4 bits of the control register (CRL, CRH).

Address offset: 0x18

Reset value: 0x0000 0000



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Bits 31:17 Reserved

#### Bit 16 LCKK[16]: Lock key

This bit can be read anytime. It can only be modified using the Lock Key Writing Sequence.  
0: Port configuration lock key not active  
1: Port configuration lock key active. GPIOx\_LCKR register is locked until an MCU reset occurs.

LOCK key writing sequence:

Write 1

Write 0

Write 1

Read 0

Read 1 (this read is optional but confirms that the lock is active)

Note: During the LOCK Key Writing sequence, the value of LCK[15:0] must not change.  
Any error in the lock sequence will abort the lock.

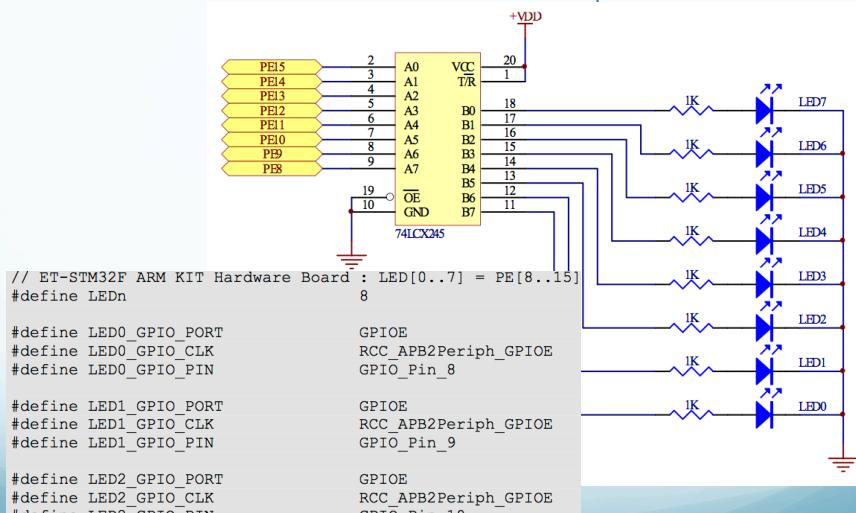
#### Bits 15:0 LCKy: Port x Lock bit y (y = 0 .. 15)

These bits are read write but can only be written when the LCKK bit is 0.  
0: Port configuration not locked  
1: Port configuration locked.

พស. សុវណ្ណៈ កិចចិទ្ទក និង នគរបាល កម្មការណ៍

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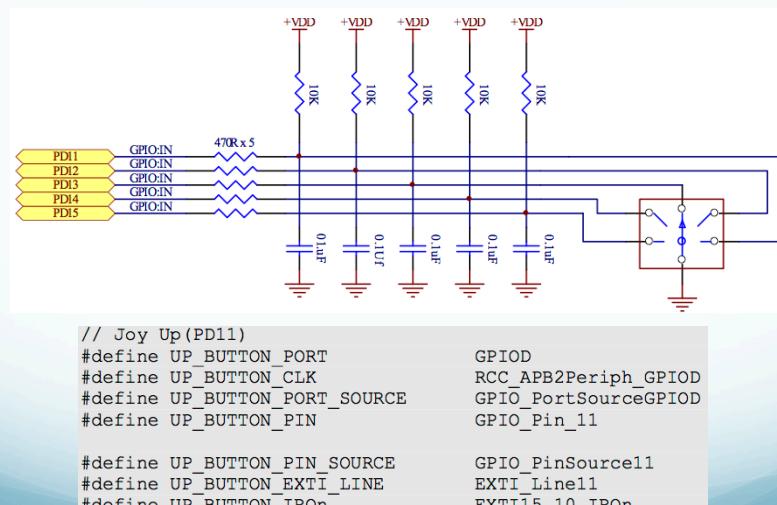
## ETT Board & LEDs (Output)



ពស. សុវណ្ណៈ កិចចិទ្ទក និង នគរបាល កម្មការណ៍

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## ETT Board & JoySwitch (Input)



ពស. សុវណ្ណៈ កិចចិទ្ទក និង នគរបាល កម្មការណ៍

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