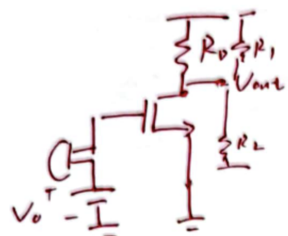
Common-Source Stage II & Variants

zrrraa

2023.11.19

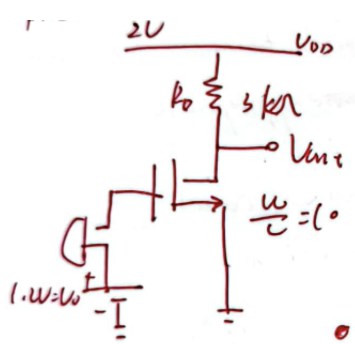
Simplification



Ignore the Channel-Length Modulation, we can simplify the gain as:
$A_V = -g_m *$(total resistance tied from drain to AC GROUND).
AC GROUND means the point which has a const voltage.
In the picture, we have:

$$A_V = -g_m(R_D||R_1||R_2)$$

Example



First assume that it's in Sat. zone and then calculate out the I_D and check if the assume is true.

If we want to double the gain, how can we do?

- Try doubling R_D? $I_D * R_D$ larger, the V_{DS} lower, the MOS will run out fo the saturation zone.

We always want an amplifier working in saturation zone because it means larger swing of I_D.We want a lower I_D in DC, but higher in AC.

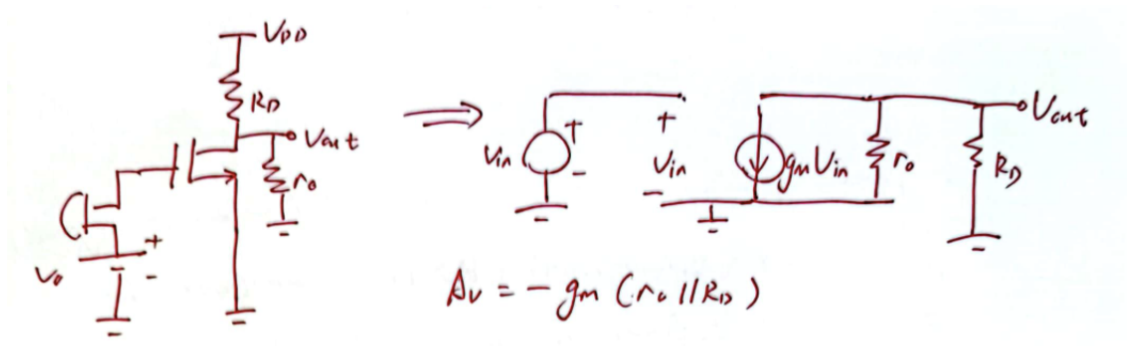
- Try increasing $g_m = \sqrt{2\mu C_{ox}\frac{W}{L}I_D}$

We shouldn't increase I_D, that leads to the same result as increasing R_D.

Then $\frac{W}{L}$?

It is worth noting that if $\frac{W}{L}$ becomes sufficiently large, $g_m \approx \frac{I_D}{1.5V_T}$. V_T here is $\frac{KT}{q}$, 26mV in air.

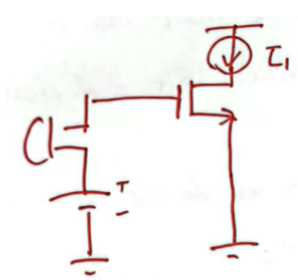
Inclusion of Channel-Length Modulation



Small-Signal Model with Inclusion of Channel-Length Modulation

It's clear that $A_V = -g_m(r_o||R_D)$.

We want the largest A_V, means the largest R_D. The circuit cannot be open, because we need bias. So, a current source is appropriate.

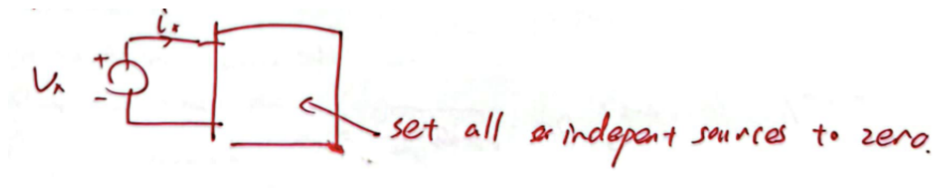


I_1 is const & ideal. We also assume the MOS working in saturation.

Now $A_V = -g_m * r_o$, we call this intrinsic gain of MOS. It's usually 5 10.

Concept of Port Impedance

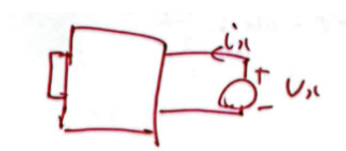
input impedance



When measuring the input impedance, we set all independent sources to zero. The output port should be open.

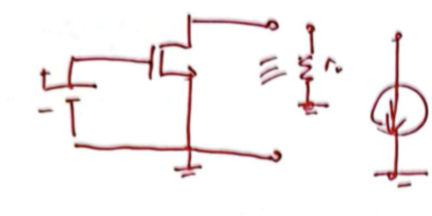
$$R_{in} = \frac{v_x}{i_x}$$

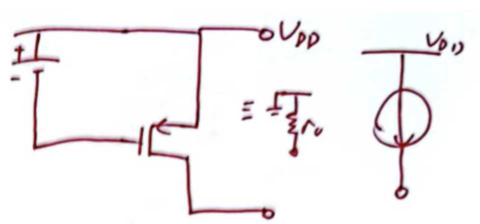
output impedance



When measuring the output impedance, the input port should be short.

Let's build a current source

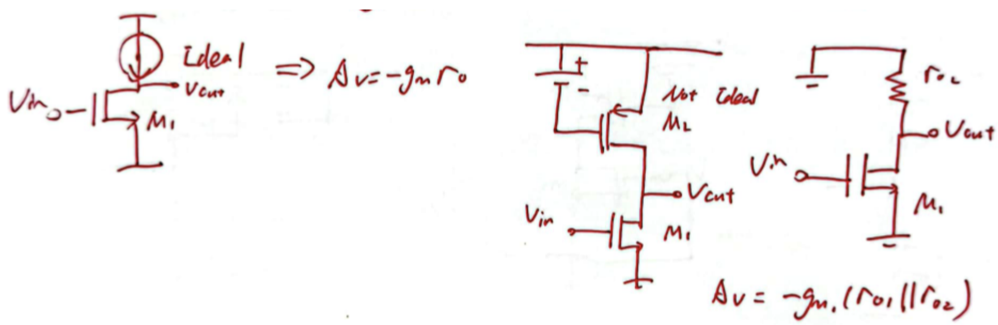




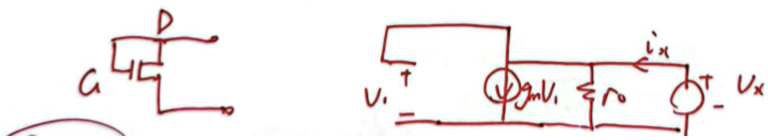
If a MOS is working as a current source, we can refer it as a resistor. (only when $\lambda > 0$)
If $\lambda = 0$, we refer it as a open circuit.

Common-Source Stage with Current-Source Load

Refer the MOS as a resistor or a open circuit.



Common-Source Stage with Diode-Connected Device Load



Diode-Connected means the Gate and Drain are short together.
From the small-signal model we can get the output impedance.

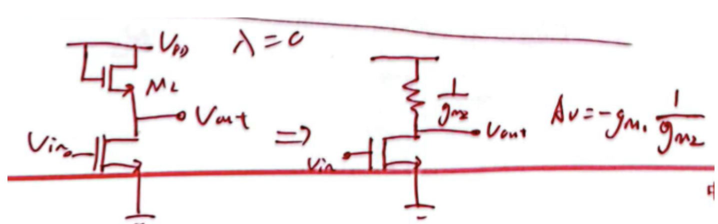
$$i_x = \frac{v_x}{r_o} + g_m v_1$$

$$v_1 = v_x$$

So,

$$\frac{v_x}{i_x} = r_o || \frac{1}{g_m}$$

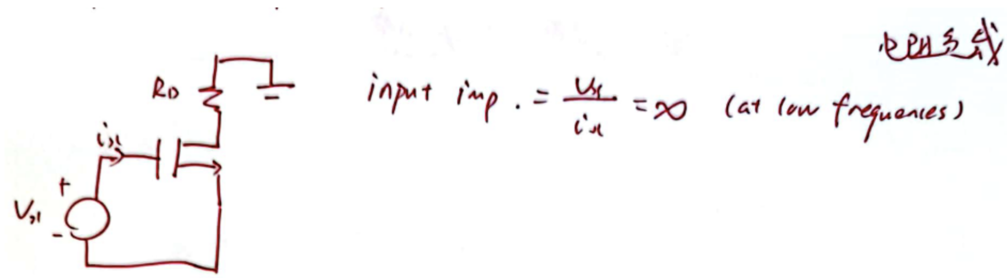
Usually, $r_o >> \frac{1}{g_m}$, so the output impedance can be approximately equal to $\frac{1}{g_m}$.



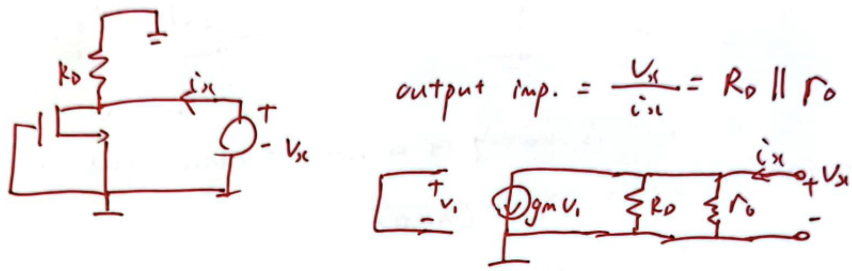
Also we have $A_V = -g_{m1}\frac{1}{g_{m2}}$.

Input and Output Impedances

Resistor Load

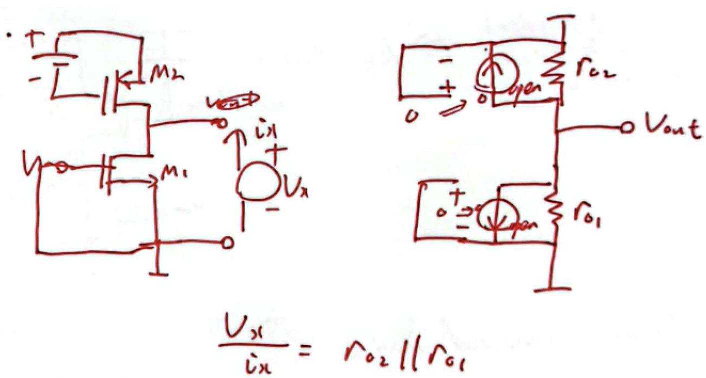


input imp. $= \frac{v_x}{i_x} = \infty$ (at low frequencies)



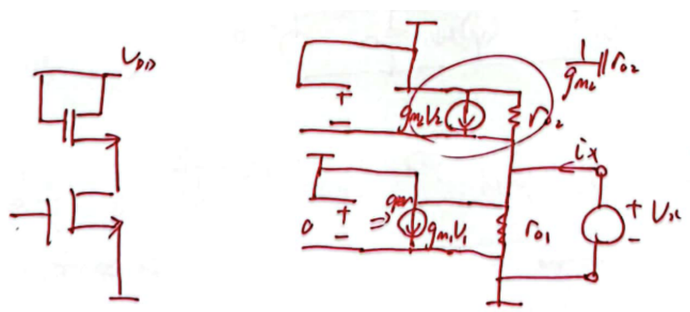
output imp. $= \frac{v_x}{i_x} = R_D || r_o$

Current-Source Load



output imp. $\frac{v_x}{i_x} = r_{o2} || r_{o1}$

Diode-Connected Device Load



output imp. $= \frac{v_x}{i_x} = \frac{1}{g_m 2}||r_{o2}||r_{o1}$
Here $\frac{1}{g_{m2}}$ is dominant.

Link

Razavi Electronics Circuits 1: lectrue 36
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