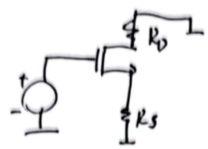
Common-Source Stage with Degeneration

zrrraa

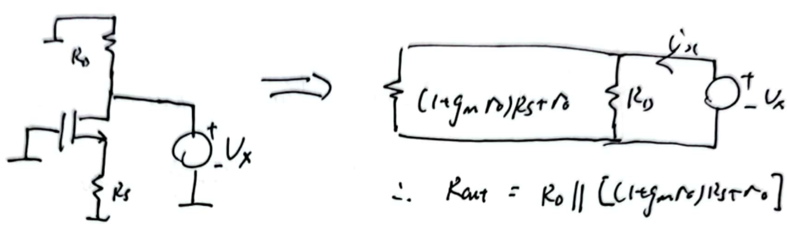
2023.12.9

I/O Impedances of Deg. CS Stage

Input Imp:



$R_{in} = \infty$ at low frequency.
Output Imp ($\lambda > 0$) :



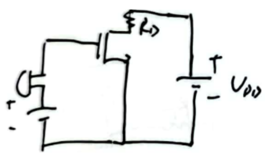
Borrow the output impedance formula of the degraded common source amplifier derived from the previous section, We can get:

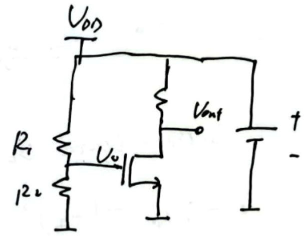
$$R_{out} = R_D||[(1 + g_m r_o)R_s + r_o]$$

Biasing Techniques

One possible way to bias the MOS is using resistors to divide the voltage.

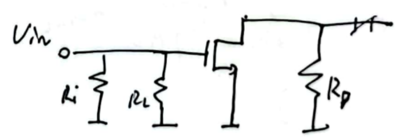
$$\frac{R_2}{R_1 + R_2} V_{DD} = V_0$$





Observations $\lambda = 0$

Input Impedance $= R_1 || R_2$



$$\frac{V_{out}}{V_{in}} = \frac{V_x}{V_{in}} * \frac{V_{out}}{V_x} = \frac{R_1||R_2}{R_1||R_2 + R_{mike}}(-g_m R_D)$$

Choose $R_1||R_2 >> R_{mike}$ to minimize the attenuation.

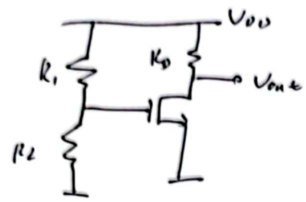
Can we increase R_D to increase gain?

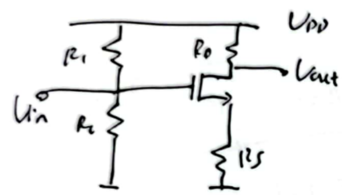
Of course, but make sure the MOSFET is in saturation zone.

Sensitivity

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{DD}\frac{R_2}{R_1 + R_2} - V_{TH})^2$$

I_D is related to V_{DD}, V_{TH}, temp and the basic process parameters.





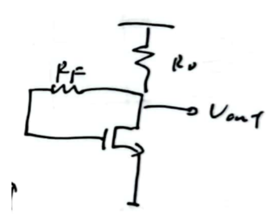
Reduced Sensitivity with Deg. CS Stage

$$\frac{R_2}{R_2 + R_1} V_{DD} = V_{GS} + I_D R_S$$

Part of the change in V_{DD} will be shared by R_S, so V_{GS} is more stable, I is more stable, and the gain is more stable.

Self-Biased CS Stage $\lambda = 0$

In this case, the drain voltage equals to the gate voltage, so the MOSFET always works in saturation zone.

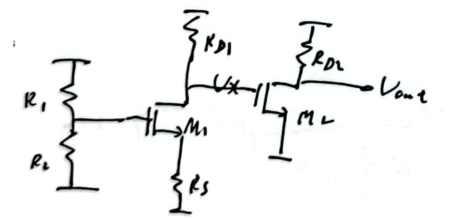


$$V_{DS} = V_{GS} = V_{DD} - I_D R_D$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{DD} - I_D R_D - V_{TH})^2$$

Therefore, when V_{TH} decreases, I_D increases.

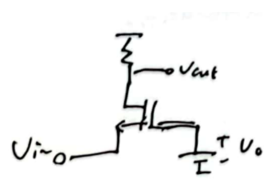
Example



$$\frac{V_{out}}{V_{in}} = \frac{V_x}{V_in} * \frac{V_{out}}{V_x} = -\frac{R_{D1}}{\frac{1}{g_{m1}} + R_S} * (-g_{m2} * R_{D2})$$

This is called a cascade amplifier.

Common-Gate Topology



when V_{in} increases, V_{out} increases, so the gain is positive.

Link

Razavi Electronics Circuits 1: lectrue 39