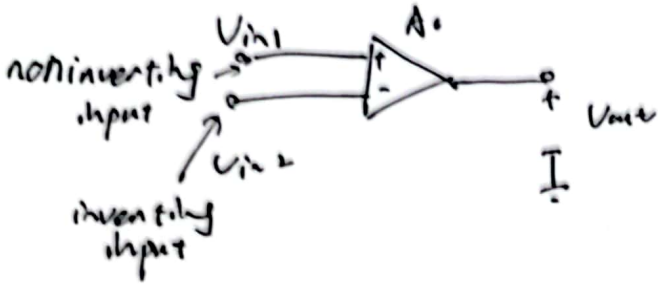
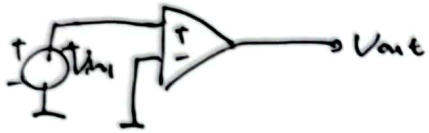
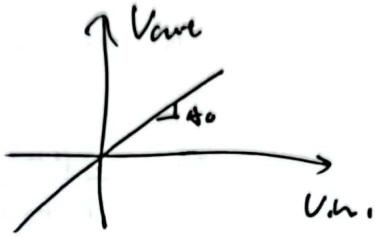
Op Amp Basics

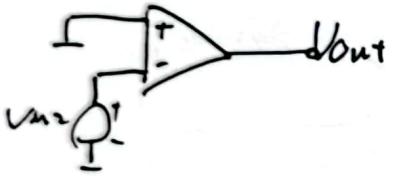


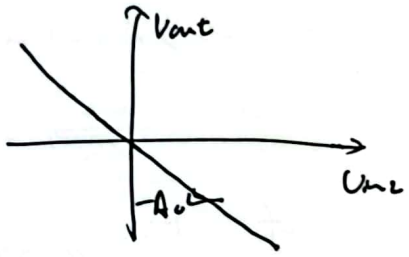
$$V_{out} = (V_{in1} - V_{in2}) A_0$$

Input / Output characteristics









for ideal Op Amp

Input Imp: ∞

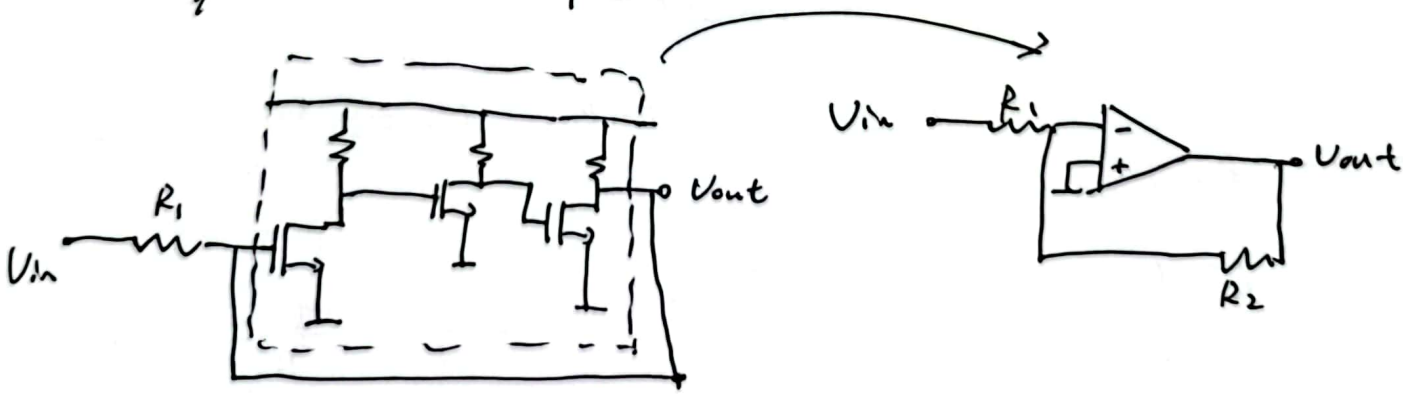
Output Imp: 0

A_0: ∞

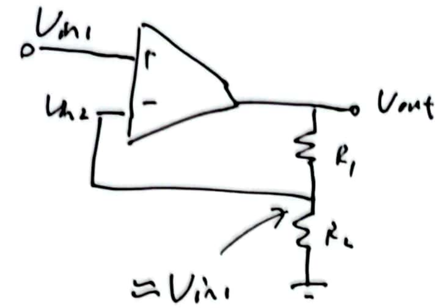
Observations

① If $V_{out} \approx$ a few volts and $A_0 \approx 1000 \Rightarrow V_{in1} - V_{in2} \approx$ a few mV.

② If we can visualize a complex circuit as an op amp, the analysis becomes simpler.



Noninverting Amplifier



Case I: $A_0 \to \infty$

$V_{out} = (V_{in1} - V_{in2}) A_0$

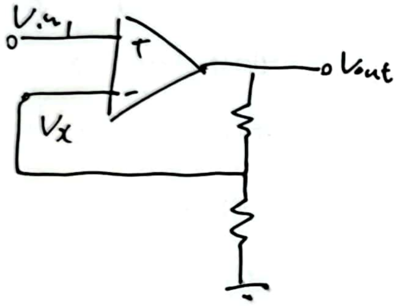
finite — very small — very large

$\Rightarrow V_{in1} \simeq V_{in2}$

$\Rightarrow V_{out} = \frac{V_{in}}{R_2}(R_1+R_2)$

至此，用OPAMP取代了MOS放大，可以减少对工艺参数的依赖，比如跨导.

Case II: A_0 not very high



$V_x = V_{out} \frac{R_2}{R_1+R_2}$

$(V_{in} - V_x) A_0 = V_{out}$

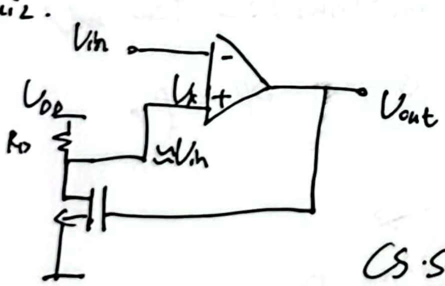
$\Rightarrow \frac{V_{out}}{V_{in}} = \frac{A_0}{1 + \frac{R_2}{R_1+R_2} A_0} = \frac{1}{\frac{1}{A_0} + \frac{R_2}{R_1+R_2}}$

A_0 → open loop gain

$\frac{V_{out}}{V_{in}}$ → close loop gain

if $\frac{R_2}{R_1+R_2} A_0 \gg 1 \Rightarrow \frac{V_{out}}{V_{in}}$ relatively indep of A_0

Quiz.

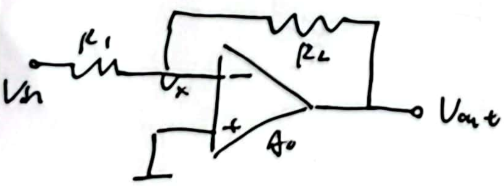


Assume $A_0 \to \infty$

$\therefore V_x \simeq V_{in}$

CS Stage: $V_{out} \cdot (-g_m R_D) = V_{in} \Rightarrow \frac{V_{out}}{V_{in}} = -\frac{1}{g_m R_D}$

Inverting Amplifier

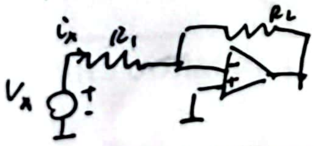


Case I. $A_0 \to \infty$

$\frac{V_{in}}{R_1} = \frac{-V_{out}}{R_2}$

$\Rightarrow \frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1}$

Input Impedance $\simeq R_1$

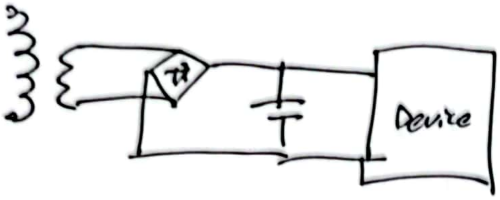


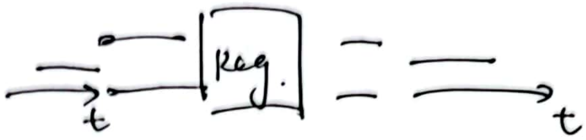
$R = \frac{V_x}{i_x} = R_1$

Case II. A_0 not very high

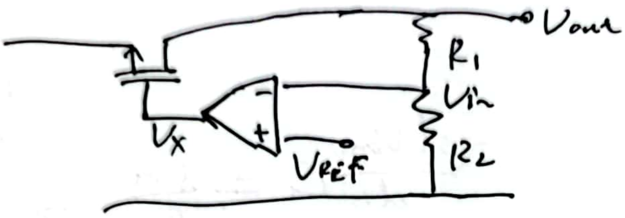
$\left.\begin{array}{l} V_x = \frac{V_{out}}{-A_0} \\ \frac{V_{in} - V_x}{R_1} = \frac{V_x - V_{out}}{R_2} \end{array}\right\} \Rightarrow \frac{V_{out}}{V_{in}} = \frac{-1}{\frac{R_1}{R_2} + \frac{1}{A_0}\frac{R_1+R_2}{R_1}}$

Example of Application: Voltage Regulator





AC-DC 降压电路中，需要一个稳压器。



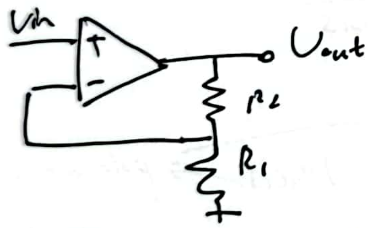
$V_{out}\uparrow \Rightarrow V_{in}\uparrow \Rightarrow V_x\downarrow \Rightarrow V_{out}\downarrow$

起负反馈稳压的作用.

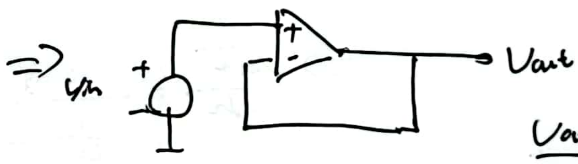
$V_{REF} > V_{in}$

$$V_{out} = V_{REF}\left(1+\frac{R_1}{R_2}\right)$$

Unity-Gain Buffer



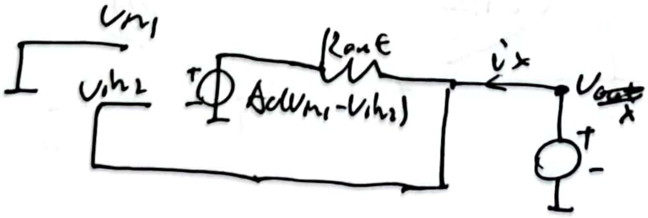
$$\frac{V_{out}}{V_{in}} \approx 1+\frac{R_2}{R_1}$$



$$\frac{V_{out}}{V_{in}} \approx 1$$

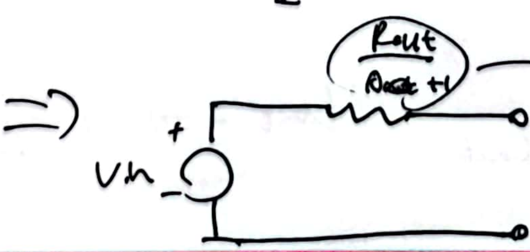
Input imp $\approx \infty \Rightarrow$ can sense voltage without loading the circuit

utilize Thevenin Equivalent to analyze Output Imp.



$$i_x = \frac{V_x - A_0(-V_x)}{R_{out}}$$

$$\frac{V_x}{i_x} = \frac{R_{out}}{A_0+1}$$



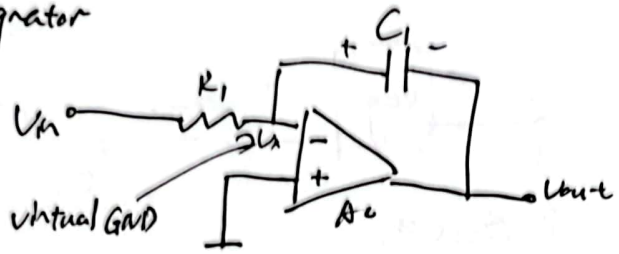
$\frac{R_{out}}{A_0+1}$ — very small

驱动能力强

General Inverting Amp.

$$\frac{V_{out}}{V_{in}} \simeq -\frac{Z_2}{Z_1}$$

Integrator



A0 large:

$$\frac{V_{out}}{V_{in}} = -\frac{\frac{1}{C_1 s}}{R_1} = -\frac{1}{R_1 C_1 s}$$

↓ pole at origin, no bound

current through $R_1 \simeq \frac{V_{in}}{R_1}$

current through cap $\simeq C\frac{dV}{dt}$

$$-\frac{dV_{out}}{dt}C_1 \simeq \frac{V_{in}}{R_1} \Rightarrow V_{out} = -\frac{1}{R_1 C_1}\int V_{in}\,dt$$

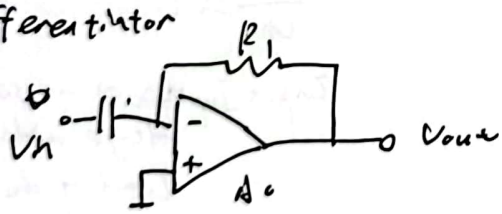
If A0 is not large

$$V_x = -\frac{V_{out}}{A_0}$$

$$\frac{V_{in} + \frac{V_{out}}{A_0}}{R_1} = \frac{0 - \frac{V_{out}}{A_0} - V_{out}}{\frac{1}{C_1 s}}$$

$$\Rightarrow \frac{V_{out}}{V_{in}} = \frac{-1}{\frac{1}{A_0} + (1+\frac{1}{A_0})R_1 C_1 s}$$ → pole not at origin, no bound

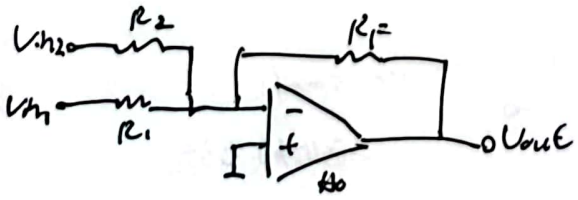
Differentiator



$$\frac{V_{out}}{V_{in}} = -\frac{R_1}{\frac{1}{C_1 s}} = -R_1 C_1 s$$

Plot the freq. response

Voltage Adder (Summer)



$$V_{out} = -R_f\left(\frac{V_{in1}}{R_1} + \frac{V_{in2}}{R_2}\right)$$