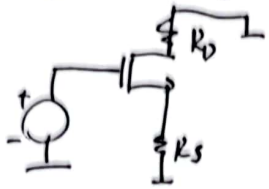
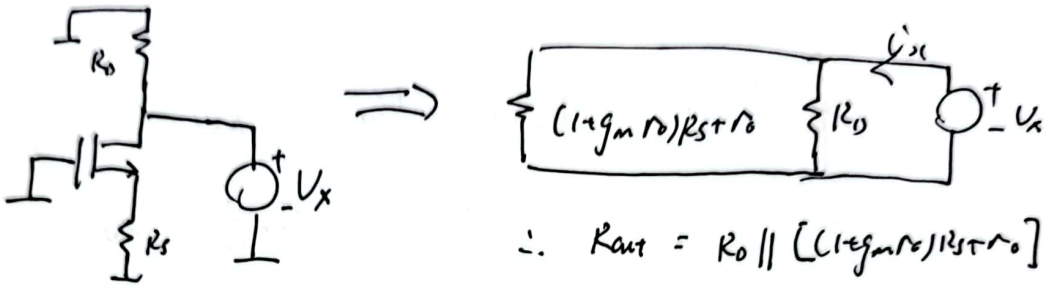
I/O impedances of Deg. Cs stage

Input Imp:



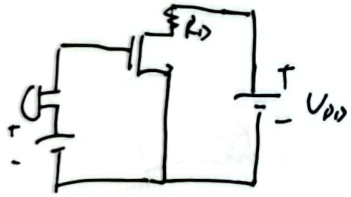
$R_{in} = \infty$ at low frequency

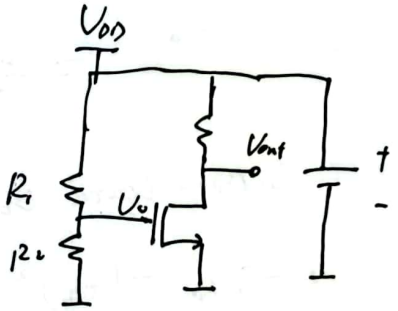
Output Imp: ($\lambda > 0$)



$\therefore R_{out} = R_D \parallel [(1+g_m r_o)R_S + r_o]$

Biasing Techniques:



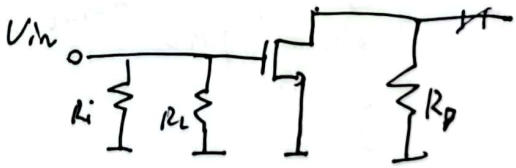


one possible choice to bias

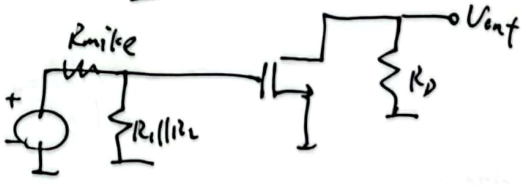
$\frac{R_2}{R_1+R_2} V_{DD} = V_{GA}$

Observations. ($\lambda = 0$)

① $R_{in} = R_1 \parallel R_2$



Input Imp: $R_1 \parallel R_2$.



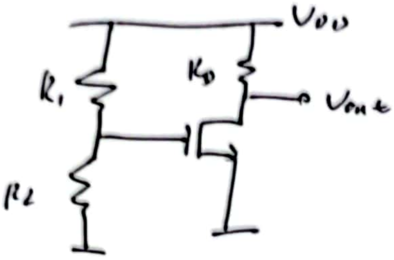
$\frac{V_{out}}{V_{in}} = \frac{V_X}{V_{in}} \cdot \frac{V_{out}}{V_X} = \frac{R_1 \parallel R_2}{R_1 \parallel R_2 + R_{mike}} (g_m R_D)$

choose $R_1 \parallel R_2 \gg R_{mike}$ to minimize the attenuation

② Can we increase R_D to increase gain?

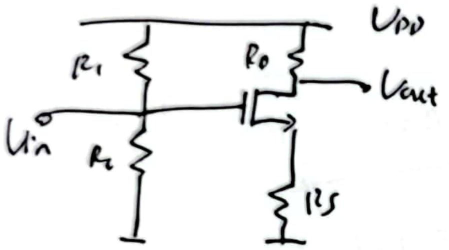
make sure the sat. it's o/c.

③ $I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{DD}\frac{R_2}{R_1+R_2} - V_{TH}\right)^2$



sensitive to V_{DD}, $\mu_n C_{ox}$, V_{TH}, temp.

④ Reduced sensitivity with Deg. CS stage



$V_{DD}\frac{R_2}{R_2+R_1} = V_{GS} + I_D R_S$ V_{DD} 的改变会由 R_S 分走一部分.

$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$

且 V_{GS} 变化变

I_D 变化变

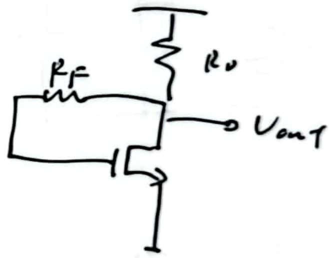
V_{out} 变化变

Self-Biased CS Stage $\lambda = 0$ ⇒ 肯定饱和

$V_{TH}\downarrow \Rightarrow I_D\uparrow$

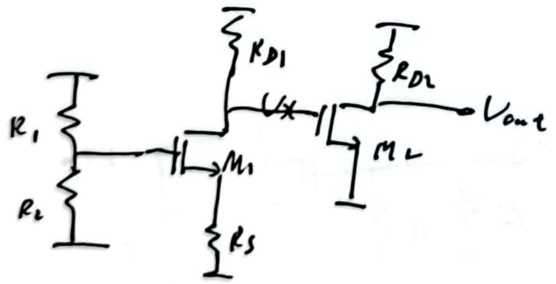
Drain Voltage $= V_{DD} - I_D R_D =$ Gate Voltage

$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{DD} - I_D R_D - V_{TH})^2$



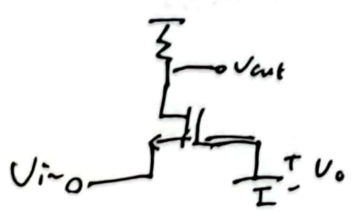
$V_{TH}\downarrow \Rightarrow I_D\uparrow$

EXAmple $\lambda = 0$



$$\frac{V_{out}}{V_{in}} = \frac{V_{out}}{V_X}\cdot\frac{V_X}{V_{in}} = -\frac{R_{D1}}{\frac{1}{g_{m1}}+R_S}\cdot(-g_{m2}\cdot R_{D2})$$

Common-Gate Topology



$V_{in}\uparrow$ $V_{out}\uparrow$ $A_v > 0$.