Coevolution of Neural Network and Computer Architecture

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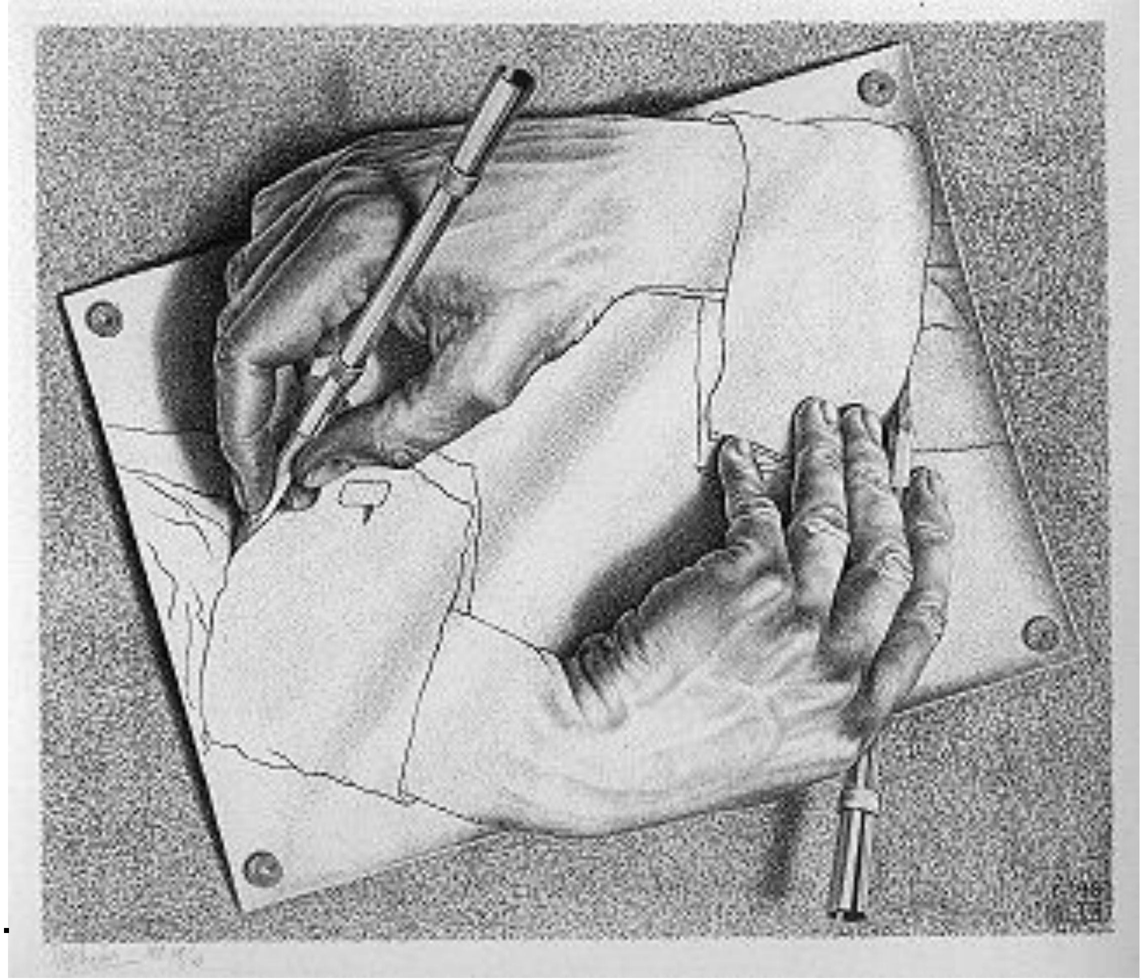
Propose new kind of Neural Network for hardware.

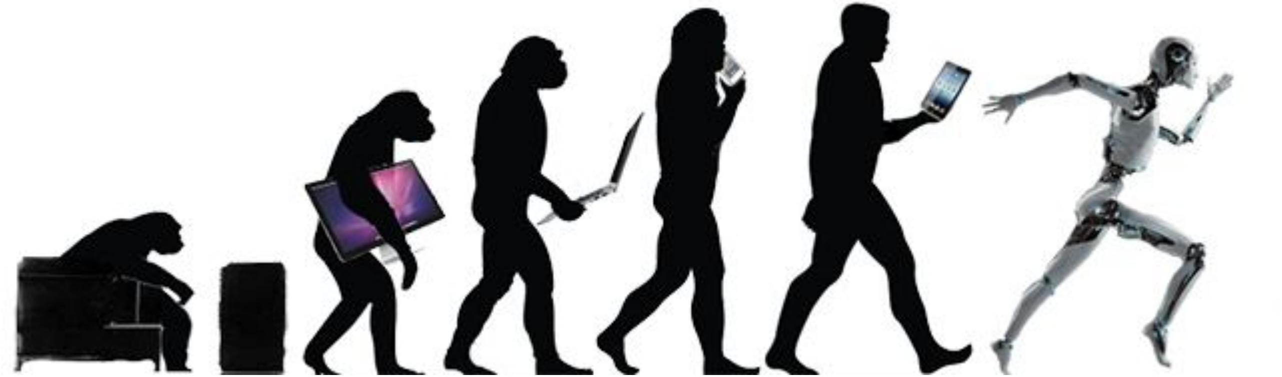


Define new hardware for Neural Network.

Software-hardware co-evolution

Deep Learning Challenge

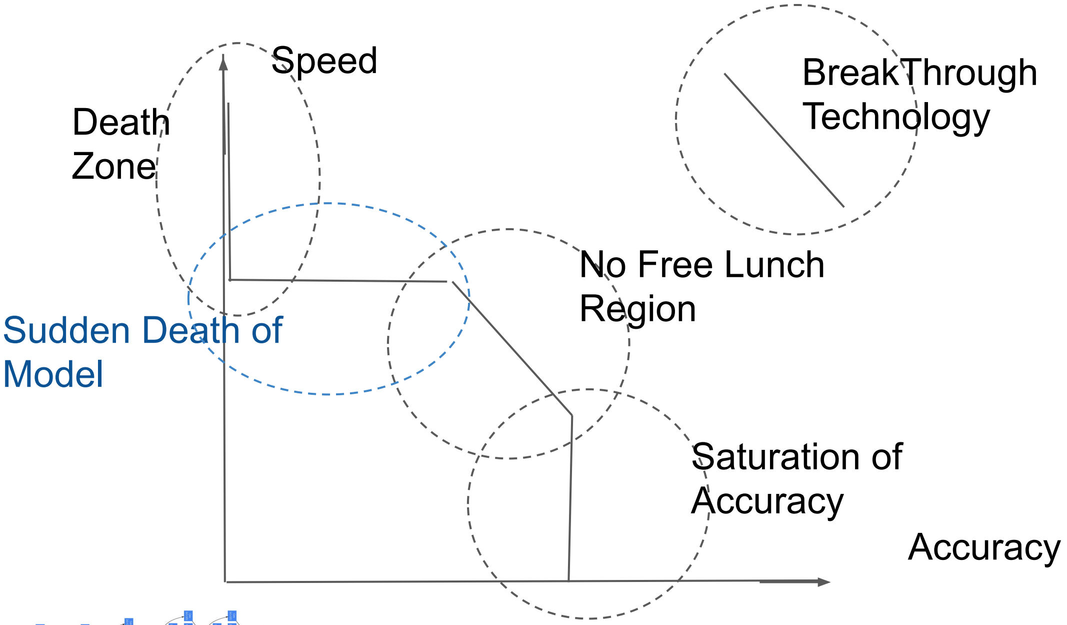
- Make it start: Conceptual Breakthrough
- Make it work: Building product
- Make it cheap: Democratize



https://medium.com/global-silicon-valley/the-evolution-of-mobile-computing-d273f23eda61

Tradeoff between Accuracy and Speed

- Breakthroughs improve both accuracy and speed
  - Factorized Convolution (GoogleNet)
  - Skip connection (ResNet)
  - Fully Convolutional Network
  - Better Loss Function
  - Batch Normalization
  - Cyclic Learning Rate



Speed

Death Zone

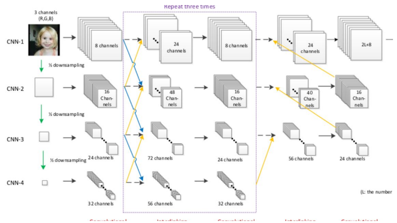
Sudden Death of Model

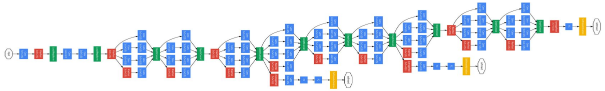
BreakThrough Technology

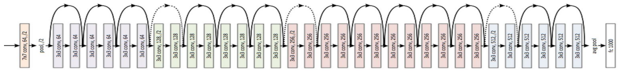
No Free Lunch Region

Saturation of Accuracy

Accuracy







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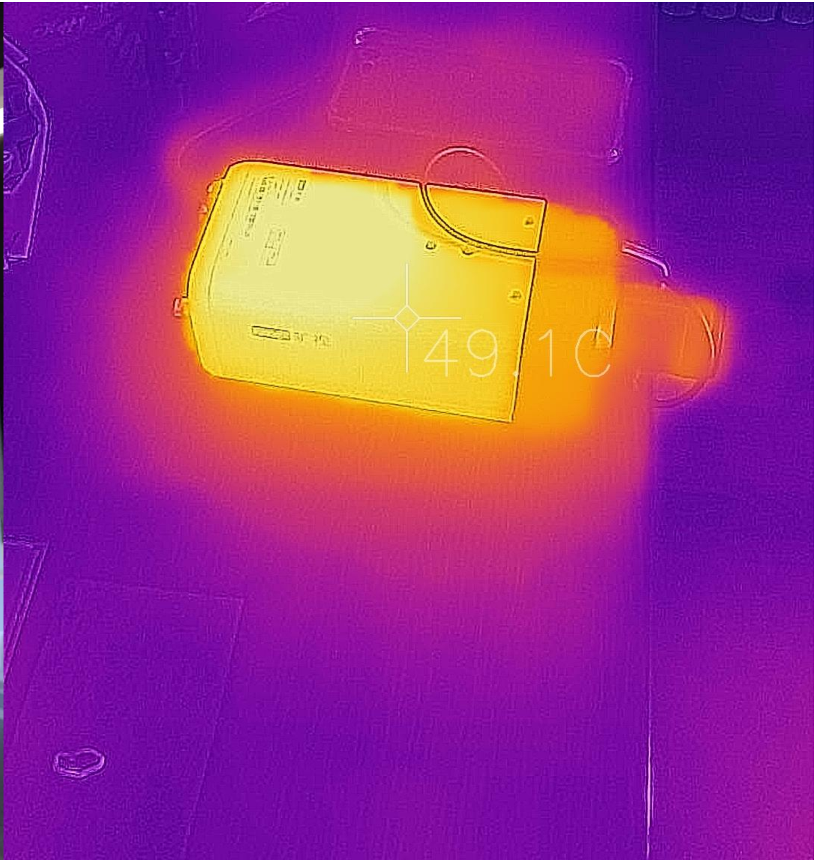
User cases: Deep Learning



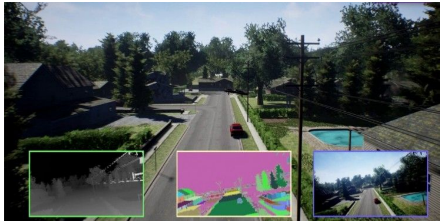
User cases: Reinforcement Learning

Characteristics: require fast & complex simulations

OpenSim

A human skeleton model for locomotive task modeling.

GTA 5
AirSim

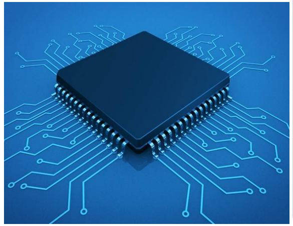


Simulation for self-driving car/ADAS and Drones.

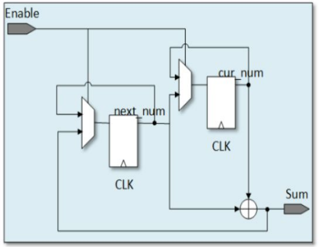
Computer Architecture answer to Deep Learning Challenge

- Make it start: Conceptual Breakthrough
    - GPU: flexible powerhouse
- Make it work: Building product
    - ISA & Programming models: Graph Compiler and Execution Engine
- Make it cheap: Democratize
    - ASIC, Edge Computing, Cloud computing: mass production of all-in-one chips

Computation Stack

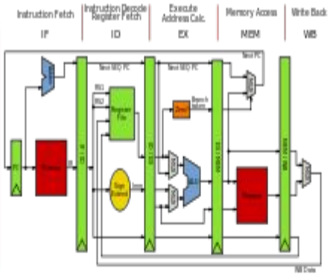


Silicon
- Partitioning & Planning
- Place & Route
- Timing Closure

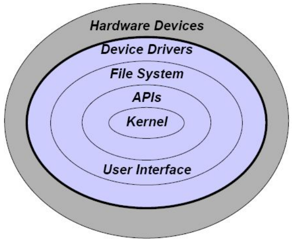


Circuit to Generate Fibonacci Series *(Fig. 13)*

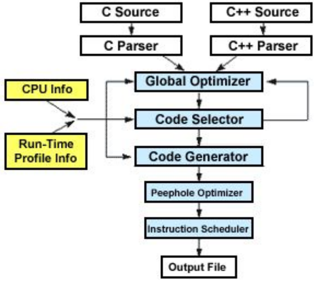
Verilog
- Karnaugh map
- Finite State Machine



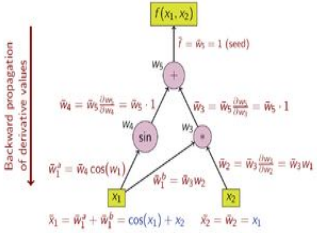
Architecture
- ISA
- Micro-code
- Resource allocation



Operating System
- Page table
- File system
- Interrupts



Compiler
- Parallelism mining
- Memory latency hiding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x_1
x_2
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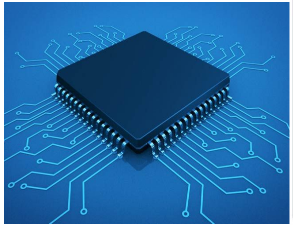
Computation Graph Engine
- Kernels
- Execution Plan

Computation Stack



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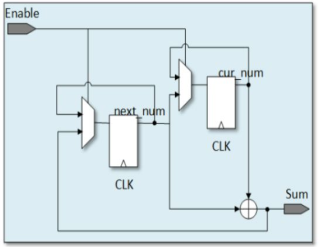

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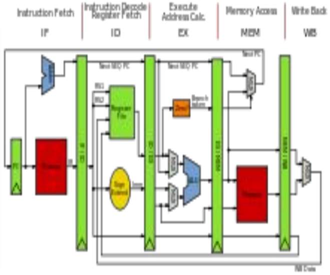

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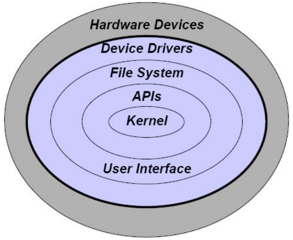

Operating System

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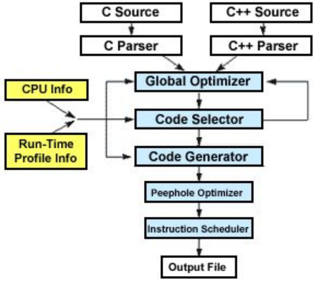

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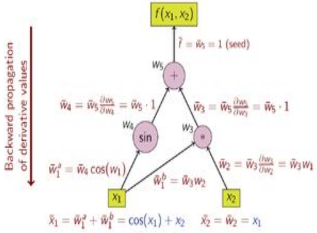
- Memory latency hiding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Backward propagation of derivative values

Computation Graph Engine

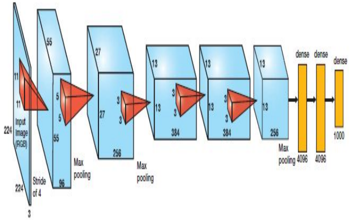
- Kernels
- Execution Plan

How will this stack deal with changes?

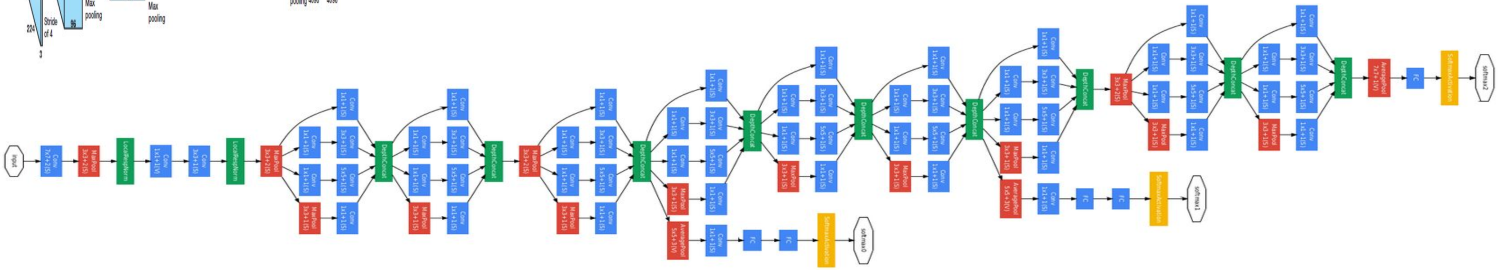
Case study: Large Neural Networks

Characteristics: many channels + side-branches + many layers

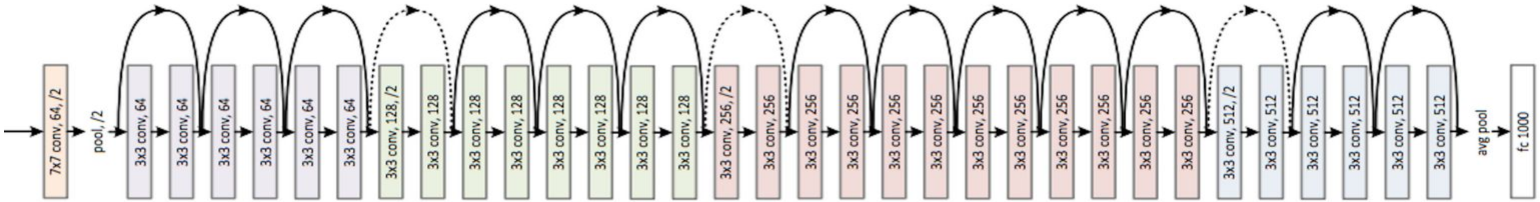
AlexNet



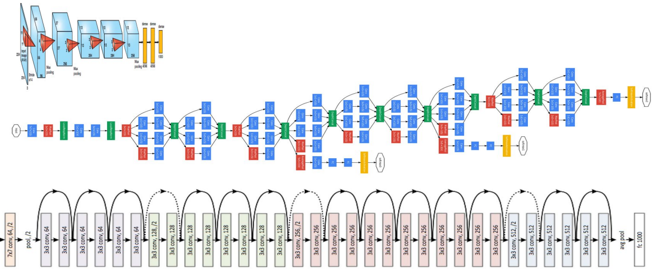
GoogLeNet



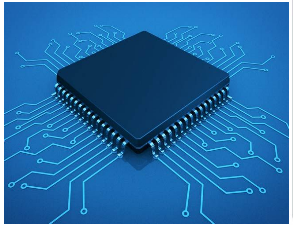
ResNet



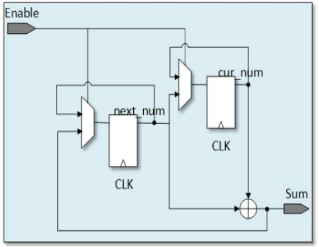
Case study: Large Neural Networks



On-Chip-Memory for caching feature maps



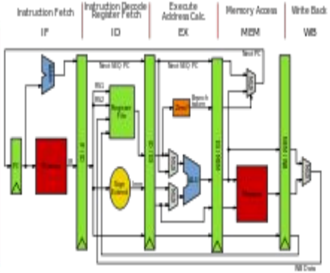
Silicon



Circuit to Generate Fibonacci Series *(Fig. 13)*

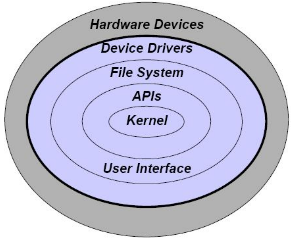
Verilog

- Instructions for convolutions & non-linearity
- Systolic Array



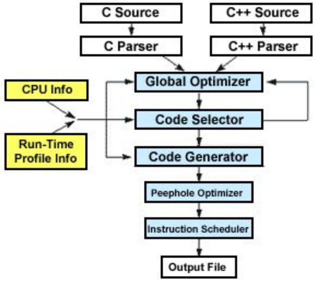
Architecture

Large page-table



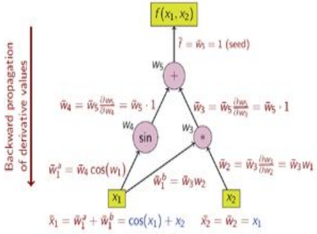
Operating System

Auto-SIMD



Compiler

Static analysis + dynamic profiling for kernel selection + execution plan

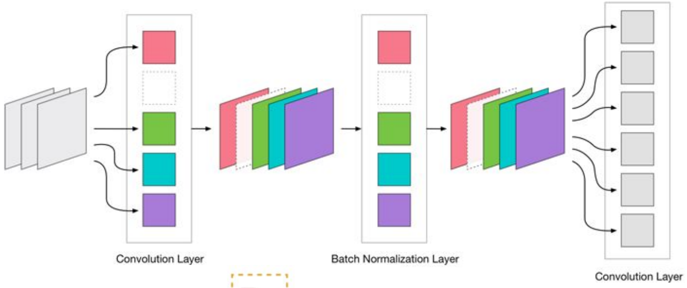


Computation Graph Engine

Case study: Small Neural Networks

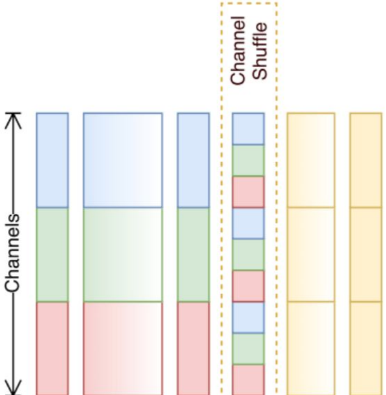
Characteristics: few channels + 1x1 convolutions

MobileNet



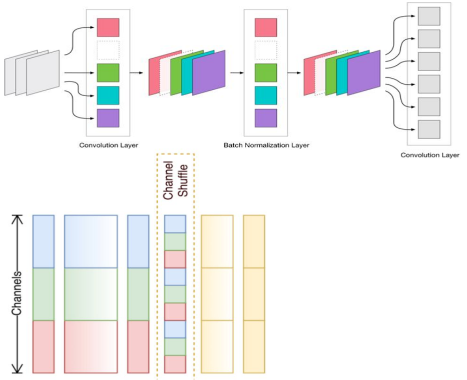
Lack of shortcut hurts its transfer learning ability.

ShuffleNet

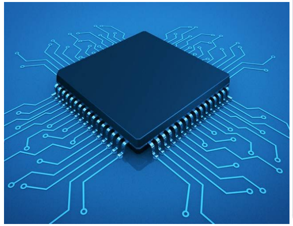


The shuffle operation is an efficient way of information mixing, but its uniqueness slows its adoption.

Case study: Small Neural Networks



On-Chip-Memory may be more important.



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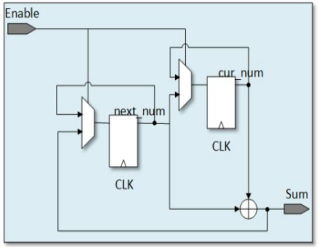
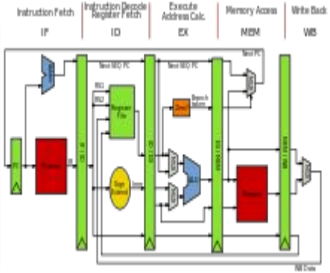


Circuit to Generate Fibonacci Series *(Fig. 13)*

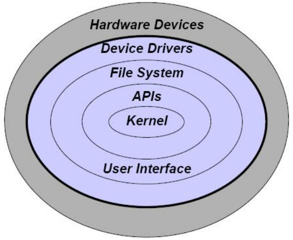
Verilog

- Specialized support for few channel layers and 1x1 convolutions.
- Different batching



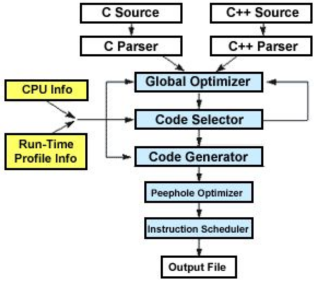
Architecture

Lower overhead



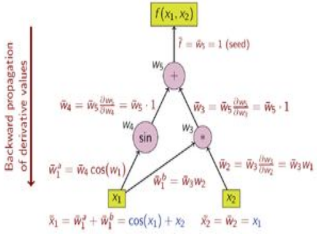
Operating System

Auto-SIMD



Compiler

Fusion of layers + handcrafted kernels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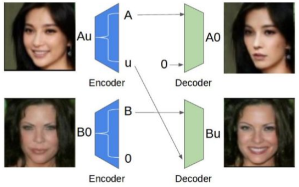
Computation Graph Engine

When a Neural Network Designers, a Computer Architect, a Compiler Expert and an OS Guru meet

- Designer wants
  - A reliable performance model
    - Open architecture design and assembly/microcode level exposure
  - Better profilers for runtime diagnostics and analyzers
  - Support for sparse matrices, dynamic operations
- Architect wants
  - Batch operations with constant delays
  - Regular memory access pattern subject to locality and many reuses
  - Streamlined memory/computation usage, no overwhelming peaks
  - Less number of operators
- Compiler Expert and OS Guru wants
  - To broker between the Designer and the Architect
    - Have a slow fallback for bizarre operators
    - Cutting peaks

IC team @ Megvii

GeneGAN



Learning2Paint

Neural Network Designer

We train our DL models and design our networks!

Computer Achitects

We build our processors and computers, from ISA to PCB!

[redacted] [redacted] [redacted]

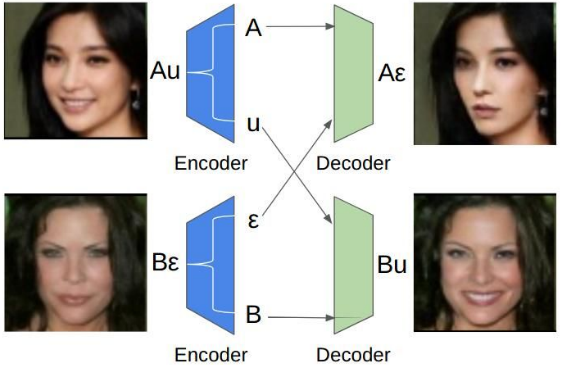
AI-product Programmers

We build our AI-products! From Javascript to Linux Kernels!

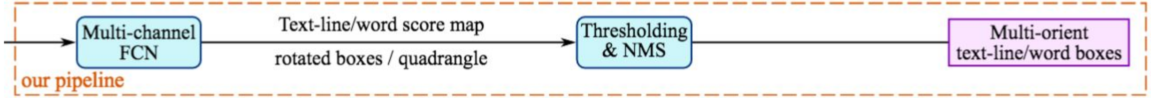
S-platform
Edge-computing platform

A-firmware
Edge Device Firmware

Neural Network Designer

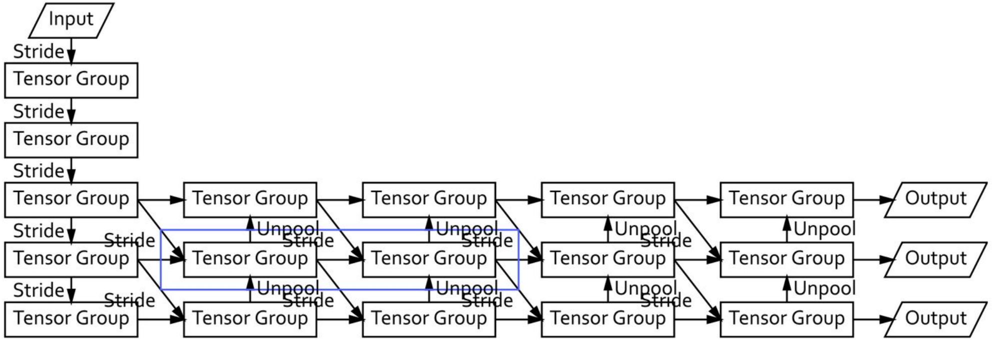


GeneGAN



EAST

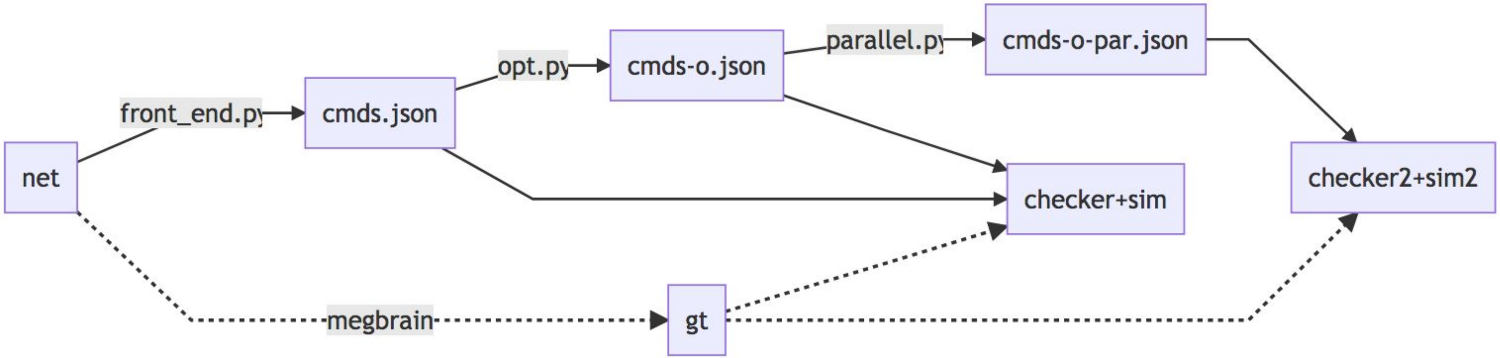
Learning2Paint



Ъ-net

Computer Architect

"X Compiler": Optimizing & Autopar Compiler

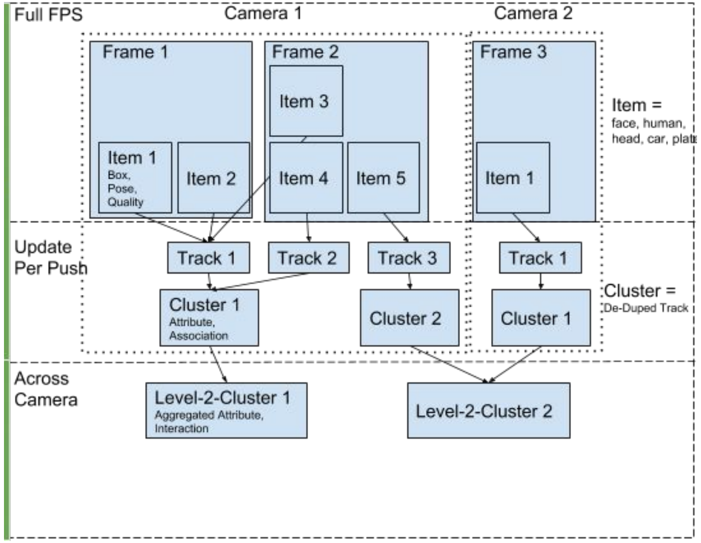


Static Scheduling

- Neural Networks are almost static
  - No branching
  - (almost always) Fixed length data: fixed input/output/intermediate size
  - Regular computation
- But there are "clouds"
  - DDR latency / bandwidth
  - Compression
  - Cache
  - Interrupts
- Dynamic Scheduling inevitable?

AI-product Programmers

S-platform: Edge-computing platform



Full FPS

Camera 1

Camera 2

Frame 1

Frame 2

Frame 3

Item 3

Item 1
Box,
Pose,
Quality

Item 2

Item 4

Item 5

Item 1

Item =
face, human,
head, car, plat

Update
Per Push

Track 1

Track 2

Track 3

Track 1

Cluster 1
Attribute,
Association

Cluster 2

Cluster 1

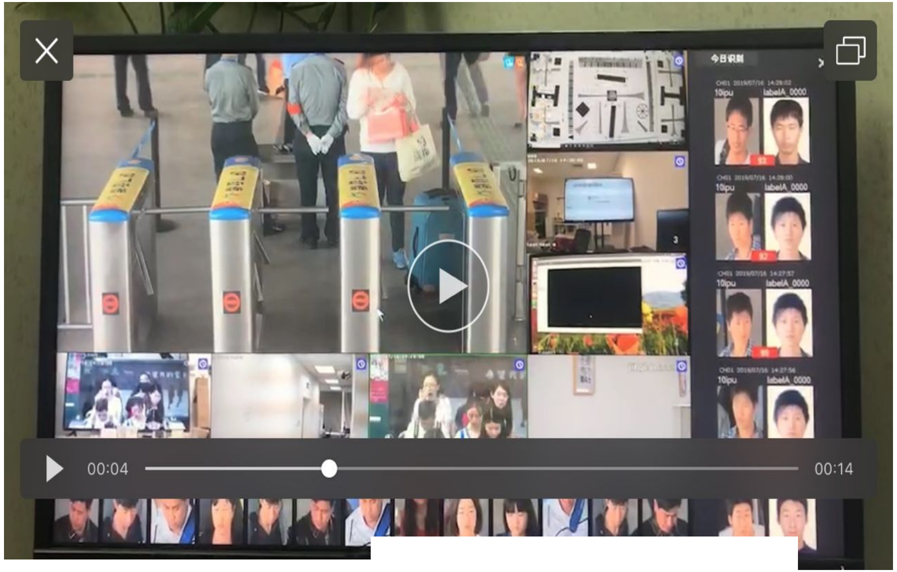
Cluster =
De-Duped Track

Across
Camera

Level-2-Cluster 1
Aggregated Attribute,
Interaction

Level-2-Cluster 2

A-firmware: Edge Device Firmware



About me

https://zsc.github.io/

● Source-to-source transformation ● Cache simulation	● Natural Language Question & Answer ● Indoor Navigation with INS ● Group Orbit Optimization	● OCR ● Quantized Neural Network ● Smart Camera ● Reinforcement Learning
Compiler Optimization	Machine Learning	Neural Network

2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019

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