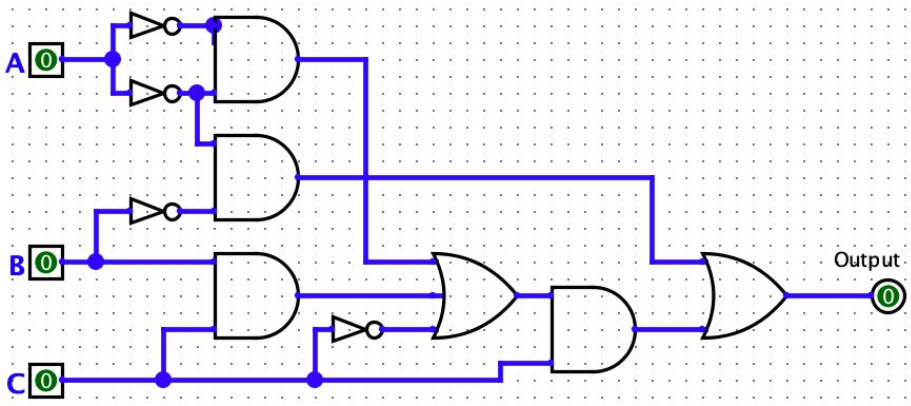
Computer Architecture Homework 4

Spring 2023, March

1 Boolean Algebra and Logic Gates

For the circuit shown below:



a. Write the Boolean Expression of the circuit and simplify it step by step (as simple as possible).(10 pts)

output = $\bar{A}\bar{B} + C(\bar{C} + BC + \bar{A}\bar{A})$

$= \bar{A}\bar{B} + C\bar{C} + BCC + \bar{A}\bar{A}C$

$= \bar{A}\bar{B} + BC + \bar{A}C$

$= \bar{A}\bar{B} + B(C + \bar{A}C(B + \bar{B}))$

$= \bar{A}\bar{B} + BC + \bar{A}BC + \bar{A}\bar{B}C$

$= \bar{A}\bar{B}(1+C) + BC(1+\bar{A})$

$= \bar{A}\bar{B} + BC$

唯一一个有变化的 $(B, \bar{B})$

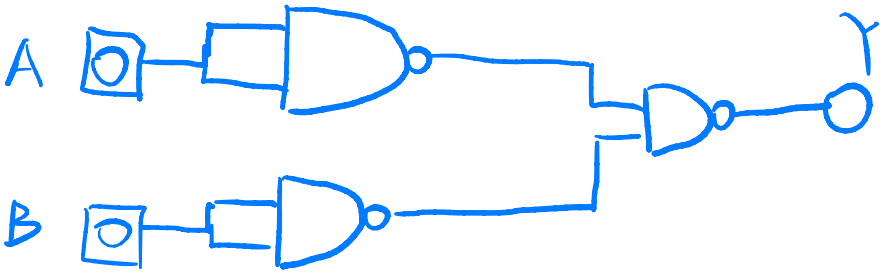
b. Write the Truth Table of the simplified Boolean Expression.(10 pts)

A	B	C	Output
1	1	1	1
1	1	0	0
1	0	1	0
1	0	0	0
0	1	1	1
0	1	0	0
0	0	1	1
0	0	0	1

c. Create a circuit of Boolean Expression Y = A + B using only NAND gates.(10 pts)

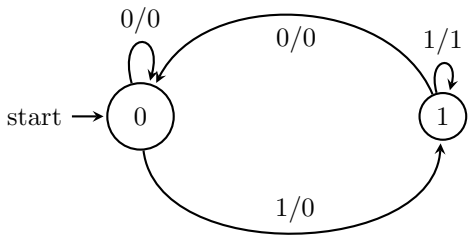
$\overline{AB} = \overline{A} + \overline{B}$ $\quad \overline{A} = \overline{AA}$

$Y = A + B = \overline{\overline{A} + \overline{B}} = \overline{\overline{A}\,\overline{B}} = \overline{\overline{AA}\;\overline{BB}}$



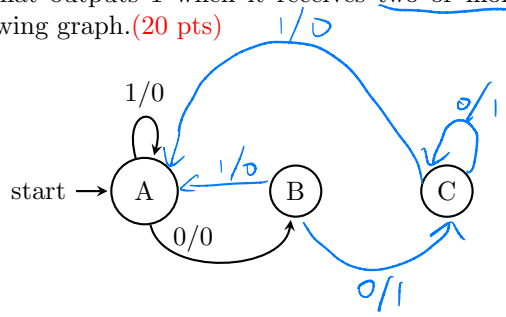
2 FSM

a.



(1) (5 pts)Start with the initial state, the FSM outputs a 1 if it detects the pattern (bitstring) : two or more successive '1'
(2) (5 pts)What would it output for the input bitstring "011001110"?
00100011 0

b. Draw a FSM that outputs 1 when it receives two or more successive '0'. Complete the following graph.(20 pts)

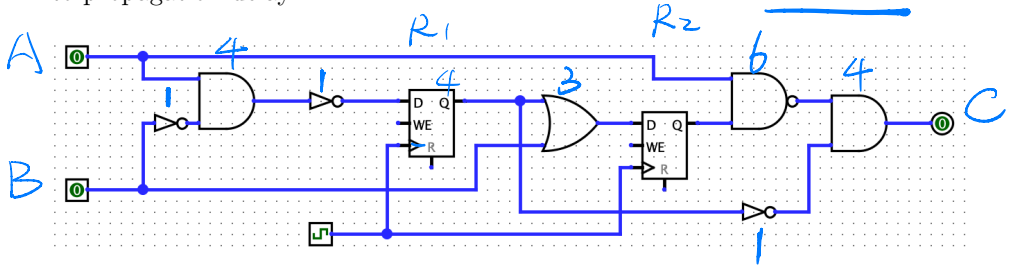


c. Fill out the remainder of the table for the FSM in (b).(10 pts)

Input	-	1	0	0	1	0	1	0	0
Next State	A	A	B	C	A	B	A	B	C
Output	-	0	0	1	0	0	0	0	1

3 SDS

In the following circuit, NOT gates have a delay of 1ns, AND gates have a delay of 4ns, NAND gates have a delay of 6ns, OR gates have a delay of 3ns. The registers have a clk-to-q delay of 4ns and setup times of 6ns. Assume the inputs comes from registers and output is connected to a register. All the delays refer to propagation delay.



a. What is the minimum acceptable clock cycle time for this circuit? What clock frequency does it correspond to? (please include enough explanation)(20 pts)

$T_{clk} \geq t_{pcq} + t_{pd} + \text{set up}$

R_1: B → NOT → AND → NOT → R_1 $\quad T_{clk} \geq 4+1+4+1+6 = 16\,ns$

R_2: B → OR → R_2 $\quad T_{clk} \geq 4+3+6 = 13\,ns$

C: R_2 → NAND → AND → C $\quad T_{clk} \geq 4+6+4+6 = 20\,ns$

$\therefore T_{clk} \geq 20\,ns$

取 $T_{clk} = 20\,ns$

$\therefore f = \frac{1}{T_{clk}} = \frac{1}{20 \times 10^{-9}} = 50\,MHz$

b. What is the maximum allowable hold time for the registers that allows this circuit run correctly? (please include enough explanation)(10 pts)

$t_{cd} \geq \text{hold time} - t_{ccq} \Rightarrow \text{hold time} \leq t_{cd} + t_{ccq}$

R_1: R_1 → OR → R_2 $\quad \text{hold time} \leq 3+4 = 7\,ns$

R_2: R_2 → NAND → AND → C $\quad \text{hold time} \leq 6+4+4 = 14\,ns$

A: A → AND → NOT → R_1 $\quad \text{hold time} \leq 4+1+4 \leq 9\,ns$

B: B → OR → R_2 $\quad \text{hold time} \leq 3+4 \leq 7\,ns$

$\therefore \text{hold time} \leq 7\,ns$

$\therefore (\text{hold time})_{max} = 7\,ns$