数字电路实验报告：实验 07 FPGA 实验平台及 IP 核使用

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实验目的

熟悉 FPGAOL 在线实验平台结构及使用

掌握 FPGA 开发各关键环节

学会使用 IP 核（知识产权核）

实验环境

VLAB 平台：vlab.ustc.edu.cn

FPGAOL 平台：fpgaol.ustc.edu.cn

Vivado

Logisim

实验过程

题目1

ROM中的初始化.coe文件内容为（为显示对应序号的数字对应需点亮的数码管号）：

```
memory_initialization_radix=2;
memory_initialization_vector=11111100 01100000 11011010 11110010 01100110
10110110 10111110 11100000 11111110 11110110 11101110 00111110 00011010
01111010 10011110 10001110;
```

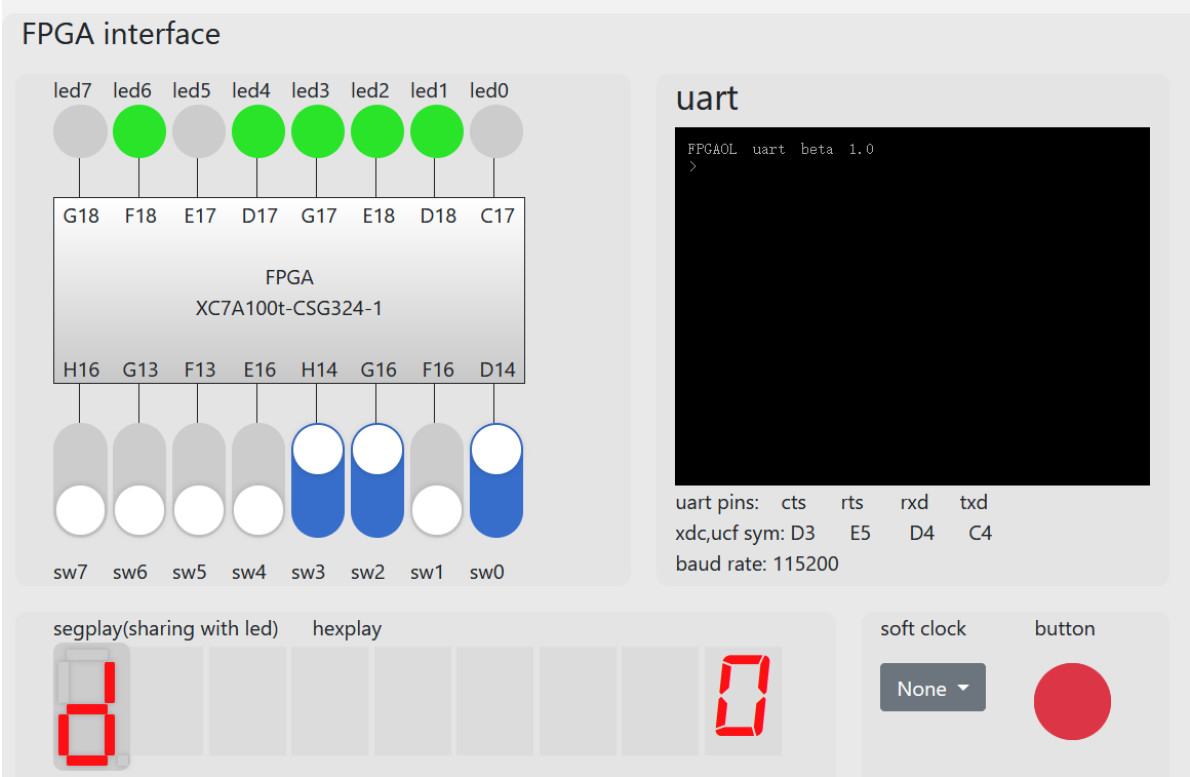
设计文件（例化调用了ip核）：

```
module week7_1(input [3:0] sw,output [7:0] out);
dist_mem_gen_0 rom(.a (sw),.spo (out));
endmodule
```

管脚约束文件：

```
# FPGAOL LED (signle-digit-SEGPLAY)

set_property -dict { PACKAGE_PIN C17   IOSTANDARD LVCMOS33 } [get_ports {
out[7] }];
set_property -dict { PACKAGE_PIN D18   IOSTANDARD LVCMOS33 } [get_ports {
out[6] }];
set_property -dict { PACKAGE_PIN E18   IOSTANDARD LVCMOS33 } [get_ports {
out[5] }];
set_property -dict { PACKAGE_PIN G17   IOSTANDARD LVCMOS33 } [get_ports {
out[4] }];
```

```
set_property -dict { PACKAGE_PIN D17   IOSTANDARD LVCMOS33 } [get_ports {
out[3] }];
set_property -dict { PACKAGE_PIN E17   IOSTANDARD LVCMOS33 } [get_ports {
out[2] }];
set_property -dict { PACKAGE_PIN F18   IOSTANDARD LVCMOS33 } [get_ports {
out[1] }];
set_property -dict { PACKAGE_PIN G18   IOSTANDARD LVCMOS33 } [get_ports {
out[0] }];


# FPGAOL SWITCH

set_property -dict { PACKAGE_PIN D14   IOSTANDARD LVCMOS33 } [get_ports {
sw[0] }];
set_property -dict { PACKAGE_PIN F16   IOSTANDARD LVCMOS33 } [get_ports {
sw[1] }];
set_property -dict { PACKAGE_PIN G16   IOSTANDARD LVCMOS33 } [get_ports {
sw[2] }];
set_property -dict { PACKAGE_PIN H14   IOSTANDARD LVCMOS33 } [get_ports {
sw[3] }];
```



题目2

设计文件为：

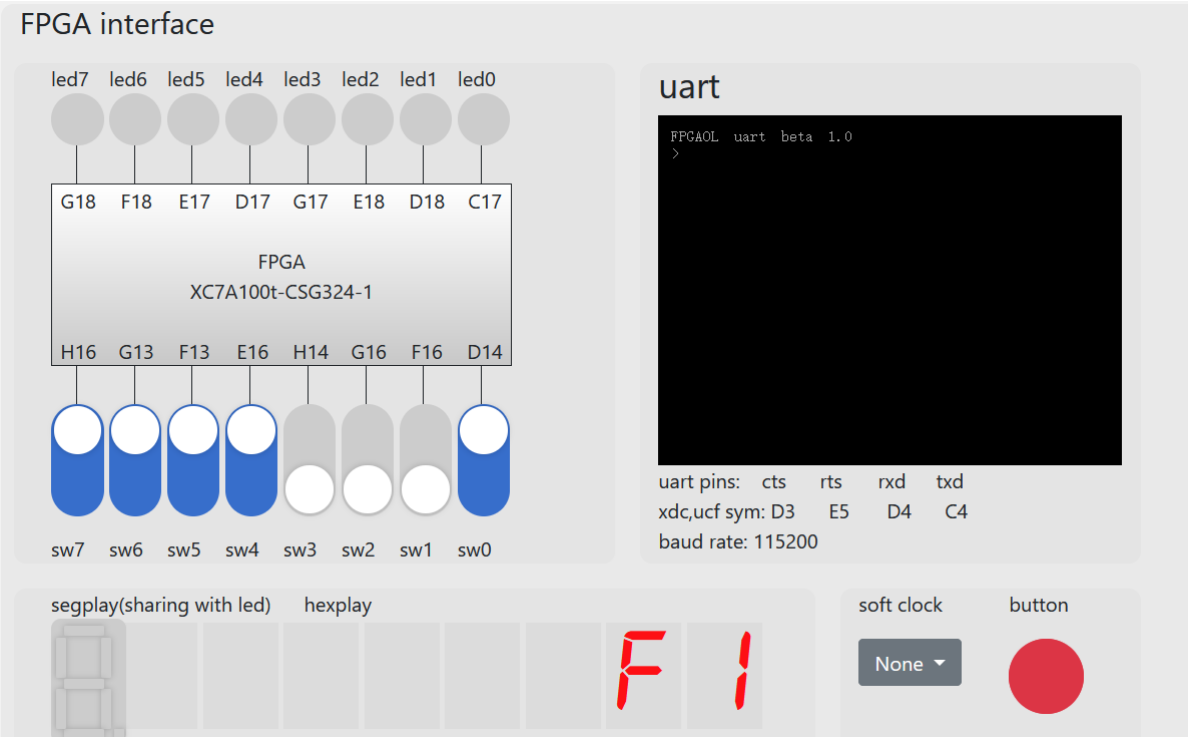
```
module week7_2(input clk,rst,[7:0] sw,output reg [3:0] d,reg [2:0] an);
wire c100hz1,c100hz2;
reg [19:0] count;
always @(posedge clk)
begin
    if (rst) count<=20'b0;
    else count <= count + 20'b1;
end
assign c100hz1 = (count == 20'b1111111111_1111111111);
```

```
assign c100hz2 = (count == 20'b0111111111_1111111111);
always @(posedge clk)
begin
    if (c100hz1)
    begin
        d<=sw[3:0];
        an<=3'b000;
    end
    if (c100hz2)
    begin
        d<=sw[7:4];
        an<=3'b001;
    end
end

endmodule
```

管脚约束文件:

```
# Clock signal
set_property -dict { PACKAGE_PIN E3    IOSTANDARD LVCMOS33 } [get_ports { clk }];

# FPGA BUTTON
set_property -dict { PACKAGE_PIN B18    IOSTANDARD LVCMOS33 } [get_ports { rst }];

# FPGAOL hex

set_property -dict { PACKAGE_PIN A14   IOSTANDARD LVCMOS33 } [get_ports { d[0] }];
set_property -dict { PACKAGE_PIN A13   IOSTANDARD LVCMOS33 } [get_ports { d[1] }];
set_property -dict { PACKAGE_PIN A16   IOSTANDARD LVCMOS33 } [get_ports { d[2] }];
set_property -dict { PACKAGE_PIN A15   IOSTANDARD LVCMOS33 } [get_ports { d[3] }];
set_property -dict { PACKAGE_PIN B17   IOSTANDARD LVCMOS33 } [get_ports { an[0] }];
set_property -dict { PACKAGE_PIN B16   IOSTANDARD LVCMOS33 } [get_ports { an[1] }];
set_property -dict { PACKAGE_PIN A18   IOSTANDARD LVCMOS33 } [get_ports { an[2] }];


# FPGAOL SWITCH

set_property -dict { PACKAGE_PIN D14   IOSTANDARD LVCMOS33 } [get_ports { sw[0] }];
set_property -dict { PACKAGE_PIN F16   IOSTANDARD LVCMOS33 } [get_ports { sw[1] }];
set_property -dict { PACKAGE_PIN G16   IOSTANDARD LVCMOS33 } [get_ports { sw[2] }];
set_property -dict { PACKAGE_PIN H14   IOSTANDARD LVCMOS33 } [get_ports { sw[3] }];
set_property -dict { PACKAGE_PIN E16   IOSTANDARD LVCMOS33 } [get_ports { sw[4] }];
```

```
set_property -dict { PACKAGE_PIN F13   IOSTANDARD LVCMOS33 } [get_ports { sw[5] }];
set_property -dict { PACKAGE_PIN G13   IOSTANDARD LVCMOS33 } [get_ports { sw[6] }];
set_property -dict { PACKAGE_PIN H16   IOSTANDARD LVCMOS33 } [get_ports { sw[7] }];
```



实验3

设计文件代码：

```
module week7_3(
input clk,
input rst,
output reg [3:0] d,
output reg [2:0] an
);
reg [3:0] s0;
reg [3:0] s1;
reg [3:0] s2;
reg [3:0] min;
reg [13:0] cnt;
reg [26:0] real_clk;
wire pulse_100hz = (cnt == 14'h1);
wire pulse_10hz = (real_clk == 27'b000101111101011110000100000);

always@(posedge clk)
begin
    real_clk <= real_clk + 17'b1;
    cnt <= cnt + 14'b1;

    if(rst)
    begin
        s0 <= 4;
        s1 <= 3;
        s2 <= 2;
```

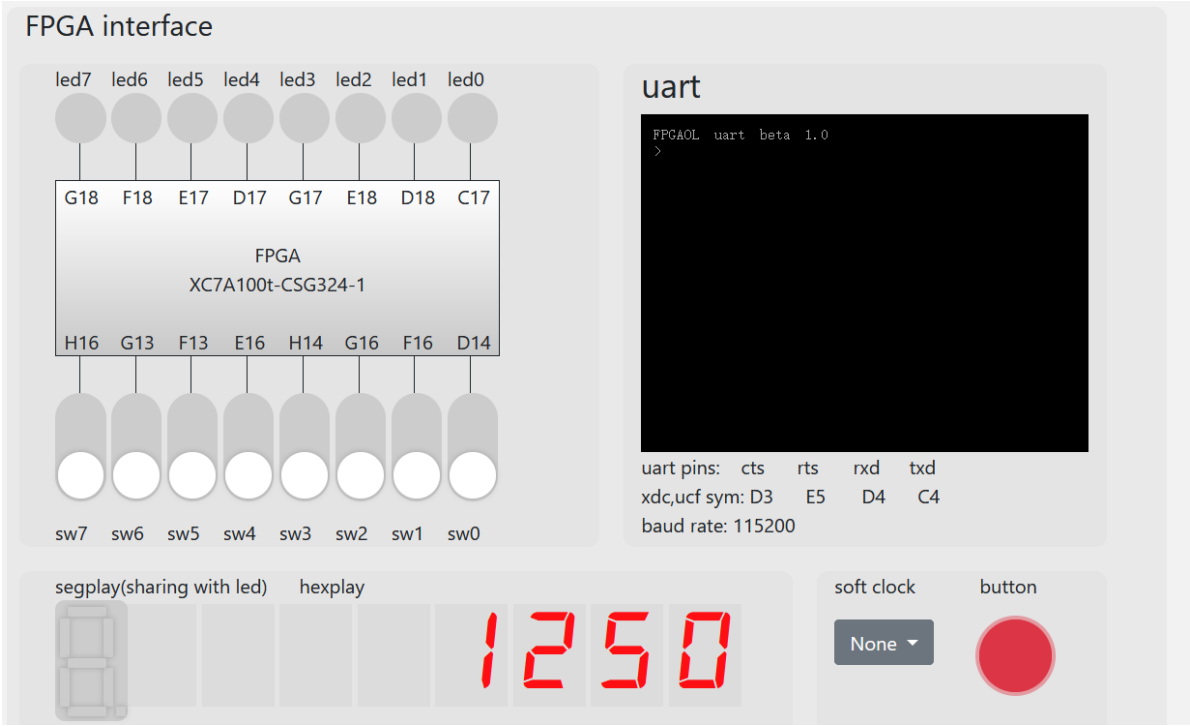
```
        min <= 1;
    end

    if (pulse_100hz)
    begin
        an[1:0] <= an[1:0]+1;
    end

    if(pulse_10hz)
    begin
        real_clk <= 0;
        s0 <= s0 + 1;

        if(s0 >= 9)
        begin
            s0 <= 0;
            s1 <= s1+1;
        end

        if(s1 >= 9)
        begin
            s1 <= 0;
            s2 <= s2+1;
        end

        if(s2 >= 5)
        begin
            s2 <= 0;
            min <= min + 1;
        end
    end

    if(pulse_100hz)
    begin
        if(an == 3'b000)
        d <= s1;
        else if(an == 3'b001)
        d <= s2;
        else if(an == 3'b010)
        d <= min;
        else if(an == 3'b011)
        d <= s0;
    end
end

endmodule
```

管脚约束文件：

```
### This file is a general .xdc for the Nexys4 DDR Rev. C
## To use it in a project:
## - uncomment the lines corresponding to used pins
## - rename the used ports (in each line, after get_ports) according to the top level signal names in the project

## Clock signal
```

```
set_property -dict { PACKAGE_PIN E3    IOSTANDARD LVCMOS33 } [get_ports { clk }]; #IO_L12P_T1_MRCC_35 Sch=clk100mhz
#create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports { clk }];


##LEDs

#set_property -dict { PACKAGE_PIN C17   IOSTANDARD LVCMOS33 } [get_ports { led[0] }]; #IO_L20N_T3_A19_15 Sch=ja[1]
#set_property -dict { PACKAGE_PIN D18   IOSTANDARD LVCMOS33 } [get_ports { led[1] }]; #IO_L21N_T3_DQS_A18_15 Sch=ja[2]
#set_property -dict { PACKAGE_PIN E18   IOSTANDARD LVCMOS33 } [get_ports { led[2] }]; #IO_L21P_T3_DQS_15 Sch=ja[3]
#set_property -dict { PACKAGE_PIN G17   IOSTANDARD LVCMOS33 } [get_ports { led[3] }]; #IO_L18N_T2_A23_15 Sch=ja[4]
#set_property -dict { PACKAGE_PIN D17   IOSTANDARD LVCMOS33 } [get_ports { led[4] }]; #IO_L16N_T2_A27_15 Sch=ja[7]
#set_property -dict { PACKAGE_PIN E17   IOSTANDARD LVCMOS33 } [get_ports { led[5] }]; #IO_L16P_T2_A28_15 Sch=ja[8]
#set_property -dict { PACKAGE_PIN F18   IOSTANDARD LVCMOS33 } [get_ports { led[6] }]; #IO_L22N_T3_A16_15 Sch=ja[9]
#set_property -dict { PACKAGE_PIN G18   IOSTANDARD LVCMOS33 } [get_ports { led[7] }]; #IO_L22P_T3_A17_15 Sch=ja[10]


##Switches

#set_property -dict { PACKAGE_PIN D14   IOSTANDARD LVCMOS33 } [get_ports { sw[0]}]; #IO_L1P_T0_AD0P_15 Sch=jb[1]
#set_property -dict { PACKAGE_PIN F16   IOSTANDARD LVCMOS33 } [get_ports { sw[1]}]; #IO_L14N_T2_SRCC_15 Sch=jb[2]
#set_property -dict { PACKAGE_PIN G16   IOSTANDARD LVCMOS33 } [get_ports { sw[2]}]; #IO_L13N_T2_MRCC_15 Sch=jb[3]
#set_property -dict { PACKAGE_PIN H14   IOSTANDARD LVCMOS33 } [get_ports { sw[3]}]; #IO_L15P_T2_DQS_15 Sch=jb[4]
#set_property -dict { PACKAGE_PIN E16   IOSTANDARD LVCMOS33 } [get_ports { sw[4]}]; #IO_L11N_T1_SRCC_15 Sch=jb[7]
#set_property -dict { PACKAGE_PIN F13   IOSTANDARD LVCMOS33 } [get_ports { sw[5]}]; #IO_L5P_T0_AD9P_15 Sch=jb[8]
#set_property -dict { PACKAGE_PIN G13   IOSTANDARD LVCMOS33 } [get_ports { sw[6]}]; #IO_0_15 Sch=jb[9]
#set_property -dict { PACKAGE_PIN H16   IOSTANDARD LVCMOS33 } [get_ports { sw[7] }]; #IO_L13P_T2_MRCC_15 Sch=jb[10]


##7-Segment Display

set_property -dict { PACKAGE_PIN A14   IOSTANDARD LVCMOS33     } [get_ports { d[0] }]; #IO_L9N_T1_DQS_AD3N_15 Sch=xa_n[1]
set_property -dict { PACKAGE_PIN A13   IOSTANDARD LVCMOS33     } [get_ports { d[1] }]; #IO_L9P_T1_DQS_AD3P_15 Sch=xa_p[1]
set_property -dict { PACKAGE_PIN A16   IOSTANDARD LVCMOS33     } [get_ports { d[2] }]; #IO_L8N_T1_AD10N_15 Sch=xa_n[2]
set_property -dict { PACKAGE_PIN A15   IOSTANDARD LVCMOS33     } [get_ports { d[3] }]; #IO_L8P_T1_AD10P_15 Sch=xa_p[2]
set_property -dict { PACKAGE_PIN B17   IOSTANDARD LVCMOS33     } [get_ports { an[0] }]; #IO_L7N_T1_AD2N_15 Sch=xa_n[3]
```

```
42 set_property -dict { PACKAGE_PIN B16   IOSTANDARD LVCMOS33     } [get_ports
   { an[1] }]; #IO_L7P_T1_AD2P_15 Sch=xa_p[3]
43 set_property -dict { PACKAGE_PIN A18   IOSTANDARD LVCMOS33     } [get_ports
   { an[2] }]; #IO_L10N_T1_AD11N_15 Sch=xa_n[4]
44
45
46 ##Buttons
47
48 set_property -dict { PACKAGE_PIN B18   IOSTANDARD LVCMOS33     } [get_ports
   { rst }]; #IO_L10P_T1_AD11P_15 Sch=xa_p[4]
```



总结与思考

1. 请总结本次实验的收获

   学会了时钟分频与ip核的使用。

2. 请评价本次实验的难易程度

   较为简单。

3. 请评价本次实验的任务量

   比较合适。

4. 请为本次实验提供改进建议

   暂无。