数字电路实验报告：实验 06 FPGA 原理及 Vivado 综合

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实验目的

了解 FPGA 工作原理

了解 Verilog 文件和约束文件在 FPGA 开发中的作用

学会使用 Vivado 进行 FPGA 开发的完整流程

实验环境

VLAB 平台： vlab.ustc.edu.cn

FPGAOL 实验平台：fpgaol.ustc.edu.cn

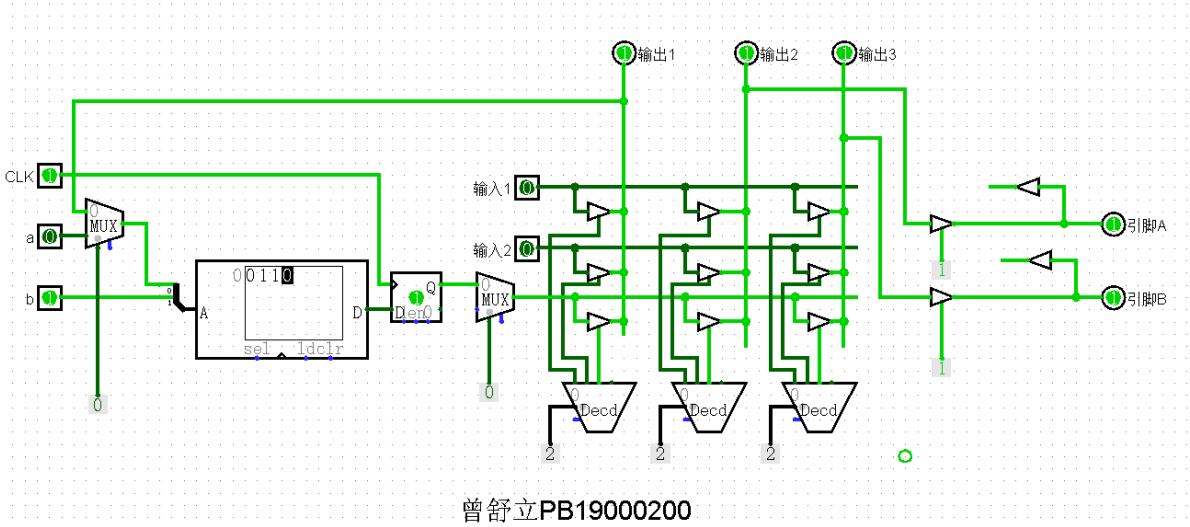
Logisim

Vivado 工具

实验过程

题目1

电路图（配置数据包括其中）如下：



题目2

将led对应引脚约束顺序反过来即可，具体xdc文件如下：

```
# This file is a general .xdc for FPGAOL_BOARD (adopted from Nexys4 DDR Rev. C)
# To use it in a project:
# - uncomment the lines corresponding to used pins
# - rename the used ports (in each line, after get_ports) according to the top level signal names in the project
```

```
5
6  # Clock signal
7  set_property -dict { PACKAGE_PIN E3    IOSTANDARD LVCMOS33 } [get_ports {
   clk }];
8
9  # FPGA BUTTON
10 set_property -dict { PACKAGE_PIN B18    IOSTANDARD LVCMOS33 } [get_ports {
   rst }];
11
12 # FPGAOL LED (signle-digit-SEGPLAY)
13
14 set_property -dict { PACKAGE_PIN C17   IOSTANDARD LVCMOS33 } [get_ports {
   led[7] }];
15 set_property -dict { PACKAGE_PIN D18   IOSTANDARD LVCMOS33 } [get_ports {
   led[6] }];
16 set_property -dict { PACKAGE_PIN E18   IOSTANDARD LVCMOS33 } [get_ports {
   led[5] }];
17 set_property -dict { PACKAGE_PIN G17   IOSTANDARD LVCMOS33 } [get_ports {
   led[4] }];
18 set_property -dict { PACKAGE_PIN D17   IOSTANDARD LVCMOS33 } [get_ports {
   led[3] }];
19 set_property -dict { PACKAGE_PIN E17   IOSTANDARD LVCMOS33 } [get_ports {
   led[2] }];
20 set_property -dict { PACKAGE_PIN F18   IOSTANDARD LVCMOS33 } [get_ports {
   led[1] }];
21 set_property -dict { PACKAGE_PIN G18   IOSTANDARD LVCMOS33 } [get_ports {
   led[0] }];
22
23
24 # FPGAOL SWITCH
25
26 set_property -dict { PACKAGE_PIN D14   IOSTANDARD LVCMOS33 } [get_ports {
   sw[0] }];
27 set_property -dict { PACKAGE_PIN F16   IOSTANDARD LVCMOS33 } [get_ports {
   sw[1] }];
28 set_property -dict { PACKAGE_PIN G16   IOSTANDARD LVCMOS33 } [get_ports {
   sw[2] }];
29 set_property -dict { PACKAGE_PIN H14   IOSTANDARD LVCMOS33 } [get_ports {
   sw[3] }];
30 set_property -dict { PACKAGE_PIN E16   IOSTANDARD LVCMOS33 } [get_ports {
   sw[4] }];
31 set_property -dict { PACKAGE_PIN F13   IOSTANDARD LVCMOS33 } [get_ports {
   sw[5] }];
32 set_property -dict { PACKAGE_PIN G13   IOSTANDARD LVCMOS33 } [get_ports {
   sw[6] }];
33 set_property -dict { PACKAGE_PIN H16   IOSTANDARD LVCMOS33 } [get_ports {
   sw[7] }];
```

实验3

30位计数器verilog代码：

```
module count30(input clk,rst,output [7:0] outled);
    reg [29:0] led;
    always @(posedge clk,posedge rst)
    begin
        if (rst == 1) led<=30'b00_0000_0000_0000_0000_0000_0000_0000;
        else led<=led + 30'b00_0000_0000_0000_0000_0000_0000_0001;
    end
    assign outled=led[29:22];
endmodule
```

32位计数器verilog代码：

```
module count32(input clk,rst,output [7:0] outled);
    reg [31:0] led;
    always @(posedge clk,posedge rst)
    begin
        if (rst == 1) led<=32'b0000_0000_0000_0000_0000_0000_0000_0000;
        else led<=led + 32'b0000_0000_0000_0000_0000_0000_0000_0001;
    end
    assign outled=led[31:24];
endmodule
```

xdc文件（两者通用）：

```
# This file is a general .xdc for FPGAOL_BOARD (adopted from Nexys4 DDR Rev. C)
# To use it in a project:
# - uncomment the lines corresponding to used pins
# - rename the used ports (in each line, after get_ports) according to the top level signal names in the project

# Clock signal
set_property -dict { PACKAGE_PIN E3    IOSTANDARD LVCMOS33 } [get_ports { clk }];


# FPGAOL LED (signle-digit-SEGPLAY)
set_property -dict { PACKAGE_PIN C17   IOSTANDARD LVCMOS33 } [get_ports { outled[0] }];
set_property -dict { PACKAGE_PIN D18   IOSTANDARD LVCMOS33 } [get_ports { outled[1] }];
set_property -dict { PACKAGE_PIN E18   IOSTANDARD LVCMOS33 } [get_ports { outled[2] }];
set_property -dict { PACKAGE_PIN G17   IOSTANDARD LVCMOS33 } [get_ports { outled[3] }];
set_property -dict { PACKAGE_PIN D17   IOSTANDARD LVCMOS33 } [get_ports { outled[4] }];
set_property -dict { PACKAGE_PIN E17   IOSTANDARD LVCMOS33 } [get_ports { outled[5] }];
set_property -dict { PACKAGE_PIN F18   IOSTANDARD LVCMOS33 } [get_ports { outled[6] }];
set_property -dict { PACKAGE_PIN G18   IOSTANDARD LVCMOS33 } [get_ports { outled[7] }];

# FPGAOL SWITCH
```

```
21 set_property -dict { PACKAGE_PIN D14   IOSTANDARD LVCMOS33 } [get_ports {
   rst }];
```

时钟信号起到了每个周期进行加一的作用，可以显著看到32位计数器led跳动速度比30位慢，因为32位的高8位对应数字大小比30位的大，需要更多时间来引起改变。

总结与思考

1. 请总结本次实验的收获

   了解了FPGA的原理，学会了vivado综合。

2. 请评价本次实验的难易程度

   较为简单。

3. 请评价本次实验的任务量

   比较合适。

4. 请为本次实验提供改进建议

   暂无。