# Shiqi Zhang

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## Education

**Shanghai Jiao Tong University** Shanghai, China

*Bachelor of Computer Science* *Sep. 2022 – Present*

- Member of ACM Honor Class, an elite CS program for highly capable students

## Research

**BCMI (Brain-Computer and Machine Intelligence) Lab** *Shanghai Jiao Tong University*

Undergraduate Researcher, advised by Professor Hai Zhao *Jun. 2024 – Present*

Research Interests

I am particularly interested in developing AI systems that can think and act more like humans. While my primary focus is on large language models, I am also exploring a broader range of topics in artificial intelligence.

## Publications[1]

**Plan-over-Graph: Structured Parallel Task Planning for Large Language Models** [link] *Submitted to ACL 2025*

***Shiqi Zhang****, Xinbei Ma*, Zouying Cao, Zhuosheng Zhang, Hai Zhao*

- We propose a novel *plan-over-graph* paradigm that guides large language models to generate parallel execution plans by decomposing complex textual tasks into executable subtasks and constructing abstract task graphs, combined with automated synthetic graph generation and a two-stage training strategy, significantly improving model performance on complex tasks while achieving globally efficient parallel scheduling.

## Selected Projects

**Liquid Physics Understanding**

*Course Project in Computer Vision (2024-2025-1)-AI3604*

- Developing a benchmark dataset to evaluate multimodal models' understanding of liquid physical properties (density, viscosity, surface tension, etc.).
- Focus on collecting realistic liquid pictures data and create a comprehensive test suite for model evaluation.
- Expected completion: 03/2025.

**RISC-V CPU Implementation via Verilog RTL**

*Course Project in Computer Architecture (2023-2024-1)-CS2951*

- Designed and implemented a single-core, single-thread RV32I CPU in Verilog RTL.
- Optimized Reservation Station (RS) latency by using combinational logic, reducing the cycle time from 4 to 2.
- Successfully simulated and executed basic RISC-V instructions, could run on a Xilinx FPGA board.
- [GitHub](https://github.com/zsq259/RISC-V-CPU)

**Compiler for Mx* Language**

*Course Project in Advanced Compiler Course (2023-2024-1)-CS2966*

- Developed a compiler from Mx* language (a variant of C++) to RV32I assembly, implemented in *C++* using LLVM.
- Key features: Register Allocation (Graph Coloring), Mem2Reg, Constant Propagation, and other optimizations.
- [GitHub](https://github.com/zsq259/MxCompiler)

[1] * denotes equal contribution.

## Teaching Experience

**Principles and Practice of Computer Algorithms** (2023-2024-3) - CS1952 - *Teaching Assistant* *Jul. 2024 – Aug. 2024*

- Led AI-focused student projects, adapted a UC Berkeley course project for hands-on algorithm design.
- Provided guidance on problem-solving and project implementation.

**Data Structures** (2023-2024-2) - CS1951 - *Teaching Assistant* *Feb. 2024 – Jun. 2024*

- Designed assignments and prepared exam questions focused on core data structures.

**Computer Programming** (2023-2024-1) - CS1953 - *Teaching Assistant* *Sep. 2023 – Jan. 2024*

- Designed a major assignment and created a large-scale engineering problem for the final exam.

## Selected Awards

**Zhiyuan Honorary Scholarship** (2022-2024)

- Zhiyuan College, top 10% in SJTU