MIPS® 4K™ / 5K™ Cache Configuration Application Note

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2 Preface

This application note describes how software is able to change cache and TLB configuration on the 4K™, 4KE™, 4KS™, and 5K™ processor family cores through manipulation of some otherwise read-only bits in the CP0 *Config* and *Config1* registers. The features that can be modified are the MMU type field in the *Config* Register, and the cache configuration bits in the *Config1* Register. The ability to change these features in software enables evaluation and benchmarking of a Fixed Mapping Translation based MMU vs. a TLB-based MMU, as well as the effect of different caches sizes and organizations below the configuration implemented in hardware. This feature could also be used for test purposes and as a part of system-bringup during an early development phase.

NOTE: The features described in this application note are present specifically to support configuration testing and evaluation of cache and memory management options, and are not supported in any other environment. Any attempt to use these features outside of this scope is a violation of the MIPS Architecture, and may cause UNDEFINED behavior of the processor.

The software-configurable features of the 4K, 4KE, 4KS and 5K processors are almost identical. However, minor differences exist. The MMU type configurability is not available on versions of the 4K processor prior to revision 2.0 and the 4KS processor but is available on all versions of the 4KE and 5K processors

3 Software-configurable Features of the *Config* and *Config1* Registers

3.1 *Config* Register

Table 1 shows the fields in the *Config* register relevant to the software-configurable features of the caches and the TLB.

- WC (bit 19): This bit is a write enable for the software-configurable features within the *Config* and *Config1* Registers. It can be written to either 1 or 0, but is initialized to 0. When this field is set to 1, the MT field of the *Config* register (not all revisions of the 4K processor) and the cache configuration fields of the *Config1* register become writeable. See note in Section 2, "Preface" on page 4 for the restrictions on the use of this field.
- MT (bits 9:7): This field becomes writeable on revision 2.0 and higher of the 4K processor and all versions of the 4KE, and 5K processors when the WC bit is set. If the core implements a standard TLB, the MMU type can be changed to standard Fixed Mapping MMU. If the core does not implement a standard TLB, the MMU type can only be a Fixed Mapping MMU. For a MTC0 which change the value of MT to be effective, the WC bit must be set before the MTC0 is executed and the new value written by the MTC0 must also have the WC bit set. Only the TLB based MMU is defined for the 4KS processor. The operation of this processor becomes UNDEFINED if software tries to change the MT field on this processor. See note in Section 2, "Preface" on page 4 for the restrictions on software that changes this field.
- AT (14:13): This field changes to reflect the contents of the MT field on the 5K processor. If the MMU type is set to Fixed Mapping MMU, AT will indicate MIPS64 with 32-bit addresses only on the 5K processor while a TLB based MMU corresponds to MIPS64 with 32/64-bit addresses. On the 4K, 4KE, and 4KS processors, this field will always indicate a MIPS32 processor regardless of MMU type. See note in Section 2, "Preface" on page 4 for the restrictions on software that changes this field.

Table 1 *Config* Register Field Descriptions

Fields		Description	Read/Write		Reset State
Name	Bit(s)		*Config*WC =0	*Config*WC =1	
WC	19	Write Control. Enable write control of cache size and special function bits in the Config1 register. 0: Write control disabled 1: Write control enabled See note in Section 2, "Preface" on page 4 for the restrictions on the use of this field.	R/W		0
AT	14:13	Architecture Type. Indicates the architecture type implemented by the processor. 0: MIPS32 (all versions of the 4K, 4KE, and 4KS processors) 1: MIPS64 with 32-bit address only (5K only) 2: MIPS64 with 32/64-bit addresses (5K only) On the 5K processor, the value 1 is used when the MMU type is a Fixed Mapping MMU and the value 2 is used when the MMU type is TLB. See note in Section 2, "Preface" on page 4 for the restrictions on software that changes this field.	R		4K, 4KE, and 4KS: 0 5K: Reflects hardware configuration

Table 1 *Config* Register Field Descriptions (Continued)

Fields		Description	Read/Write		Reset State
Name	Bit(s)		*Config*WC =0	*Config*WC =1	
MT	9:7	MMU Type. Specifies the type of MMU implemented. 1: Standard TLB 3: Standard Fixed Mapping (not the 4KS processor) See note in Section 2, "Preface" on page 4 for the restrictions on software that changes this field.	R	R/W	Reflects hardware configuration

3.2 *Config1* Register

Table 2 shows the fields in the *Config1* register relevant to cache configuration.

Here is an overview of the modified fields in this register: The instruction cache configuration fields (IS, IL and IA) and the data cache configuration fields (DS, DL and DA) which are otherwise read-only become writeable when the WC bit in the *Config* register is set. Note that only certain values for these fields are legal, while other encodings are reserved or exceed the available hardware configuration and will cause UNDEFINED behavior of the processor. No hardware checks exist to ensure that software does not write a cache configuration which exceeds the hardware configuration. Note that the TLB size can not be changed by software. See note in Section 2, "Preface" on page 4 for the restrictions on software that changes these fields.

Table 2 *Config1* Register Field Descriptions

<table>
<tr><th colspan="2">Fields</th><th rowspan="2">Description</th><th colspan="2">Read/Write</th><th rowspan="2">Reset State</th></tr>
<tr><th>Name</th><th>Bit(s)</th><th>ConfigWC =0</th><th>ConfigWC =1</th></tr>
<tr><td>IS</td><td>24:22</td><td>This field contains the number of instruction cache sets per way. Three options are available in both cores. All others values are reserved:
<table><tr><th></th><th>4K</th><th>4KE</th><th>4KS</th><th>5K</th></tr><tr><td>0</td><td colspan="3">64</td><td>N/A</td></tr><tr><td>1</td><td colspan="4">128</td></tr><tr><td>2</td><td colspan="4">256</td></tr><tr><td>3</td><td>N/A</td><td colspan="3">512</td></tr><tr><td>4</td><td>N/A</td><td colspan="2">1024</td><td>N/A</td></tr></table>All other values are reserved. See note in Section 2, "Preface" on page 4 for the restrictions on software that changes this field.</td><td rowspan="3">R</td><td rowspan="3">R/W</td><td rowspan="3">Reflects hardware configuration</td></tr>
<tr><td>IL</td><td>21:19</td><td>This field contains the instruction cache line size. If an instruction cache is present, it must contain a fixed line size of 16 bytes.
<table><tr><th></th><th>4K</th><th>4KE</th><th>4KS</th><th>5K</th></tr><tr><td>0</td><td colspan="4">No Icache present</td></tr><tr><td>3</td><td colspan="3">16 bytes</td><td>N/A</td></tr><tr><td>4</td><td colspan="3">N/A</td><td>32 bytes</td></tr></table>All other values are reserved. See note in Section 2, "Preface" on page 4 for the restrictions on software that changes this field.</td></tr>
<tr><td>IA</td><td>18:16</td><td>This field contains the level of instruction cache associativity.
<table><tr><th></th><th>4K</th><th>4KE</th><th>4KS</th><th>5K</th></tr><tr><td>0</td><td colspan="4">Direct mapped</td></tr><tr><td>1</td><td colspan="4">2-way</td></tr><tr><td>2</td><td colspan="4">3-way</td></tr><tr><td>3</td><td colspan="4">4-way</td></tr></table>All other values are reserved. See note in Section 2, "Preface" on page 4 for the restrictions on software that changes this field.</td></tr>
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Table 2 *Config1* Register Field Descriptions

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<tr><th colspan="2">Fields</th><th rowspan="2">Description</th><th colspan="2">Read/Write</th><th rowspan="2">Reset State</th></tr>
<tr><th>Name</th><th>Bit(s)</th><th>ConfigWC =0</th><th>ConfigWC =1</th></tr>
<tr><td>DS</td><td>15:13</td><td>This field contains the number of data cache sets per way:
<table><tr><th></th><th>4K</th><th>4KE</th><th>4KS</th><th>5K</th></tr><tr><td>0</td><td colspan="3">64</td><td>N/A</td></tr><tr><td>1</td><td colspan="4">128</td></tr><tr><td>2</td><td colspan="4">256</td></tr><tr><td>3</td><td>N/A</td><td colspan="3">512</td></tr><tr><td>4</td><td>N/A</td><td colspan="2">1024</td><td>N/A</td></tr></table>All other values are reserved. See note in Section 2, "Preface" on page 4 for the restrictions on software that changes this field.</td><td></td><td></td><td></td></tr>
<tr><td>DL</td><td>12:10</td><td>This field contains the data cache line size. If a data cache is present, it must contain a line size of 16 bytes.
<table><tr><th></th><th>4K</th><th>4KE</th><th>4KS</th><th>5K</th></tr><tr><td>0</td><td colspan="4">No Dcache present</td></tr><tr><td>3</td><td colspan="3">16 bytes</td><td>N/A</td></tr><tr><td>4</td><td colspan="3">N/A</td><td>32 bytes</td></tr></table>All other values are reserved. See note in Section 2, "Preface" on page 4 for the restrictions on software that changes this field.</td><td>R</td><td>R/W</td><td>Reflects hardware configuration</td></tr>
<tr><td>DA</td><td>9:7</td><td>This field contains the type of set associativity for the data cache.
<table><tr><th></th><th>4K</th><th>4KE</th><th>4KS</th><th>5K</th></tr><tr><td>0</td><td colspan="4">Direct mapped</td></tr><tr><td>1</td><td colspan="4">2-way</td></tr><tr><td>2</td><td colspan="4">3-way</td></tr><tr><td>3</td><td colspan="4">4-way</td></tr></table>All other values are reserved. See note in Section 2, "Preface" on page 4 for the restrictions on software that changes this field.</td><td></td><td></td><td></td></tr>
</table>

3.3 MT configuration in the *Config* register

On the 4K (not all revisions), 4KE, and 5K processors, the MT field in the *Config* Register can be written so that a processor implementing a TLB-based MMU can be configured to mimic a Fixed Mapping MMU. On the 4K (not all revisions) and 4KE processors, the MMU type can also be set to TLB if no TLB is implemented in hardware, but the behavior of the processor will be UNDEFINED in this case. The 5K processor family does not allow software to set the MMU type to TLB if no TLB is implemented.

Here is the sequence which must be used to accomplish a change in the MT field. This sequence should be executed in unmapped space to avoid UNDEFINED behavior.

1. MTC0 instruction to set WC field in the *Config* register.
2. An additional MTC0 instruction to write the MT field to its desired value (the WC field must remain set).
3. If changing the MT field to select the Fixed Mapping MMU, then one or more additional MTC0 instructions are required to write the KU and K23 fields to desired values to control the cacheability of those regions. On a 4K processor, the KU and K23 fields can only be written when the MT value is 3. On a 5K processor these fields can be written regardless of the value of the MT field. Therefore, it is also possible to combine steps 2 and 3 on a 5K processor.

3.4 Cache Configuration in *Config1*

The cache configuration bits in the *Config1* Register can be written to modify the default cache size and organization.

Here is the sequence which must be used to accomplish a change in the cache configuration bits. This sequence should be executed in uncacheable space to avoid unpredictable behavior.

1. MTC0 instruction to set WC field in *Config*.
2. One or more additional MTC0 instructions to write the instruction and data cache configuration bits in *Config1* to their desired values.

Here are some additional considerations to keep in mind:

- Obviously, you should not select a larger cache size or organization than the largest size present on the processor.
- The instruction and data caches can be configured independently.
- It is possible to disable a cache by setting the line size field (IL or DL) to zero.
- Only certain values for the cache configuration fields are legal for a given processor core, as partly shown in Table 2. The values available in a specific implementation can be determined by software by reading the reset value of the *Config1* register.
- If you downsize or disable a cache, only new line allocations are disabled. Fetches, loads and stores to “old” entries will still hit, even if they are in that part of the cache which has been downsized. If you do not desire this behavior, then you should initialize all the tag entries for the maximum cache configuration to be invalid before you select your new cache configuration.

4 References

1. MIPS32 4K™ Processor Core Family Software User's Manual
   Document no: MD00016
   MIPS Technologies, Inc.

2. MIPS32 4KE™ Processor Core Family Software User's Manual
   Document no: MD00103
   MIPS Technologies, Inc.

3. MIPS32 4KS™ Processor Core Family Software User's Manual
   Document no: MD00105
   MIPS Technologies, Inc.

4. MIPS64 5K™ Processor Core Family Software User's Manual
   Document no: MD00012
   MIPS Technologies, Inc.

5 Revision history

Rev. Number	Date	Comments
01.00	Nov. 17, 2001	Initial Release.