EECE2412— INTRODUCTION TO ELECTRONICS— Spring 2016

Syllabus

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OFFICE HOURS:	Wed. 1–2 and Fri 11–12 Feel free to email questions as well.

TEXT:	Hambley, Allan R. *Electronics*, Second Edition, Prentice–Hall.

OTHER RESOURCES:	For PSPICE, you can download a student version from http://www.electronics-lab.com/downloads/schematic/013/ There will be some use of Matlab or other software for calculations. I recommend Matlab, but I don't insist on it. I will put pointers to other resources on the class website.

LOCATION:	309KA

12140syl:2 — 29 December 2015

TIME:	Mon, Wed, Thu, 4:35 — 5:40 PM

LAB:	As scheduled, in 9HA EECE2413, Electronics Lab. This lab must be taken simultaneously since the material in the lab supplements the lecture. Note that students from the two lectures sections are intermixed in the labs.

READING:	Reading is to be done before the start of the week. When I lecture, I will assume that you have read the related material.

COURSE DESCRIPTION:	In this course you will learn about four types of electronic devices: op–amps, diodes, bipolar junction transistors (BJTs), and metal-oxide-semiconductor field effect transistors (MOSFETs). You will learn how to design and analyze useful electronic circuits (such as amplifiers and logic circuits) using these components.

GRADING:	20 % on homework (Equal weight on best $n-1$ of n assignments where $n \approx 10$) 40 % on 2 mid–term exams 40 % on final exam. Please discuss questions regarding homework grading first with the TA and then with the instructor. Discuss questions regarding exam grading with the instructor.

HOMEWORK:	Homework is typically given on Thursday and due at the beginning of class the following Thursday. Working together is acceptable, and even encouraged, on homework, BUT the work that you submit must be your own (no copies of the group's solution!) If you are working with a group, make certain you understand every part of your solution. Late homework will incur a penalty of 10 points out of 100 until solutions are posted. After that, late homework will not be graded and will be scored as a zero in the gradebook.

ETHICAL BEHAVIOR:	Collaboration on homework is allowed. However each student must submit his or her own work (No copying of a group solution).

SPECIAL NEEDS:	The University will make reasonable accommodations for persons with documented disabilities. Students should notify the Disability Resource Center located in 20 Dodge Hall and their instructors of any special needs. Instructors should be notified the first day of classes.

Tentative Schedule

1	11,13,14 Jan	Administrivia. Schedule. Expectations. Syllabus. Introduction. Course overview. Review of Circuits Properties and uses of controlled sources **Reading:** Sections 1.4 to 1.8.

21 Jan — MLK Holiday: No class

2	20, 21 Jan	Op–Amps: Basic Applications. **Reading:** Sections 1.9 to 1.11, 2.1 to 2.5.

3	25, 27, 28 Jan	Amplifier Circuits: Applications. Deviations from Ideal in Op–Amps. **Reading:** Sections 2.6 to 2.11. **Lab:** 1 (Op Amps) Parts 1-2: 26 or 29 Jan.

4	1,3, 4 Feb	Diodes: Characteristics, modeling, and applications. **Reading:** Sections 3.1 to 3.6 and 3.12. **Lab:** 1 (Op. Amps) Part 3: 2 or 5 Feb.

5	8, 10, 11 Feb	Diode Circuits. Physical operation of the junction diode. **Reading:** Sections 3.7 to 3.11. **Lab:** 2a (Diode Circuits): 9 or 12 Feb.

15 Feb — Presidents' Holiday: No class

6	17 Feb	Review Day

	18 Feb	Exam 1

7	22, 24, 25 Feb	Introduction to the biopolar junction transistor (BJT): Physics of operation and circuit models **Reading:** Sections 4.1 through 4.4. **Lab:** 2b (Diode Circuits): 23 or 26 Feb.

8	29 Feb 2,3 Mar	BJT Circuit Analysis: Large signal and small signal analysis of BJT circuits. **Reading:** Sections 4.5 to 4.7. **Lab:** 3a (BJT): 1 or 4 Mar.

Spring Break 7–11 Mar

9	14,16,17 Mar	BJT Applications: Amplifiers and Logic circuits. **Reading:** Sections 4.8 and 4.9. **Lab:** 3b (BJT): 15 or 18 Mar.

10	21,23,24 Mar	Introduction to the field–effect transistor (FET): Physical operation, large–signal analysis. **Reading:** Sections 5.1 to 5.3. **Lab:** 4a (BJT Amplifier): 22 or 25 Mar.

11	28 Mar	FET Bias: DC Biasing circuits. **Reading:** Sections 5.4 to 5.6. **Lab:** 4b (BJT Amplifier): 29 Mar or 1 Apr.

	30 Mar	Review Day

	31 Mar	Exam 2

12	4,6,7 Apr	FET Circuits: Amplifiers and switches including small–signal analysis. **Reading:** Section 5.8. **Lab:** 5a (MOS): 5 or 8 Apr.

13	11,13,14 Apr	Digital Logic: Basic logic circuits in MOS and CMOS. **Reading:** Sections 6.1 to 6.9. **Lab:** 5b (MOS): 12 or 15 Apr.

Patriots' Day Holiday, 18 Apr

14	20 Apr	Review Day

Reading Day: No Class, 21 Apr

	TBD before 30 Apr	Final Exam (2 hours, Common Exam for Both Sections). Closed–book with two sheets of notes (both sides) allowed.

Notation

This is the notation used by the text to represent voltages and currents. While I like the choice, I've found it adds some extra confusion for the student. This table may help.

Quantity	V or I	Subscript	Voltage Example
Total Instantaneous Signal	lower case	CAPITAL	v_A
DC Signal	CAPITAL	CAPITAL	V_A
AC Signal	lower case	lower case	v_a
Phasor of AC	CAPITAL	lower case	V_a

Thus, any signal is represented by

$$v_A = V_A + v_a \qquad \text{Text}$$

and a sinusoidal signal is represented by

$$v_A = V_A + V_a \sin(\omega t + \phi) \qquad \text{Text}$$

Remember that the RMS of an AC signal is $V_a/\sqrt{2}$.

Decibels

Decibels are a convenient concept to describe gains and losses in electronic systems. The gain of an amplifier is described in terms of the power ratio of output to input, and is expressed in dB. (note lower–case "d," meaning "deci–," and capital "B" for "Bel.") as

$$g = 10\log(p_{OUT}/p_{IN}).$$

If the output and input impedances are the same, then the power gain is the square of the voltage (or current) gain, and

$$g = 10\log\left(\frac{v_{OUT}}{v_{IN}}\right)^2] = 20\log(v_{OUT}/v_{IN}).$$

Although it is not needed for this course, signals are often expressed in dBm. This is not a measure of gain, but of signal level. It is the ratio of the power to one milliwatt.

$$y = 10\log(p/10^{-3}\text{W}).$$

Typically, this concept is used with 50–Ohm impedances common in RF work, and

$$y = 10\log(v^2/10^{-3}\text{W}/50\text{Ohms}).$$