

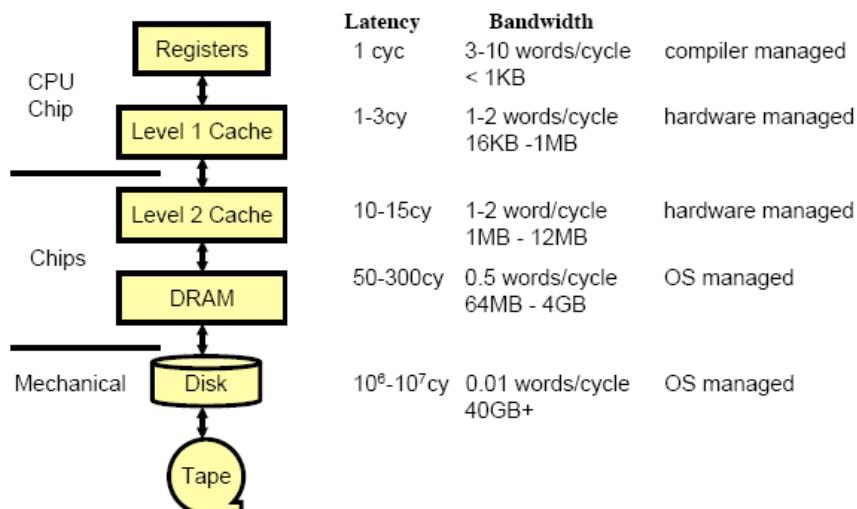
Lectures 6-8 – 1/31/11 – 2/4/11

- Announcements
 - Hwk 1 due Thursday beginning of discussion section
 - Hwk 2 posted
 - Make sure to check Blackboard for corrections to assignments
- Last Week
 - Combinational logic circuits
- This Week (P&P 3.4-3.6)
 - Storage
 - Sequential logic
 - Clocks
- Next Week
 - Finite State Machines
 - Let's Build a Computer

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Storage

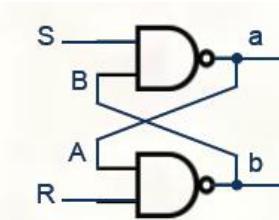
- Ideally: inexpensive, large & fast - Can't have all three
- Computer programs exhibit locality of reference
 - Reasonable likelihood that:
 - A memory address will be referenced again soon (instruction in a loop)
 - A nearby memory address will be referenced soon (array processing)



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R-S Latch

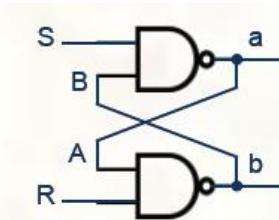
- Two interconnected NAND gates
- Quiescent when $R = S = 1$
 - If $a = 1$: $A = 1, b = 0, B = 0$
 - a won't change as long as R & S remain $= 1$
 - The R-S latch stores the value "1"
 - If $b = 1$: $B = 1, a = 0, A = 0$
 - b won't change as long as R & S remain $= 1$
 - The R-S latch stores the value "0"
- We have two stable states
 - Can thus store a bit!
- We say that the latch stores a "1" when $a = 1$
 - b , the 2nd output, is the inverse of the stored value



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Changing the Latch's Value

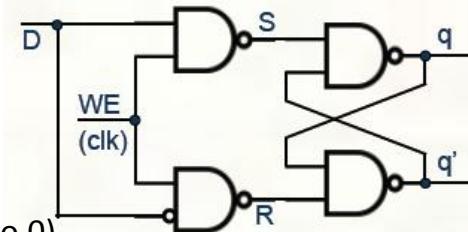
- To set the latch to "1"
 - Set $S = 0$ for a "moment"
 - Keeping $R = 1$
 - A gets set to 1
 - Reset $S = 1$ after the "moment"
- To set the latch to "0"
 - Set $R = 0$ for a "moment"
 - Keeping $S = 1$
 - B gets set to 1
 - Reset $R = 1$ after the "moment"
- Avoid setting $R = S = 0$
 - Final state depends on electrical properties of the transistors and NOT the logic



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Gated D Latch

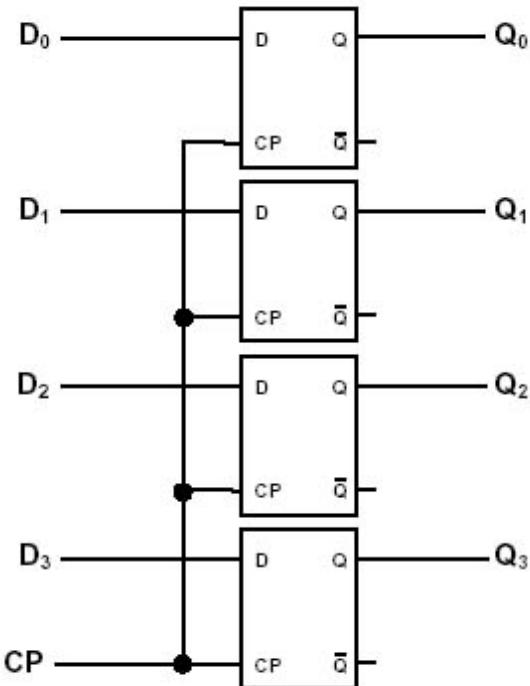
- R-S latch that is set to D only when WE == 1
- Write Enable (WE)
 - WE == 0: R = 1, S = 1
 - The latch remains unchanged
 - WE == 1:
 - Either R or S (but not both) cleared (set to 0)
 - D determines which is cleared
 - The latch's value = D
 - When WE returns to 0 the latch is quiescent and holds the new value (whatever D was)



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A 4-Bit Register

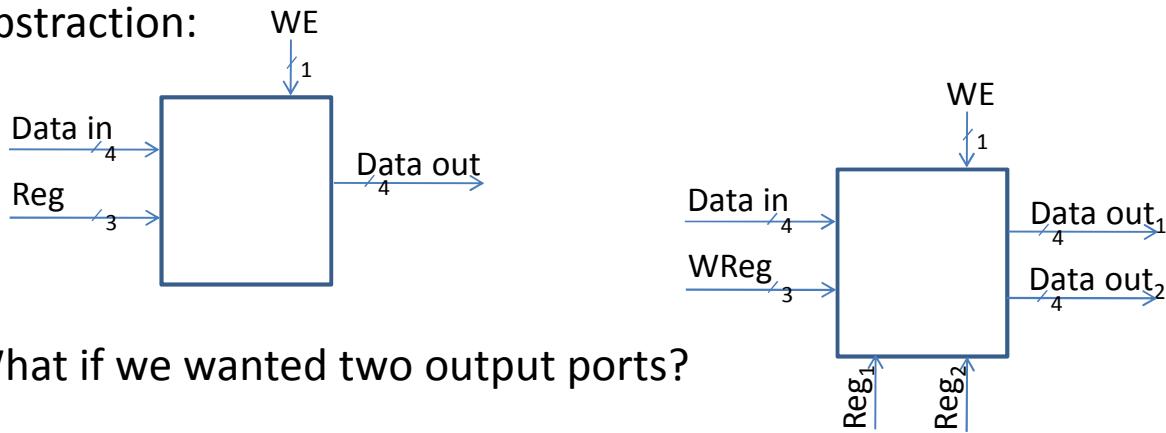
- Four D-latches
 - all sharing a WE input (CP in the diagram)
 - $D_0 - D_3$ are inputs
 - $Q_0 - Q_3$ are outputs



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Register File Abstraction

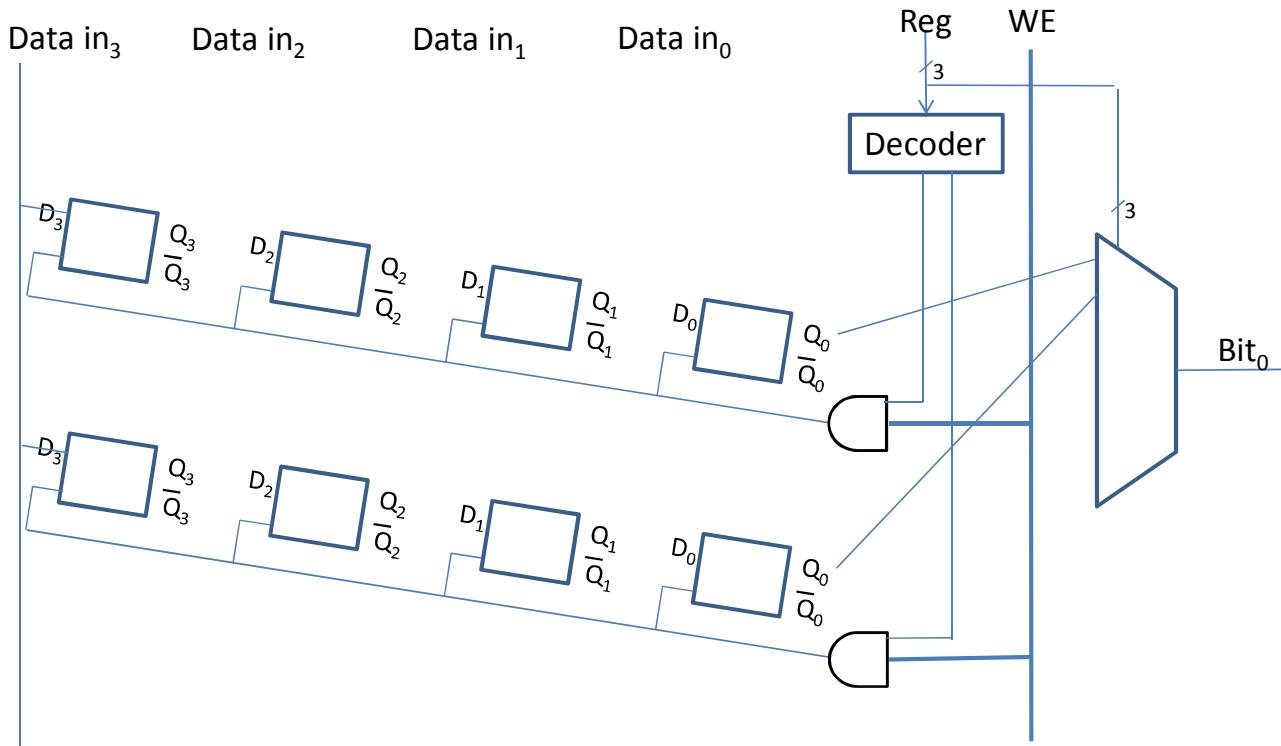
- Register file provides the CPU with temporary, fast storage
 - N registers
 - Each of K bits
 - L output ports
- Suppose we want eight 4-bit registers and one output port
- Abstraction:



- What if we wanted two output ports?

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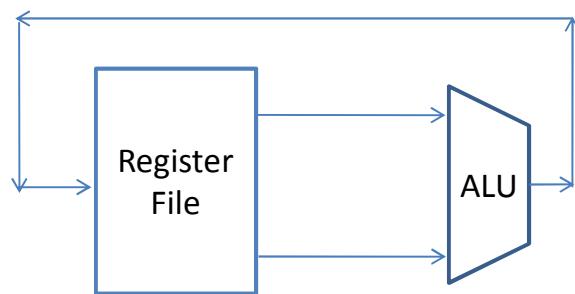
One Port Register File Implementation



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Race Through Conditions With D Latches

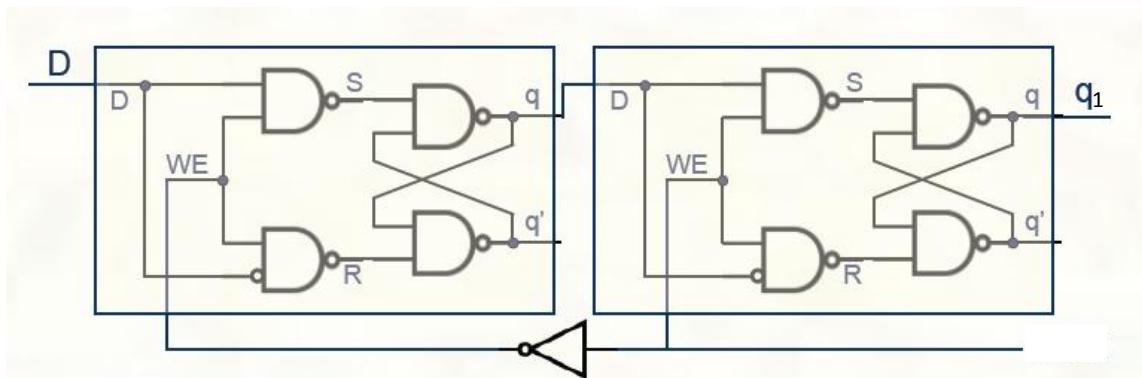
- WE must be set to “1” for a sufficiently long interval to allow
 - Data to be read
 - Operation (addition) to be performed
 - Result to be stored in target register
- For R1 = R1 + R2, R1 = 0000, R2 = 0001
 - What’s the value of R1 when WE is reset to “0”?
 - 0001, 0010 or maybe even 0011?



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Enter the Master-Slave Flip Flop

- Flip flop consists of a positive latch followed by a negative latch
- A two-step action controlled by WE
 1. WE == 0: $q = D$, $q_1 = \text{old } q_1$
 2. WE == 1: $q = \text{old } q$; $q_1 = q$



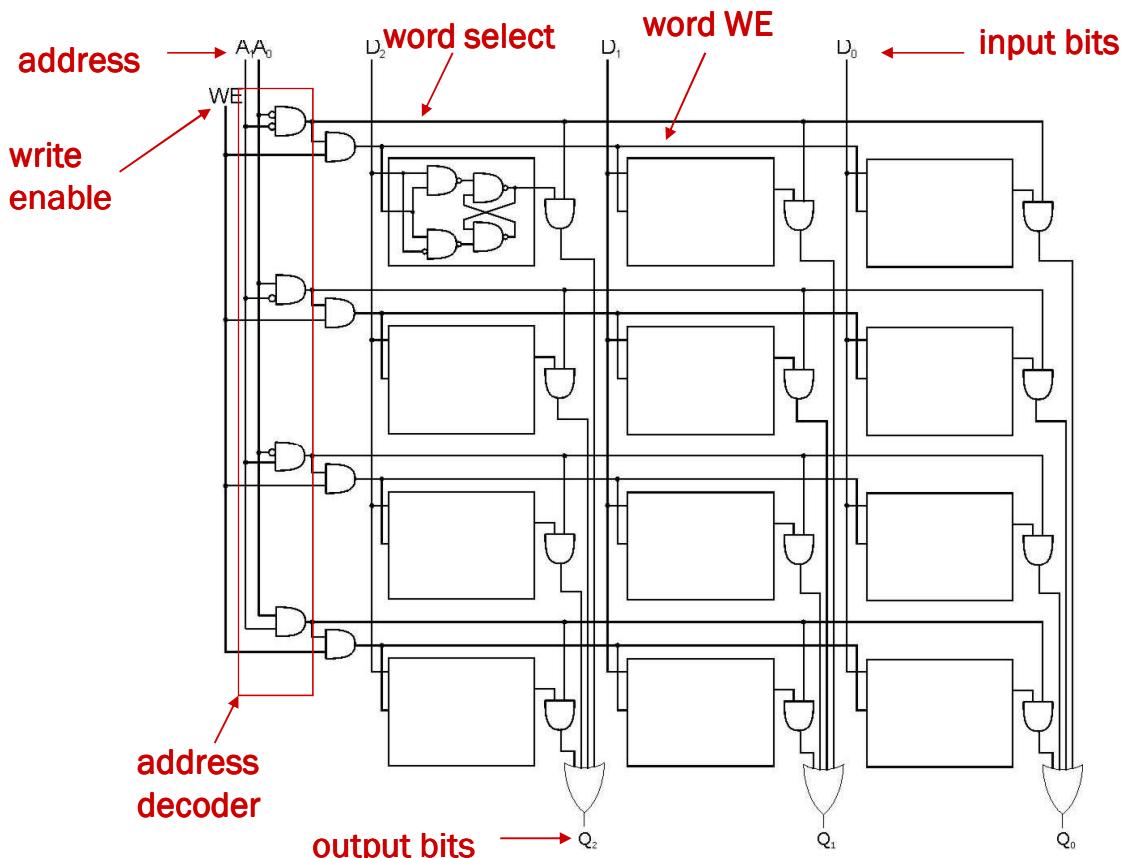
<http://tams-www.informatik.uni-hamburg.de/applets/hades/webdemos/16-flipflops/10-srff/chapter.html>

Memory

- Large number of identifiable locations
- Address space
 - The total number of identifiable locations in memory
- Addressability
 - The unit of memory at each identifiable location
- Examples:
 - 8Kb (K: Kilo = 2^{10} – 1,024 ~ one thousand; b: bit)
 - 16MW (M: Mega = 2^{20} – 1,048,576 ~ one million; W: word)
 - 4GB (G: Giga = 2^{30} – 1,073,741,824 + one billion; B: byte)

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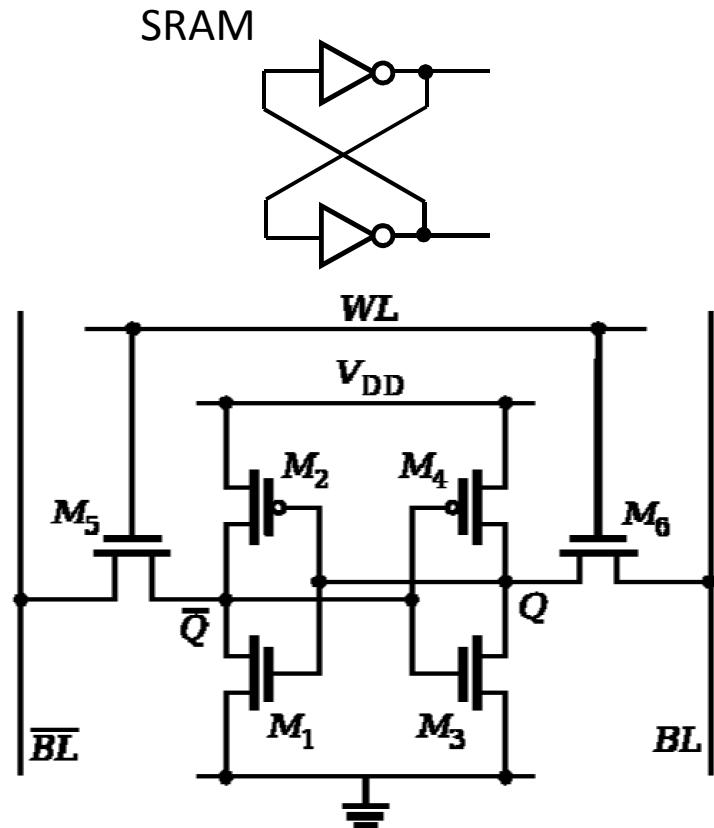
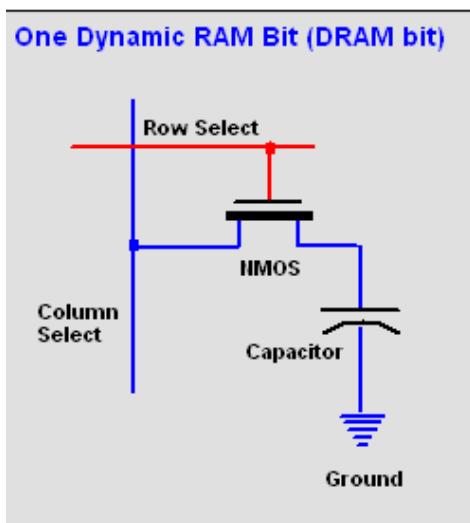
A 2^2 -by 3-bit Memory



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Memory Cells

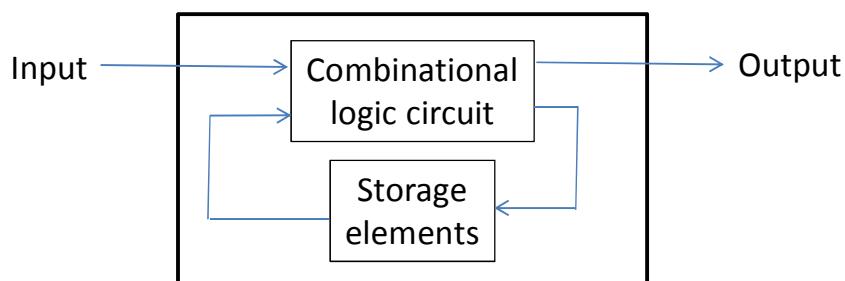
- DRAM



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Sequential Logic

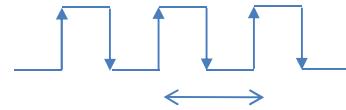
- Combinational logic (adder, MUX, ...)
 - Memory-less
 - Output is purely a function of the inputs
 - E.g., $5 + 3$
- But, often output is a function of input as well as previous values
 - E.g. a counter of some periodic signal or event
 - Also see the locks example in P&P 3.6.1



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Clock Signals 1

- A square wave signal distributed globally around the chip
 - The clock *period* is the interval between two rising edges
 - AKA clock *cycle*
 - The clock *frequency* is the inverse of the period
- Why global distribution? Synchronicity
 - We want all inputs to combinational circuits arrive at the same time
 - Adder, mux, etc.
- Storage elements use clocks (the WE signal) to force synchronicity
- Traffic light analogy
 - Cars arrive at different times
 - Leave simultaneously



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Clock Signals 2

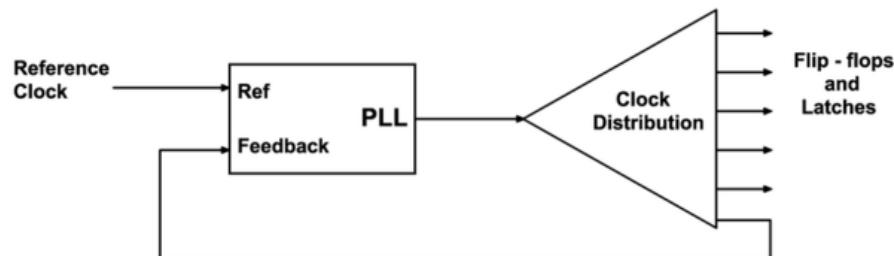
- Clock signal can be gated
 - To turn off activity in part of the chip
- A 2GHz clock means the clock goes through 2 billion cycles per second
 - Equivalently, the clock cycle is 0.5 nanoseconds
- Aside:

10^{-3}	Milli	10^3	Kilo
10^{-6}	Micro	10^6	Mega
10^{-9}	Nano	10^9	Giga
10^{-12}	Pico	10^{12}	Tera
10^{-15}	Femto	10^{15}	Peta

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Clock Signals 3

- A crystal has a natural resonance frequency of vibration
 - Depends on size, shape, elasticity & speed of sound in the material
- To cause the crystal to resonate:
 - Apply voltage – piezoelectric effect causes crystal to physically change
 - Remove voltage – crystal returns to original shape and resonates
 - Generating a signal at “its” natural frequency
 - Tens of KHz to tens of MHz
- On-chip the frequency is multiplied using a Phase Locked Loop
 - BIOS controlled!



- Issues:
 - Clock skew
 - Power consumption

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Aside: Power

- Power = $f(\text{capacitive load, voltage, switching frequency})$
- More power = more heat generated
 - More, larger fans = lots of noise
 - And if you want to overclock...
- (Also, means more electricity, more powerful batteries, ...)
- So, what's a girl to do?
 - Especially if she wants her overclocked computer in the living room?

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