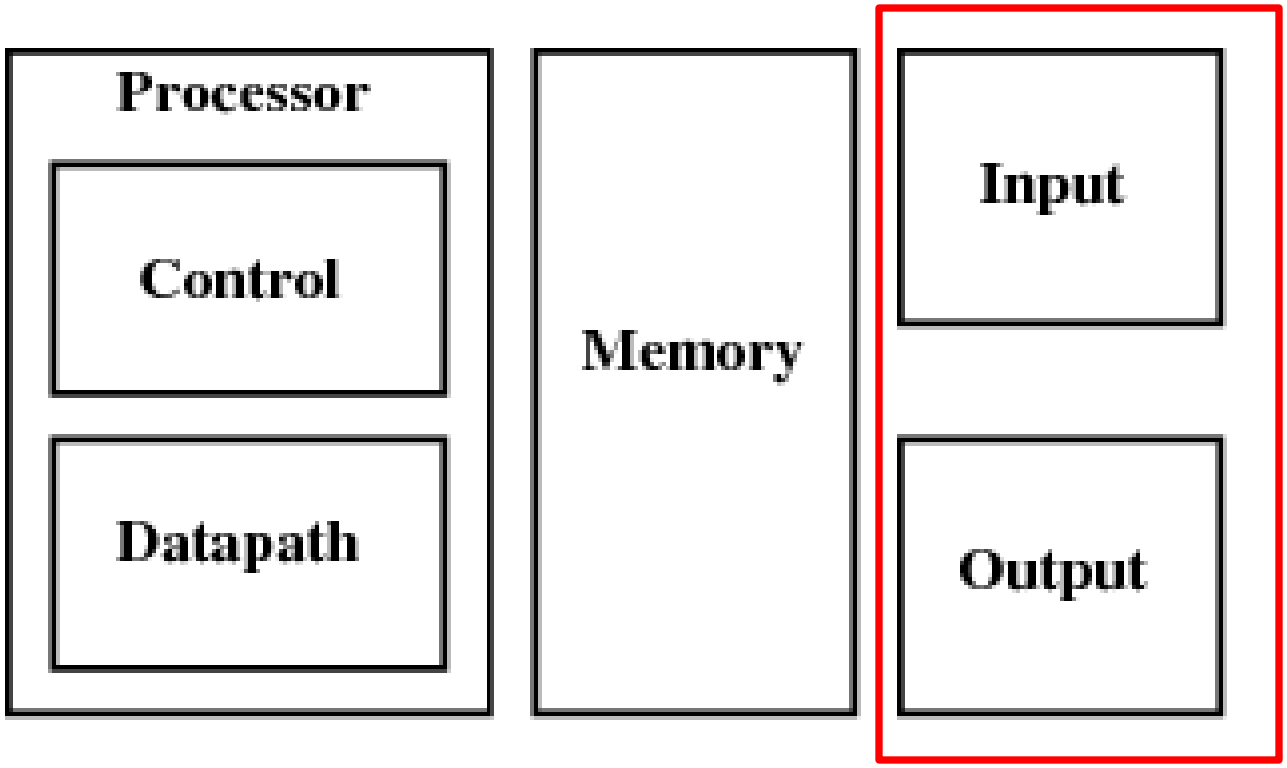
COMPUTER SYSTEMS ORGANIZATION

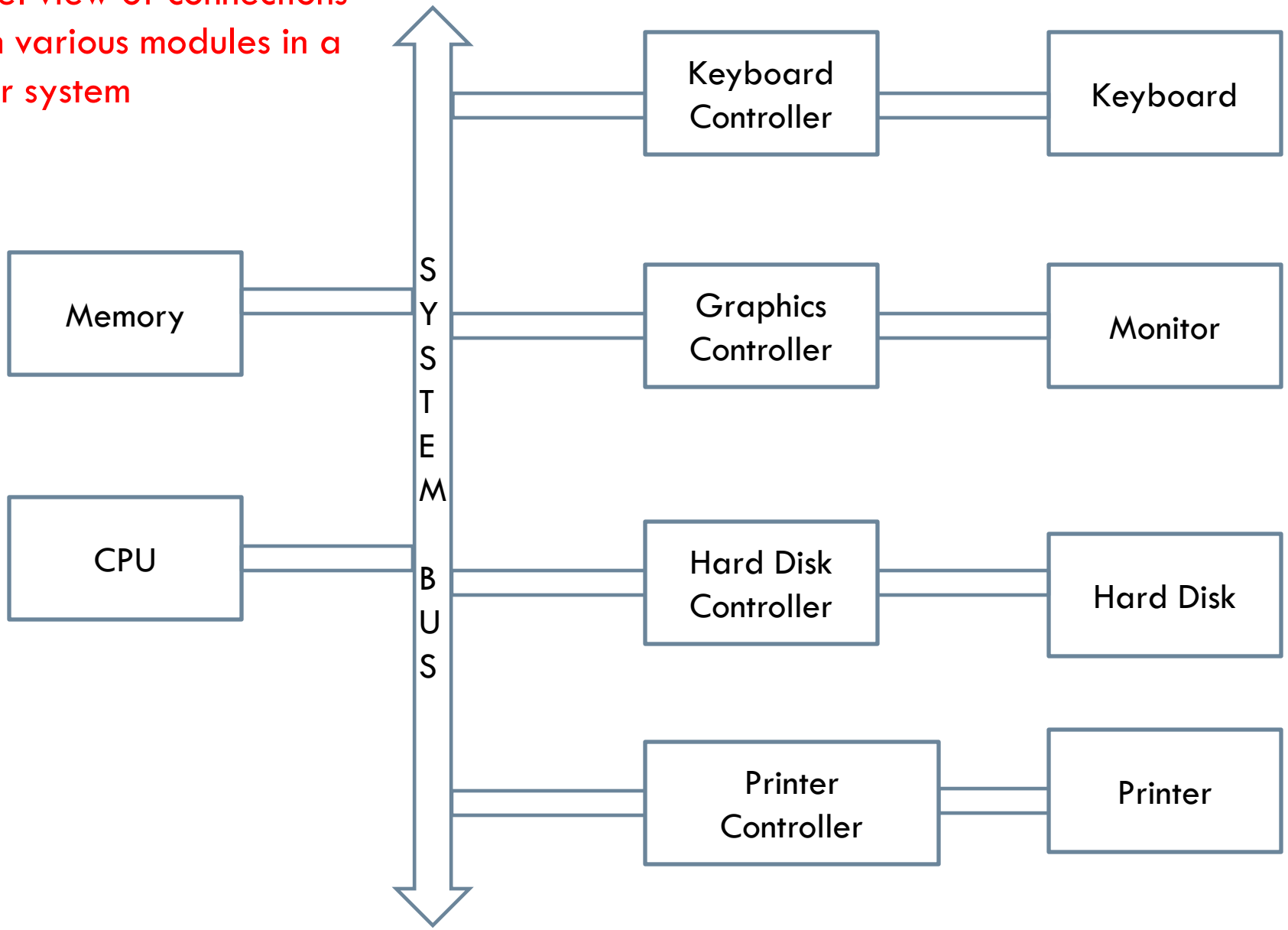
Input/Output -- Spring 2010 -- IIIT-H -- Suresh Purini

The Big Picture: Where are we now?

Input and Output

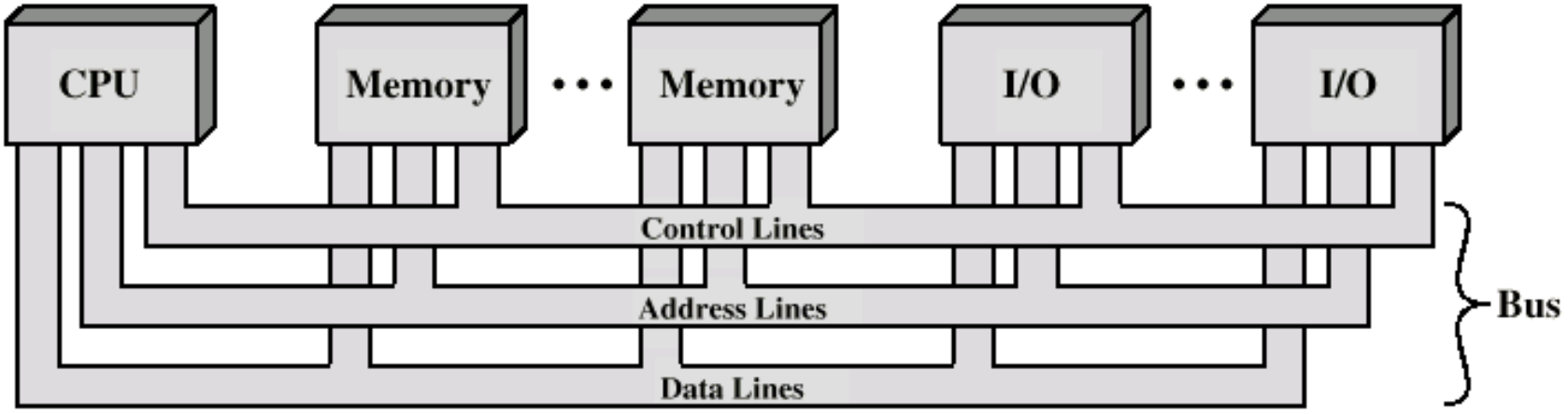


High level view of connections between various modules in a computer system



System Bus Consists of:

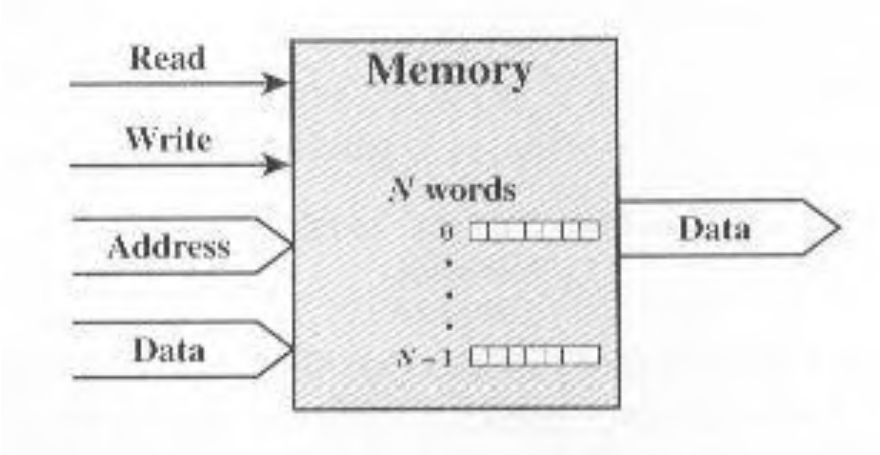
- Address lines
- Data lines
- Control lines

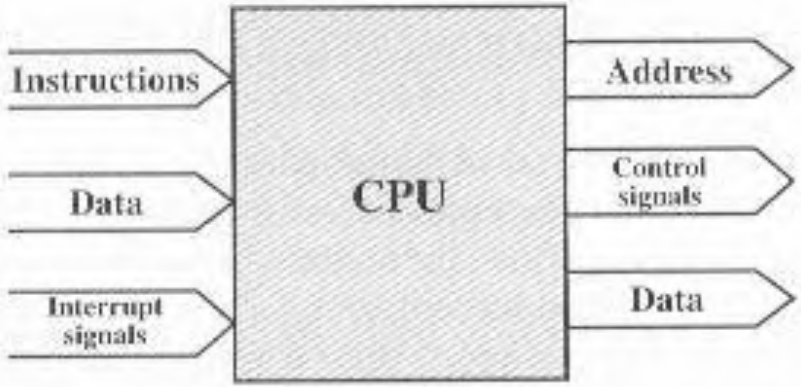


Typical Control Lines:

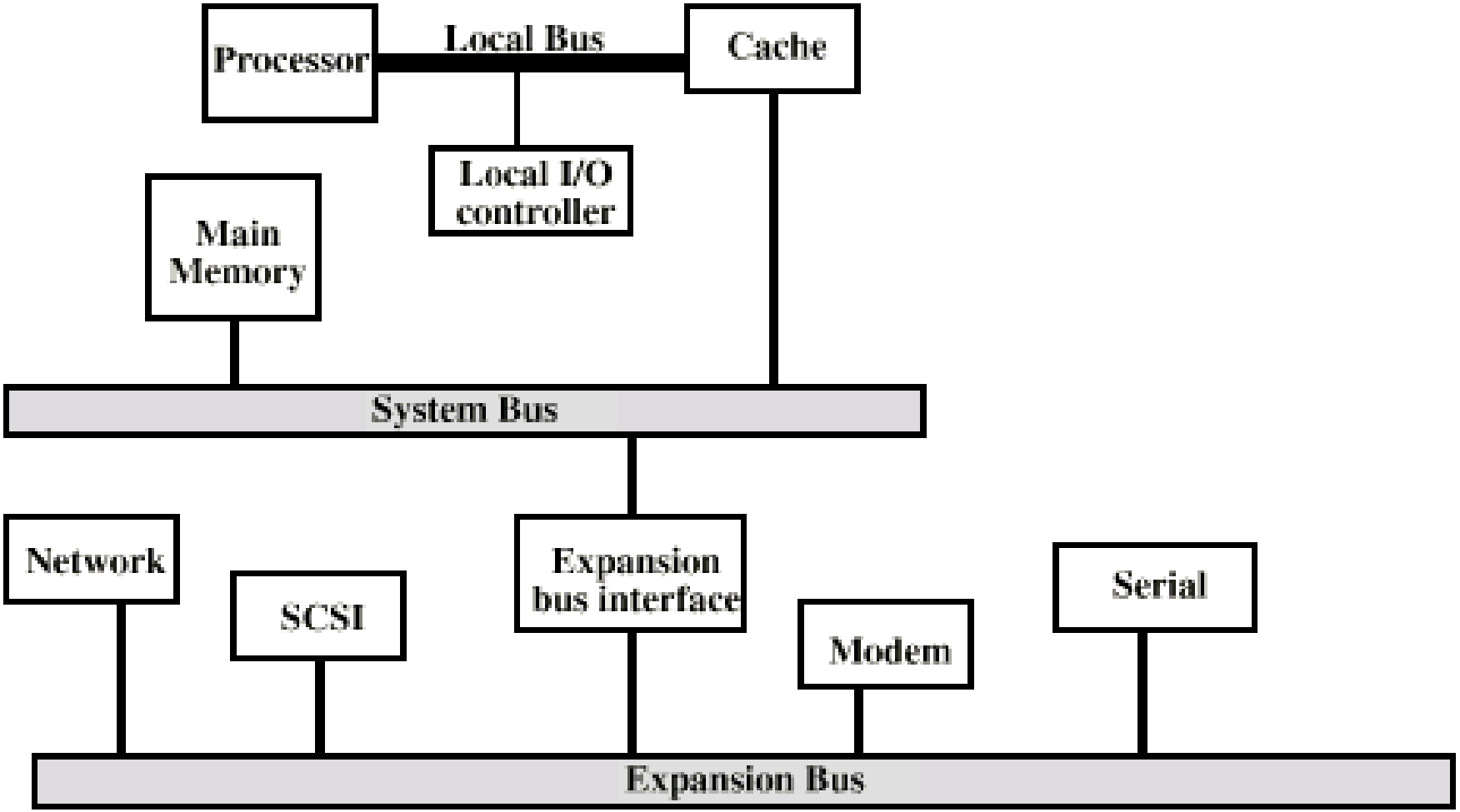
- Memory write
- Memory read
- I/O write
- I/O read
- Transfer ACK
- Bus request
- Bus grant
- Interrupt request
- Interrupt ACK
- Clock

Typical Signal Lines for Memory and CPU

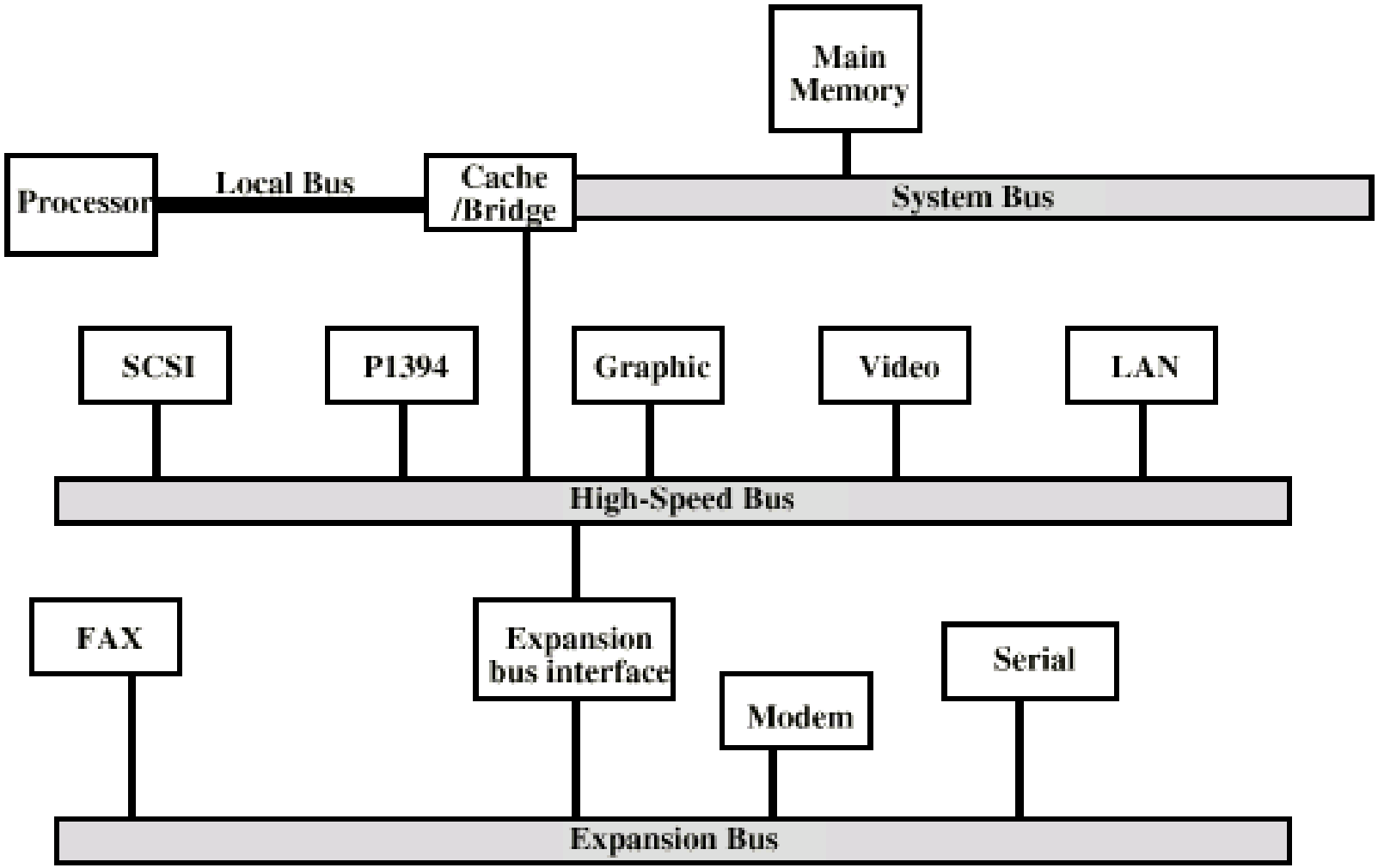




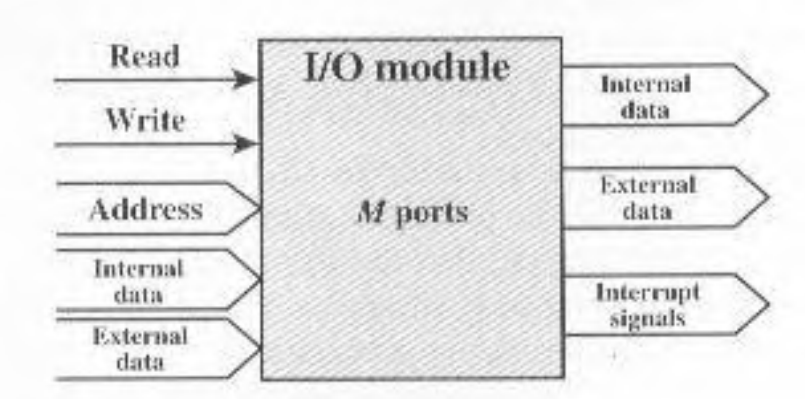
Traditional Bus Architecture

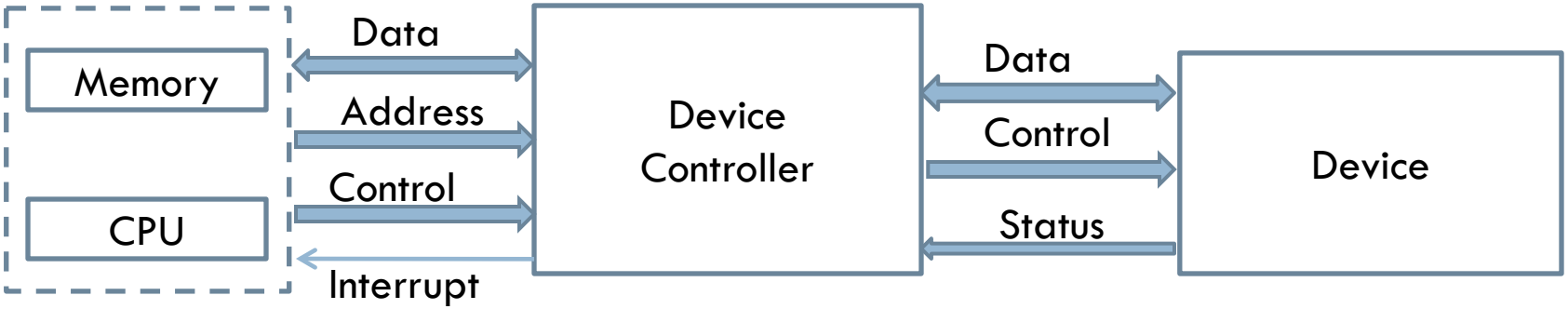


Another Possible Bus Architecture

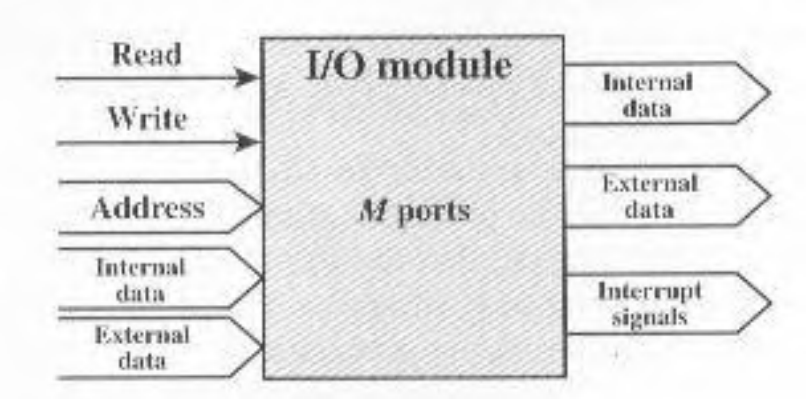


Typical Signal Lines for I/O Modules (Device Controllers)

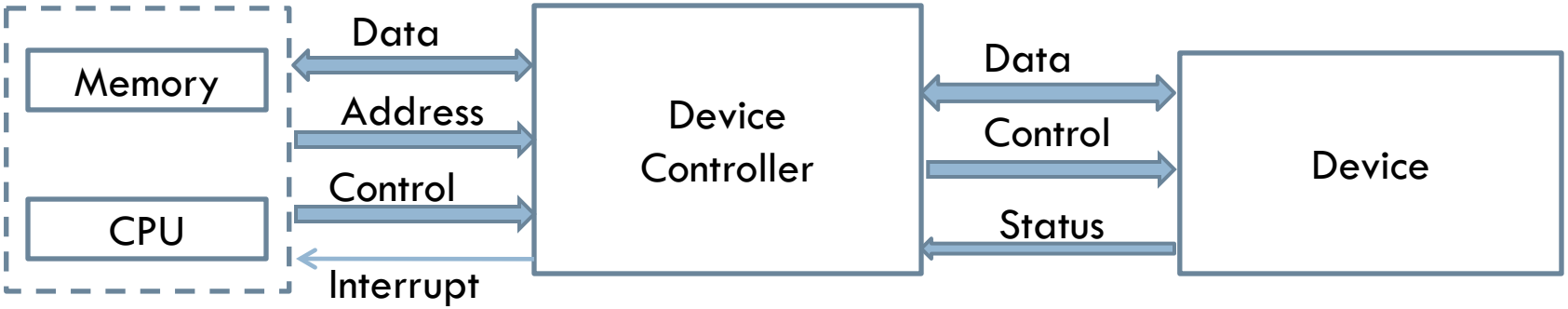




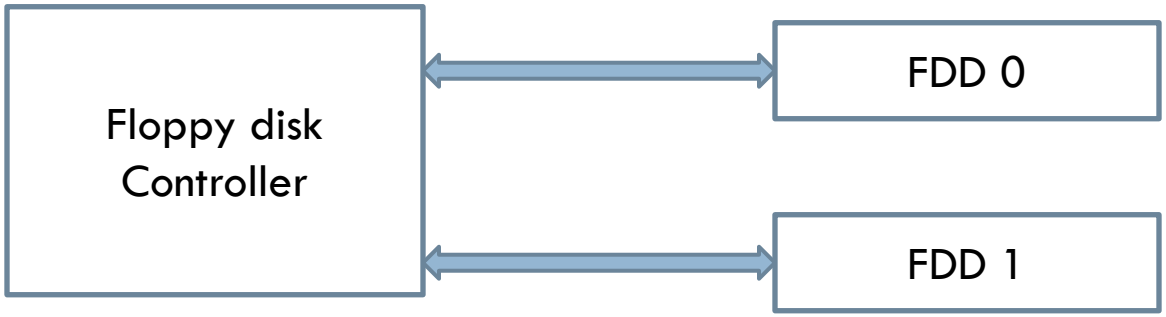
Typical Signal Lines for I/O Modules (Device Controllers)



We need a device drive which knows how to interface with the Device Controller



Floppy Disk Controller



Control Signal	Action by the device
Drive Select	FDD gets logically connected
Head Select	FDD selects either the top or bottom head
Direction	Indicate the direction of head movement (inward or outward)
Step	Move one track
……..	……

Status Signal	Action by the device
Track 0	Read/write head is positioned over the track 0
Write Protect	FDD is write protected
Ready	FDD is ready for operation
……..	……

Types of Data Transfer

Bus interconnection should support the folllowing types of transfer:

- Memory to processors
- Processor to memory
- I/O to processor
- Processor to I/O
- I/O to or from memory (Direct Memory Access – DMA)

Elements of Bus Design: Bus Type

- Dedicated
  - Separate data & address lines
- Multiplexed
  - Shared lines
  - Address valid or data valid control line
  - Advantage - fewer lines
  - Disadvantages
    - More complex control
    - Ultimate performance

Elements of Bus Design: Method of Arbitration

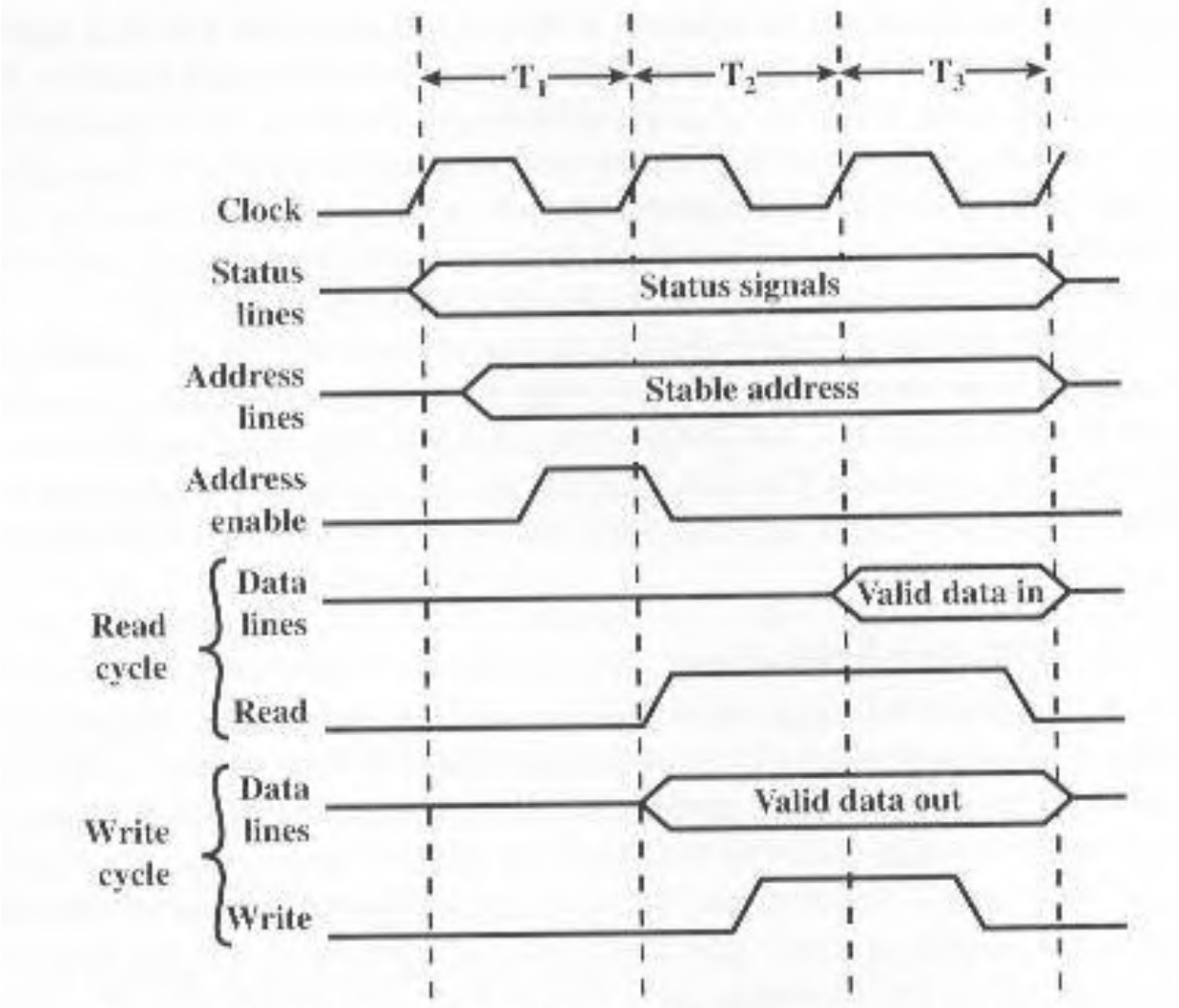
- More than one module controlling the bus
  - e.g. CPU and DMA controller
- Only one module may control bus at one time
- Arbitration may be Centralised (Bus Controller) or Distributed

Elements of Bus Design: Timing

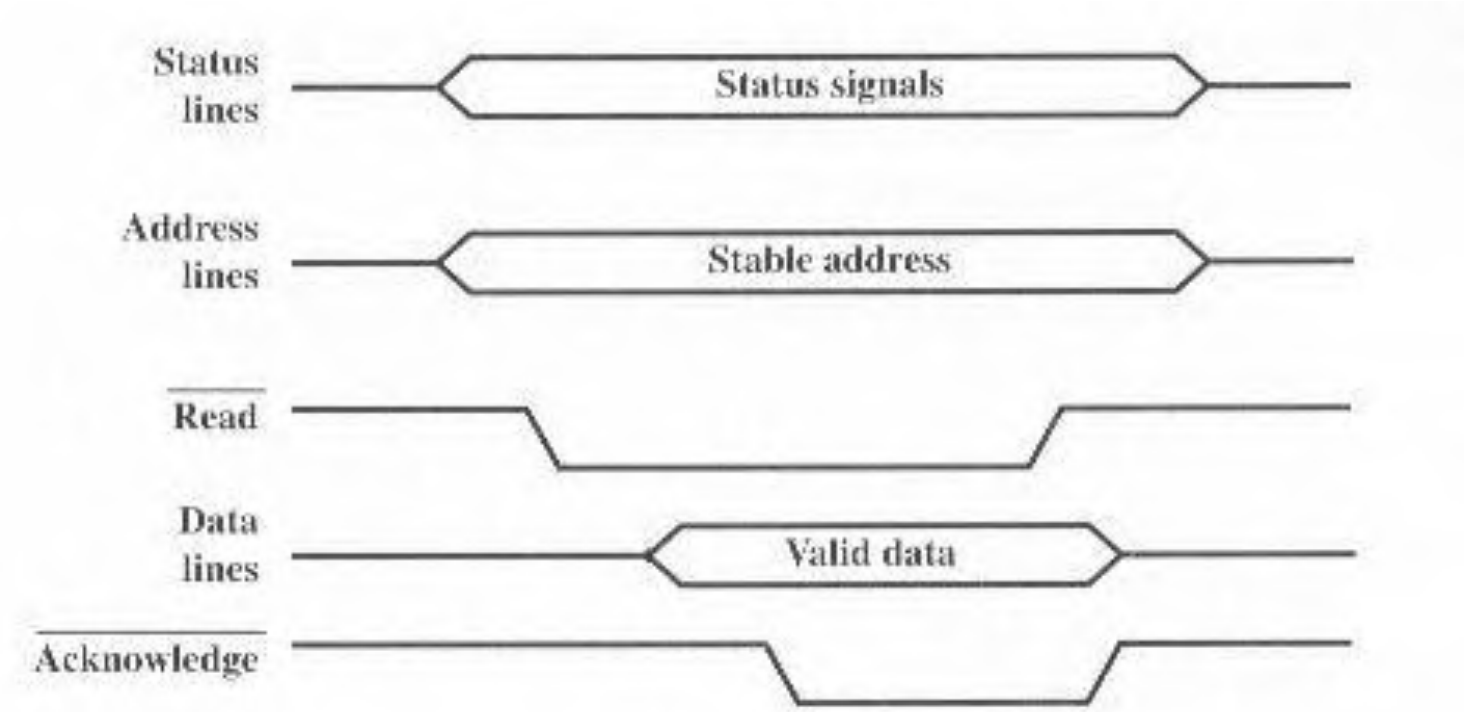
- Co-ordination of events on bus
- Synchronous
  - Events determined by clock signals
  - Control Bus includes clock line
  - A single 1-0 is a bus cycle
  - All devices can read clock line
  - Usually sync on leading edge
  - Usually a single cycle for an event
- Asynchronous

Timing of Synchronous Bus Operations

Important Remark: Bus clock and Processor clock are different.

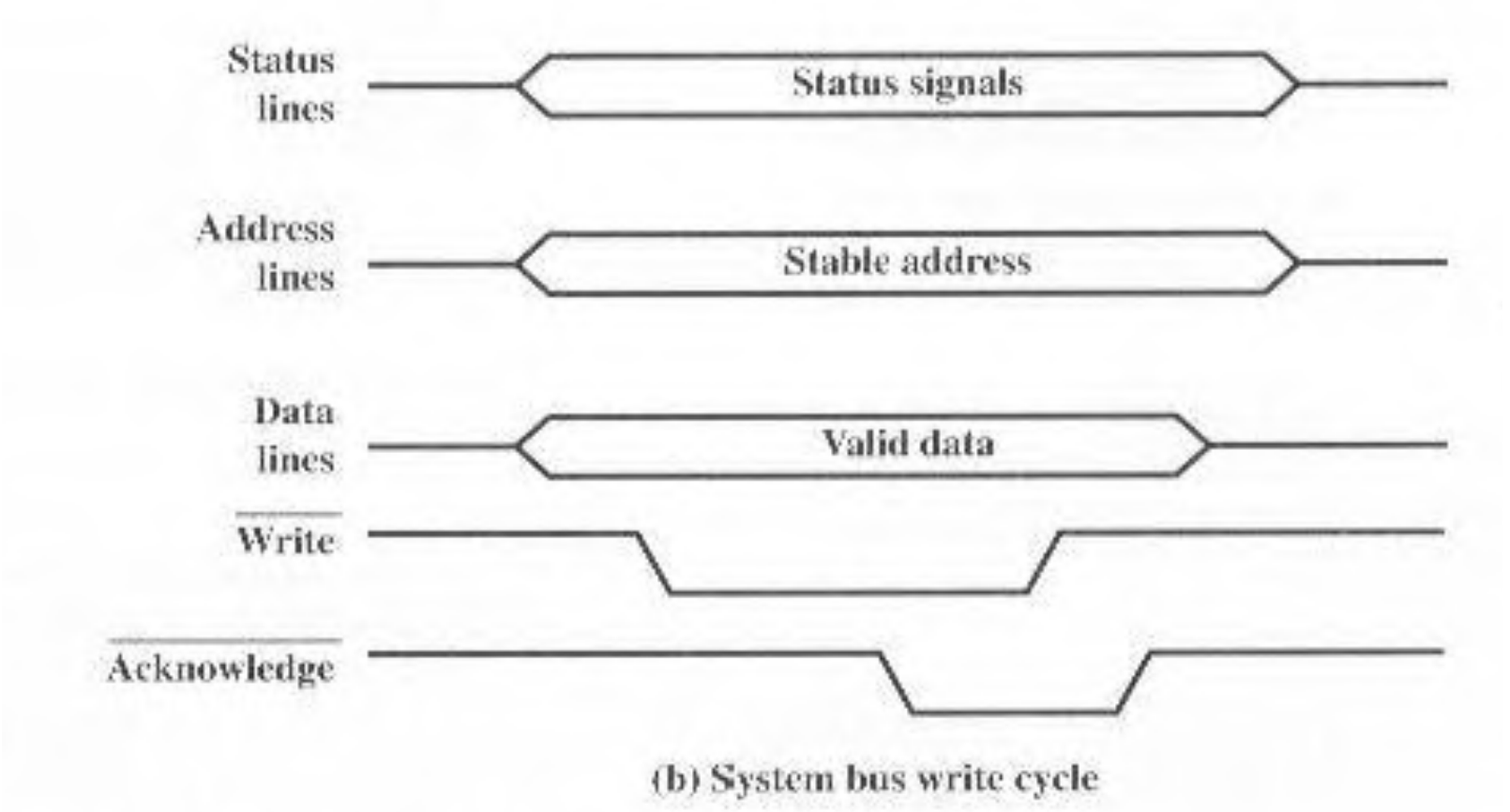


Timing of Asynchronous Bus Operations



(a) System bus read cycle

Timing of Asynchronous Bus Operations



(b) System bus write cycle

Various Bus Protocols

- Industry Standard Architecture – ISA (1982)
- Extended Industry Standard Architecture – EISA
- Vesa Local Bus – VL Bus
- Peripheral Component Interconnect – PCI (Early 1990s)

Typical Desktop System