Assignment 4

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Group no. - 4
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Objective

The objective of this lab is to go through the basic architecture of CPU, build one and test a few set of instructions. It involves developing of op-code for the instructions and seeing the result of accumulator using seven segment display. The program counter in this lab is used to count the number of counts required for each operation. It's LSB is also used as clock for other registers in the circuit.

List of Components Used

Chip Number / Serial Number	Description	Quantity
74LS00	Quad 2-input NAND IC	2
74LS04	Hex inverter IC	2
74LS247	BCD to Seven Segment Decoder IC	2
08TIE524	Dual 7-segment display	1
17DIP8SS	8 switch dip switch set	2
17TOGSD -M SPDT	ON-ON Toggle switch	1
210321A29FA0	Analog Discovery 2	1
AFG 1022	Function Generator	1
74LS569N	Four Bit Up/Down Counter	1
74LS181	ALU	1
SN7489N	64 Bit RAM	1
74LS174	Hex D flip-flop	2
74LS157	2 Line to 1 Line data Selector	1
74LS74	Dual Positive Edge D Flip Flops	1
470 ohms	resistors	20

Experimental Approach

The main task of this lab to create a basic 4-bit CPU which takes the opcode, performs the respective action and stores the data in accumulator. The opcode for the 4 bit CPU is 16 bit, this is further divided into two bytes- odd and even to segregate instruction from direct data and RAM address. The odd byte is reserved for direct data and RAM address. Even byte consist of instruction which is given to the instruction register, hence every operation is synchronous with clock. The output of instruction register was given as a mode selector to the ALU, select line for MUX and read/write to the scratchpad RAM. The inputs to the MUX are the direct data and the value from given RAM address, the output of the multiplexer is connected to the ALU. By this selecting the mode through the instruction register, all the desired results are found. The ALU is connected to the Accumulator in order to update the result of operation with clock, which is then connected to the BCD - 7-segment decoder. The output of the accumulator is also provided back to the ALU, scratchpad RAM and 'program counter' although the PC merely does up-down count. The clock is given at PC whereas for rest of the registers used in the design take clock from LSB of the PC. The outputs of PC are also connected to 7-segment display through BCD. For the jump instructions two additional bits were required for JMPZ and JMP instruction whereas for JMPN the 'A=B' pin of ALU was used. The extra bits along with 'A=B' pin were passed through D flip flops and the outputs were given to a controller unit which comprises of combinational circuit. The output of the controller was then given to synchronous clear of PC. The clock is provided using the toggle switch. This experiment needs us to debounce the clock in order to provide the smooth transition between high to low and vice versa[1]. For this a latch circuit was created for which the inputs were taken from the positive pins of the toggle switch while the central pin was grounded[1].

Logic Works Design

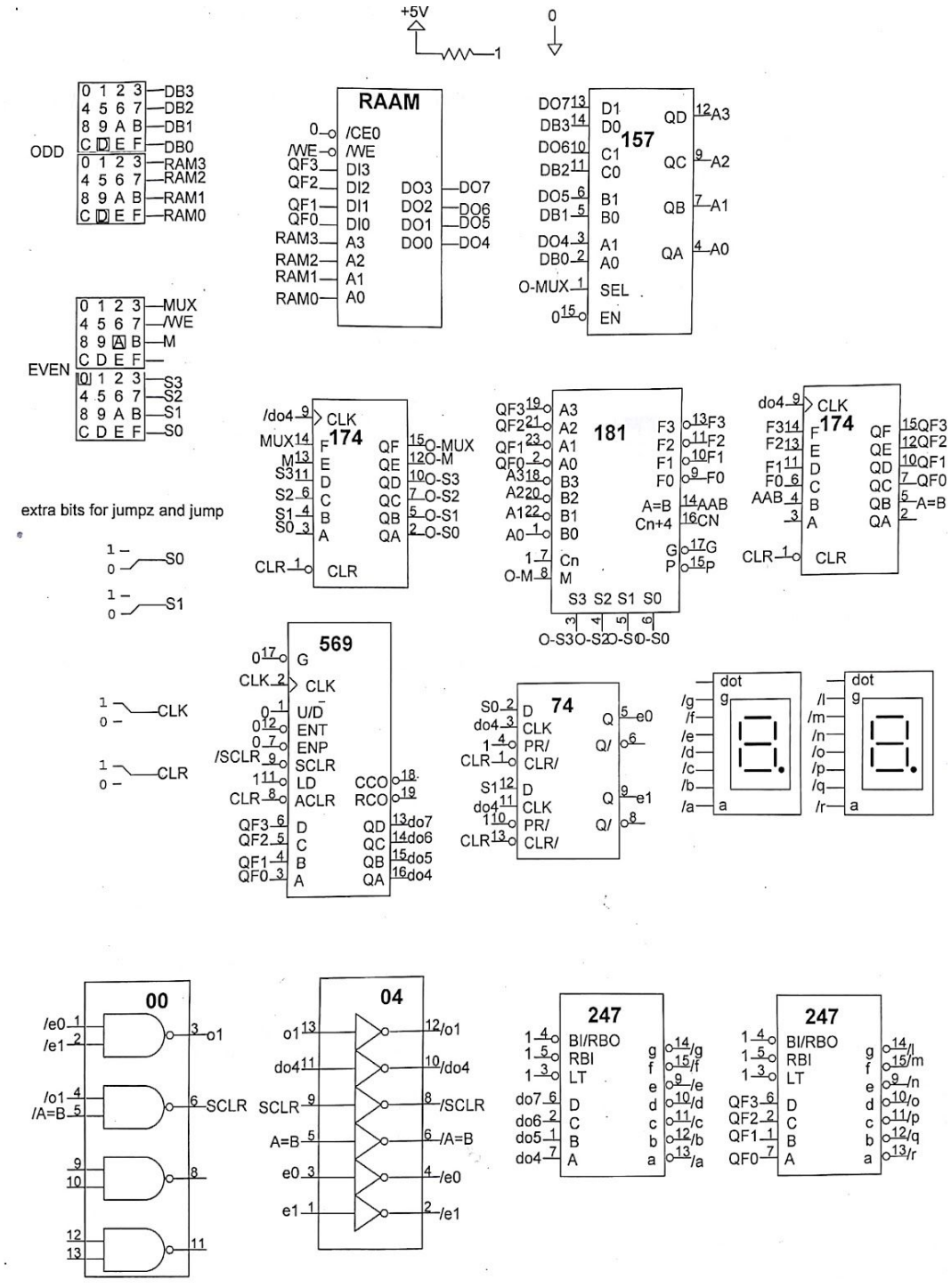


Fig 1. Schematic For 4-Bit CPU

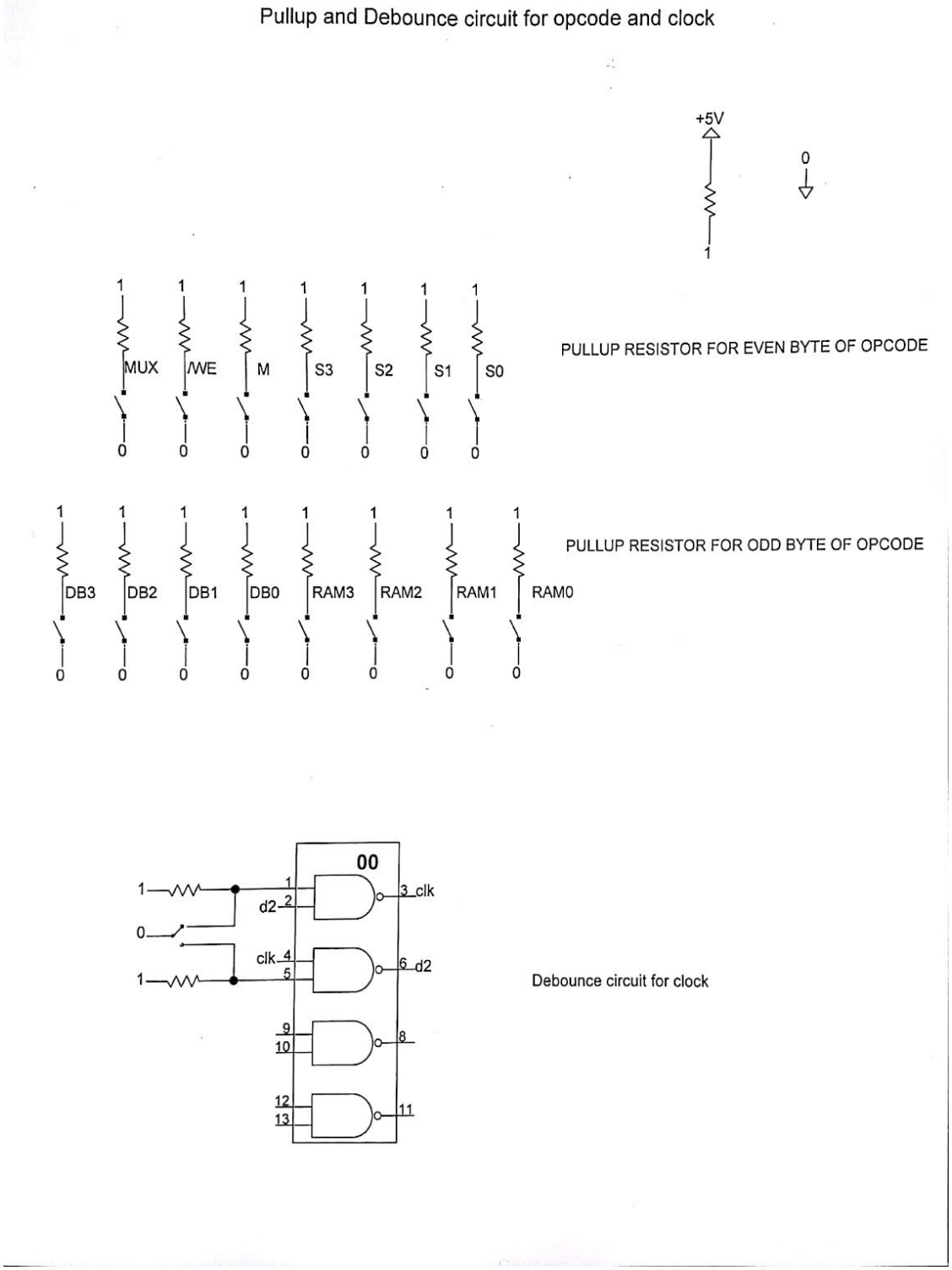


Fig 2. Pull Up and Debounce Circuit

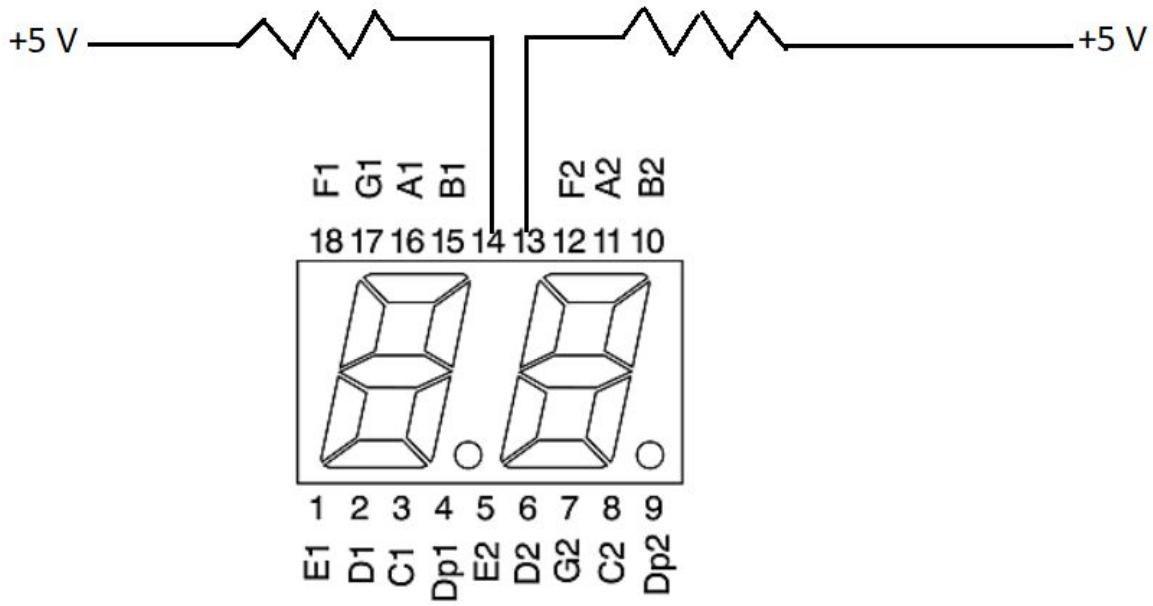


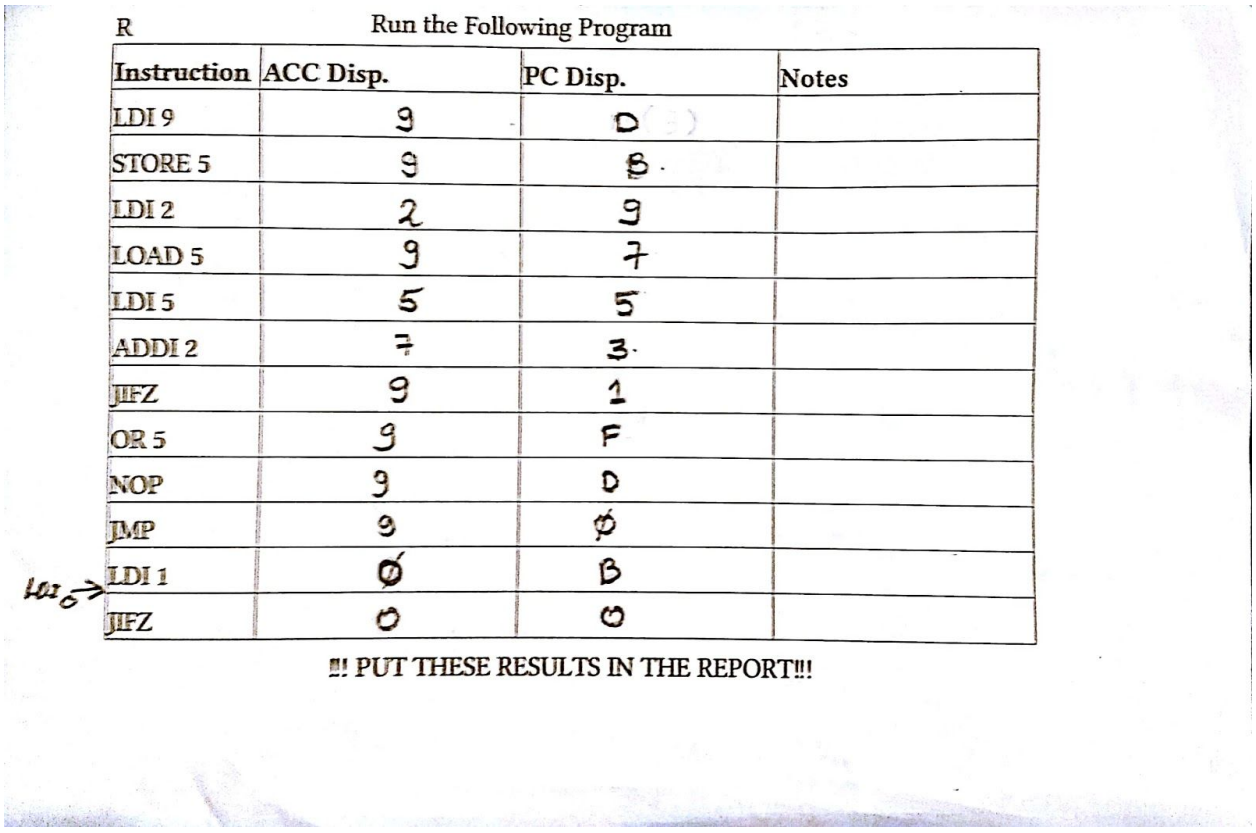
Fig. 3 Seven segment display common anode connections.

Results

Table 1. List of Opcodes used.

	MUX	W'	M	Cn	S3	S2	S1	S0
NOP	0	1	1	1	1	1	1	1
INV	0	X	1	1	0	0	0	0
SHIFT	0	X	0	1	1	1	0	0
LDI	0	X	1	1	1	0	1	0
LOAD	1	1	1	1	1	0	1	0
STORE	1	0	1	1	1	0	1	0

ADD	1	1	0	1	1	0	0	1
SUB	1	1	0	1	0	1	1	0
AND	1	1	1	1	1	0	1	1
OR	1	1	1	1	1	1	1	0
ADD I	0	1	0	1	1	0	0	1
SUB I	0	1	0	1	0	1	1	0
AND I	0	1	1	1	1	0	1	1
OR I	0	1	1	1	1	1	1	0



R Run the Following Program

Instruction	ACC Disp.	PC Disp.	Notes
LDI 9	9	D	
STORE 5	9	6	
LDI 2	2	9	
LOAD 5	9	7	
LDI 5	5	5	
ADDI 2	7	3	
JIFZ	9	1	
OR 5	9	F	
NOP	9	D	
JMP	9	0	
LDI 1	0	B	
JIFZ	0	0	

!! PUT THESE RESULTS IN THE REPORT!!!

Fig 3. Executed Instruction Set.

The circuit was successfully built and implemented.At first, the circuit failed to provide proper output for jump instructions. The shortcomings were identified. Two extra bits were taken and passed through a D flip flop and a combinational logic was developed

for the same. The RAM used in simulation did not have inverted outputs. As a result, an extra inverter IC was required while building the hardware.

Conclusion

The circuit built was able to perform any given instructions and was able to display the desired outputs. After the circuit was given a synchronous clear, it was observed that the next instruction would require three clock pulses. We tried playing around with different instructions and the output was as desired in two clock pulses. Thus, the circuit was successfully designed and implemented.

FTQs

29.

Byte 0					Byte 1	
M	MUX	W’	Cn	S	DB	RAM
1	0	1	1	1001	0001	0111

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As M = 1, it indicated Logic Operations are to be performed. MUX= 0 which indicates that value of DB will be loaded. W’ = 0 which indicates Read. S = 1001 which after looking at the datasheet indicates A’ XOR DB’. The output of this operation will be stored in accumulator.

11.

Byte 0					Byte 1	
M	MUX	W’	Cn	S	DB	RAM

1	1	0	0	0000	0001	1011

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Here, first of all Cn is ‘0’ that means the inputs are active low type, hence referring the function table (datasheet) M=1, it turns out that the operation is inverting of accumulator and storing the updated value in accumulator and RAM address 1011 (since W’=0).

References

[1] ADSD Assignment 3