CSE350

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Sec: 07

ID-19101147

NAND

Input A	Input B	V_{DA}	V_{DB}	V_p	I_{R1}	I_{R2}	V_b	Output Y
0	0	0.657667	0.657667	0.657667	0.0022734	0	-0.51792	5
0	1	0.675583	-4.3244	0.675583	0.0022640	0	-0.500605	5
1	0	-4.3244	0.675583	0.675583	0.0022640	0	-0.500605	5
1	1	-2.85155	-2.85155	2.14845	0.0014929	0.0025676	0.817524	0.0958615

Inverter

Input A	Input B	V_p	V_b	Output Y
1	0	0.675583	-0.500605	5
1	1	2.14845	0.817524	0.0958615

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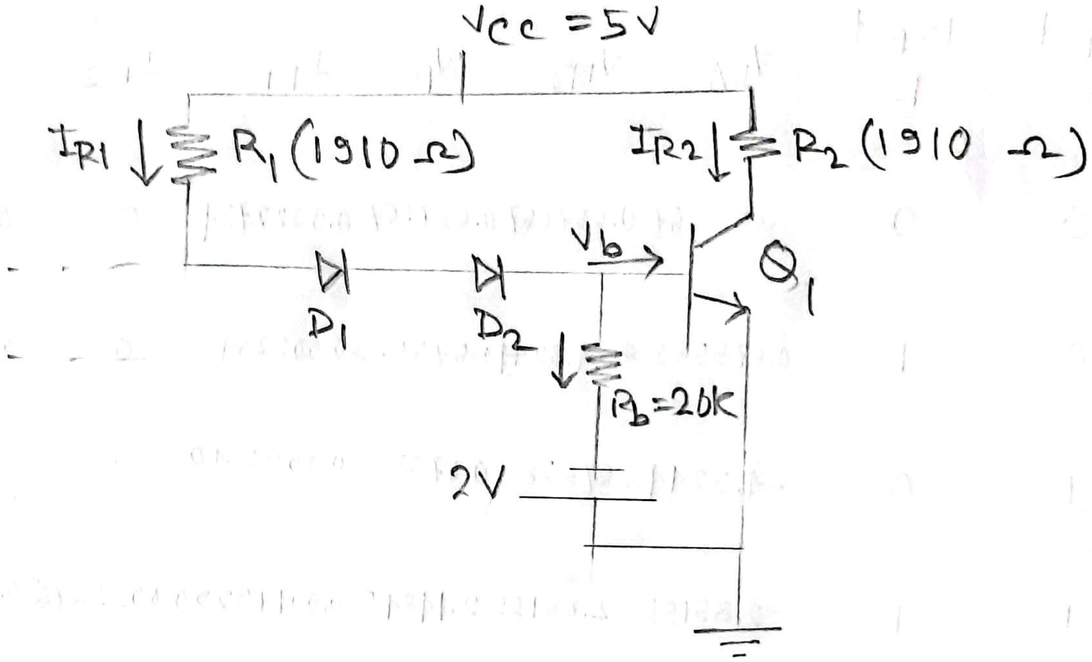
Report

1.



2. From table 2, we see that the value of Input A is fixed as logical high or 1. On the other hand, we are playing with the value of Input B. when we set logical low or 0 as the input we get logical high as the output and when we set logical high as the input we get logical ~~high~~ low as the output.

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So, this circuit is working as an inverter. However, the whole circuit is a NAND gate. As a result, when there's a single 0 in the actual input combination of this circuit we are getting logical high ie. [A=1, B=0, Y=logical high]. Again, when there's no 0 in the actual input combination the output is logical low just like how any NAND gate would work. [A=1, B=1, Y=logical low]

3. When both the inputs are 0, the value of V_P is 0.7 as we know diodes need 0.7V to conduct current. As a result, $V_B = 0.7 - 0.7 - 0.7 = -0.7V$ but we need 0.7V for the transistor to get turned ON. This then gets us logical high or 5V as the output as the transistor is OFF. The same thing happens whenever

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there's a 0 in the ~~inp~~ input i.e. we get 5 as the output.

However, when both the inputs are 1, the value of V_p is greater 2.1 V which is enough to turn the transistor ON.

[$2.1-0.7-0.7=0.7=V_B$].

4. We know that when one of the inputs is high and the other one is low, the transistor is in cutoff mode and we need 0.7 V to turn the transistor ON.

If we set A=0, B=5 we see from proteus data that the voltage of the base of the transistor is −0.500605 V but it needs to be 0.7 V for the transistor to be in saturation mode. So, we can say the transistor is in cutoff mode.

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The same happens when we set A=5 and B=0.

5. If we fix the value of A as 5V and set the value of B as 0V we see the output is logical high. If we increase the value of B by 0.5 V we still get logical high as the output. If we increase the value by 0.5 V more i.e. set the value of B as 1 V we get 4.99 V and that is still high. If we increase the input value 0.1 V more we get 4.94 V as the output and this too is high. However, when we set the value of B as 1.2 ~~5~~ V, we get ~~2.18~~ 2.86 as the output which is low. So, the maximum value of B is 1.1 V when A is ~~0~~ 5 and the maximum value of A is 1.1 V when B is 5 V. to keep the output high.

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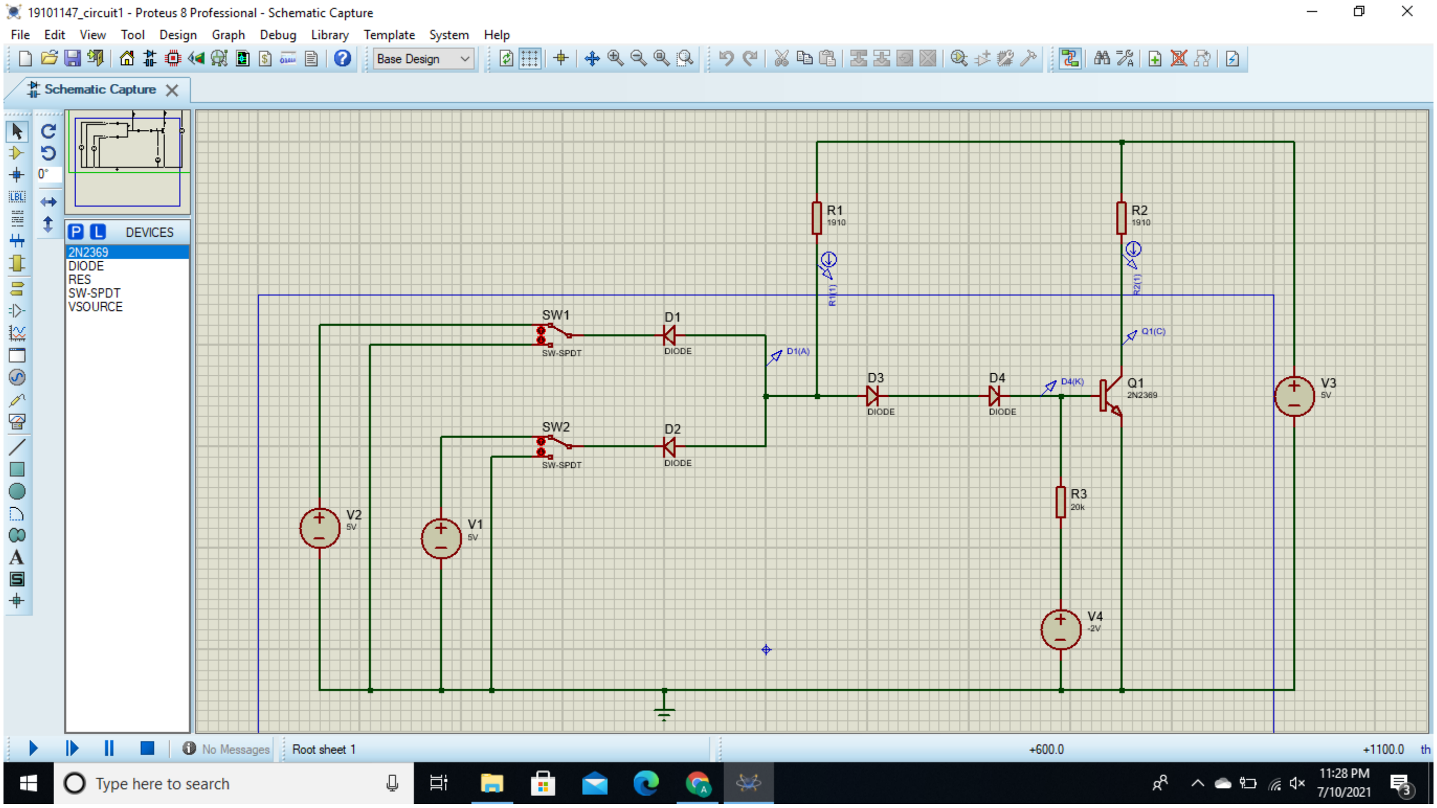
19101147_circuit1 - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Base Design
Schematic Capture
DEVICES
2N2369
DIODE
RES
SW-SPDT
VSOURCE
SW1
SW-SPDT
D1
DIODE
SW2
SW-SPDT
D2
DIODE
R1
1910
R2
1910
D1(A)
D3
DIODE
D4
DIODE
D4(K)
Q1(C)
Q1
2N2369
R3
20k
V1
5V
V2
5V
V3
5V
V4
-2V
No Messages
Root sheet 1
+600.0
+1100.0
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