CSE460: VLSI Design

Lab Assignment 3

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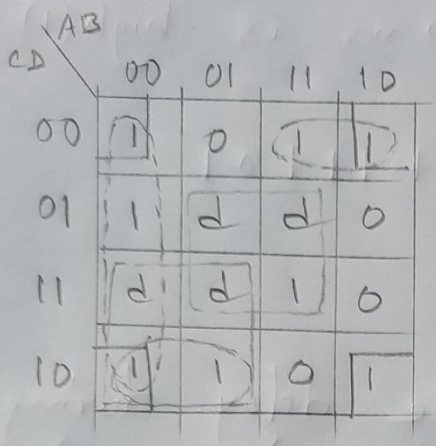
Sec: 09

1.



∴ Logic expression = $A'B' + B'D' + AC'D' + A'C + BD$

Bits	Value	Output	Timestamp
ABCD	1001	0	90 ns
ABCD	1011	0	110 ns
ABCD	0011	1	30 ns
ABCD	1000	1	80 ns

The value at 90 ns is low (0)

as,

$0.1 + 1.0 + 1.1.0 + 0.0 + 0.1$

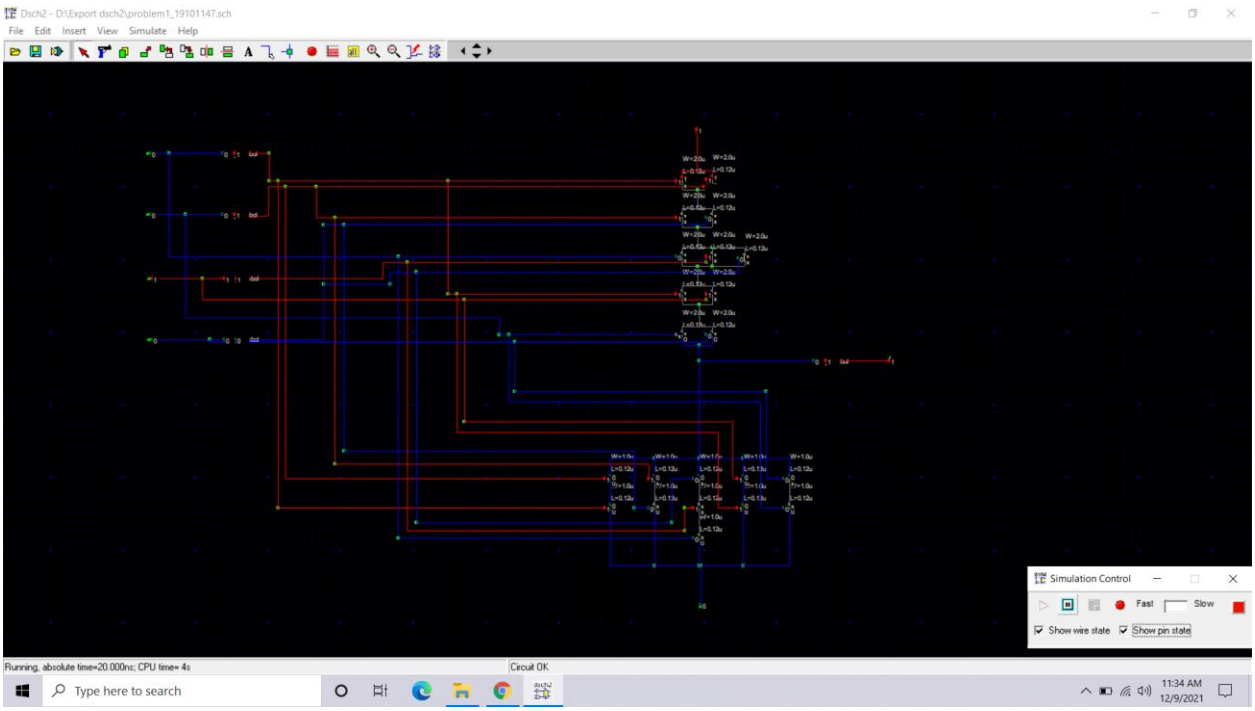
$= 0$

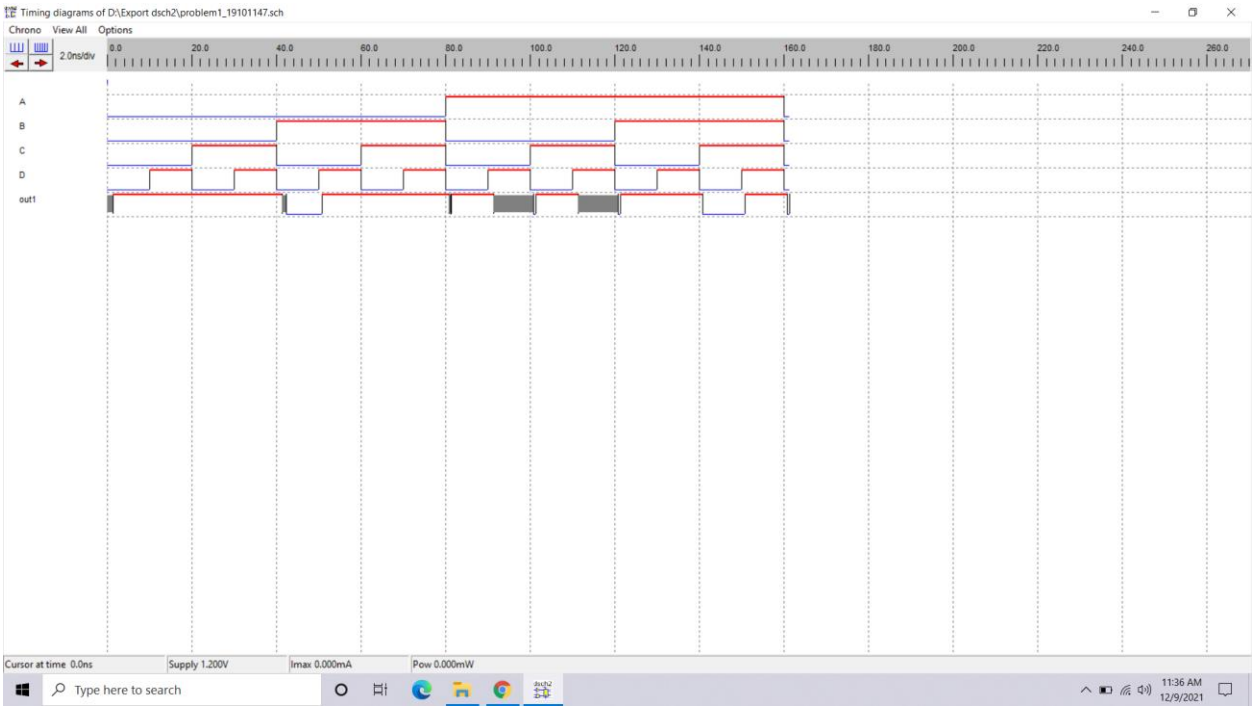
The value at 30 ns is high(1) as

$$1.1 + 1.0 + 0.0.0 + 1.1 + 0.1$$

$$= 1$$

There is a little delay during the output. However, during 90 and 110 ns the delay is too much when the output is low.


Dsch2 - D:\Export dsch2\problem1_19101147.sch
File Edit Insert View Simulate Help
Simulation Control
Fast
Slow
Show wire state
Show pin state
Running, absolute time=20.000ns; CPU time= 4s
Circuit OK
Type here to search
11:34 AM
12/9/2021


Timing diagrams of D:\Export dsch2\problem1_19101147.sch
Chrono View All Options
2.0ns/div
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
180.0
200.0
220.0
240.0
260.0
A
B
C
D
out1
Cursor at time 0.0ns
Supply 1.200V
Imax 0.000mA
Pow 0.000mW
Type here to search
11:36 AM
12/9/2021

2.

$f(A, B, C, D, E) = \Sigma(0, 4, 5, 8, 9, 12, 15, 21, 22, 29, 30)$; don't care 7

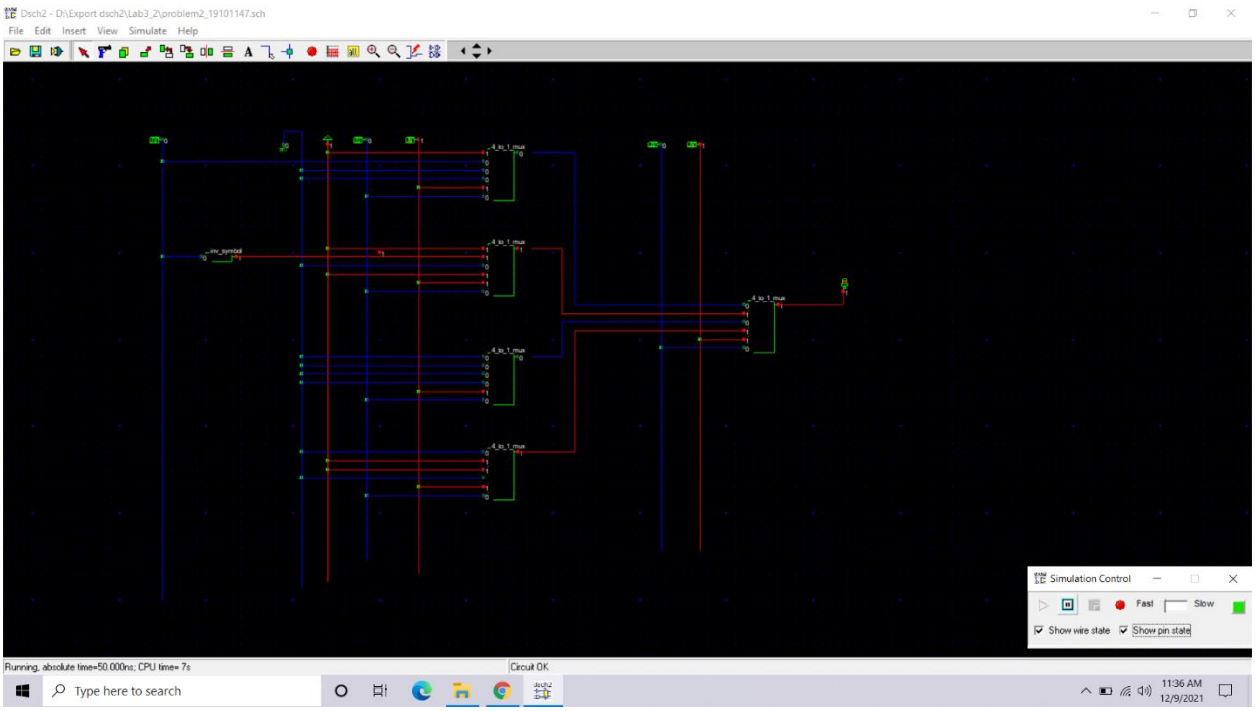
Input Pin	A	C	D	E	B′	B	Data Input
I_0	0	0	0	0	0	8	1
I_1	0	0	0	1	1	9	B
I_2	0	0	1	0	2	10	0
I_3	0	0	1	1	3	11	0
I_4	0	1	0	0	4	12	1
I_5	0	1	0	1	5	13	B′
I_6	0	1	1	0	6	14	0
I_7	0	1	1	1	7	15	B or 1
I_8	1	0	0	0	16	24	0
I_9	1	0	0	1	17	25	0
I_{10}	1	0	1	0	18	26	0
I_{11}	1	0	1	1	19	27	0
I_{12}	1	1	0	0	20	28	0
I_{13}	1	1	0	1	21	29	1
I_{14}	1	1	1	0	22	30	1
I_{15}	1	1	1	1	23	31	0

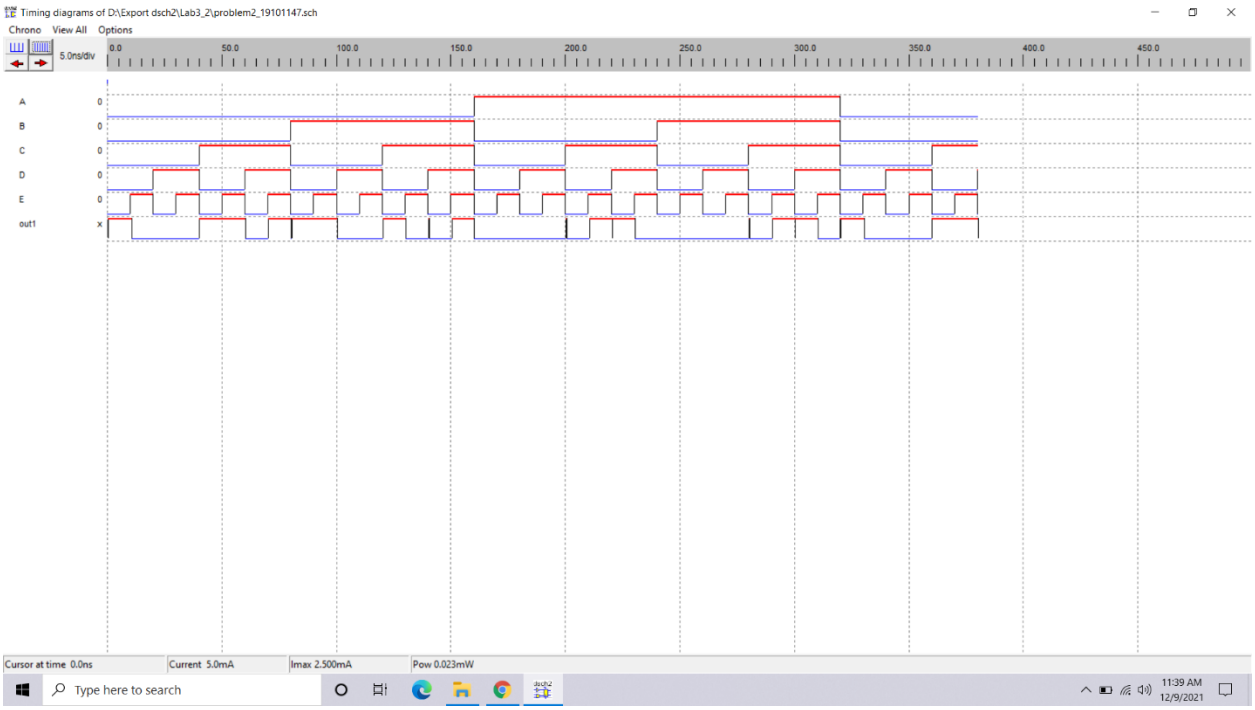
Selector Bits	Input Bits		Output	Timestamp
A C D E	B	B'		
0 0 0 0	0	1	1	0 ns
0 0 0 1	0	1	0	10 ns
0 1 0 1	0	1	1	50 ns
0 1 1 1	0	1	1	70 ns
1 1 0 1	1	0	1	290 ns
1 1 1 0	1	0	1	300 ns

At 0 ns when ACDE is 0000, data input is 1 and we get output 1.

At 10 ns when ACDE is 0001, data input is B. We get output 0 as, B = 0.

At 50 ns when ACDE is 0101, data input is B'. and we get output 1 as B = 0.


Dsch2 - D:\Export dsch2\Lab3_2\problem2_19101147.sch
File Edit Insert View Simulate Help
4_to_1_mux
inv_symbol
Simulation Control
Fast
Slow
Show wire state
Show pin state
Running, absolute time=50.000ns; CPU time= 7s
Circuit OK
Type here to search
11:36 AM
12/9/2021

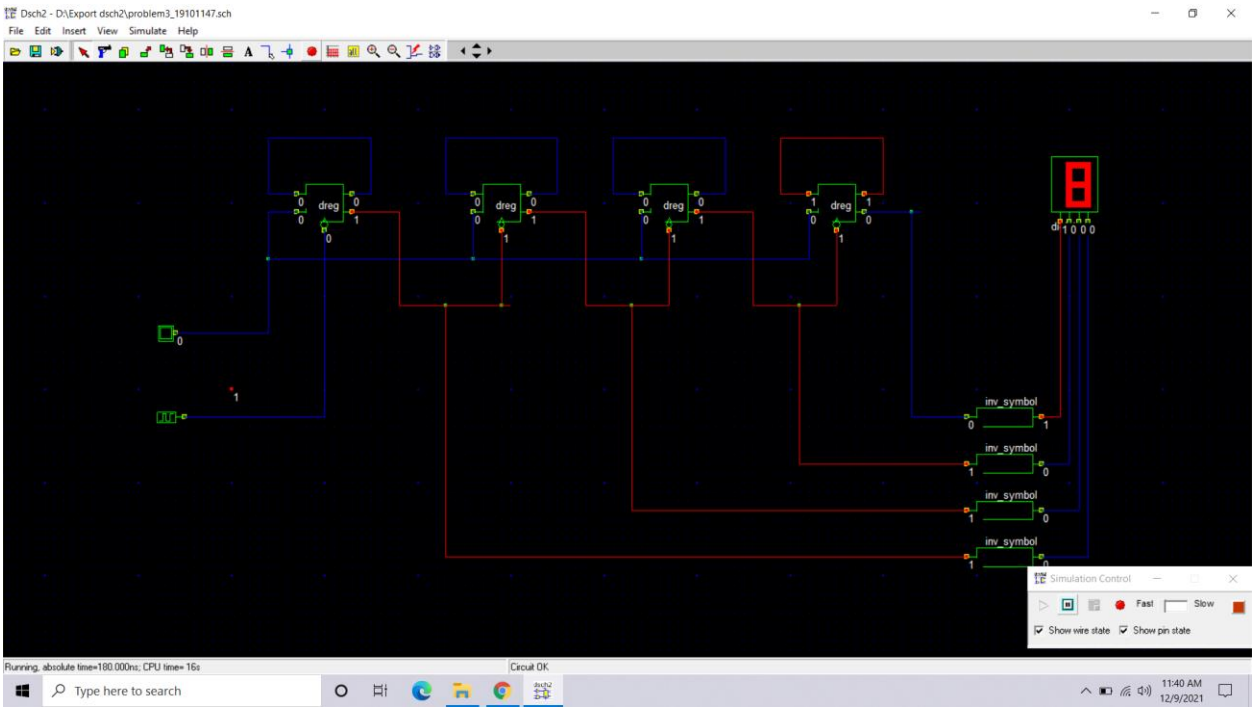

Timing diagrams of D:\Export dsch2\Lab3_2\problem2_19101147.sch
Chrono View All Options
5.0ns/div
0.0
50.0
100.0
150.0
200.0
250.0
300.0
350.0
400.0
450.0
A
B
C
D
E
out1
Cursor at time 0.0ns
Current 5.0mA
Imax 2.500mA
Pow 0.023mW
Type here to search
11:39 AM
12/9/2021

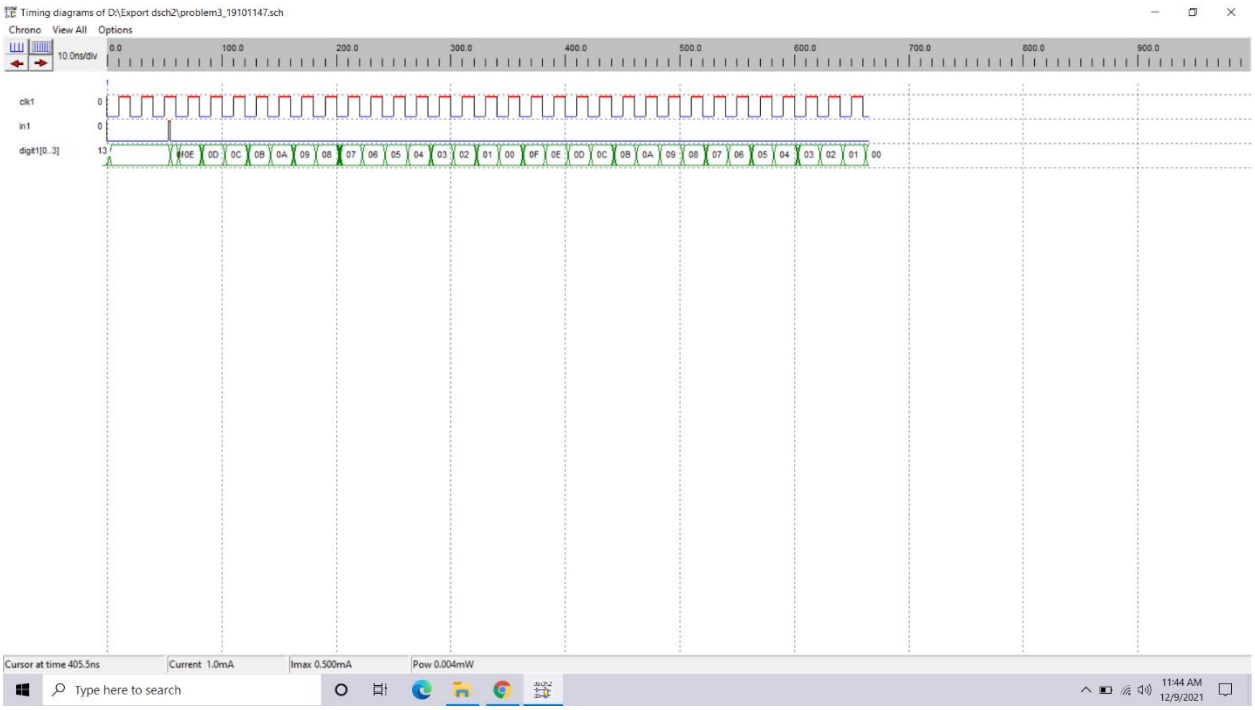
3.

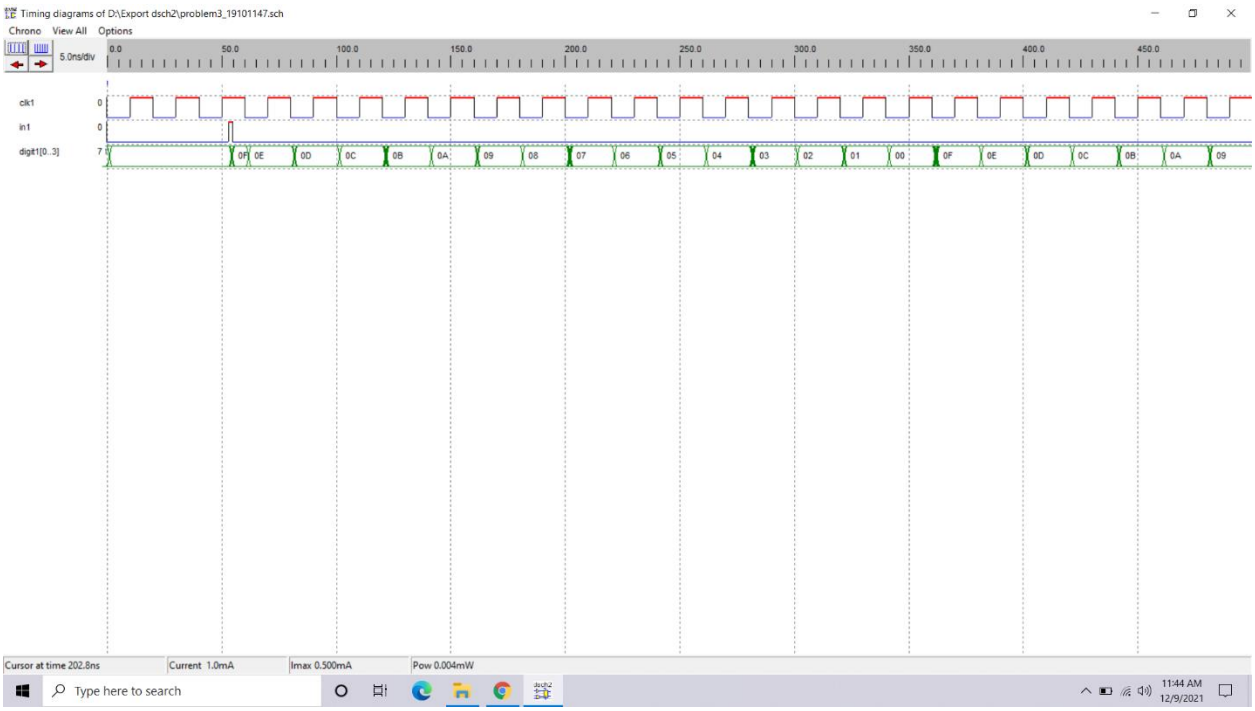
Timestamp	Output
around 54 ns	F
around 61 ns	E
around 81 ns	D
around 101 ns	C
around 121 ns	B
around 141 ns	A
around 161 ns	9
around 181 ns	8
around 201 ns	7
around 221 ns	6
around 241 ns	5
around 261 ns	4
around 281 ns	3
around 301 ns	2
around 321 ns	1
around 341 ns	0

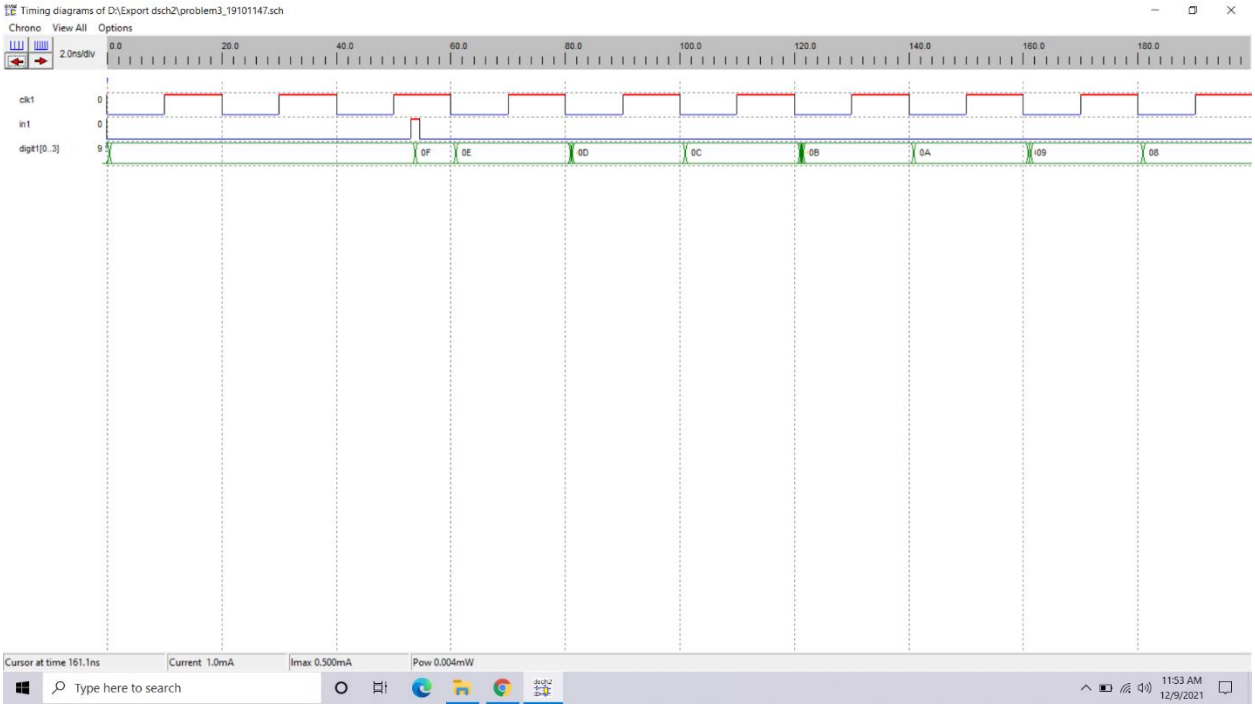
A suitable clock frequency has been chosen so that the simulation takes place for a minimum of two counting cycles.

From the timing diagram we can see there are some delay. We don't see any output after starting the simulation. We need to turn the reset button ON and then turn it OFF to see results. At around 51 ns we get the first output i.e. F. Then at 361 ns we get F for the second time. We get the first E at around 61 ns and the first D at around 81 ns. So, we can see it takes 20 ns for a number to change.


Dsch2 - D:\Export dsch2\problem3_19101147.sch
File Edit Insert View Simulate Help
dreg
inv_symbol
Simulation Control
Fast
Slow
Show wire state
Show pin state
Running, absolute time=180.000ns; CPU time= 16s
Circuit OK
Type here to search
11:40 AM
12/9/2021


Timing diagrams of D:\Export dsch2\problem3_19101147.sch
Chrono View All Options
10.0ns/div
clk1
in1
digit1[0..3]
Cursor at time 405.5ns
Current 1.0mA
Imax 0.500mA
Pow 0.004mW
Type here to search
11:44 AM
12/9/2021


Timing diagrams of D:\Export dsch2\problem3_19101147.sch
Chrono View All Options
5.0ns/div
0.0 50.0 100.0 150.0 200.0 250.0 300.0 350.0 400.0 450.0
clk1
in1
digit1[0..3]
0F 0E 0D 0C 0B 0A 09 08 07 06 05 04 03 02 01 00 0F 0E 0D 0C 0B 0A 09
Cursor at time 202.8ns
Current 1.0mA
Imax 0.500mA
Pow 0.004mW
Type here to search
11:44 AM
12/9/2021


Timing diagrams of D:\Export dsch2\problem3_19101147.sch
Chrono View All Options
2.0ns/div
0.0 20.0 40.0 60.0 80.0 100.0 120.0 140.0 160.0 180.0
clk1
in1
digit1[0..3]
0F 0E 0D 0C 0B 0A 09 08
Cursor at time 161.1ns
Current 1.0mA
Imax 0.500mA
Pow 0.004mW
Type here to search
11:53 AM
12/9/2021