CSE460: VLSI Design

Lab Assignment 2

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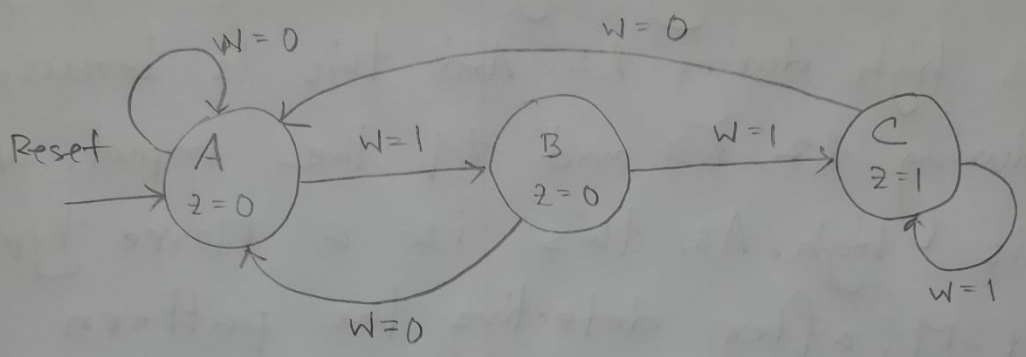
ID: 19101147

Sec: 09

1.



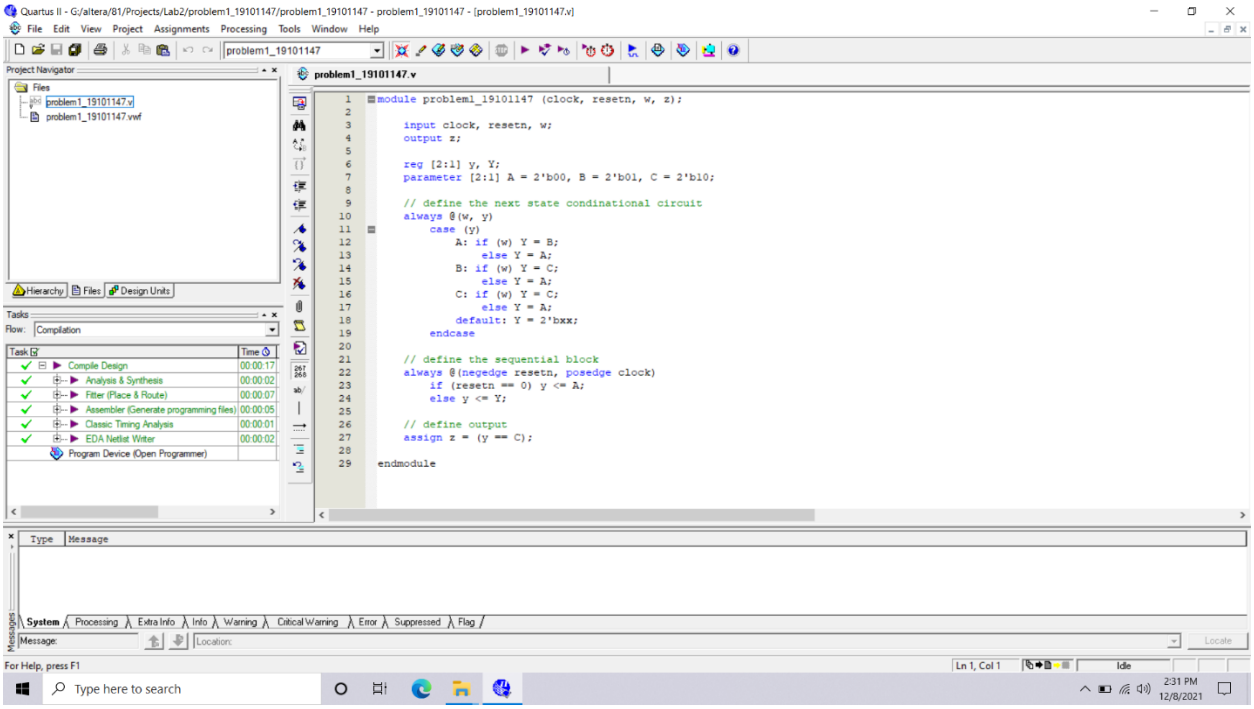
Present state	Next state		Output
	W = 0	W = 1	
$y_2 y_1$	$Y_2 Y_1$	$Y_2 Y_1$	z
A 00	00	01	0
B 01	00	10	0
C 10	00	10	1

In the timing diagram the output is high during t_4 and the input is high during t_2 and t_3. We get output 1 for the input pattern 11 in the state diagram. Hence, the output during t_4 is high.

In t_2, t_3 and t_4 the input is high i.e. the input pattern is 111. We get output 1 for the pattern 111 from the state diagram. As a result, the output during t_5 is high.

The input during t_8 and t_9 is high. As, the state diagram accepts the pattern 11, the output during t_{10} is high.

Again, the state diagram accepts the input pattern 111. As a result, ~~is hi~~ the output is high during t11 because of t8, t9 and t10 and the output is high during t12 because of t9, t10 and t11.


Quartus II - G:/altera/81/Projects/Lab2/problem1_19101147/problem1_19101147 - problem1_19101147 - [problem1_19101147.v]
File Edit View Project Assignments Processing Tools Window Help
problem1_19101147
Project Navigator
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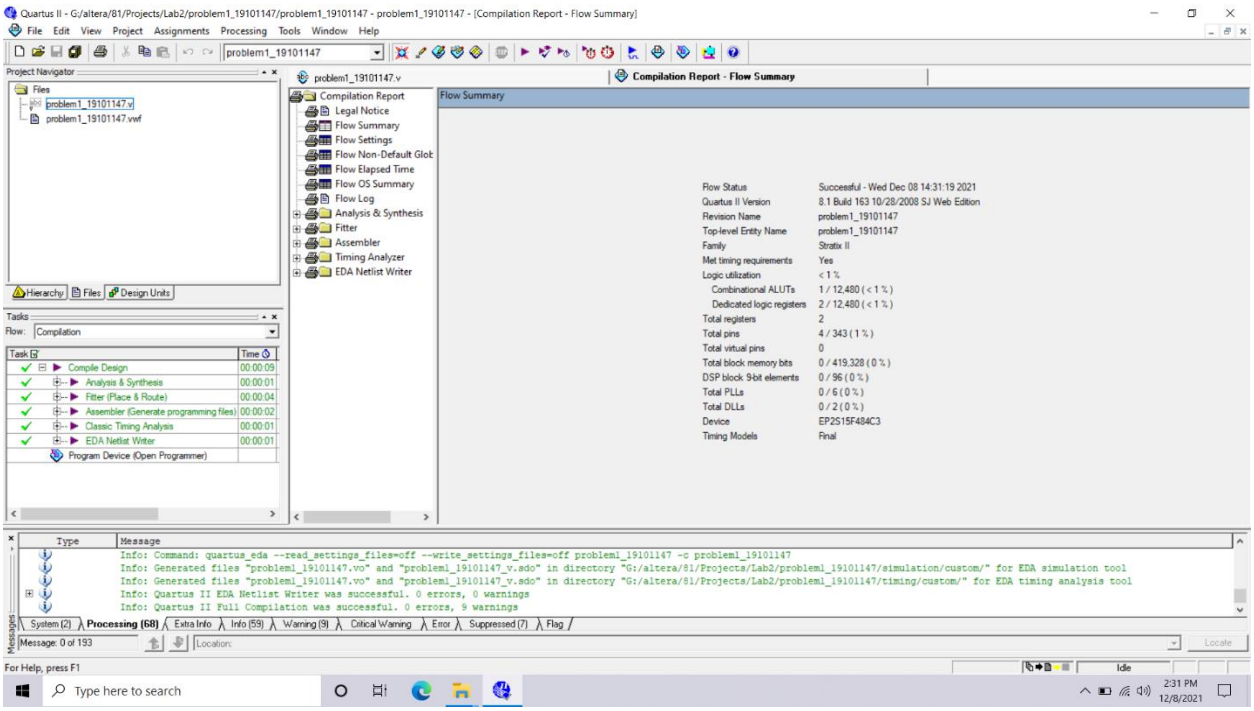
problem1_19101147.vwf
Hierarchy Files Design Units
Tasks
Flow: Compilation
Task Time
Compile Design 00:00:17
Analysis & Synthesis 00:00:02
Fitter (Place & Route) 00:00:07
Assembler (Generate programming files) 00:00:05
Classic Timing Analysis 00:00:01
EDA Netlist Writer 00:00:02
Program Device (Open Programmer)
problem1_19101147.v
1 module problem1_19101147 (clock, resetn, w, z);
3 input clock, resetn, w;
4 output z;
6 reg [2:1] y, Y;
7 parameter [2:1] A = 2'b00, B = 2'b01, C = 2'b10;
9 // define the next state condinational circuit
10 always @(w, y)
11 case (y)
12 A: if (w) Y = B;
13 else Y = A;
14 B: if (w) Y = C;
15 else Y = A;
16 C: if (w) Y = C;
17 else Y = A;
18 default: Y = 2'bxx;
19 endcase
21 // define the sequential block
22 always @(negedge resetn, posedge clock)
23 if (resetn == 0) y <= A;
24 else y <= Y;
26 // define output
27 assign z = (y == C);
29 endmodule
Type Message
System Processing Extra Info Info Warning Critical Warning Error Suppressed Flag
Message:
Location:
For Help, press F1
Ln 1, Col 1
Idle
Type here to search
2:31 PM
12/8/2021


Quartus II - G:/altera/81/Projects/Lab2/problem1_19101147/problem1_19101147 - problem1_19101147 - [Compilation Report - Flow Summary]
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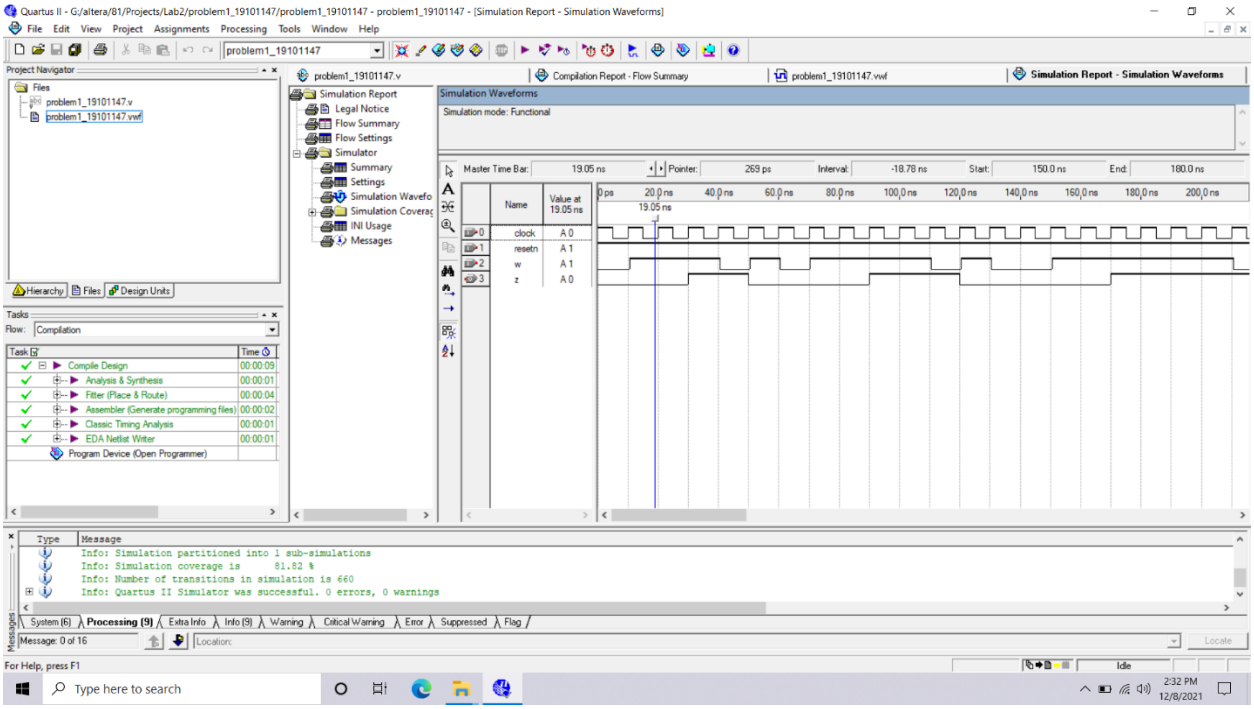
Timing Analyzer
EDA Netlist Writer
Flow Summary
Flow Status Successful - Wed Dec 08 14:31:19 2021
Quartus II Version 8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name problem1_19101147
Top-level Entity Name problem1_19101147
Family Stratix II
Met timing requirements Yes
Logic utilization < 1 %
Combinational ALUTs 1 / 12,480 (< 1 %)
Dedicated logic registers 2 / 12,480 (< 1 %)
Total registers 2
Total pins 4 / 343 (1 %)
Total virtual pins 0
Total block memory bits 0 / 419,328 (0 %)
DSP block 9-bit elements 0 / 96 (0 %)
Total PLLs 0 / 6 (0 %)
Total DLLs 0 / 2 (0 %)
Device EP2S15F484C3
Timing Models Final
Type Message
Info: Command: quartus_eda --read_settings_files=off --write_settings_files=off problem1_19101147 -c problem1_19101147
Info: Generated files "problem1_19101147.vo" and "problem1_19101147_v.sdo" in directory "G:/altera/81/Projects/Lab2/problem1_19101147/simulation/custom/" for EDA simulation tool
Info: Generated files "problem1_19101147.vo" and "problem1_19101147_v.sdo" in directory "G:/altera/81/Projects/Lab2/problem1_19101147/timing/custom/" for EDA timing analysis tool
Info: Quartus II EDA Netlist Writer was successful. 0 errors, 0 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 9 warnings
System (2) Processing (68) Extra Info Info (59) Warning (9) Critical Warning Error Suppressed (7) Flag
Message: 0 of 193
Location:
For Help, press F1
Idle
Type here to search
2:31 PM
12/8/2021


Quartus II - G:/altera/81/Projects/Lab2/problem1_19101147/problem1_19101147 - problem1_19101147 - [Simulation Report - Simulation Waveforms]
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Simulation Coverag
INI Usage
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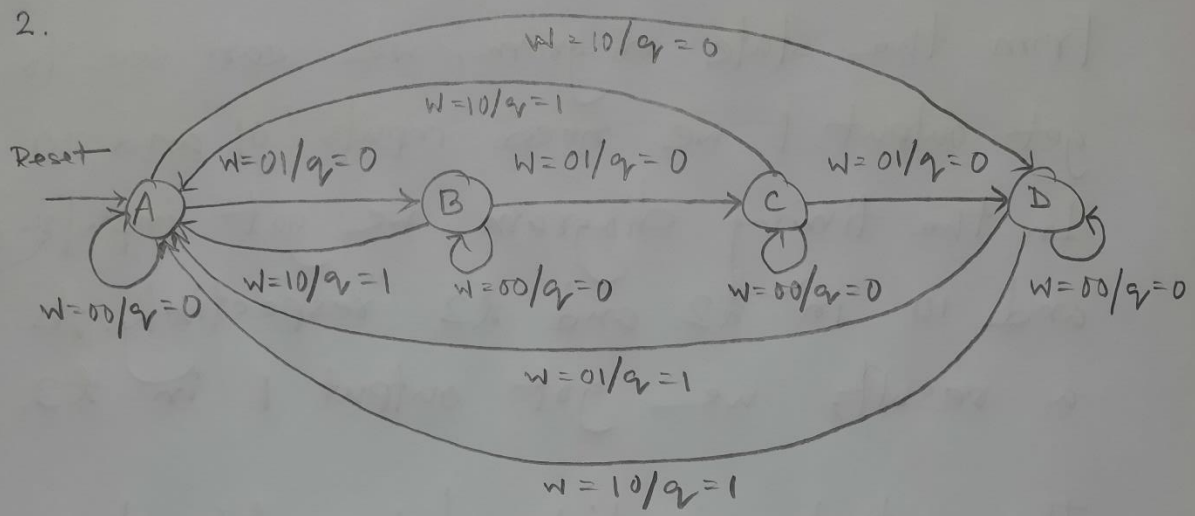
Simulation Waveforms
Simulation mode: Functional
Master Time Bar: 19.05 ns
Pointer: 269 ps
Interval: -18.78 ns
Start: 150.0 ns
End: 180.0 ns
Name
Value at 19.05 ns
clock A 0
resetn A 1
w A 1
z A 0
0 ps 20.0 ns 40.0 ns 60.0 ns 80.0 ns 100.0 ns 120.0 ns 140.0 ns 160.0 ns 180.0 ns 200.0 ns
19.05 ns
Type Message
Info: Simulation partitioned into 1 sub-simulations
Info: Simulation coverage is 81.82 %
Info: Number of transitions in simulation is 660
Info: Quartus II Simulator was successful. 0 errors, 0 warnings
System (6) Processing (9) Extra Info Info (9) Warning Critical Warning Error Suppressed Flag
Message: 0 of 16
Location:
Locate
For Help, press F1
Idle
Type here to search
2:32 PM
12/8/2021

2.



Present state	Next state			output		
	w=00	w=01	w=10	w=00	w=01	w=10
y_2y_1	Y_2Y_1	Y_2Y_1	Y_2Y_1	z	z	z
A 00	00	01	11	0	0	0
B 01	01	10	00	0	0	1
C 10	10	11	00	0	0	1
D 11	11	00	00	0	0	1

From the state diagram, we can see to get output 1 we need inputs 01 and 10. In the timing diagram we got inputs 01 and 10 in t2 and t3 respectively. As a result, we got output 1 in t3.

The output is high during t6 also. In t5 and t6, the inputs are 10 and 01. From the state diagram we can see that to get output 1 the input combination 10 and 01 is also acceptable.

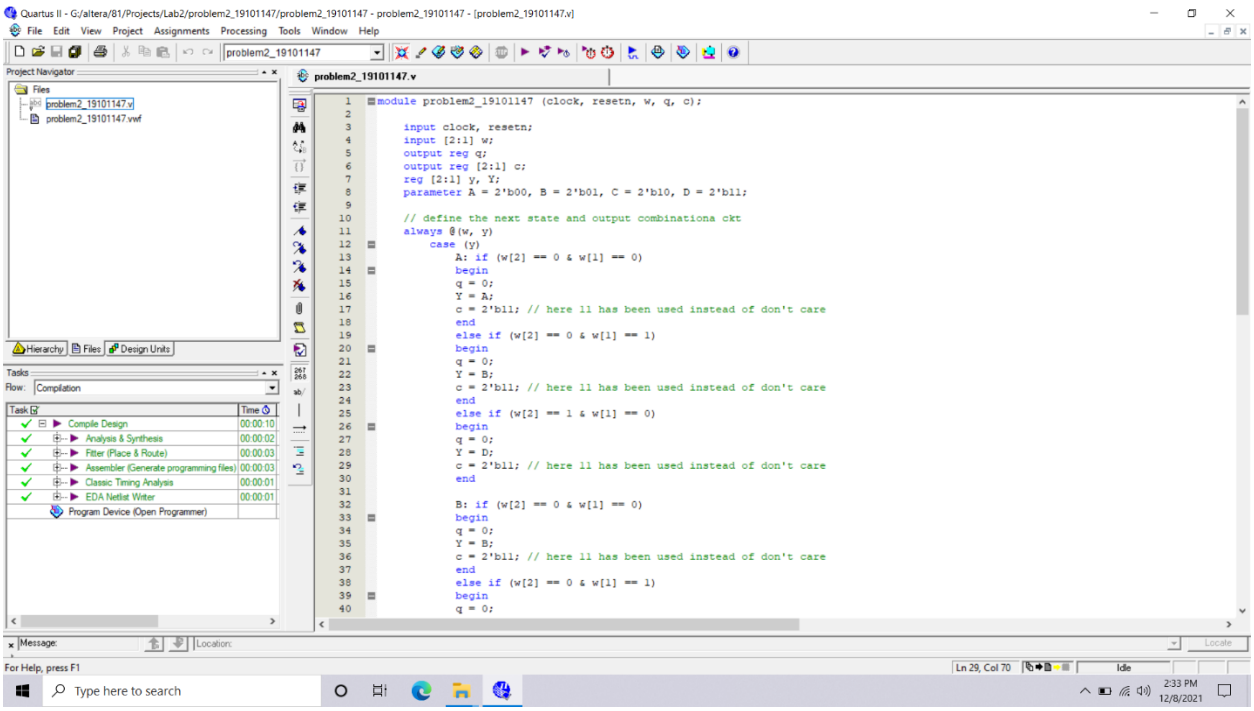
from the state diagram, we can see the ~~outp~~ input combination 10 and 10 is acceptable to get output 1. And in the timing diagram the inputs are 10 and 10 in t8 and t9. As a result, we got output high in t9.

From the state diagram, we can see the change is required when the input is 5 i.e. when we go from state C to state A and when the input is 6 i.e. when we go from state D to A for input, w=10.

We set c=00 when we go from state C to A and c=01 when we go from state D to A for input w=10.

We don't care about other cases. So, we can use don't care for other cases. However, c=11 has been used in the verilog code instead. In the timing diagram wherever there is c=3, that means there is no change required.

Again, in the timing diagram we see there is c=1 sometimes. That is when the input is The 6. And sometimes c is 0. That's when the input is equal to The 5.


Quartus II - G:/altera/81/Projects/Lab2/problem2_19101147/problem2_19101147 - problem2_19101147 - [problem2_19101147.v]
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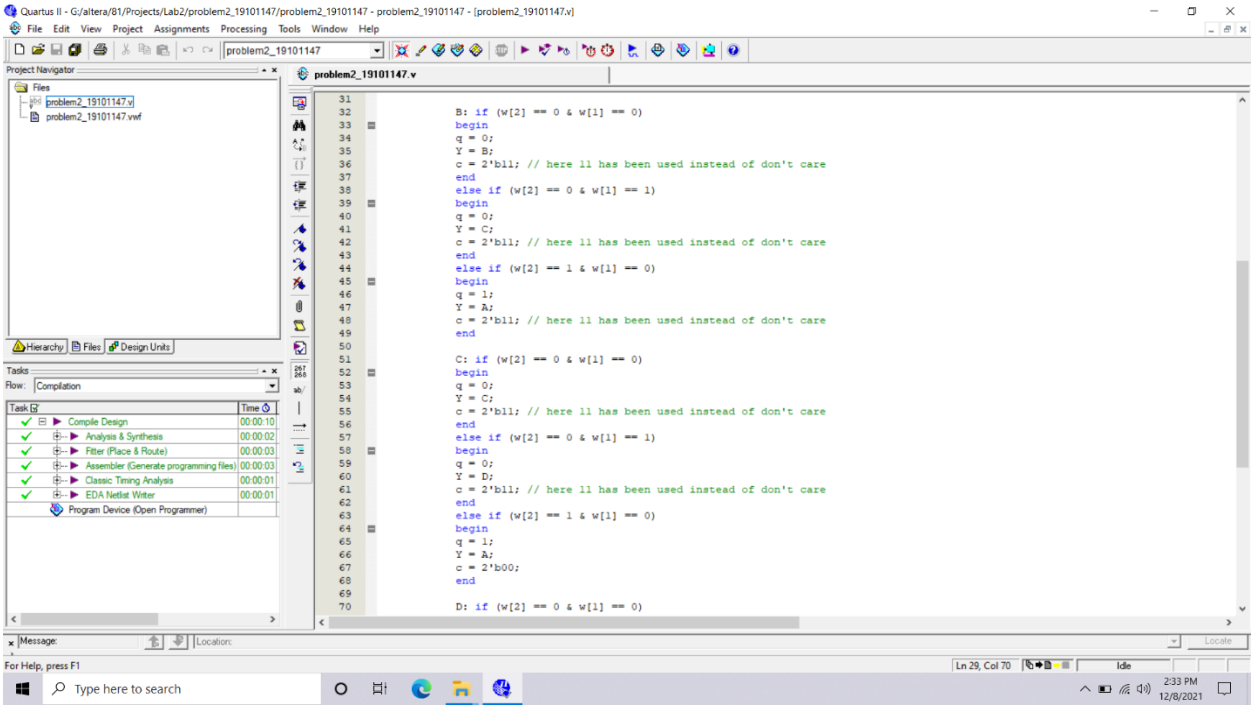
Assembler (Generate programming files) 00:00:03
Classic Timing Analysis 00:00:01
EDA Netlist Writer 00:00:01
Program Device (Open Programmer)
problem2_19101147.v
1 module problem2_19101147 (clock, resetn, w, q, c);
3 input clock, resetn;
4 input [2:1] w;
5 output reg q;
6 output reg [2:1] c;
7 reg [2:1] y, Y;
8 parameter A = 2'b00, B = 2'b01, C = 2'b10, D = 2'b11;
10 // define the next state and output combinationa ckt
11 always @(w, y)
12 case (y)
13 A: if (w[2] == 0 & w[1] == 0)
14 begin
15 q = 0;
16 Y = A;
17 c = 2'b11; // here 11 has been used instead of don't care
18 end
19 else if (w[2] == 0 & w[1] == 1)
20 begin
21 q = 0;
22 Y = B;
23 c = 2'b11; // here 11 has been used instead of don't care
24 end
25 else if (w[2] == 1 & w[1] == 0)
26 begin
27 q = 0;
28 Y = D;
29 c = 2'b11; // here 11 has been used instead of don't care
30 end
32 B: if (w[2] == 0 & w[1] == 0)
33 begin
34 q = 0;
35 Y = B;
36 c = 2'b11; // here 11 has been used instead of don't care
37 end
38 else if (w[2] == 0 & w[1] == 1)
39 begin
40 q = 0;
Message:
Location:
For Help, press F1
Ln 29, Col 70
Idle
Type here to search
2:33 PM
12/8/2021


Quartus II - G:/altera/81/Projects/Lab2/problem2_19101147/problem2_19101147 - problem2_19101147 - [problem2_19101147.v]
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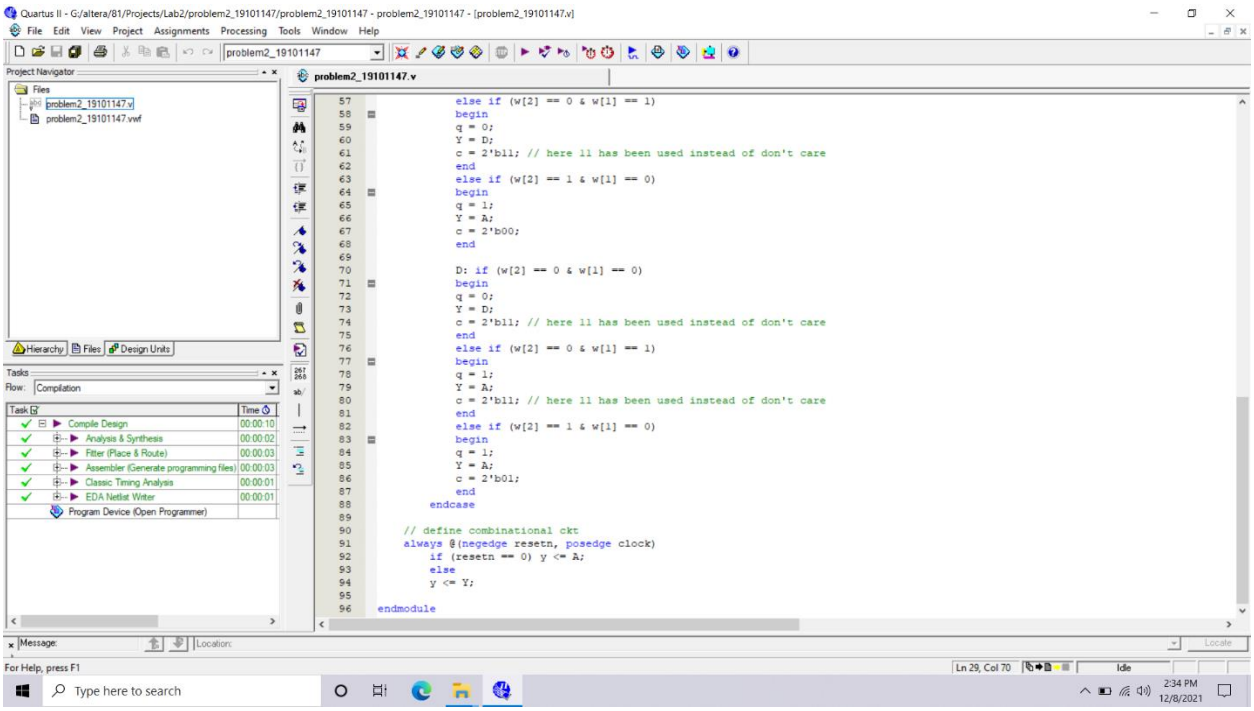
Classic Timing Analysis 00:00:01
EDA Netlist Writer 00:00:01
Program Device (Open Programmer)
problem2_19101147.v
32 B: if (w[2] == 0 & w[1] == 0)
33 begin
34 q = 0;
35 Y = B;
36 c = 2'b11; // here 11 has been used instead of don't care
37 end
38 else if (w[2] == 0 & w[1] == 1)
39 begin
40 q = 0;
41 Y = C;
42 c = 2'b11; // here 11 has been used instead of don't care
43 end
44 else if (w[2] == 1 & w[1] == 0)
45 begin
46 q = 1;
47 Y = A;
48 c = 2'b11; // here 11 has been used instead of don't care
49 end
51 C: if (w[2] == 0 & w[1] == 0)
52 begin
53 q = 0;
54 Y = C;
55 c = 2'b11; // here 11 has been used instead of don't care
56 end
57 else if (w[2] == 0 & w[1] == 1)
58 begin
59 q = 0;
60 Y = D;
61 c = 2'b11; // here 11 has been used instead of don't care
62 end
63 else if (w[2] == 1 & w[1] == 0)
64 begin
65 q = 1;
66 Y = A;
67 c = 2'b00;
68 end
70 D: if (w[2] == 0 & w[1] == 0)
Message:
Location:
For Help, press F1
Ln 29, Col 70
Idle
Type here to search
2:33 PM
12/8/2021


Quartus II - G:/altera/81/Projects/Lab2/problem2_19101147/problem2_19101147 - problem2_19101147 - [problem2_19101147.v]
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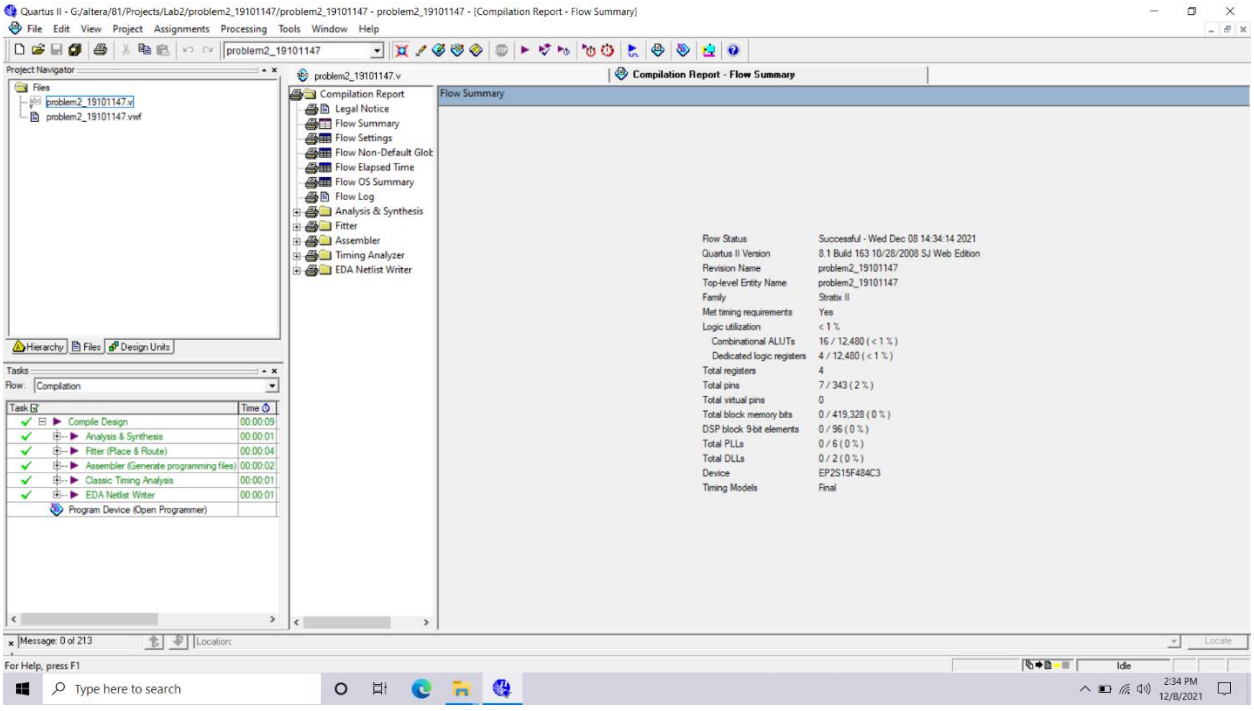
Classic Timing Analysis 00:00:01
EDA Netlist Writer 00:00:01
Program Device (Open Programmer)
problem2_19101147.v
else if (w[2] == 0 & w[1] == 1)
begin
q = 0;
Y = D;
c = 2'b11; // here 11 has been used instead of don't care
end
else if (w[2] == 1 & w[1] == 0)
begin
q = 1;
Y = A;
c = 2'b00;
end
D: if (w[2] == 0 & w[1] == 0)
begin
q = 0;
Y = D;
c = 2'b11; // here 11 has been used instead of don't care
end
else if (w[2] == 0 & w[1] == 1)
begin
q = 1;
Y = A;
c = 2'b11; // here 11 has been used instead of don't care
end
else if (w[2] == 1 & w[1] == 0)
begin
q = 1;
Y = A;
c = 2'b01;
end
endcase
// define combinational ckt
always @(negedge resetn, posedge clock)
if (resetn == 0) y <= A;
else
y <= Y;
endmodule
Message:
Location:
For Help, press F1
Ln 29, Col 70
Idle
Type here to search
2:34 PM
12/8/2021


Quartus II - G:/altera/81/Projects/Lab2/problem2_19101147/problem2_19101147 - problem2_19101147 - [Compilation Report - Flow Summary]
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EDA Netlist Writer 00:00:01
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Flow OS Summary
Flow Log
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Timing Analyzer
EDA Netlist Writer
Flow Summary
Flow Status Successful - Wed Dec 08 14:34:14 2021
Quartus II Version 8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name problem2_19101147
Top-level Entity Name problem2_19101147
Family Stratix II
Met timing requirements Yes
Logic utilization < 1 %
Combinational ALUTs 16 / 12,480 (< 1 %)
Dedicated logic registers 4 / 12,480 (< 1 %)
Total registers 4
Total pins 7 / 343 (2 %)
Total virtual pins 0
Total block memory bits 0 / 419,328 (0 %)
DSP block 9-bit elements 0 / 96 (0 %)
Total PLLs 0 / 6 (0 %)
Total DLLs 0 / 2 (0 %)
Device EP2S15F484C3
Timing Models Final
Message: 0 of 213
Location:
For Help, press F1
Idle
Type here to search
2:34 PM
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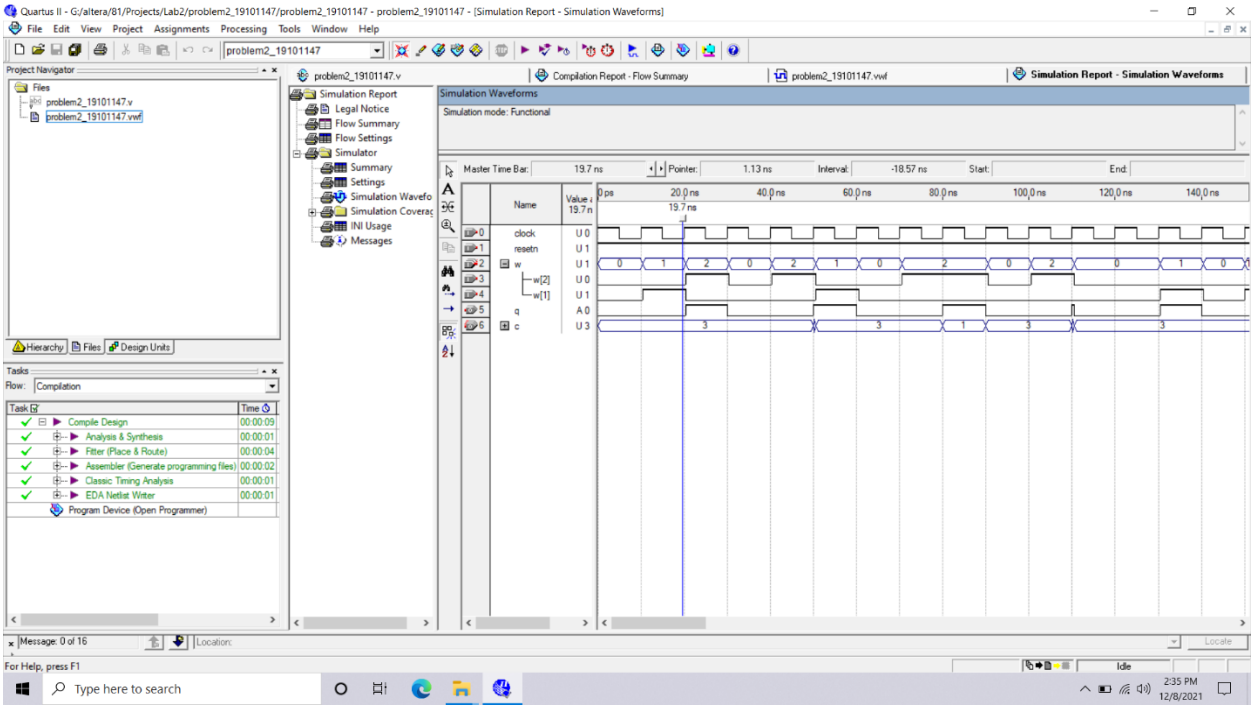
Quartus II - G:/altera/81/Projects/Lab2/problem2_19101147/problem2_19101147 - problem2_19101147 - [Simulation Report - Simulation Waveforms]
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Simulation Coverag
INI Usage
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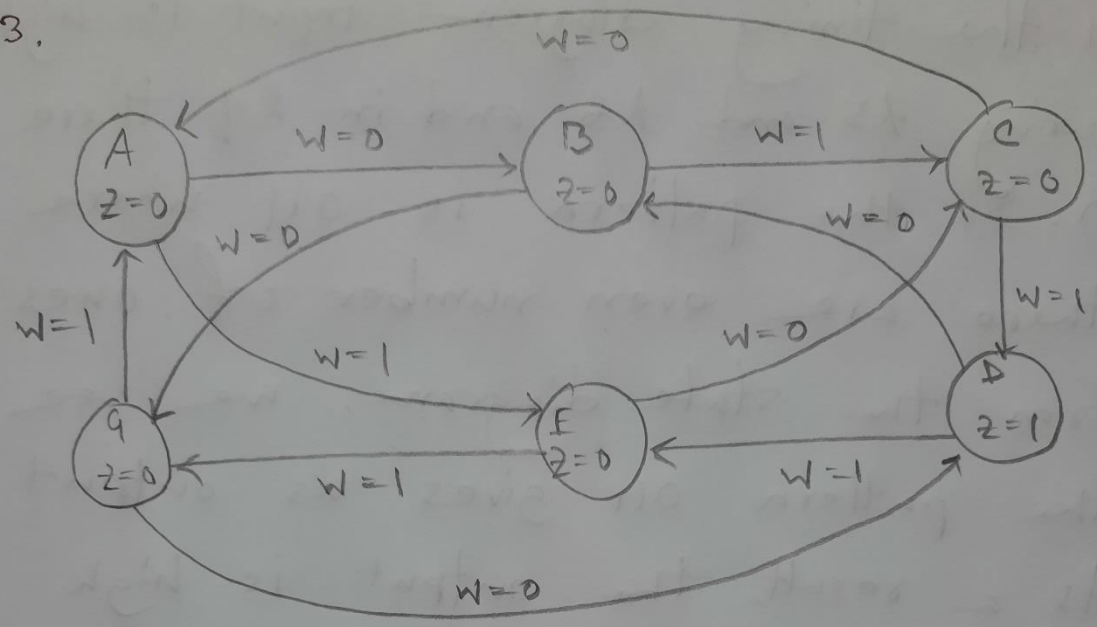
Simulation mode: Functional
Master Time Bar: 19.7 ns
Pointer: 1.13 ns
Interval: -18.57 ns
Start:
End:
Name
clock
reseth
w
w[2]
w[1]
q
c
0 ps
20.0 ns
40.0 ns
60.0 ns
80.0 ns
100.0 ns
120.0 ns
140.0 ns
19.7 ns
Message: 0 of 16
Location:
Locate
For Help, press F1
Idle
Type here to search
2:35 PM
12/8/2021

3.

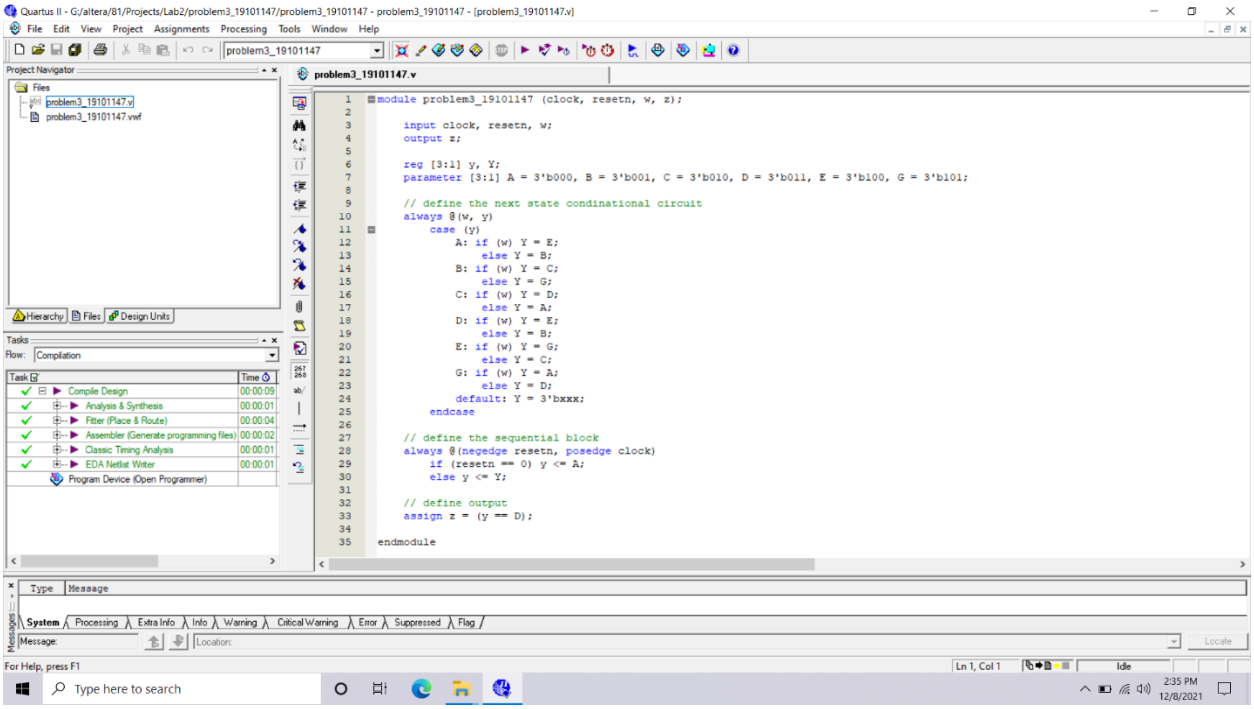


Present state	Next state W=0	Next state W=1	Output
$y_3y_2y_1$	$Y_3Y_2Y_1$	$Y_3Y_2Y_1$	z
A 000	001	100	0
B 001	101	010	0
C 010	000	011	0
D 011	001	100	1
E 100	010	101	0
G 101	011	000	0

In the timing diagram input is high during t5 and t6 and in t4 there is 0. So the pattern is 011 where there are even number of ones. from the state diagram, we see the pattern 011 gives us output 1. As a result, the output is high during t7.

from t10 to t12 the input pattern is 101. In the state diagram we get output 1 for the pattern 101. Hence, the output during t13 is high.

The inputs during t13, t14 and t15 are 0,1,1. From the state diagram we get output 1 for the input pattern 011 as the number of ones is even. That's why ~~input dur~~ output during t16 is high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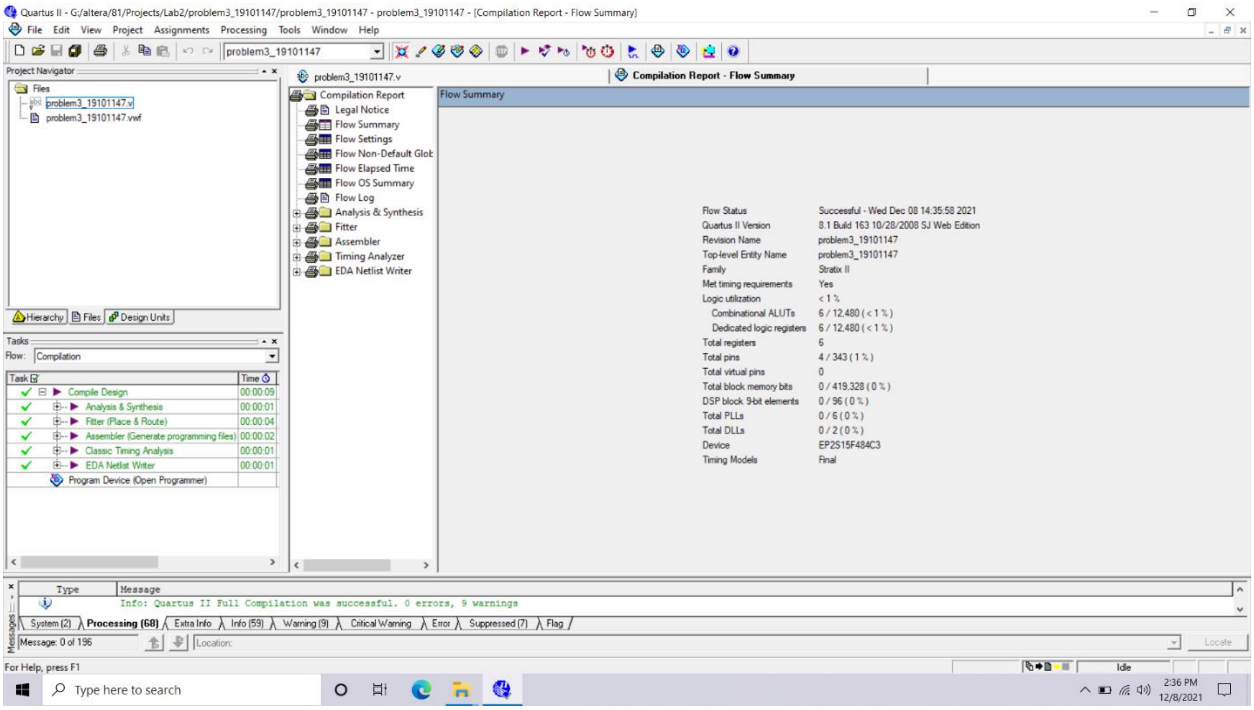
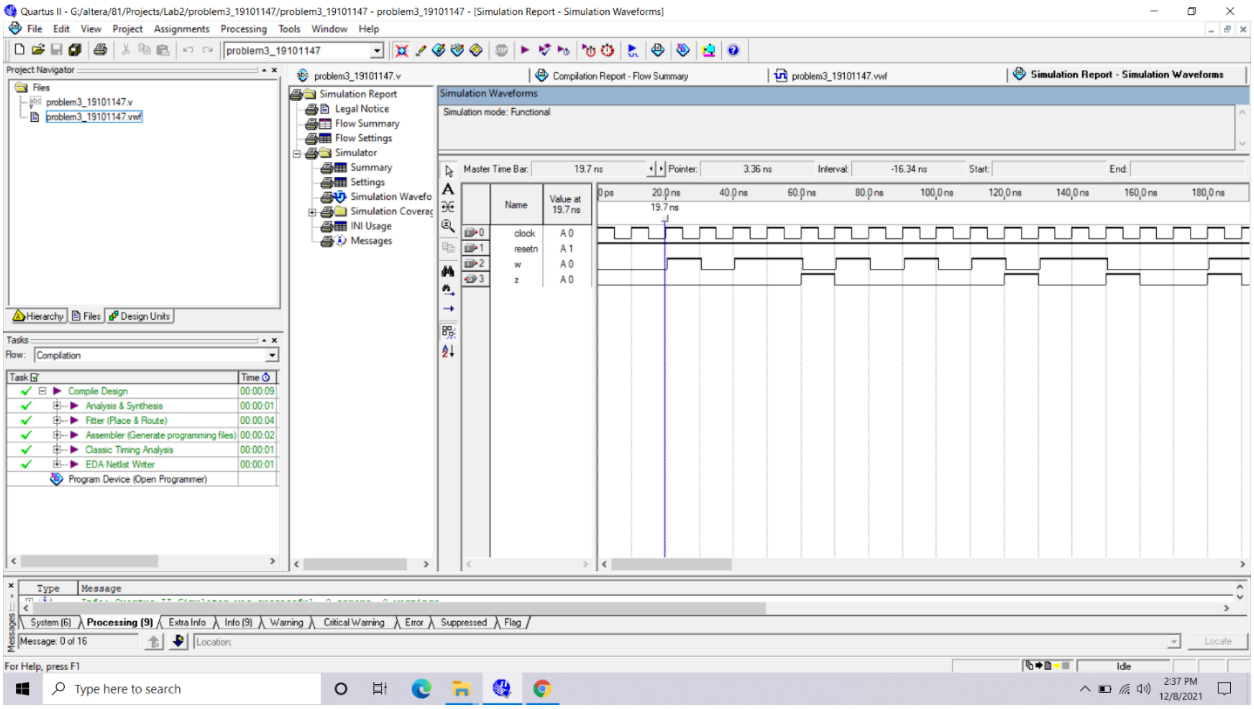
Program Device (Open Programmer)
problem3_19101147.v
1 module problem3_19101147 (clock, resetn, w, z);
3 input clock, resetn, w;
4 output z;
6 reg [3:1] y, Y;
7 parameter [3:1] A = 3'b000, B = 3'b001, C = 3'b010, D = 3'b011, E = 3'b100, G = 3'b101;
9 // define the next state condinational circuit
10 always @(w, y)
11 case (y)
12 A: if (w) Y = E;
13 else Y = B;
14 B: if (w) Y = C;
15 else Y = G;
16 C: if (w) Y = D;
17 else Y = A;
18 D: if (w) Y = E;
19 else Y = B;
20 E: if (w) Y = G;
21 else Y = C;
22 G: if (w) Y = A;
23 else Y = D;
24 default: Y = 3'bxxx;
25 endcase
27 // define the sequential block
28 always @(negedge resetn, posedge clock)
29 if (resetn == 0) y <= A;
30 else y <= Y;
32 // define output
33 assign z = (y == D);
35 endmodule
Type Message
System Processing Extra Info Info Warning Critical Warning Error Suppressed Flag
Message: Location:
For Help, press F1
Ln 1, Col 1
Idle
Type here to search
2:35 PM
12/8/2021


Quartus II - G:/altera/81/Projects/Lab2/problem3_19101147/problem3_19101147 - problem3_19101147 - [Compilation Report - Flow Summary]
File Edit View Project Assignments Processing Tools Window Help
problem3_19101147
Project Navigator
Files
problem3_19101147.v
problem3_19101147.vwf
Hierarchy Files Design Units
Tasks
Flow: Compilation
Task Time
Compile Design 00:00:09
Analysis & Synthesis 00:00:01
Fitter (Place & Route) 00:00:04
Assembler (Generate programming files) 00:00:02
Classic Timing Analysis 00:00:01
EDA Netlist Writer 00:00:01
Program Device (Open Programmer)
problem3_19101147.v
Compilation Report - Flow Summary
Compilation Report
Legal Notice
Flow Summary
Flow Settings
Flow Non-Default Glob
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Fitter
Assembler
Timing Analyzer
EDA Netlist Writer
Flow Summary
Flow Status Successful - Wed Dec 08 14:35:58 2021
Quartus II Version 8.1 Build 163 10/28/2008 SJ Web Edition
Revision Name problem3_19101147
Top-level Entity Name problem3_19101147
Family Stratix II
Met timing requirements Yes
Logic utilization < 1 %
Combinational ALUTs 6 / 12,480 (< 1 %)
Dedicated logic registers 6 / 12,480 (< 1 %)
Total registers 6
Total pins 4 / 343 (1 %)
Total virtual pins 0
Total block memory bits 0 / 419,328 (0 %)
DSP block 9-bit elements 0 / 96 (0 %)
Total PLLs 0 / 6 (0 %)
Total DLLs 0 / 2 (0 %)
Device EP2S15F484C3
Timing Models Final
Type Message
Info: Quartus II Full Compilation was successful. 0 errors, 9 warnings
System (2) Processing (68) Extra Info Info (59) Warning (9) Critical Warning Error Suppressed (7) Flag
Message: 0 of 196 Location:
For Help, press F1
Idle
Type here to search
2:36 PM
12/8/2021


Quartus II - G:/altera/81/Projects/Lab2/problem3_19101147/problem3_19101147 - problem3_19101147 - [Simulation Report - Simulation Waveforms]
File Edit View Project Assignments Processing Tools Window Help
problem3_19101147
Project Navigator
Files
problem3_19101147.v
problem3_19101147.vwf
Hierarchy Files Design Units
Tasks
Flow: Compilation
Task Time
Compile Design 00:00:09
Analysis & Synthesis 00:00:01
Fitter (Place & Route) 00:00:04
Assembler (Generate programming files) 00:00:02
Classic Timing Analysis 00:00:01
EDA Netlist Writer 00:00:01
Program Device (Open Programmer)
problem3_19101147.v
Compilation Report - Flow Summary
problem3_19101147.vwf
Simulation Report - Simulation Waveforms
Simulation Report
Legal Notice
Flow Summary
Flow Settings
Simulator
Summary
Settings
Simulation Wavefo
Simulation Coverag
INI Usage
Messages
Simulation Waveforms
Simulation mode: Functional
Master Time Bar: 19.7 ns
Pointer: 3.36 ns
Interval: -16.34 ns
Start:
End:
Name
Value at 19.7 ns
clock A 0
resetn A 1
w A 0
z A 0
0 ps 20.0 ns 40.0 ns 60.0 ns 80.0 ns 100.0 ns 120.0 ns 140.0 ns 160.0 ns 180.0 ns
19.7 ns
Type Message
System (6) Processing (9) Extra Info Info (9) Warning Critical Warning Error Suppressed Flag
Message: 0 of 16
Location:
Locate
For Help, press F1
Idle
Type here to search
2:37 PM
12/8/2021