CSE460: VLSI Design

Lab Assignment 1

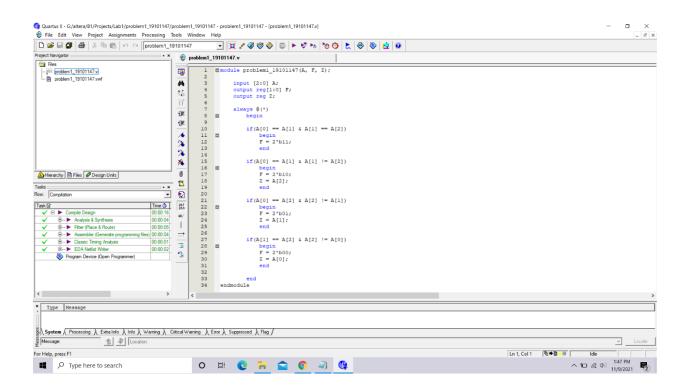
Ahmad Zubair

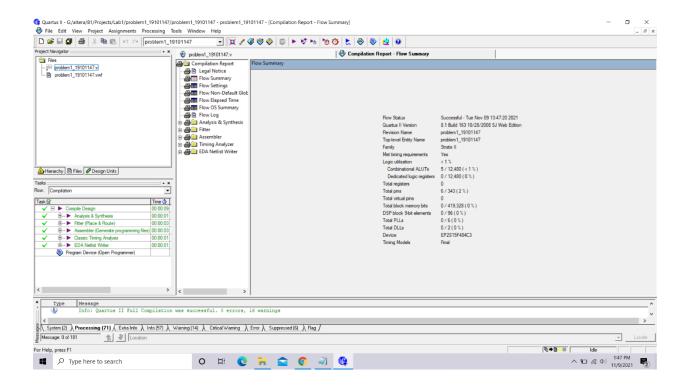
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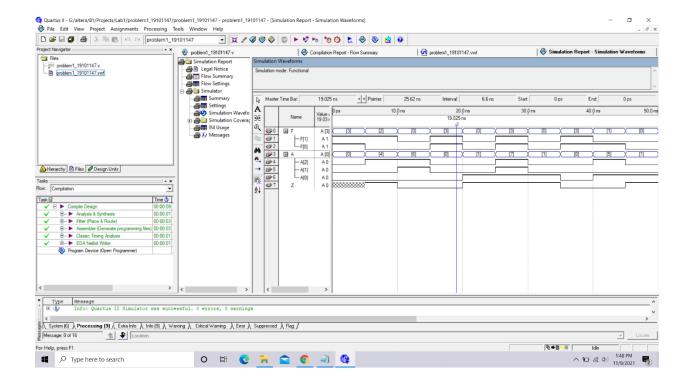
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1. expires out loss 1 is lugluo al From the fining diogram, we can see that at ons the input, A is Oile. all the bits are o'ors equal. As a result, we get 3 as the output and for the same reason there is no unique bit to show. At 5 ns, we see A is 4. The binary representation towns out to be 100 and so this combination gets us 2 as the output and the unique bit here is 1. Again, at 20 ms the imput is 1 (001) and so, the output is to As a result, the same unique value here is 1. Lastly, at 40 ms the input is 5 for which 101 is the bimary value. As a result, here

the output is I and the unique value is 9. result me get is a stre output and la the some recessor there is no copye tel la stan. At E 25 me see A is 1. The labory represented This combinations gits us a as the and tid aupino at bus trafted led. Agin at 20 sa the input 0 01 trytuo est 10 pro (100) 1 01 As a result. The server usique value where is I leastly at 40 as also







I performed the simulation for erough time to get at least two repetitions of 14 which was my initial input after the external load. From the timing diagram I can see 14 was the input for the first time at 10 mg and the second time 14 was the imput at 60 mg. So, if took 50 mg or 5 clock cycles for 14 to get one repetition of itself. The rea reason for the no of clock eycles being 5 is the imput is of 5 bits. As a result, if there is an n bit input it will take n clock cycles to get one repetition of the initial input.

