CSE460: VLSI Design

Lab Assignment 4

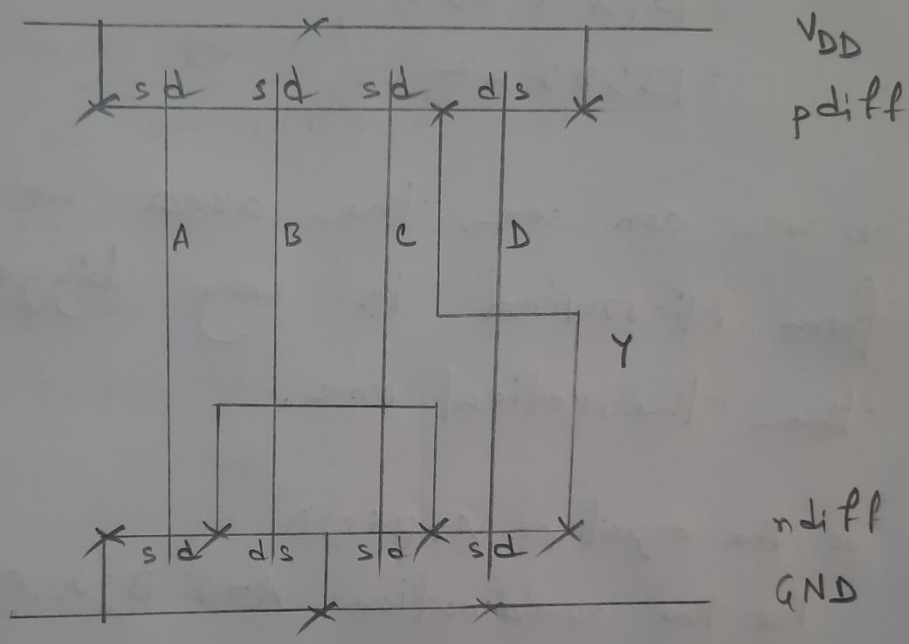
Ahmad Zubair

ID: 19101147

Sec: 09

1.

$$Y = \overline{(A+B+C)D}$$



Area = W × L

$= 5 \times 8\lambda \times 6 \times 8\lambda$

$= 40 \times 48\lambda^2$

$= 1920\lambda^2$

From Microwind,

Area = W × L

= dx × dy

= 151λ × 90λ

= 13590 λ^2

So, we can see, the area we got from Microwind is way bigger than the theoretical one.

For the equation, $\overline{(A+B+C)D}$

For the combination, A=0, B=0, C=1, D=0

Y=1

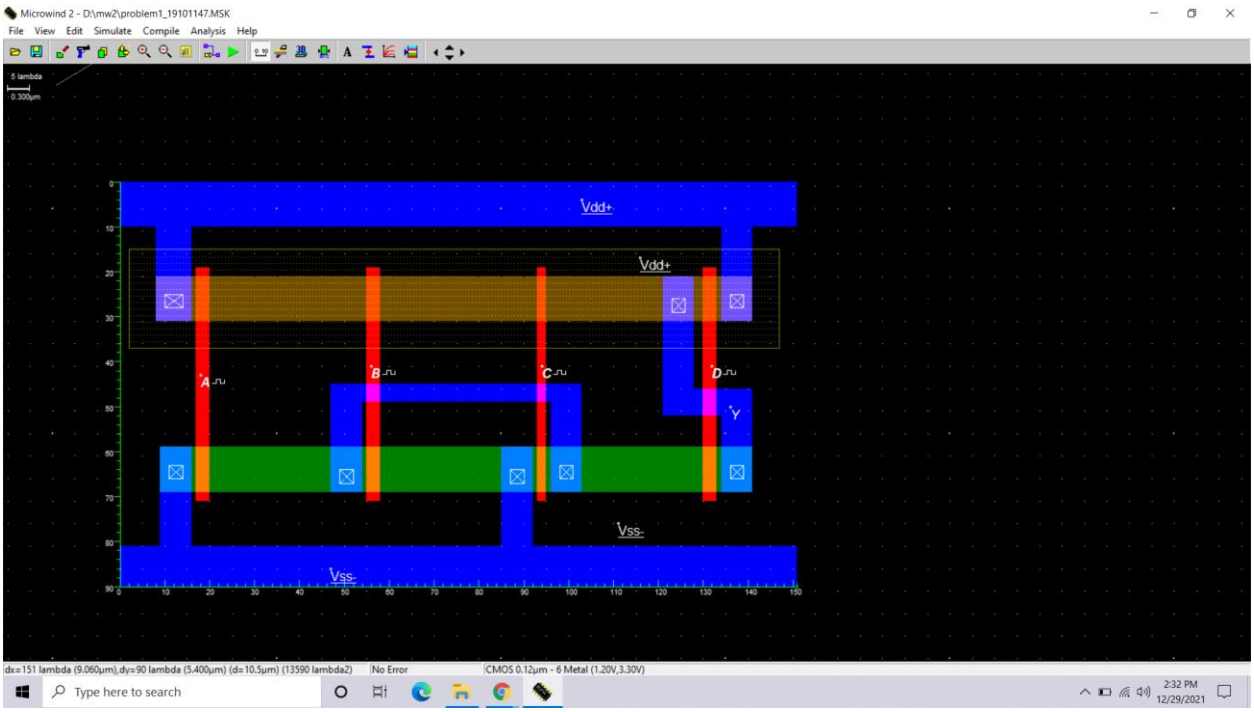
In the timing diagram at around 1ns, we see A=0, B=0, C=1, D=0 and Y=1.

For the combination, A=1, B=0, C=0, D=1

Y=0

In the timing diagram at around 2.5 ns, we see A=1, B=0, C=0, D=1 and Y=0.

So, the circuit is working correctly.


Microwind 2 - D:\mw2\problem1_19101147.MSK
File View Edit Simulate Compile Analysis Help
5 lambda
0.300µm
Vdd+
Vdd+
A
B
C
D
Y
Vss-
Vss-
dx=151 lambda (9.060µm),dy=90 lambda (5.400µm) (d=10.5µm) (13590 lambda2)
No Error
CMOS 0.12µm - 6 Metal (1.20V,3.30V)
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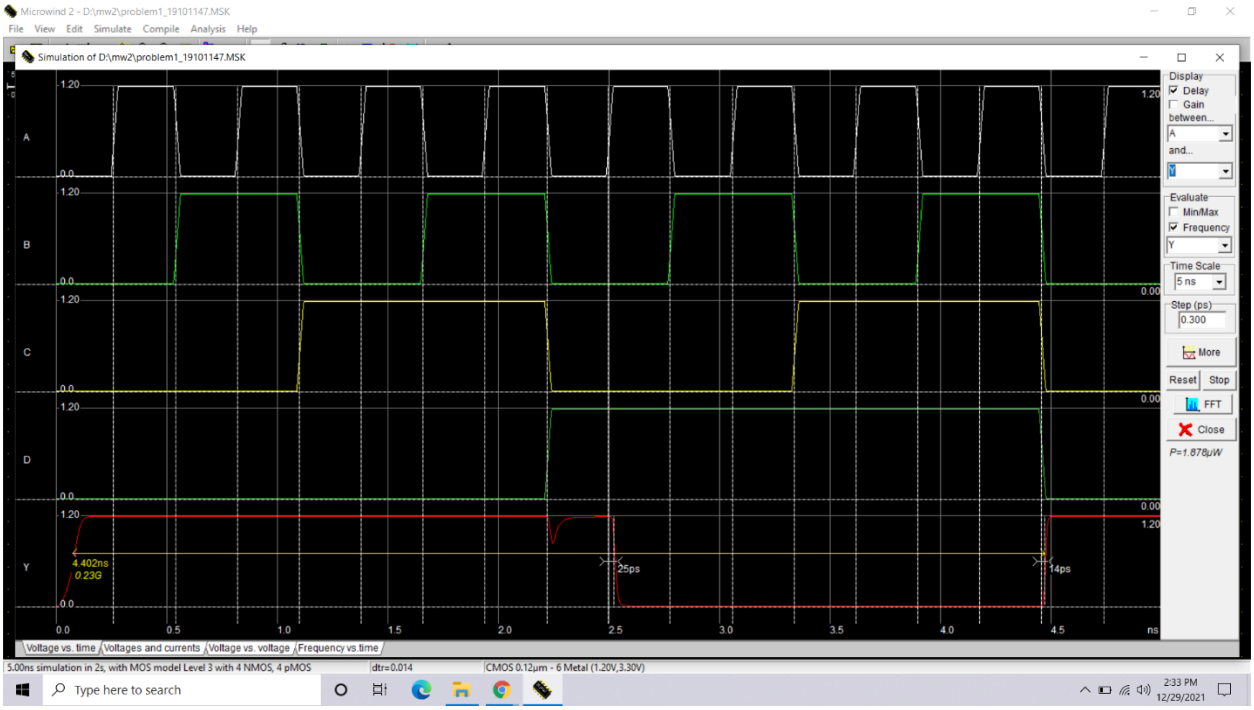
12/29/2021


Microwind 2 - D:\mw2\problem1_19101147.MSK
File View Edit Simulate Compile Analysis Help
Simulation of D:\mw2\problem1_19101147.MSK
A
B
C
D
Y
1.20
0.0
4.402ns
0.23G
25ps
14ps
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
ns
Display
Delay
Gain between...
and...
Evaluate
Min/Max
Frequency
Time Scale
5 ns
Step (ps)
0.300
More
Reset
Stop
FFT
Close
P=1.878µW
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs.time
5.00ns simulation in 2s, with MOS model Level 3 with 4 NMOS, 4 pMOS
dtr=0.014
CMOS 0.12µm - 6 Metal (1.20V,3.30V)
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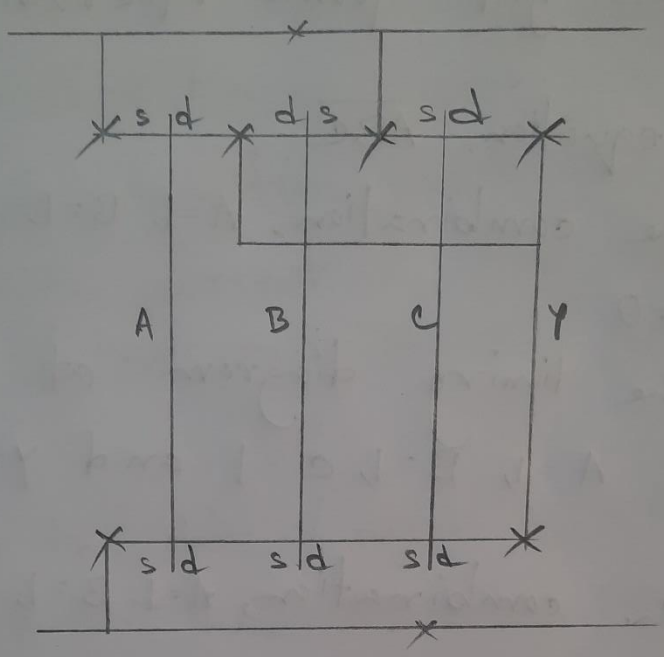
2:33 PM
12/29/2021

2.

3-input NAND, $\overline{ABC}$



Area = W × L

= 4×8λ × 5×8λ

= 32λ × 40λ

= 1280 λ^2

From Microwind,

Area = W × L

= ~~dy ×~~ dx × dy

= 108λ × 88λ

= 9504 λ^2

So, we can see, the theoretical area is way smaller than the practical one we got from Microwind.

For the equation, $\overline{ABC}$

For the combination, A=1, B=1, C=1

Y=0

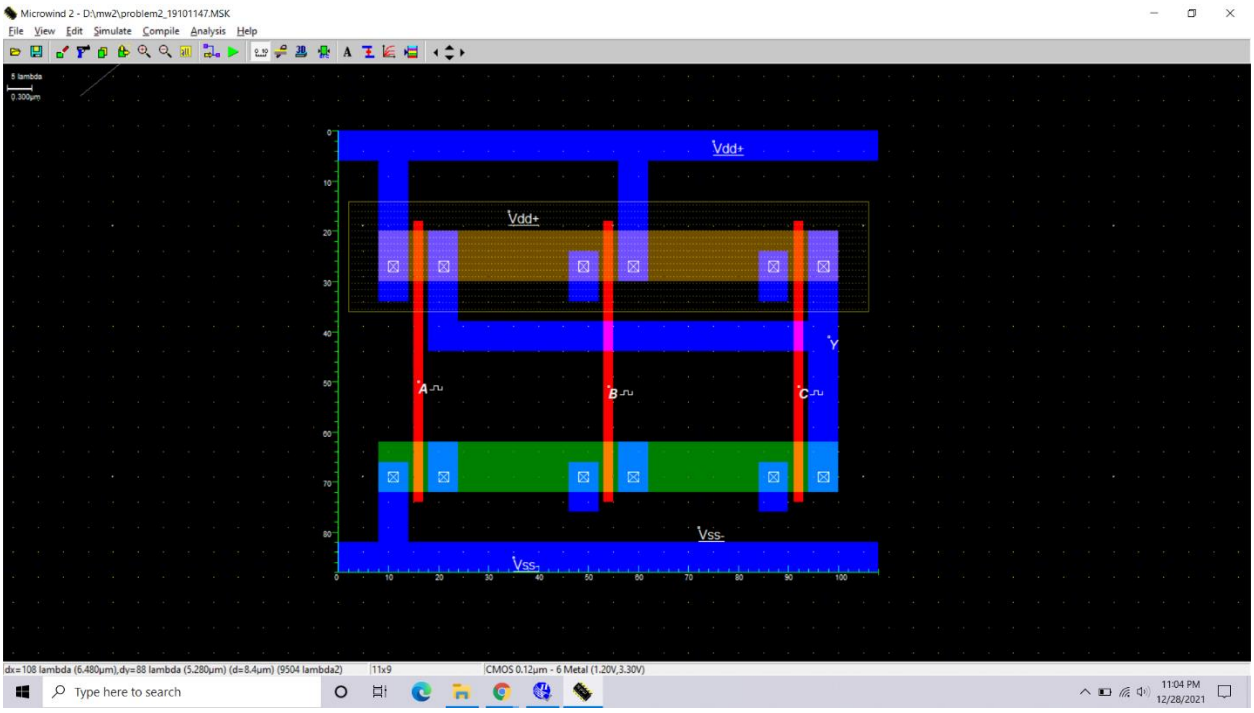
In the timing diagram at around 2 ns, A=1, B=1, C=1 and Y=0

For the combination, A=1, B=1, C=0

Y=1

In the timing diagram at around 3 ns, A=1, B=1, C=0 and Y=1.

So, the circuit is working correctly.


Microwind 2 - D:\mw2\problem2_19101147.MSK
File View Edit Simulate Compile Analysis Help
5 lambda
0.300µm
Vdd+
Vdd+
Y
A
B
C
Vss-
Vss-
dx=108 lambda (6.480µm),dy=88 lambda (5.280µm) (d=8.4µm) (9504 lambda2)
11x9
CMOS 0.12µm - 6 Metal (1.20V,3.30V)
Type here to search
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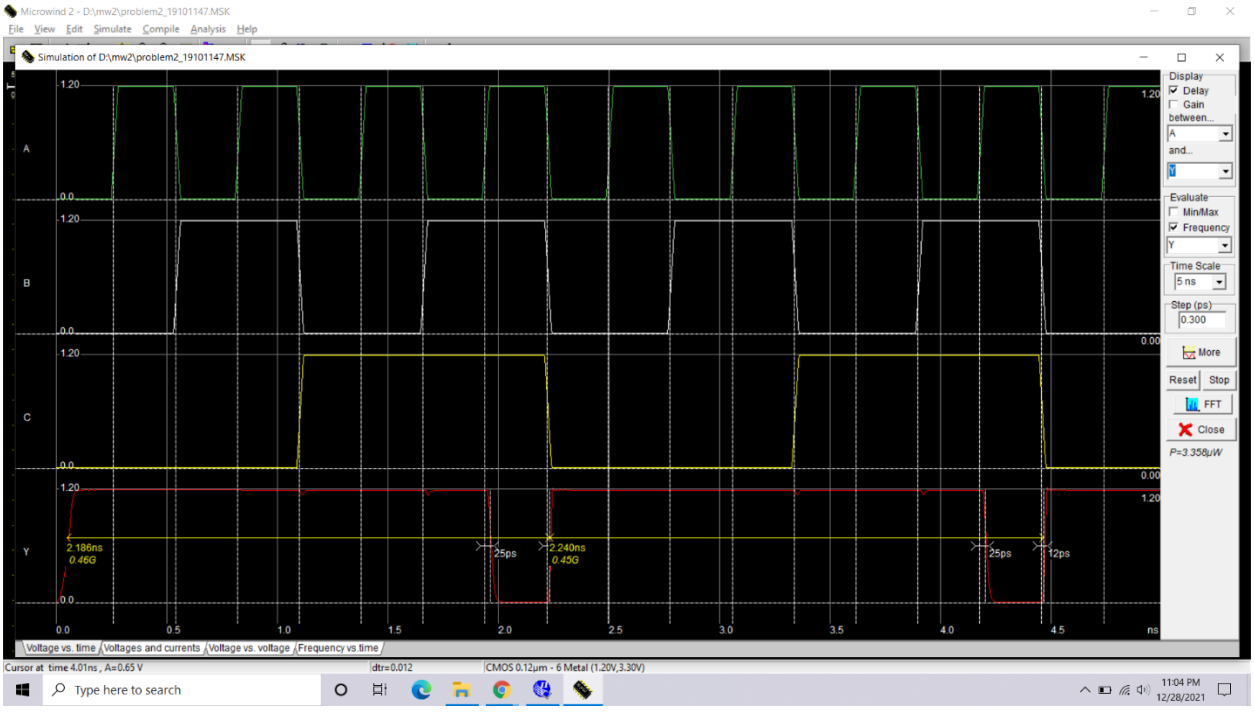
Microwind 2 - D:\mw2\problem2_19101147.MSK
File View Edit Simulate Compile Analysis Help
Simulation of D:\mw2\problem2_19101147.MSK
A
B
C
Y
1.20
0.0
2.186ns
0.46G
25ps
2.240ns
0.45G
25ps
12ps
0.0 0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0 4.5 ns
Display
Delay
Gain between...
A
and...
Y
Evaluate
Min/Max
Frequency
Y
Time Scale
5 ns
Step (ps)
0.300
More
Reset
Stop
FFT
Close
P=3.356µW
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs.time
Cursor at time 4.01ns , A=0.65 V
dtr=0.012
CMOS 0.12µm - 6 Metal (1.20V,3.30V)
Type here to search
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3.

From Microwind,

Area = W × L

= dx × dy

= 391λ × 206λ

= 80516 λ^2

By simplifying the circuit we get,

$y = DC + (\overline{D + C})$

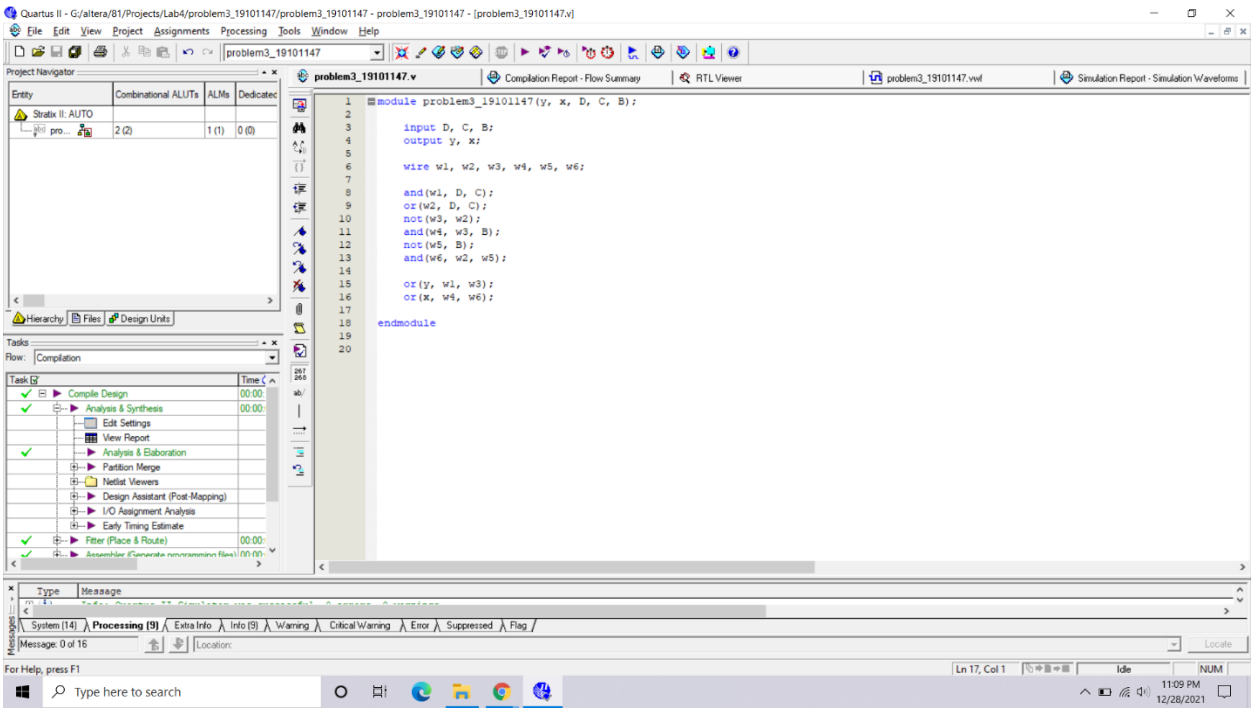
$x = B(\overline{D + C}) + \bar{B}(D + C)$

For the input combination, B = 1, C = 0, D = 0 the output, x = 1, y = 1

In the timing diagram, at around 4 ns, B = 1, C = 0, D = 0 and x = 1, y = 1

For the input combination, B = 0, C = 1, D = 0 the output combination, x = 1, y = 0

In the timing diagram, at around 6 ns, B = 0, C = 1, D = 0 and


Quartus II - G:/altera/81/Projects/Lab4/problem3_19101147/problem3_19101147 - problem3_19101147 - [problem3_19101147.v]
File Edit View Project Assignments Processing Tools Window Help
problem3_19101147
Project Navigator
Entity
Combinational ALUTs
ALMs
Dedicatec
Stratix II: AUTO
2 (2)
1 (1)
0 (0)
Hierarchy
Files
Design Units
Tasks
Flow: Compilation
Task
Time
Compile Design
Analysis & Synthesis
Edit Settings
View Report
Analysis & Elaboration
Partition Merge
Netlist Viewers
Design Assistant (Post-Mapping)
I/O Assignment Analysis
Early Timing Estimate
Fitter (Place & Route)
problem3_19101147.v
Compilation Report - Flow Summary
RTL Viewer
problem3_19101147.vwf
Simulation Report - Simulation Waveforms
module problem3_19101147(y, x, D, C, B);
input D, C, B;
output y, x;
wire w1, w2, w3, w4, w5, w6;
and(w1, D, C);
or(w2, D, C);
not(w3, w2);
and(w4, w3, B);
not(w5, B);
and(w6, w2, w5);
or(y, w1, w3);
or(x, w4, w6);
endmodule
Type
Message
System (14)
Processing (9)
Extra Info
Info (9)
Warning
Critical Warning
Error
Suppressed
Flag
Message: 0 of 16
Location:
Locate
For Help, press F1
Ln 17, Col 1
Idle
NUM
Type here to search
11:09 PM
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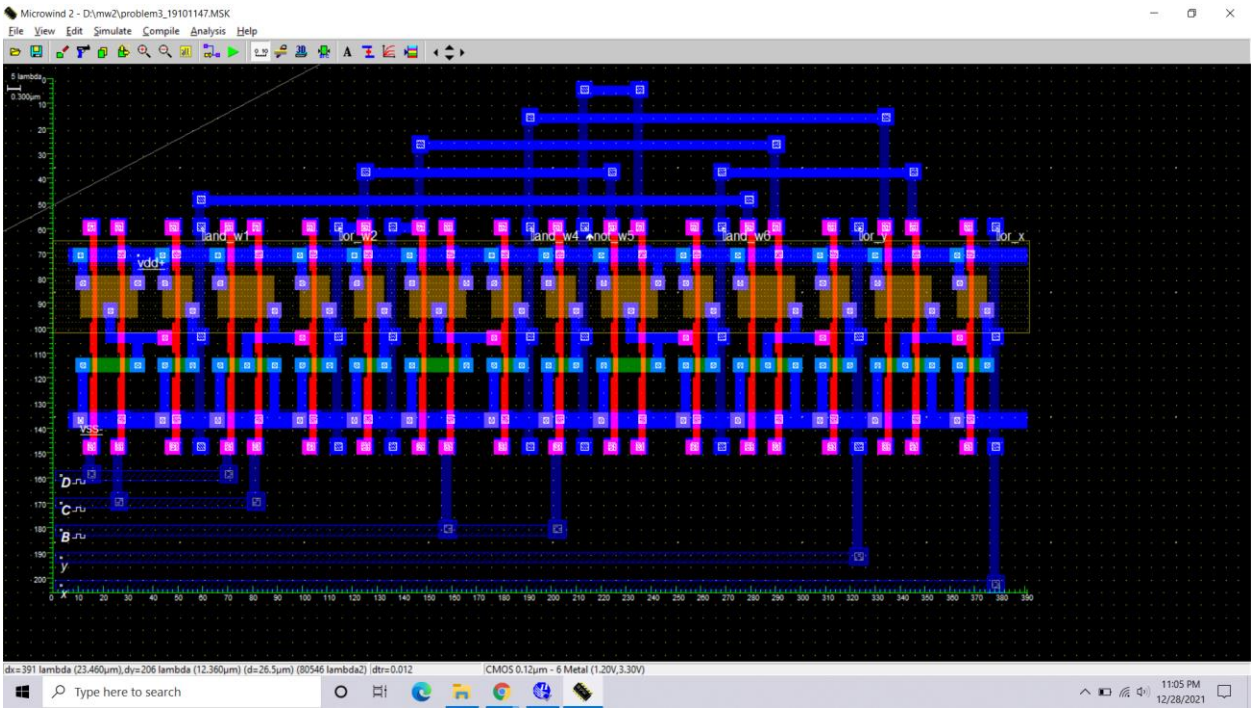
Microwind 2 - D:\mw2\problem3_19101147.MSK
File View Edit Simulate Compile Analysis Help
land_w1
lor_w2
land_w4
not_w3
land_w6
lor_y
lor_x
vdd
vss
D
C
B
y
dx=391 lambda (23.460µm),dy=206 lambda (12.360µm) (d=26.5µm) (80546 lambda2) |dtr=0.012
CMOS 0.12µm - 6 Metal (1.20V,3.30V)
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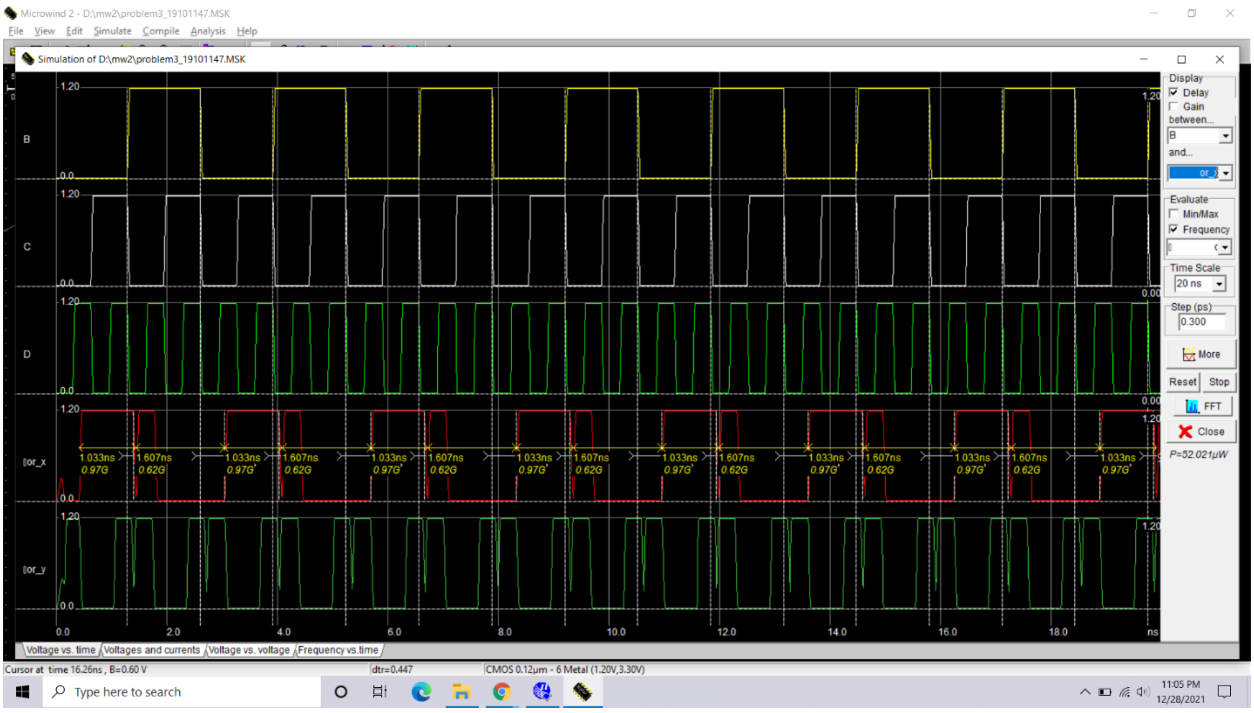
Microwind 2 - D:\mw2\problem3_19101147.MSK
File View Edit Simulate Compile Analysis Help
Simulation of D:\mw2\problem3_19101147.MSK
B
C
D
[or_x
[or_y
1.033ns 0.97G
1.607ns 0.62G
Display
Delay
Gain between...
and...
Evaluate
Min/Max
Frequency
Time Scale
20 ns
Step (ps)
0.300
More
Reset
Stop
FFT
Close
P=52.021µW
0.0
2.0
4.0
6.0
8.0
10.0
12.0
14.0
16.0
18.0
ns
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs.time
Cursor at time 16.26ns , B=0.60 V
dtr=0.447
CMOS 0.12µm - 6 Metal (1.20V,3.30V)
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