

CSE460

Lab Assignment 0

Ahmad Zubair

ID: 19101147

Sec: 09

1a. 1b.

The equation is,

$$Y = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

From the truth table we get by working on this equation,

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

From the table, we can see, whenever the input pins i.e. A, B, C together have odd number of '1's, the output is '1' or true. However, when all the input pins together have even number of '1's, the output pin gives '0' or false as the result.

And this pattern is exactly like an XOR gate's. So, we can say, the circuit performing XOR operation

and I have performed simulation for 150 ns and so, the timing diagram is shown from 0 ns to 50 ns on the screen. Again, my selected time periods for the input pins are,

$$A = 40 \text{ ns}$$
$$B = 20 \text{ ns}$$
$$C = 10 \text{ ns}$$

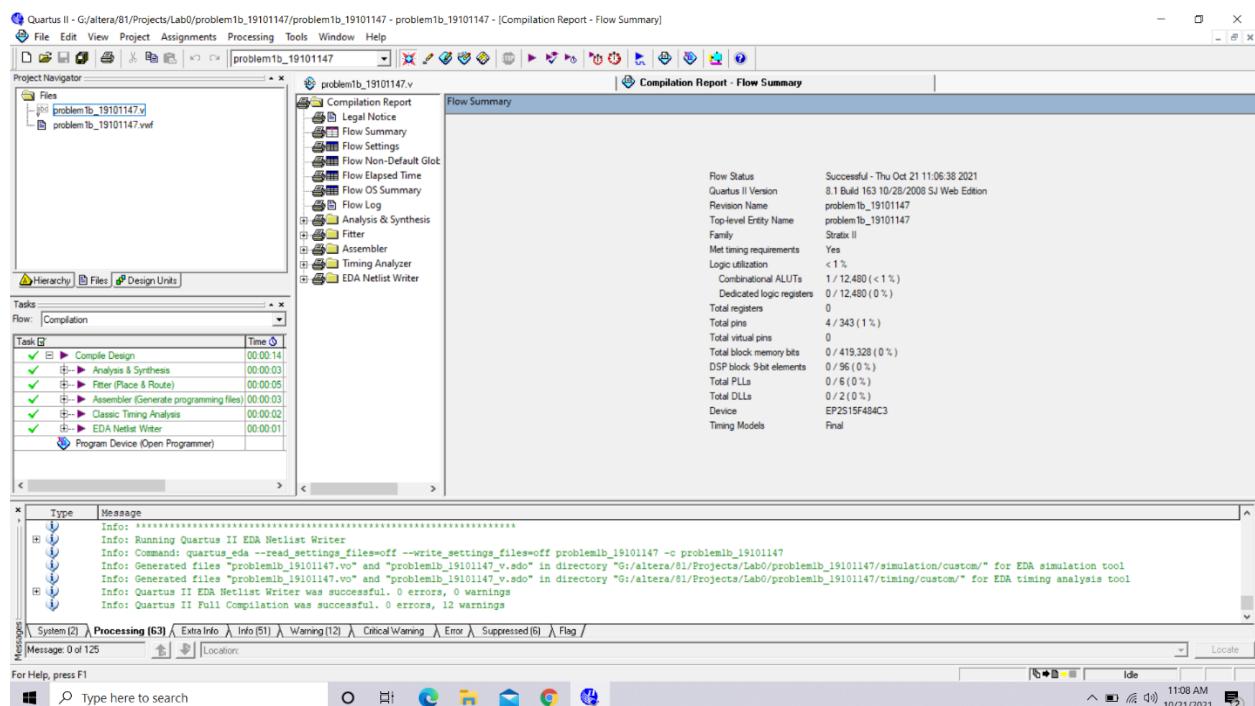
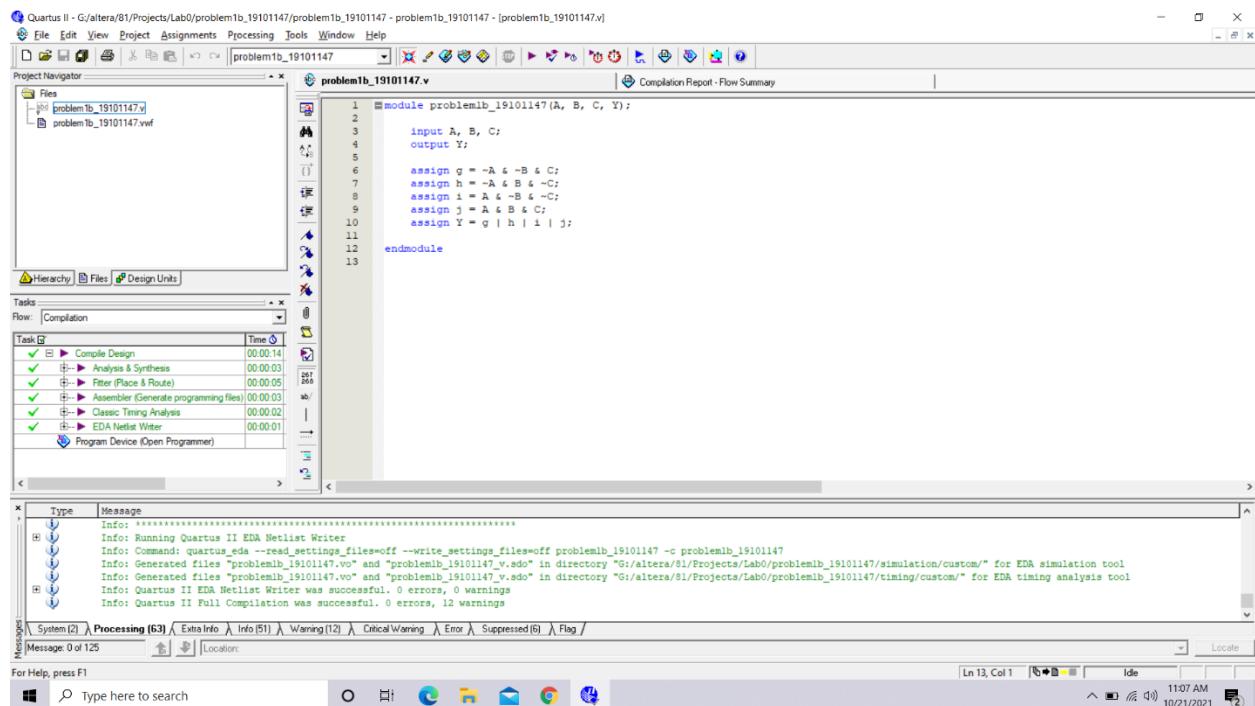
From the timing diagram, my randomly selected timing instances help get feedback. As a result,

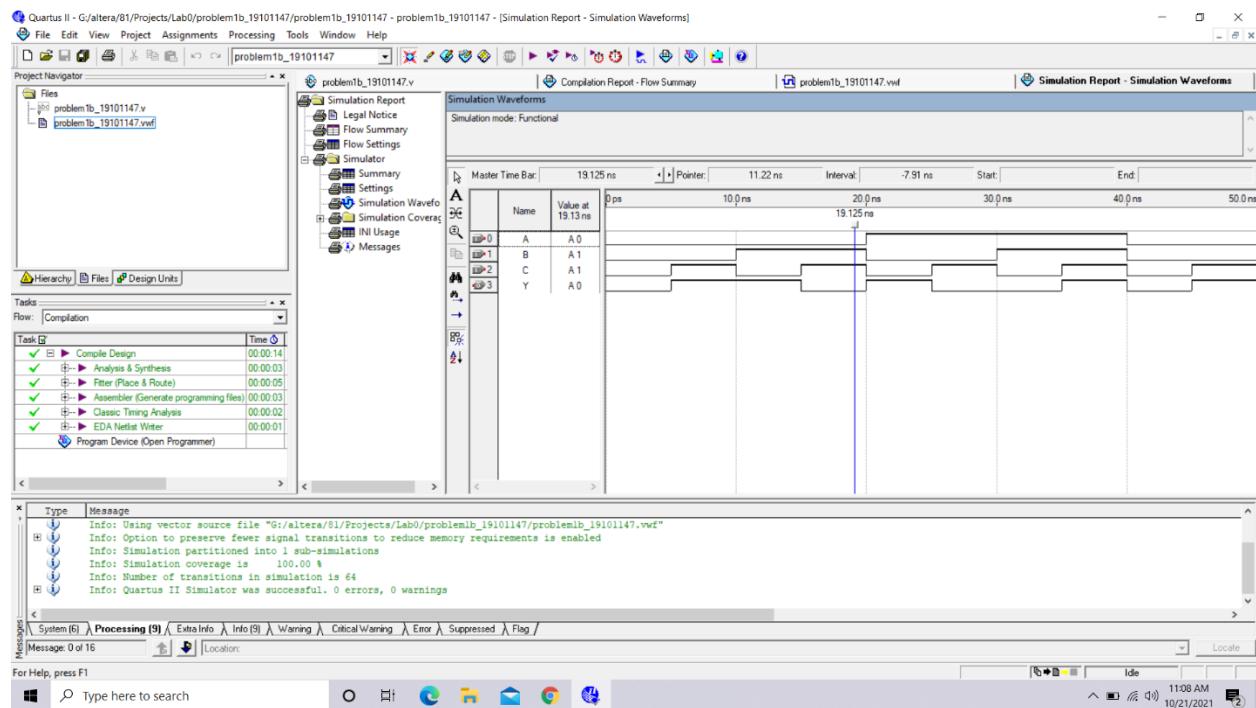
are, 15.5 ns and 20 ns.

In case of 15.5 ns, A is 0, B is 1, C is 1 and Y, the output is 0. This exactly matches the fourth combination from the truth table in

As for 20 ns, A is 1, B is 0, C is 0 and Y is 1. And this matches the fifth combination from the truth table.

In conclusion, the outputs of my randomly selected time instances do match with the truth table's.





1c.

I have performed simulation for 50 ns and so, the timing diagram is shown from 0 ns to 50 ns on the screen.

Again, my selected time periods for the set input pins are,

A = 40 ns

B = 20 ns

C = 10 ns

However, this time my task was to randomize the values of the input pins in Verilog at half grid intervals. As a result,

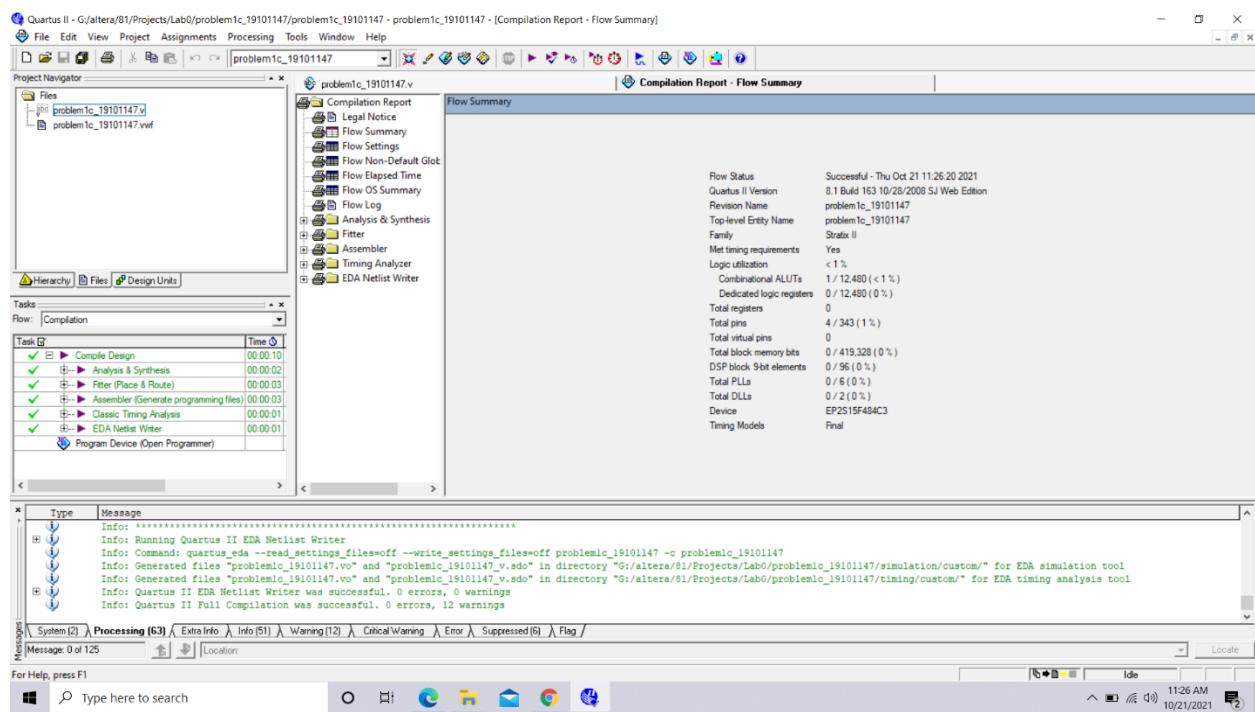
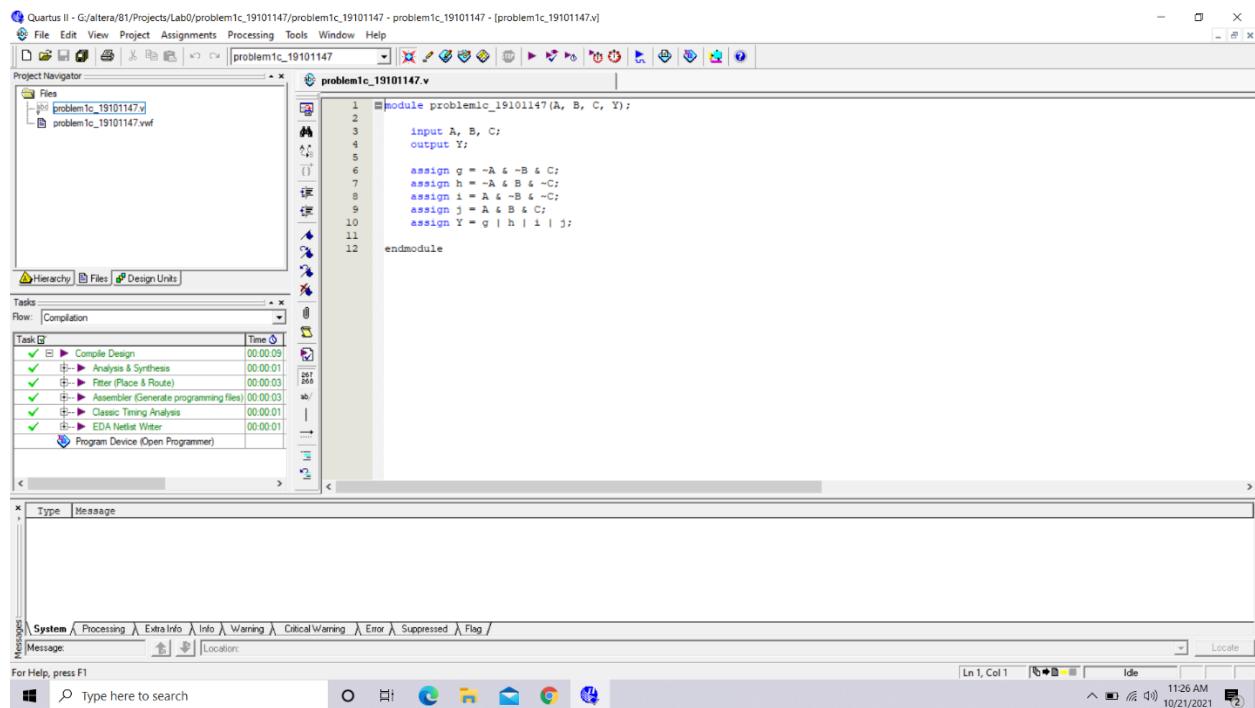
my selected input time periods for the input pins won't really match with the ones shown in the timing diagram. And I pick 15.5 ns and 20 ns this time for to crosscheck the outputs.

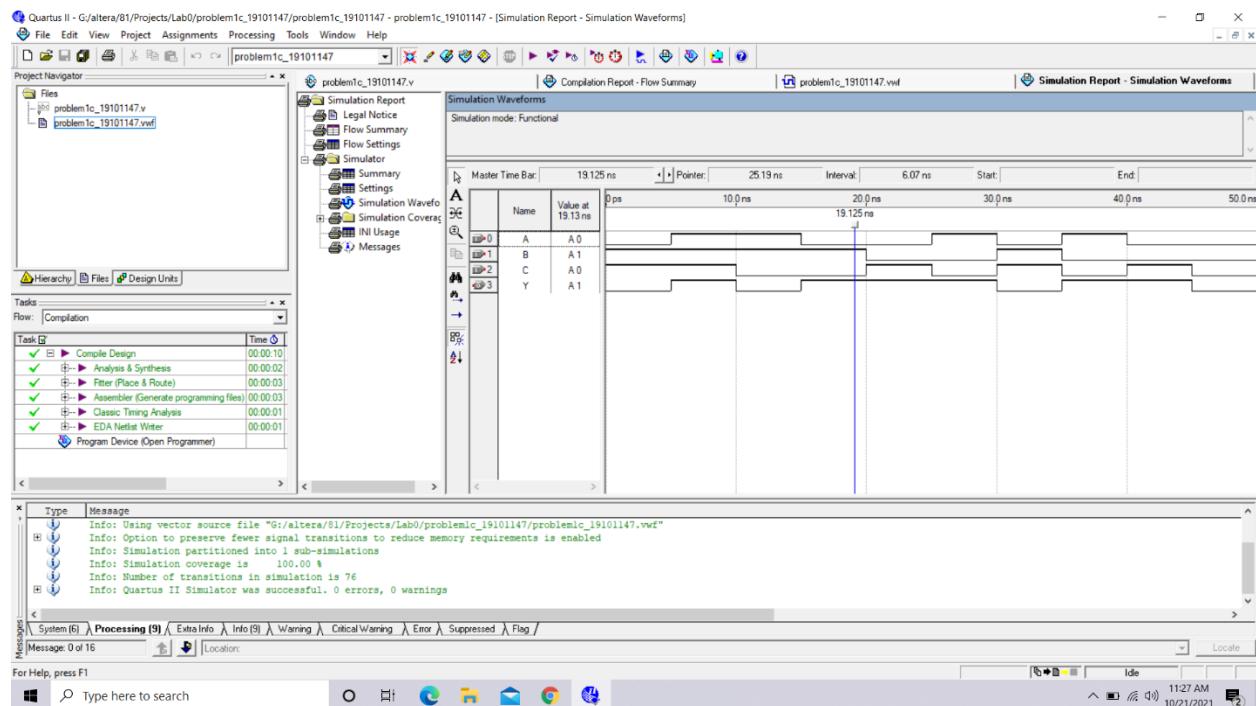
In case of 15.5 ns, A is 0, B is 1, C is 0 and Y is 1 which exactly matches the third combination of the fourth table from la.

As for 20 ns, A is 0, B is 0, C is 1 and Y is 1, this combin-

lation matches the second one from the truth table.

To conclude the outputs of my randomly selected time instances matched with the ones in the truth table.





1d.) Implement the required logic
My modified equation is,

$$Y = \overline{\bar{A}\bar{B}C} \cdot \overline{\bar{A}\bar{B}\bar{C}} \cdot \overline{\bar{A}\bar{B}\bar{C}} \cdot \overline{\bar{A}\bar{B}C}$$

As

$$Y = \overline{\bar{A}\bar{B}C} \cdot \overline{\bar{A}\bar{B}\bar{C}} \cdot \overline{\bar{A}\bar{B}\bar{C}} \cdot \overline{\bar{A}\bar{B}C}$$

$$Y = \overline{\bar{A}\bar{B}C} + \overline{\bar{A}\bar{B}\bar{C}} + \overline{\bar{A}\bar{B}\bar{C}} + \overline{\bar{A}\bar{B}C}$$

$$Y = \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + A\bar{B}C$$

This proves that the modified equation will get us the same result as the one in the question.

I have performed simulation for 50 ns and so, the timing diagram is shown from 0 ns to 50 ns on the screen

Again, my selected time periods for the input pins are,

A = 40 ns
B = 20 ns

If I pick the same time instances as 1b's i.e. 15.5 ns and 20 ns, I would see both the outputs of 15.5 ns and

20 ns will get me the same result as 1b's. As a result, the modified equation and the circuit which is composed of only NAND gates does match with the equation and the circuit from the question.

