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BILKENT UNIVERSITY

COMPUTER ENGINEERING DEPT.

CS223 LAB 2 SECTION 4

LAB REPORT

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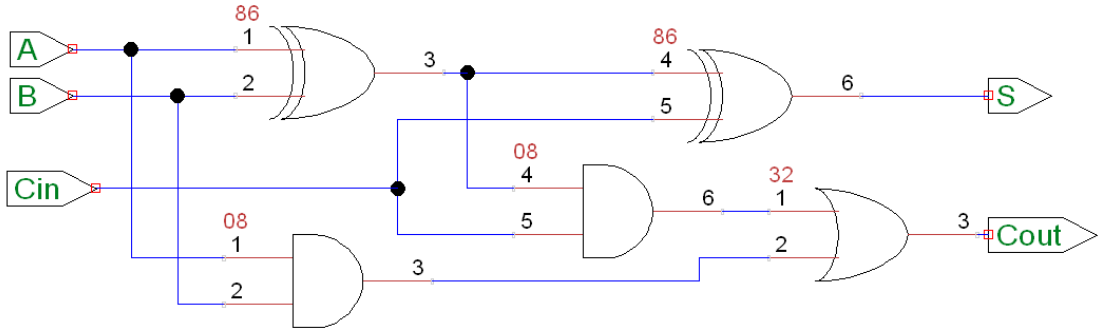
Spring 2021

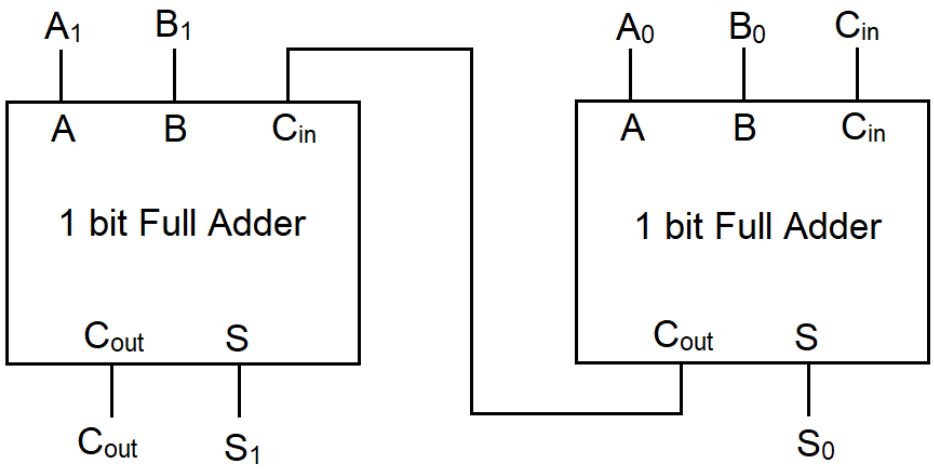
1. Circuit Schematics

For all IC's, their pin number for GND is 7 and for Vcc(+5V) is 14. Proper pin numbers are drawn on top of each port.

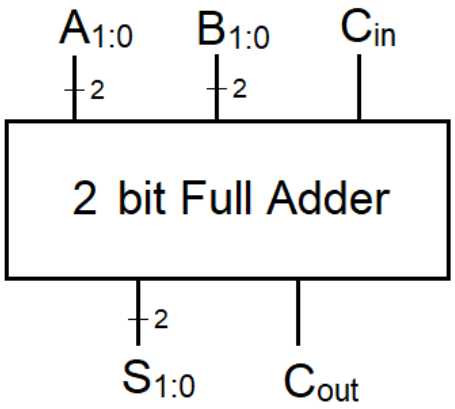
a) 1 bit Full Adder



b) 2 bit Full Adder



This design can be represented in a single black box:



2. SystemVerilog Modules & Testbenches

a) Dataflow - 1 bit Full Adder

```
module adder1D(input logic a, b, c_in,
               output logic s, c_out
);
   assign s = a ^ b ^ c_in;
   assign c_out = a & b | a & c_in | b & c_in;
endmodule
```

```
module testadder1D();
   logic c_in, c_out;
   logic a, b, s;
   integer i, j, k;
   adder1D uut(.a(a),
           .b(b),
           .c_in(c_in),
           .s(s),
           .c_out(c_out)
           );
   initial begin
      a <= 0;
      b <= 0;
      c_in <= 0;
      for(i = 0; i < 2; i = i + 1) begin
         for (j = 0; j < 2; j = j + 1) begin
            for (k = 0; k < 2; k = k + 1) begin
               #10 c_in <= c_in + 1;
            end
            b <= b + 1;
         end
         a <= a + 1;
      end
   end
endmodule
```

b) Structural - 1 bit Full Adder

```
module adder1S( input logic a, b, c_in,
                output logic s, c_out
              );
   logic a_xor_b, a_and_b, c_in_and_axorb;
   xor2 xor_1(a_xor_b, a, b);
   xor2 xor_2(s, a_xor_b, c_in);
   and2 and_1(a_and_b, a, b);
   and2 and_2(c_in_and_axorb, c_in, a_xor_b);
   or2 or_(c_out, a_and_b, c_in_and_axorb);
endmodule



module testadder1S();
   logic c_in, c_out;
   logic a, b, s;
   integer i, j, k;
   adder1S uut( .a(a),
                .b(b),
                .c_in(c_in),
                .s(s),
                .c_out(c_out)
                );
   initial begin
      a <= 0;
      b <= 0;
      c_in <= 0;
      for(i = 0; i < 2; i = i + 1) begin
         for (j = 0; j < 2; j = j + 1) begin
            for (k = 0; k < 2; k = k + 1) begin
               #10 c_in <= c_in + 1;
            end
            b <= b + 1;
         end
         a <= a + 1;
      end
   end
endmodule
```

c) Structural - 2 bit Full Adder

```
module adder2S(   input logic[1:0] a, b,
                  input logic c_in,
                  output logic[1:0] s,
                  output logic c_out
);
   logic c_in_1;
   adder1D  zerothbit(a[0],  b[0],  c_in,  s[0],
c_in_1);
   adder1D  firstbit(a[1],  b[1],  c_in_1,  s[1],
c_out);
endmodule
```

```
module testadder2S();
   logic c_in, c_out;
   logic[1:0] a, b, s;
   integer i, j;

   adder2S uut( .a(a),
                .b(b),
                .c_in(c_in),
                .s(s),
                .c_out(c_out)
                );

   initial begin
      a <= 0;
      b <= 0;
      c_in <= 0;
      for(i = 0; i < 4; i = i + 1) begin
         for (j = 0; j < 4; j = j + 1) begin
            #10 b <= b + 1;
         end
         a <= a + 1;
      end
   end
endmodule
```