

Junction Transistor Characteristics

7.1 THE JUNCTION TRANSISTOR

J. Bardeen, W. Brattain, and W. Shockley invented the point-contact transistor in the Bell Telephone Laboratories in 1947, and the first public announcement was made on June 30, 1948. The junction transistor appeared in 1950. The term 'transistor' is attributed to John R. Pierce. It is the solid-state version of the vacuum triode, and so was initially termed crystal triode or semiconductor triode. However, the name 'transistor' has survived. Junction transistors are among the important elements of modern electronic systems. Shockley, Bardeen and Brattain were awarded the Nobel Prize for physics in 1956 for their work.

A junction transistor is made up of a semiconductor, such as Ge or Si, in which a *p*-type thin layer is sandwiched between two *n*-type layers. The transistor so formed is called an *n-p-n transistor*.

Alternatively, a transistor can also have an *n*-type layer between two *p*-type layers. The transistor is then termed a *p-n-p transistor*.

p-n-p and *n-p-n* transistors are schematically shown in Fig. 7.1. The middle portion of the transistor is called the *base*, and the two end portions are known as the *emitter* and the *collector*. The emitter-base junction is usually referred to as the *emitter junction* (J_E), and the collector-base junction as the *collector junction* (J_C). The size of the transistor is quite small. The structure is sealed inside a metal or a plastic case to protect it from moisture. Metal leads *E*, *B* and *C* come out of the package for connection to the emitter, the base, and the collector, respectively. Since both the majority and the minority carriers are involved in a junction transistor, this device is termed the *bipolar junction transistor* (BJT), *bipolar transistor* or *bipolar device*.

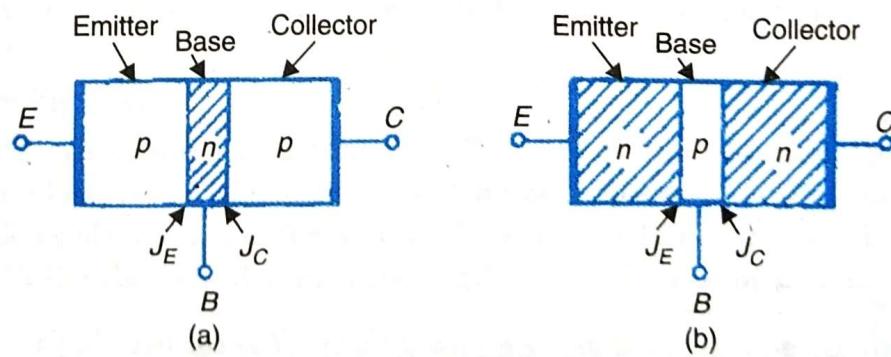


Fig. 7.1 Bipolar junction transistors (a) *p-n-p*, (b) *n-p-n*.

In the normal transistor operation, emitter-base junction is forward-biased and the collector-base junction is reverse-biased. The circuit symbols for the *p-n-p* and *n-p-n* transistors are shown in Fig. 7.2(a) and (b), respectively. The arrow on the emitter specifies the direction of the current when the emitter-base junction is forward-biased. Therefore, the current enters the transistor through the emitter terminal for a *p-n-p* transistor and leaves the transistor through the emitter terminal for an *n-p-n* transistor. In both the cases, the emitter, base, and

collector currents, I_E , I_B and I_C , respectively, are taken positive when the currents go *into* the transistor. The symbols V_{EB} , V_{CB} and V_{CE} represent respectively the emitter-base, collector-base and collector-emitter voltages. These are assumed positive when the terminal marked by the first subscript is positive with respect to the terminal marked by the second subscript. These chosen reference current directions and voltage polarities are depicted in Fig 7.2.

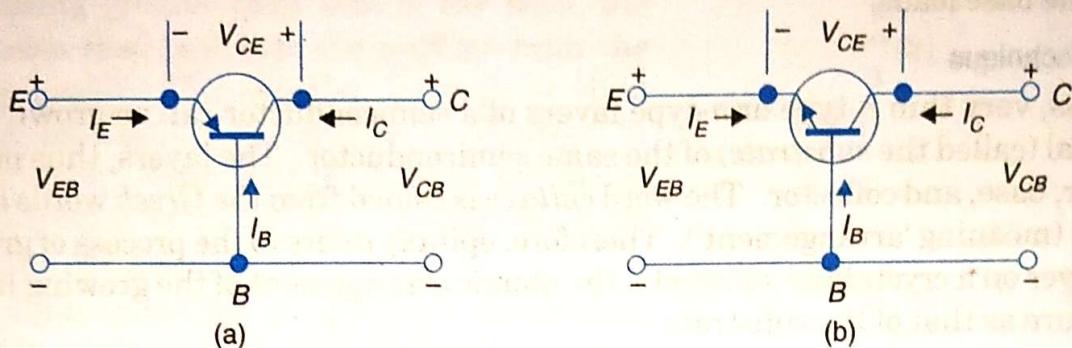


Fig. 7.2 Circuit symbols with reference current directions and voltage polarities for
(a) a *p-n-p* and (b) an *n-p-n* transistor.

As the emitter junction is usually forward-biased, I_E is negative in the case of an *n-p-n* transistor and positive for a *p-n-p* transistor. Since the collector junction is reverse-biased, the voltage V_{CB} is negative for a *p-n-p* transistor and positive for an *n-p-n* transistor. Table 7.1 contains the signs of the different voltages and currents for the *p-n-p* and the *n-p-n* transistors. Note that the signs are opposite for the two types of transistors.

Table 7.1. Signs of currents and voltages for normal transistor operation

Transistor type	I_E	I_B	I_C	V_{EB}	V_{CB}	V_{CE}
<i>p-n-p</i>	+	-	-	+	-	-
<i>n-p-n</i>	-	+	+	-	+	+

7.2 TRANSISTOR MANUFACTURING TECHNIQUES

Transistors are generally fabricated with the help of the following four basic techniques.

(i) Grown Technique

In this method, an *n-p-n* transistor is constructed by drawing a single crystal from a melt of Si or Ge having *n*-type impurities. During the drawing operation, the conductivity type is changed by adding *p*-type impurities to form the base region of the transistor. Finally, *n*-type impurities are added again. In a similar fashion, a *p-n-p* transistor can be grown.

(ii) Alloy or Fused Technique

Here, to construct a *p-n-p* transistor, a thin wafer of an *n*-type material is taken to serve as the base of the transistor. Two small dots of indium (which is an acceptor) are placed on the opposite sides of the wafer. The system is heated for a short time to a high temperature above the melting point of indium but below that of the wafer material. Indium dissolves and penetrates a little in the wafer, producing a *p*-type material on either side of the *n*-type base. On cooling, a *p-n-p* transistor is thus formed. Similarly, an *n-p-n* transistor can be developed.

(iii) Diffusion Technique

In this technique *planar transistors* can be formed. The adjective 'planar' signifies that the fabrication is carried out on a nearly flat wafer surface. A wafer of *n*-type silicon (to serve as the collector) is heated in a furnace containing *p*-type impurities in a gaseous form. The

impurities diffuse into the surface of the wafer, producing a *p*-type region which is the base of the transistor. The system is now covered by a mask with apertures and heated again in an atmosphere of gaseous *n*-type impurities. The *n*-type atoms diffuse through the apertures, producing an *n*-layer over the *p*-layer. This *n*-layer serves as the emitter of the transistor. A thin layer of silicon dioxide is grown over the whole surface and photoetched to make aluminium contacts for the emitter and the base leads.

(iv) Epitaxial Technique

In this process, very thin *p*-type or *n*-type layers of a semiconductor can be grown on a heavily doped material (called the *substrate*) of the same semiconductor. The layers, thus produced, can be the emitter, base, and collector. The word *epitaxy* is coined from the Greek words *epi* (meaning 'on') and *taxis* (meaning 'arrangement'). Therefore, epitaxy refers to the process of growing a thin crystalline layer on a crystalline substrate, the atomic arrangement of the growing layer being of the same nature as that of the substrate.

Observation

The doping of the emitter section of a transistor is greater than that of the collector section. The base region is oppositely doped at a level intermediate between the emitter and the collector. The doping profile of a *p-n-p* transistor is schematically shown in Fig. 7.3. Here, N_D^+ and N_A^- denote respectively the concentrations of ionized donor and acceptors, and x is the distance through the transistor from the emitter end. The width W_B of the base is typically a few micrometers while the widths W_E and W_C of the emitter and the collector, respectively, are a few millimetres or less. The doping concentrations of the emitter, base, and collector are typically about 10^{18} , 10^{16} and 10^{15} per cm^{-3} , respectively.

Interestingly, the first transistor invented was a point-contact type that employed two tungsten wires pressed against a semiconductor wafer. Such transistors are not used now because of their poor reliability and reproducibility.

7.3 MECHANISM OF TRANSISTOR ACTION

The normal operation of a transistor is shown in the circuit of Fig. 7.4. The voltage source V_{EE} makes the emitter-base junction of the *n-p-n* transistor forward-biased. The other voltage source V_{CC} biases the collector-base junction in the reverse direction.

As the transistor may be viewed as an *n-p* diode followed by a *p-n* diode, the physical action of the transistor can be explained with the help of the energy-band diagram of the *p-n* junctions. In the absence of the biasing voltage sources, the energy diagram for the conduction band in the transistor is therefore as shown schematically in Fig. 7.5(a). Here, x represents the distance through the transistor. When the biasing voltages are applied, the energy-band diagram takes the shape shown in Fig. 7.5(b). The resistances of the bulk emitter, base, and collector regions are taken to be negligible so that the applied voltage drops appear across the junctions. The forward-biasing of the emitter junction reduces the barrier energy there whereas the reverse-biasing of the collector junction enhances the corresponding barrier energy. The reduction of the barrier energy at the emitter junction is

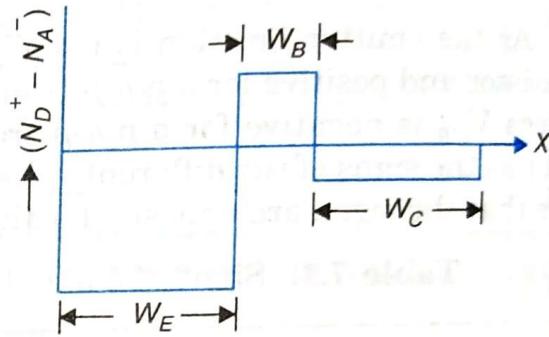


Fig. 7.3 Doping profile of a *p-n-p* transistor.

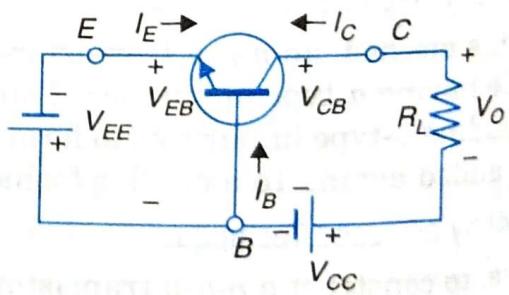


Fig. 7.4 An *n-p-n* transistor with bias voltages and a load resistance.

The normal operation of a transistor is shown in the circuit of Fig. 7.4. The voltage source V_{EE} makes the emitter-base junction of the *n-p-n* transistor forward-biased. The other voltage source V_{CC} biases the collector-base junction in the reverse direction.

$|eV_{EB}|$ and the increase of the barrier energy at the collector junction is $|eV_{CB}|$, where e is the electronic charge. As a result of the decrease in the barrier height at the emitter junction, a large number of electrons are injected from the emitter into the base. The doping of the emitter being greater than that of the base, the number of holes that flow into the emitter from the base is very small. The emitter current is thus contributed almost totally by the flow of electrons in an $n-p-n$ transistor. Note that for a $p-n-p$ transistor the emitter current is carried by the holes injected from the emitter into the base.

For an $n-p-n$ transistor, the electrons on entering the base region, create a concentration gradient there. Since the electron concentration at the emitter junction due to injection exceeds that at the collector junction, the injected electrons diffuse through the base region towards the collector junction. In the process, some of the electrons recombine with the holes in the base region and are thus lost. The width of the base is made *very thin* to increase the electron concentration gradient in the base region thereby enhancing the diffusion current, and also to diminish the number of electrons lost by recombination in the base. As the collector potential is positive with respect to the base, the negatively charged electrons on reaching the collector junction, are at once attracted by the collector terminal, producing the collector current. The collector current is a little less than the emitter current since a few electrons are lost by recombination with holes while diffusing through the base.

The dynamic resistance at the emitter junction is very small since it is forward-biased. But the dynamic resistance at the collector junction is very large since the junction is reverse-biased. Therefore, in the transistor a current from a low-resistance input circuit is transferred to a high-resistance output circuit with almost unchanged magnitude. This results in a power gain. In fact, the name "transistor" is coined from "transfer resistor".

Observation

When the transistor is regarded as two back-to-back $p-n$ junctions, for an $n-p-n$ transistor the p regions of the two $p-n$ junctions (forming the base) must be very thin and must be of the same semiconductor of proper doping. The carriers injected across one junction must diffuse across the second junction to give the transistor action. Two $p-n$ diodes having metal leads and connected back-to-back will not make a transistor since the above conditions may not be satisfied. Furthermore, the contact potentials at the metal semiconductor junctions will not give the desired energy diagram of Fig. 7.5.

7.4 A TRANSISTOR AMPLIFIER

The principle of operation of a transistor amplifier can be understood with the help of Fig. 7.4. A small change ΔV_i of the emitter-base voltage changes the barrier height and hence the emitter current by ΔI_E . The corresponding change ΔI_C in the collector current is a little less than ΔI_E . This change in the collector current develops a voltage drop ΔV_o across the load resistance R_L , where

$$\Delta V_o = -R_L \Delta I_C \quad (7.1)$$

The change ΔV_o gives the output voltage of the amplifier. The negative sign in Eq. (7.1) appears because an enhancement of the collector current gives a voltage drop across R_L with polarity opposite to the reference polarity for the voltage drop V_o across R_L in Fig. 7.4.

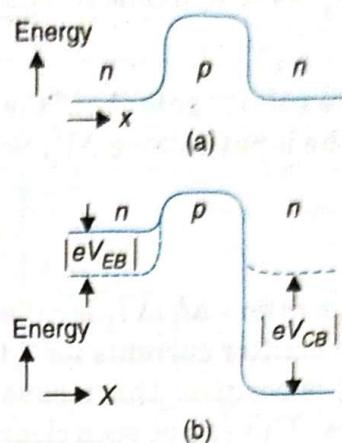


Fig. 7.5 Energy variation in the conduction band for the (a) unbiased and (b) biased transistor.

If r_e is the dynamic resistance of the emitter junction, we have

$$\Delta V_i = r_e \Delta I_E \quad (7.2)$$

The voltage gain A_V of the amplifier is defined to be the ratio between the output voltage ΔV_0 to the input voltage ΔV_i . So,

$$A_V = \frac{\Delta V_0}{\Delta V_i} = - \frac{R_L}{r_e} \frac{\Delta I_c}{\Delta I_E} \quad (7.3)$$

The ratio $-\Delta I_c / \Delta I_E$ is called the current gain A_I of the transistor. The signs of the collector and the emitter currents for a transistor being opposite, A_I is positive. Therefore, the voltage gain A_V is positive. This means that there is no phase shift between the input and the output voltages. This can be seen clearly from the circuit of Fig. 7.4. An increase of the emitter voltage voltages. This can be seen clearly from the circuit of Fig. 7.4. An increase of the emitter voltage produces a change in V_0 with polarity in conformity with the reference polarity. That is, an increase of ΔV_i is accompanied by an increase of ΔV_0 , implying that the output voltage and the input voltage are in phase.

Although A_I is slightly less than unity, R_L can be much larger than r_e . Therefore, A_V , as given by Eq. (7.3), can be much larger than unity, giving a voltage amplification. As an example, let $A_I = -(\Delta I_c / \Delta I_E) = 0.98$, $R_L = 3000\Omega$ and $r_e = 30\Omega$. Equation (7.3) then gives $A_V = 98$.

The power gain A_P of the transistor is the ratio between the output power and the input power. The output power is $(\Delta I_c)^2 R_L$ and the input power is $(\Delta I_E)^2 r_e$. Therefore

$$A_P = \left(\frac{\Delta I_c}{\Delta I_E} \right)^2 \frac{R_L}{r_e} = A_I A_V \quad (7.4)$$

7.5 CURRENT COMPONENTS IN A TRANSISTOR

Fig. 7.6 shows the different current components flowing across the forward-biased emitter-base junction (J_E) and the reverse-biased collector-base junction (J_C) of a $p-n-p$ transistor. The emitter current I_E is made up of the component $I_E(p)$ due to the holes injected from the emitter into the base and the component $I_E(n)$ due to the electrons crossing from the base into the emitter. Thus

$$I_E = I_E(p) + I_E(n) \quad (7.5)$$

The component $I_E(p)$ gives the transistor action because only the holes injected into the base can reach the junction J_C . The ratio $I_E(p)/I_E$ is the fraction of the emitter current that is effective for the transistor action and is known as the *emitter injection efficiency factor*.

As the emitter doping is much higher than the base doping in a commercial transistor, $I_E(p) \gg I_E(n)$, so that the emitter current arises almost entirely from the injected holes, and the emitter injection efficiency factor is very close to unity. All the currents in Eq. (7.5) are positive for a $p-n-p$ transistor.

Most of the holes crossing the emitter junction J_E reach the collector junction J_C producing a hole component $I_{C1}(p)$ of the collector current. The remaining holes recombine with the electrons in the base, giving a recombination hole current $I_E(p) - I_{C1}(p)$, leaving the base.

When the emitter-base junction is open-circuited and the collector-base junction is reverse biased, then $I_E = 0$ and the collector current I_C must be the reverse saturation current I_{C0} of the reverse-biased diode at J_C . This reverse current has two components: (i) $I_{C0}(n)$ consisting of the electrons moving from the p -side to the n -side across J_C , and (ii) $I_{C0}(p)$ due to the holes travelling from the n -side to the p -side across J_C . With the chosen reference directions in Fig. 7.6, we write

$$-I_{C0} = I_{C0}(n) + I_{C0}(p) \quad (7.6)$$

The total collector current when the emitter is forward-biased, is

$$I_C = I_{C0} - I_{C1}(p) \quad (7.7)$$

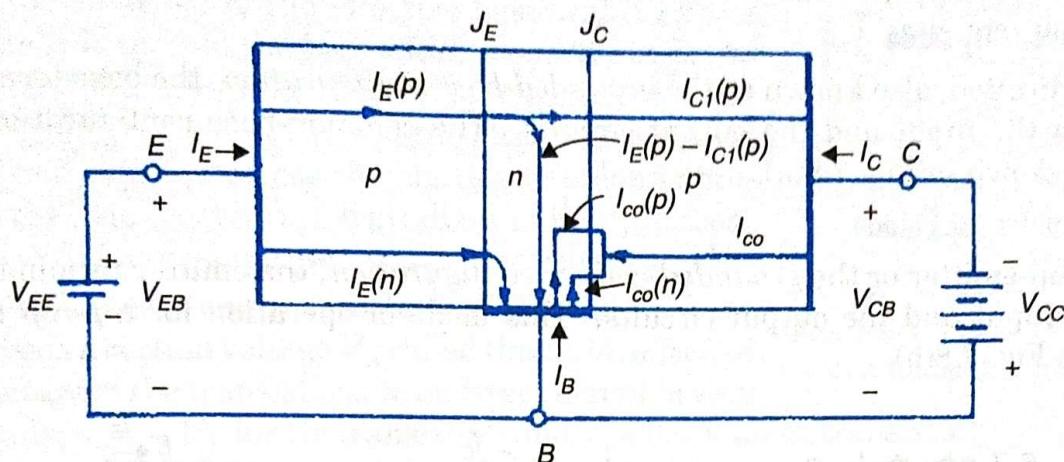


Fig. 7.6 Current components in a *p-n-p* transistor.

Usually, I_{C0} (sometimes denoted by I_{CBO}) is in μA or less and I_C is in mA , so that

$$I_{C0} \ll I_{C1}(p).$$

For a *p-n-p* transistor, I_E is positive while both I_C and I_{C0} are negative. This means that the collector current in Fig. 7.6 actually flows in the direction opposite to that indicated by the arrowhead of I_C . For an *n-p-n* transistor, these currents are reversed.

7.6 MINORITY CARRIER CONCENTRATION PROFILE

The minority carrier concentration in each section of a *p-n-p* transistor for normal operation is shown in Fig. 7.7. The quantities n_{p0} and p_{n0} give the thermal equilibrium concentrations of the electrons and holes, respectively. The emitter doping being much higher, the value of n_{p0} (the minority carrier concentration) in the *p*-type emitter is less than the value of p_{n0} (the minority carrier concentration) of the *n*-type base. Under normal operation when the emitter is forward-biased and the collector is reverse-biased, the minority carrier densities differ from the thermal equilibrium values. Because of the injected carriers across the junction J_E , the hole concentration p_n in the base and the electron concentration n_p in the emitter near J_E are enhanced. They fall off as one moves away from J_E . The hole density p_n becomes zero at the collector junction J_C which is reverse-biased. The collector electron concentration n_p is also reduced to zero at J_C due to the reverse bias.

Because of the concentration gradient of holes in the base region, they move through this region by the process of diffusion.

Observation

In a bipolar junction transistor, the emitter-base junction is forward-biased so that the impedance of the emitter circuit is low and a current flows between the emitter and the base. A change in the emitter current produces a change in the collector current, giving the transistor action. Thus *bipolar junction transistors are current-operated devices.*

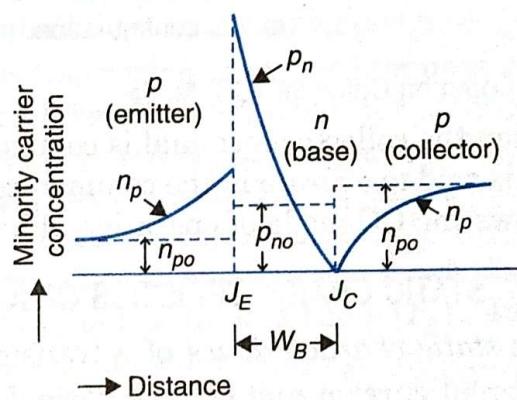


Fig. 7.7 Minority carrier concentration profile in the emitter, base, and collector for normal operation of a *p-n-p* transistor.

7.7 MODES OF TRANSISTOR OPERATION

A transistor can be operated in any of the following three modes depending on the common terminal between the input and the output circuits:

(i) Common-Base (CB) Mode

In this configuration, also known as the *grounded-base configuration*, the base terminal is common between the input and the output circuits. The common-base configuration of a *p-n-p* transistor is shown in Fig. 7.8(a).

(ii) Common-Emitter (CE) Mode

In the common-emitter or the *grounded-emitter configuration*, the emitter terminal is common between the input and the output circuits. This mode of operation for a *p-n-p* transistor is illustrated in Fig. 7.8(b).

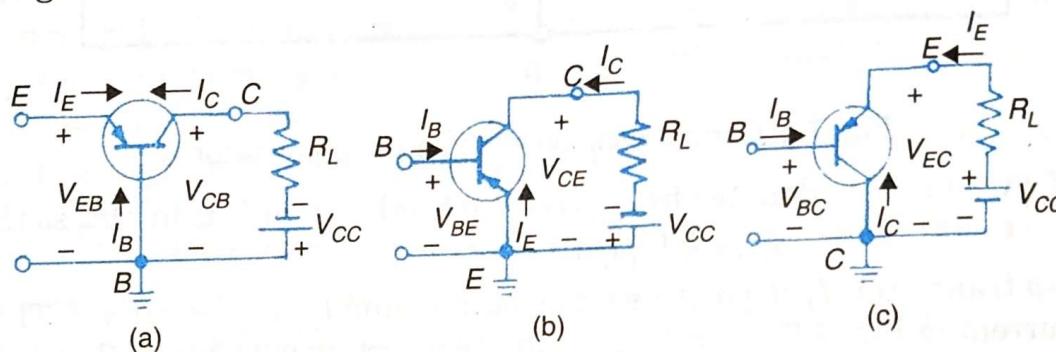


Fig. 7.8 Modes of operation of a *p-n-p* transistor:

(a) CB configuration, (b) CE configuration, and (c) CC configuration.

(iii) Common-Collector (CC) Mode

When the collector terminal is common between the input and the output circuits, the transistor is said to operate in the common-collector or the *grounded-collector configuration*. Fig. 7.8(c) shows the CC mode of operation of a *p-n-p* transistor.

7.8 STATIC CHARACTERISTICS OF A TRANSISTOR

The *static characteristics* of a transistor give the graphical forms of relationships among the different current and voltage variables of the transistor. The sets of characteristic curves, referred to as the *input characteristics* and the *output characteristics* for the CB and the CE configurations, are important from practical considerations. These sets of characteristics for a *p-n-p* transistor are discussed below.

The input characteristics for a given configuration refer to the plot of the input current versus the input voltage with the output voltage as a parameter. On the other hand, the output characteristics give the plot of the output current versus the output voltage with the input current as a parameter.

(i) Common-Base Characteristics

(a) Input Characteristics

Here the input current is the emitter current (I_E), the input voltage is the emitter-base voltage (V_{EB}), and the output voltage is the collector-base voltage (V_{CB}). Thus the input characteristic for the CB configuration is the plot of I_E versus V_{EB} with V_{CB} as a parameter. A set of such input characteristics is depicted in Fig. 7.9.

For normal operation, the emitter-base junction is biased in the forward direction. Therefore, the variation of I_E with V_{EB} is similar to the forward characteristic of a *p-n* diode. However,

with an increase of $|V_{CB}|$, I_E increases for a fixed V_{EB} . When $|V_{CB}|$ increases, the width of the depletion region at the collector-base junction increases, thereby reducing the effective base width. The change of the effective base width by the collector voltage is termed the *base width modulation* or the *Early effect*. The decrease of the effective base width enhances the concentration gradient of holes in the base region. Since the hole current injected across the emitter junction is proportional to the hole concentration gradient at that junction, I_E increases with increasing reverse collector voltage.

Note that unless the forward bias of the emitter-base junction exceeds a certain voltage V_y , called the *cutin, offset, or threshold voltage* of the transistor, the emitter current is very small. Usually, $V_y \approx 0.1$ V for Ge transistors and $V_y \approx 0.5$ V for Si transistors.

(b) Output Characteristics

For the CB mode, the collector current I_C is the output current, the collector-base voltage V_{CB} is the output voltage, and the emitter current I_E is the input current. Thus the plot of I_C versus V_{CB} with I_E as a parameter is the CB output characteristic of the transistors. Fig. 7.10 shows a typical set of CB output characteristics for a *p-n-p* transistor. I_E and V_{EB} are positive, and I_C , I_B and V_{CB} are negative for a *p-n-p* transistor. The signs are reversed for an *n-p-n* transistor.

The output characteristics can be divided into three distinct regions, namely, the *active region*, the *saturation region*, and the *cutoff region*. We shall discuss these regions now.

Active region: The active region is the normal operating region of a transistor used as an amplifier. In this region, the emitter junction is forward-biased and the collector junction is reverse-biased. If the emitter current is zero, the collector current equals the reverse saturation current I_{C0} , which is in the μA range for Ge and in the nA range for Si. When the emitter junction is forward biased, an emitter current I_E flows. Since the recombination in the base region is small, most of this current will reach the collector. The collector current I_C will be this current superimposed on I_{C0} . Since I_{C0} is very small, $|I_C|$ is a little less than $|I_E|$. In the active region, I_C is practically independent of V_{CB} and is determined only by I_E . Owing to the Early effect, however, $|I_C|$ rises slightly with an increase of $|V_{CB}|$. In the active region, the output characteristics are nearly parallel lines which are equispaced for equal changes in the emitter current.

Saturation region: The region of the output characteristics where both the emitter and the collector junctions are forward-biased, is referred to as the saturation region of the transistor. In Fig. 7.10, the saturation region is located to the left of the ordinate $V_{CB} = 0$ and above the characteristic for $I_E = 0$. V_{CB} is slightly positive for a *p-n-p* transistor in this region. This forward biasing of the collector-base junction causes the collector current to change exponentially with the collector-base forward voltage, as in a *p-n* diode. The large change in the collector current for a small change in V_{CB} in the saturation region is thus accounted for. A forward bias implies that the collector *p* material is at a positive

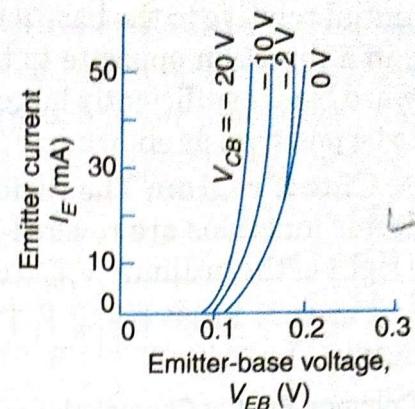


Fig. 7.9 CB input characteristics of a typical *p-n-p* transistor.

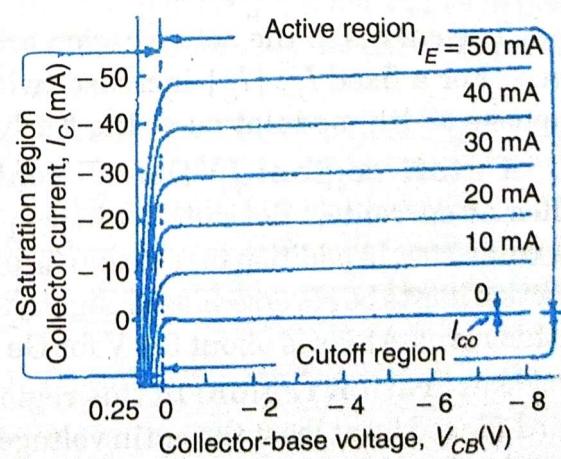


Fig. 7.10 CB output characteristics of a typical *p-n-p* transistor.

potential relative to the base n material. A hole current thus flows from the collector to the base, i.e., in a direction opposite to the original hole current due to the transistor action. When the forward bias is sufficiently large, the hole flow from the collector to the base predominates, forcing I_C to be positive, as shown in Fig. 7.10.

Cutoff region: The region of the output characteristics where both the emitter and the collector junctions are reverse-biased is the cutoff region. In Fig. 7.10, this region is located to the right of the ordinate $V_{CB} = 0$ and below the characteristic for $I_E = 0$.

For very large $|V_{CB}|$, $|I_C|$ increases due to breakdown. The breakdown region is not shown in Fig. 7.10.

(ii) Common-Emitter Characteristics

(a) Input Characteristics

For the CE mode, I_B is the input current, V_{BE} is the input voltage and V_{CE} is the output voltage. The CE input characteristics thus constitute the plot of I_B against V_{BE} with V_{CE} as a parameter. A set of typical CE input characteristics is depicted in Fig. 7.11. The characteristics are similar to that of a forward-biased $p-n$ diode. With increasing $|V_{CE}|$ for a constant V_{BE} , the effective base width decreases. Consequently, the recombination base current diminishes, as shown in Fig. 7.11.

(b) Output Characteristics

The output characteristics for the common-emitter mode refer to the plot of the collector current I_C versus the collector-emitter voltage V_{CE} with the base current I_B as a parameter. Fig. 7.12 shows the typical CE output characteristics of a $p-n-p$ transistor. As in the case of the CB configuration, the family of curves can be divided into the three regions : *active*, *cutoff* and *saturation regions*.

Active region: In this region, the collector junction is reverse-biased and the emitter junction is forward-biased. In Fig. 7.12 the active region is located to the right of the ordinate $V_{CE} = 0$ and above the characteristic for $I_B = 0$. If a transistor is to be used as an amplifier without much distortion, it has to be operated in the active region.

The curves in the active region are not horizontal lines. For a fixed I_B , $|I_C|$ increases with $|V_{CE}|$ due to the base width modulation or the Early effect.

Cutoff region: In the CE configuration, the collector current is not cutoff when $I_B = 0$. To cut off the transistor, in addition to reducing I_B to zero, the emitter junction has to be reverse-biased slightly. The magnitude of this reverse bias is about 0.1 V for Ge and about 0 V for Si transistors.

Saturation region: In this region, both the collector and the emitter junctions are forward-biased by at least the cutin voltage. Since the voltage $|V_{EB}|$ or $|V_{CB}|$ for a forward-biased junction is only a few tenths of a volt and $V_{CE} = V_{CB} - V_{EB}$, we find that V_{CE} is also a few tenths of a volt at saturation. Therefore, in Fig. 7.12 the saturation region lies very close to the zero voltage axis where all the curves coincide and fall quickly towards the origin. The onset of

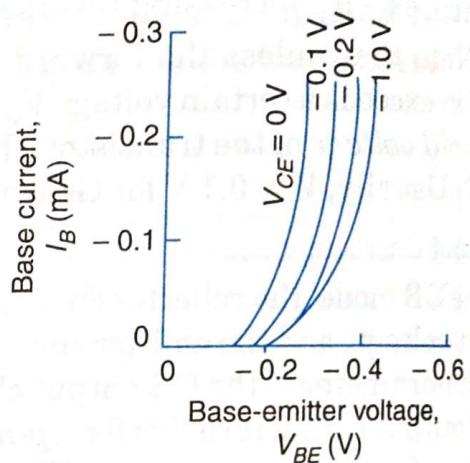


Fig. 7.11 CE input characteristics of a typical $p-n-p$ transistor.

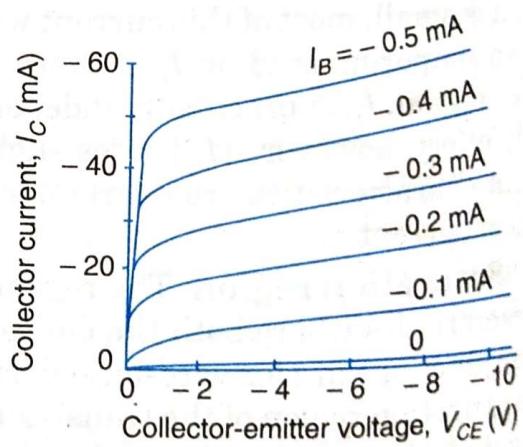


Fig. 7.12 CE output characteristics of a typical $p-n-p$ transistor.

saturation can thus be considered to occur at the knee of the curves in Fig. 7.12. In this region the collector current is nearly independent of the base current.

For very large $|V_{CE}|$, $|I_C|$ increases due to breakdown, which is not shown in Fig. 7.12.

Observations

- (i) At 25°C , for a typical Si $n-p-n$ transistor, $V_{BE, sat} = 0.8 \text{ V}$, $V_{BE, active} = 0.7 \text{ V}$, and $V_{CE, sat} = 0.2 \text{ V}$. For a Ge $n-p-n$ transistor, the corresponding values are 0.3 V , 0.2 V , and 0.1 V , respectively. For $p-n-p$ transistors, the signs of the above voltages are reversed. It is instructive to remember these values in solving numerical problems in situations where they are not specifically mentioned.
- (ii) If the emitter junction is reverse biased and the collector junction is forward biased the transistor is said to operate in the *reverse active* or *inverse active* mode. This mode has very limited application.

7.9 EXPERIMENTAL ARRANGEMENT FOR STUDYING TRANSISTOR CHARACTERISTICS

Fig. 7.13 shows a circuit diagram to study the characteristics of a $p-n-p$ transistor operating in the CE mode. The polarity of the batteries and of the meters would have to be reversed for an $n-p-n$ transistor. The base-emitter voltage (V_{BE}) of the transistor T is recorded by the dc voltmeter V_1 and the base current I_B is recorded by the dc microammeter A_1 . The collector-emitter voltage V_{CE} is measured by the dc voltmeter V_2 , and the collector current I_C is measured by the dc milliammeter A_2 .

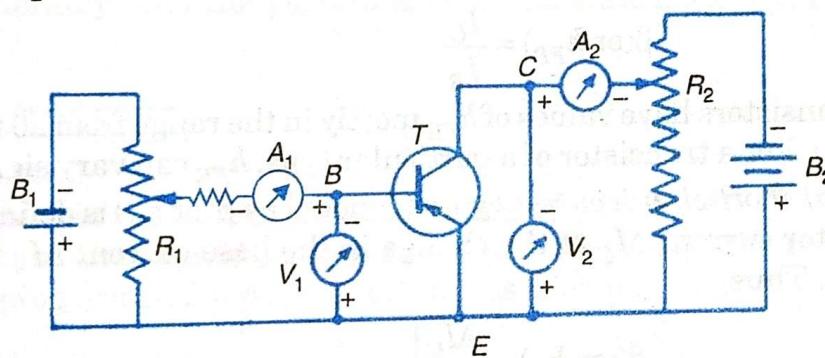


Fig. 7.13 A circuit arrangement to study transistor characteristics for CE configuration.

To obtain the input characteristics, the slider of the potentiometer R_1 is first set at its lowest position. The emitter-base voltage is then a minimum. The slider of the potentiometer R_2 is adjusted for a desired value of V_{CE} . The slider of R_1 is shifted in steps, and at each step I_B and V_{BE} are noted, keeping V_{CE} constant by adjusting R_2 , if necessary. The plot of I_B against V_{BE} then gives the input characteristic for the chosen fixed V_{CE} . For different values of V_{CE} , the experiment can be repeated to get a family of curves with V_{CE} as a parameter.

To obtain the output characteristics, I_B is kept at a desired low value by adjusting R_1 . The slider of R_2 is shifted in steps from its minimum position. At each step, V_{CE} and I_C are noted for the fixed I_B . I_C is then plotted against V_{CE} to obtain an output characteristic for a constant I_B . The slider of R_1 is shifted such that I_B is increased to a desired value. The experiment is repeated for this new value of I_B to obtain another output characteristic. Thus a set of output characteristics can be drawn with I_B as a parameter.

The CB characteristics of a transistor can be studied similarly with the circuit diagram modified to suit the CB operation.

7.10 EXPRESSIONS FOR CURRENTS

When the emitter is forward-biased, the collector current given by Eq. (7.7), can be written as

$$I_C = I_{C0} - \alpha I_E \quad (7.8)$$

$$\text{where } \alpha = -\frac{I_C - I_{C0}}{I_E} \quad (7.9)$$

The quantity α represents the fraction of the emitter current contributed by the carriers injected into the base and reaching the collector. α is called the *dc current gain* of the common-base transistor. Since I_C and I_E have opposite signs for a given transistor (*p-n-p* or *n-p-n*), α is always positive. Typically, α lies between 0.95 and 0.995. In general, α is not a constant for a given transistor, but varies with the emitter current I_E , the collector voltage V_{CB} , and the temperature. Since $I_{C0} \ll I_C$, we obtain $\alpha \approx -I_C/I_E$.

The *small-signal short-circuit current transfer ratio* (or *gain*) of a transistor in the common-base mode is denoted by α' . It is defined by the ratio of the change in the collector current to the change in the emitter current at a constant collector-base voltage. Thus

$$\alpha' = -\left. \frac{\Delta I_C}{\Delta I_E} \right|_{V_{CB} = \text{constant}} \quad (7.10)$$

Here ΔI_C and ΔI_E are respectively the increments in the collector current I_C and the emitter current I_E . The negative sign in Eq. (7.10) accounts for the fact that α' is positive although ΔI_C and ΔI_E have opposite signs for a given transistor. For a good transistor, $\alpha' \approx \alpha$. Clearly, α' can be found from the CB output characteristics.

The maximum current gain of a transistor operated in the common-emitter mode is denoted by the parameter β . The *dc* β (also called the *forward current transfer ratio* or the *dc current gain*) is denoted by β or h_{FE} . It is defined as the ratio of the collector current I_C and the base current I_B . Thus

$$\beta(\text{or } h_{FE}) = \frac{I_C}{I_B} \quad (7.11)$$

Commercial transistors have values of h_{FE} mostly in the range from 20 to 200. However, h_{FE} can be as high as 400. For a transistor of a particular type, h_{FE} can vary significantly.

The *small signal short-circuit current gain* (denoted by β' or h_{fe}) is defined as the ratio of the change in the collector current ΔI_C to the change in the base current ΔI_B for a fixed collector-emitter voltage V_{CE} . Thus

$$\beta'(\text{or } h_{fe}) = \left. \frac{\Delta I_C}{\Delta I_B} \right|_{V_{CE} = \text{constant}} \quad (7.12)$$

Usually, β' differs from β by less than 20 per cent. Note that β' can be obtained from the CE output characteristics.

Relationship between α and β

Applying Kirchhoff's current law, we have for the *p-n-p* transistor of Fig. 7.2 (a)

$$I_E = -(I_C + I_B) \quad (7.13)$$

Substituting for I_E from Eq. (7.8) in Eq. (7.13), we get

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{C0}}{1-\alpha} \quad (7.14)$$

Usually, $I_B > > I_{C0}$ so that in the active region, Eq. (7.14) gives

$$I_C = \frac{\alpha}{1-\alpha} I_B \quad (7.15)$$

Hence,

$$\beta = \frac{I_C}{I_B} = \frac{\alpha}{1-\alpha} \quad (7.16)$$

which is the desired relationship between α and β . As α is close to unity, a small change in α produces a relatively large change in β due to the term $(1-\alpha)$ in the denominator on the right-hand side of Eq. (7.16).

Observations

(i) Equation (7.16) shows that a small change in α causes a large change in the value of β and therefore affects the common-emitter characteristics. So, the CE characteristics can differ significantly even for transistors of a given type.

(ii) With the aid of Eq. (7.16), we can write Eq. (7.14) as

$$I_C = \beta I_B + (1 + \beta) I_{C0} \quad (7.17)$$

Putting

$$I_{CE0} = (1 + \beta) I_{C0} \quad (7.18)$$

Equation (7.17) gives

$$I_C = \beta I_B + I_{CE0} \quad (7.19)$$

The quantity I_{CE0} is the collector current when the base is open-circuited, (i.e., $I_B = 0$) and the collector junction is reverse-biased.

(iii) Since β is much larger than unity, a transistor operating in the CE configuration (where the input current is I_B and the output current is I_C), can be used as a current amplifier. The CC configuration where the input current is I_B and the output current is I_E , also gives current amplification. Here, the dc current gain is

$$-I_E/I_B = (I_B + I_C)/I_B = 1 + (I_C/I_B) = 1 + \beta.$$

(iv) β increases with increasing temperature. At low temperatures, β drops appreciably. For example, if $\beta = 80$ at 20°C , it can drop to 45 at -50°C . Furthermore, at very low temperatures, some of the carriers are lost due to freeze-out. As a result, the currents drop considerably, and the performance of the transistor is degraded at such temperatures.

7.11 SOME TRANSISTOR TERMS

(i) Base-spreading Resistance

The dc ohmic resistance of the part of the base region of a transistor through which the base current flows, is termed the *base-spreading resistance*. Typically, the base-spreading resistance has a value ranging from a few ohms to some tens of ohms.

(ii) Saturation Resistance

For a transistor operating in the saturation region of the CE configuration, the ratio of the collector-emitter voltage and the collector current for a given base current is termed the common-emitter *saturation resistance*. It is denoted by R_{CES} .

In Fig. 7.12, we note that $I_C = -40 \text{ mA}$ when $V_{CE} = -0.24 \text{ V}$ and $I_B = -0.5 \text{ mA}$.

Hence,

$$R_{CES} = \frac{-0.24}{-40 \times 10^{-3}} = 6 \Omega.$$

The significance of R_{CES} is that for a given I_B , it predicts the slope of the CE output characteristics to the left of the knee (which is almost a straight line). Typically, R_{CES} ranges from a few ohms to some tens of ohms.

(iii) Punch-through

As the reverse bias of the collector junction is increased, the effective base width decreases (the Early effect). At a certain reverse bias of the collector junction, the depletion region covers the base, reducing the effective base width to zero. As the collector voltage penetrates the base, the potential barrier at the emitter junction is lowered. As a result, an excessively large emitter current flows. This phenomenon is called *punch-through or reach-through*, and puts an upper limit to the reverse collector voltage. Punch-through is different from avalanche breakdown of the reverse-biased collector junction. In a particular transistor, the collector voltage limit is dictated by punch-through or breakdown, whichever takes place at a lower voltage.

Ebers-Moll Model

Equation (7.8) holds for the active region, i.e. when the emitter is forward biased and the collector is reverse biased. To obtain a general form of this equation that will hold for any voltage across the collector junction, I_{C0} must be replaced by the current in a pn diode formed of the base and the collector regions. Thus the collector current can be generally written as

$$I_c = I_{C0} \left[1 - \exp\left(\frac{eV_c}{k_B T}\right) \right] - \alpha_N I_E = -\alpha_N I_E - I_{C0} \left[\exp\left(\frac{eV_c}{k_B T}\right) - 1 \right] \quad (7.20)$$

where V_c is the voltage drop across J_c from the p to the n side, and is positive for a forward biased collector junction. The subscript N to α refers to the use of the transistor in the *normal* fashion. If the roles of the emitter and the collector junctions are interchanged, i.e., the transistor is used in the *inverted* manner, we can write corresponding to Eq. (7.20)

$$I_E = -\alpha_I I_c - I_{E0} \left[\exp\left(\frac{eV_E}{k_B T}\right) - 1 \right] \quad (7.21)$$

where α_I is the inverted common-base current gain, I_{E0} is the reverse saturation current at the emitter junction, and V_E is the voltage drop from the p to the n side at J_E and is positive if the emitter junction is forward biased. Equations (7.20) and (7.21) are known as *Ebers-Moll equations*. It can be shown that $\alpha_N I_{E0} = \alpha_I I_{C0}$. Manufacturers quote α_N , I_{C0} , and I_{E0} ($\approx 0.01 I_{C0}$ to $0.9 I_{C0}$). Hence α_I can be found. Sometimes, α_R (reverse alpha) and α_F (forward alpha) are used in place of α_I and α_N , respectively.

The circuit model of Eqs. (7.20 and 7.21) is called the *Ebers-Moll model*, which for a pnp transistor is given in Fig. 7.13A. The circuit contains two pn diodes connected back-to-back and having reverse saturation currents $-I_{E0}$ and $-I_{C0}$; the diodes are shunted by two current-controlled current sources. The current sources are necessary for the minority carrier transport across the base. Applying Kirchhoff's current law at the collector node C of Fig. 7.13A gives

$$I_C = -\alpha_N I_E + I_1 = -\alpha_N I_E - I_{C0} \left[\exp\left(\frac{eV_c}{k_B T}\right) - 1 \right]$$

which is Eq. (7.20). The model applies for both forward and reverse voltages across J_E and J_C . The circuit is approximate because the base-spreading resistance is neglected. The circuit shows that $I_B + I_E + I_C = 0$.

The current sources in Fig. 7.13A are removed if $\alpha_N = \alpha_I = 0$. This happens for a thick base where all the minority carriers recombine in the base region and none can reach the collector. The transistor action then ceases, and we have just two back-to-back diodes. Thus the two pn diodes placed back-to-back will exhibit transistor properties only if the carriers injected across one junction can diffuse across the other junction.

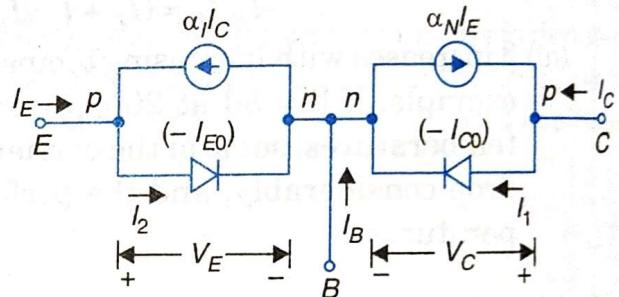


Fig. 7.13A Ebers-Moll model for a pnp transistor.

7.12 TRANSISTOR AS A SWITCH

In many circuits such as those required in high-speed counters and computers, a transistor is made to act as a switch. It is 'ON' when it is in saturation, and 'OFF' when it is in cutoff condition. By applying pulse voltages, the transistor is caused to go over from one state to the other.

We consider the circuit of Fig. 7.14; to the input we apply the pulse voltage waveform of Fig. 7.15 (a), the waveform making transitions between the voltage levels V_2 and V_1 . Initially, $v_i = V_2$ and the transistor is cut off. When v_i changes to V_1 the transistor goes over to saturation, but not immediately. The time required for the collector current i_c to attain 10% of its steady-state saturation value $I_{CS} = V_{CC}/R_L$ is known as the *delay time* t_d [Fig. 7.15(b)]. The time needed for the current i_c to rise from 10% to 90% of I_{CS} is termed the *rise time* t_r . The sum of the delay time and the rise time is called the *turn-on time* t_{ON} . Thus $t_{ON} = t_d + t_r$.

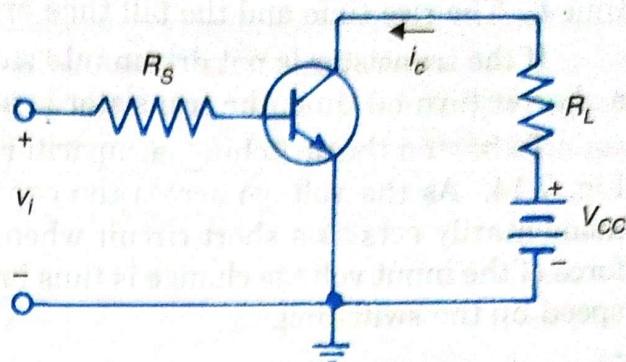


Fig. 7.14 A transistor switching circuit.

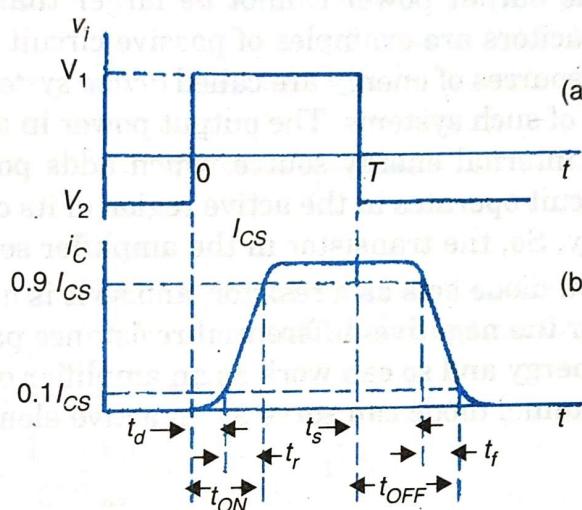


Fig. 7.15 (a) Pulse voltage input; (b) collector current response.

At time $t = T$, the input signal returns to its initial state, but the collector current does not respond at once. The time interval that elapses between the change-over of the input voltage and the instant at which i_c falls to 90% of I_{CS} is referred to as the *storage time* t_s . The time in which i_c drops from 90% to 10% of I_{CS} is the *fall time* t_f . The sum of t_s and t_f is called the *turnoff time* t_{OFF} : $t_{OFF} = t_s + t_f$. For commercial switching transistors, t_{ON} and t_{OFF} are in the range of some tens of nano-second.

The delay time t_d originates primarily from two factors. First, when the input voltage changes from V_2 to V_1 , some time is required to charge the emitter-base junction transition capacitance, so that the junction is brought from the reverse-biased condition to the forward-biased condition. Second, time must be allowed for the carriers injected from the emitter into the base to diffuse through the base and arrive at the collector junction to be recorded as the collector current.

The base current flowing into the transistor now increases the collector current and brings the transistor to saturation through the active region. The time interval required for this purpose is the rise time t_r .

In the saturated condition, both the emitter and the collector junctions are forward biased. So minority carriers (electrons for an $n-p-n$ transistor and holes for a $p-n-p$ transistor) are injected into the base from both the emitter and the collector. A fairly high amount of charge is thus stored in the base. When the input voltage changes from V_1 to V_2 , the collector current is not immediately cut off. In fact, i_c maintains its value till the excess charge density stored in the base region is swept out. This gives rise to the storage time t_s . Some more time is now to be

allowed for the transistor to go over to cutoff through the active region. This accounts the fall time t_f . The rise time and the fall time are determined by the collector transition capacitance.

If the transistor is not driven into saturation, the storage time t_s does not appear. So, for a shorter turn-off time, the transistor is not allowed to go into saturation.

To hasten the switching, a capacitor is often connected in parallel with the resistor R_s in Fig. 7.14. As the voltage across the capacitor cannot change instantaneously, the capacitor momentarily acts as a short circuit whenever the input voltage v_i changes abruptly. The full force of the input voltage change is thus immediately transferred to the base of the transistor to speed up the switching.

Observation

The circuit elements which contain no internal sources of energy are known as *passive elements*. In such elements, the output power cannot be larger than the input power. Typical resistors, inductors, and capacitors are examples of passive circuit elements. On the contrary, the systems having internal sources of energy are called *active systems*. Generators, amplifiers, and oscillators are examples of such systems. The output power in an active system can exceed the input power due to the internal energy source which adds power to the input signal. A transistor in an amplifier circuit operates in the active region of its characteristics and provides this internal source of energy. So, the transistor in the amplifier serves as an *active element*.

An ordinary *p-n* junction diode acts as a resistor, and so it is a passive element. However, a tunnel diode operating over the negative-differential-resistance part of its characteristic contains an internal source of energy and so can work as an amplifier or oscillator. Thus, although it is a *p-n* junction diode, a tunnel diode can serve as an active element.

7.13 SOLVED PROBLEMS

1. A transistor having $\alpha = 0.99$ is used in a common-base amplifier. If the load resistance is $4.5 \text{ k}\Omega$ and the dynamic resistance of the emitter junction is 50Ω , find the voltage gain and the power gain.

Ans. The voltage gain is

$$A_V \approx \alpha \frac{R_L}{r_e}$$

Here $\alpha = 0.99$, $R_L = 4.5 \text{ k}\Omega = 4500 \Omega$, and $r_e = 50 \Omega$.

Hence,

$$A_V = 0.99 \times \frac{4500}{50} = 89.1$$

The power gain is

$$A_P = \text{current gain} \times \text{voltage gain} = 0.99 \times 89.1 = 88.2$$

2. An *n-p-n* transistor with $\alpha = 0.98$ is operated in the CB configuration. If the emitter current is 3 mA and the reverse saturation current is $I_{C0} = 10 \mu\text{A}$, what are the base current and the collector current?

Ans. The collector current I_C for an emitter current I_E is given by

$$I_C = -\alpha I_E + I_{C0}$$

For an *n-p-n* transistor, I_E is negative. Therefore,

$$I_C = \alpha I_E + I_{C0}$$

Since $\alpha = 0.98$, $I_E = 3 \text{ mA}$, and $I_{C0} = 10 \mu\text{A} = 10 \times 10^{-3} \text{ mA}$, we have

$$I_C = 0.98 \times 3 + 10^{-2} = 2.95 \text{ mA.}$$

Also, from Kirchhoff's current law,

$$I_E + I_C + I_B = 0$$

(cf. C.U. 2006)

For an *n-p-n* transistor, I_E is negative. Hence,

$$-I_E + I_C + I_B = 0$$

or, $I_B = I_E - I_C = 3 - 2.95 = 0.05 \text{ mA} = 50 \mu\text{A}$.

3. A transistor having $\alpha = 0.975$ and a reverse saturation current $I_{C0} = 10 \mu\text{A}$, is operated in CE configuration. What is β for this configuration? If the base current is $250 \mu\text{A}$, calculate the emitter current and the collector current.

Ans. We have

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.975}{0.025} = 39.$$

Also, the collector current is

$$I_C = \beta I_B + (\beta + 1) I_{C0}$$

$$= 39 \times 0.25 + (39 + 1) \times 0.01 \text{ mA} = 10.2 \text{ mA}$$

Since

$$\alpha = \left| \frac{I_C - I_{C0}}{I_E} \right|,$$

$$0.975 = \frac{10.2 - 0.01}{I_E}$$

we have

whence $I_E = 10.4 \text{ mA}$.

4. A transistor is operating in the CE mode (Fig. 7.16). Calculate V_{CE} if $\beta = 125$, assuming $V_{BE} = 0.6 \text{ V}$. (cf. C.U. 1991, 2002)

Ans. When $V_{BE} = 0.6 \text{ V}$, the base current is

$$I_B = \frac{10 - V_{BE}}{310 \text{ k}\Omega} = \frac{10 - 0.6}{310} \text{ mA}$$

$$= 0.0303 \text{ mA}$$

Now,

$$\beta = 125. \text{ Therefore,}$$

$$I_C = \beta I_B = 125 \times 0.0303 \text{ mA}$$

$$= 3.79 \text{ mA} = 3.79 \times 10^{-3} \text{ A.}$$

Again,

$$V_{CE} = 20 - I_C \times 5 \times 10^3 \text{ V}$$

$$= 20 - 3.79 \times 5 = 1.05 \text{ V.}$$

5. A silicon *n-p-n* transistor having $\beta = 100$ and $I_{C0} = 22 \text{nA}$ is operated in the CE configuration (Fig. 7.17). Assuming $V_{BE} = 0.7 \text{ V}$, determine the transistor currents and the region of operation of the transistor. What happens if the resistance R_C is indefinitely increased?

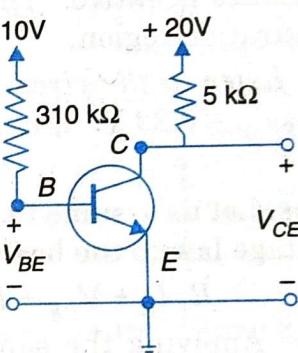


Fig. 7.16 Figure for Problem 4.

Ans. Since the base is forward-biased, the transistor is not cut off. So it is either in the active region or in the saturation region.

Let us assume that the transistor is in the active region. Application of Kirchhoff's voltage law to the base circuit gives

$$I_B R_B + V_{BE} = V_{BB}$$

$$\text{or } I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{5 - 0.7}{220} \text{ mA}$$

$$= 0.0195 \text{ mA}$$

$$= 19.5 \mu\text{A.}$$

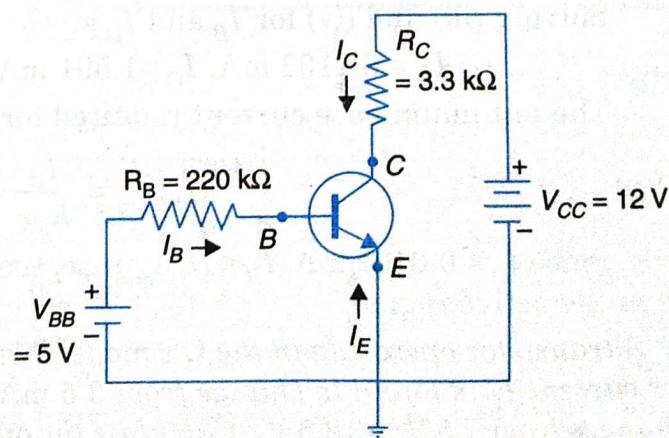


Fig. 7.17 Figure for Problem 5.

Here, $I_{C0} \ll I_B$. Therefore,

$$I_C \approx \beta I_B = 100 \times 195 \times 10^{-3} \text{ mA} = 1.95 \text{ mA.}$$

To justify the assumption that the transistor operates in the active region, we must show that the collector junction is reverse-biased. Applying Kirchhoff's voltage law to the collector circuit, we get

$$I_C R_C + V_{CB} + V_{BE} = V_{CC}$$

or,

$$\begin{aligned} V_{CB} &= V_{CC} - I_C R_C - V_{BE} \\ &= 12 - 1.95 \times 3.3 - 0.7 \\ &= 4.86 \text{ V.} \end{aligned}$$

A positive value of V_{CB} implies that for the *n-p-n* transistor, the collector junction is reverse-biased. Therefore, the transistor is actually in the active region.

The emitter current is

$$\begin{aligned} I_E &= -(I_C + I_B) = -(1.95 + 0.0195) \text{ mA} \\ &= -1.97 \text{ mA.} \end{aligned}$$

The negative sign indicates that I_E actually flows in the direction opposite to the arrow-head shown in Fig. 7.17.

In the active region, I_B and I_C do not depend on the collector circuit resistance R_C . So, if R_C is gradually increased, we see from the collector circuit equation that at one stage V_{CB} becomes negative. The transistor is then no longer in the active region; it goes over to the saturation region.

6. Refer to the circuit of Fig. 7.18. At saturation, V_{BE} and V_{CE} are $V_{BE, sat} = 0.85 \text{ V}$ and $V_{CE, sat} = 0.22 \text{ V}$. If $h_{FE} = 110$, is the transistor operating in the saturation region?

(cf. C.U. 1998)

Ans. Let us assume that the transistor operates in the saturation region. Applying Kirchhoff's voltage law to the base circuit we get

$$R_I I_B + V_{BE} + R_E (I_C + I_B) = V_{BB} \quad (i)$$

Applying the same to the collector circuit we obtain

$$R_2 I_C + V_{CE} + R_E (I_C + I_B) = V_{CC} \quad (ii)$$

Substituting the numerical values, expressing I_B and I_C in mA, and rearranging, (i) and (ii) are written as

$$49.2 I_B + 2.2 I_C = 4.15 \quad (iii)$$

$$\text{and} \quad 2.2 I_B + 5.5 I_C = 8.78 \quad (iv)$$

Solving (iii) and (iv) for I_B and I_C gives

$$I_B = 0.0132 \text{ mA}, I_C = 1.591 \text{ mA.}$$

The minimum base current required for saturation is

$$(I_B)_{\min} = \frac{I_C}{h_{FE}} = \frac{1.591}{110} = 0.0145 \text{ mA.}$$

Since $I_B = 0.0132 \text{ mA}$, $I_B < (I_B)_{\min}$. So, the transistor is not in the saturation region. It must be in the active region.

7. A transistor operating in the CE mode draws a constant base current I_B of $30 \mu\text{A}$. The collector current I_C is found to change from 3.5 mA to 3.7 mA when the collector-emitter voltage V_{CE} changes from 7.5 V to 12.5 V . Calculate the output resistance and β at $V_{CE} = 12.5 \text{ V}$. What is the value of α ?

(C.U. 2002)

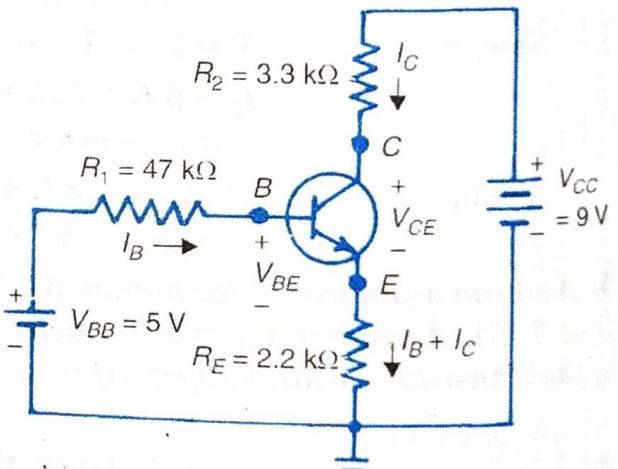


Fig. 7.18 Figure for Problem 6.

Ans. The change in the collector current is $\Delta I_C = 3.7 - 3.5 = 0.2 \text{ mA}$. The corresponding change in the collector-emitter voltage is $\Delta V_{CE} = 12.5 - 7.5 = 5\text{V}$. So, the output resistance is

$$\frac{\Delta V_{CE}}{\Delta I_C} = \frac{5}{0.2 \times 10^{-3}} \Omega = 25 \text{ k}\Omega$$

Since the base current is $I_B = 30 \mu\text{A} = 0.03 \text{ mA}$,

we have

$$\beta = \frac{I_C}{I_B} = \frac{3.7}{0.03} = 123.3$$

Also,

$$\beta = \frac{\alpha}{1-\alpha}, \text{ so that } \alpha = \frac{\beta}{\beta+1} = \frac{123.3}{124.3} = 0.992.$$

8. In the circuit of Fig. 7.19, the transistors Q_1 and Q_2 have $\beta = 100$. The Zener diode voltage is $V_Z = 4\text{V}$. Given, $I_L = 2 \text{ mA}$, $I_Z = 5 \text{ mA}$, $V_{EB1} = V_{EB2} = 0.7\text{V}$. Find R_1 , R_2 , and the range of R_L for Q_1 to remain in the active region. (GATE 2001)

Ans. Let I_E and I_B be the emitter and the base currents, respectively, of Q_1 . Since I_L is the collector current of Q_1 , we have $I_B = I_L/\beta = 2/100 = 0.02 \text{ mA}$.

Also, $I_E = I_B + I_L = 0.002 + 2 = 2.02 \text{ mA}$.

If V_{R1} is the voltage drop across R_1 , we obtain

$$\begin{aligned} V_{R1} &= 12 - V_{EB2} - V_Z \\ &= 12 - 0.7 - 4 = 7.3 \text{ V} \end{aligned}$$

The resistance R_1 is

$$R_1 = \frac{V_{R1}}{I_B + I_Z} = \frac{7.3}{0.02 + 5} = \frac{7.3}{5.02} = 1.45 \text{ k}\Omega.$$

The voltage drop across R_2 is

$$V_{R2} = V_{EB2} + V_Z - V_{EB1} = 4\text{V}.$$

$$\text{So, } R_2 = \frac{V_{R2}}{I_E} = \frac{4}{2.02} = 1.98 \text{ k}\Omega$$

The base-collector voltage drop for Q_1 is

$$V_{BC} = 12 - V_{R2} - V_{EB1} - I_L R_L = 7.3 - 2R_L$$

where R_L is in $\text{k}\Omega$. For Q_1 to remain in the active region, $V_{BC} \geq 0$, i.e.

$$R_L \leq \frac{7.3}{2} \text{ k}\Omega \text{ or } R_L \leq 3.65 \text{ k}\Omega. \text{ So, } 0 \leq R_L \leq 3.65 \text{ k}\Omega.$$

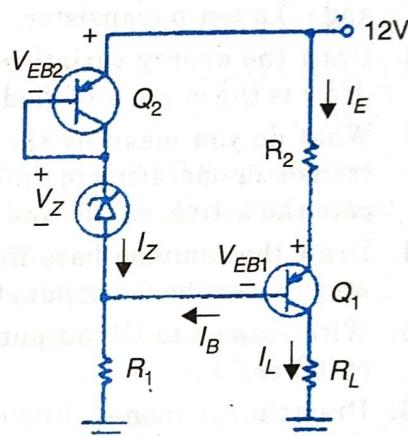


Fig. 7.19 Figure for Problem 8.

REVIEW QUESTIONS

1. (a) What is a transistor? (C.U. 1993)
 (b) The metal lead of the p -side of a $p-n$ diode is soldered to the metal lead of the p -side of another $p-n$ diode. Will the structure form an $n-p-n$ transistor? If not, why? (cf. C.U. 1990)
 (c) "Bipolar transistors are current-operated devices." Explain.
2. (a) Indicate the reference current directions and voltage polarities of a transistor. Give the signs of the actual current directions and voltage polarities for an $n-p-n$ and a $p-n-p$ transistor operating normally.
 (b) Why are junction transistors called bipolar devices?
 (c) Why is the emitter region of a transistor more heavily doped than the base region?
 (d) Why is BJT not suitable at very low temperatures?