2022

INFORMATION TECHNOLOGY

Paper : IT-502

(Digital Signal Processing)

Full Marks : 70

The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own words
as far as practicable.*

Answer *question no.* 1 and *any four* questions from the rest.

2×5

1. Answer *any five* questions :

   (a) State any two advantages of Digital Signal Processing.

   (b) Define unit STEP sequence.

   (c) Define UNIT sample sequence.

   (d) What is time-invariant system?

   (e) What is the condition for the BIBO stable?

   (f) Find the Z transform of the sequence : $\{1, 0, 2, 0, 3\}$.

2. (a) Explain the process of analog to digital conversion of signals in terms of sampling quantization and coding.

   (b) Plot the sequence : $p[n] = a_{-3}\delta[n+3] + a_1\delta[n-1] + a_2\delta[n-2] + a_7\delta[n-7]$.

6+5+4

   (c) Define periodic and Aperiodic Discrete-Time Sequences.

3. (a) What is meant by causal and non-causal system?

   (b) Define a Linear Time Invariant (LTI) System and give one example of it.

   (c) Define linear convolution and show that LTI systems can be completely characterized by their impulse response.

4+5+6

4. (a) Find the convolution of $X(n) = \{1, 2, 3, 1, 2, 1\}$ and $h(n) = \{1, 2, 1\}$.

   (b) Explain Discrete Time Fourier Transform.

   (c) An LTI system has impulse response $h(n) = 5(-1/2)^n u(n)$. Determine Fourier Transform to find the output of this system when the input is $x(n) = (1/3)^n u(n)$.

5+4+6

5. (a) Estimate the time complexity of Discrete Fourier Transform.

   (b) Explain Fast Fourier Transform and justify why it is better than Discrete Fourier Transform.

   (c) Explain with an example the role of difference equation in designing Discrete Time Linear Systems.

3+(5+2)+5

Please Turn Over

6. (a) What do you mean by Digital Filter?

   (b) Explain the design principle of an FIR Low Pass Filter.

   (c) State the characteristics of an IIR filter.

   (d) Compare between FIR and IIR Filters. 2+6+4+3
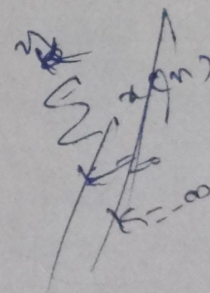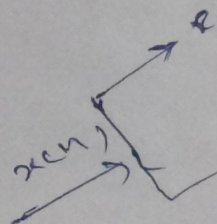
7. (a) Obtain Z-transform for (i) $x_1(n) = (1/2)^n u(n) + (2)^n u(n)$. Plot pole-zero diagram and state ROC.

   (b) Discuss the processing pipelines for the following DSP architectures: (i) SIMD, (ii) VLIW.

   (c) Explain the operational principle of Multiplier Accumulator (MAC) unit. (3+3)+(3+3)+3